Intel® Xeon® 6900E+ Series Processors

Specification Update

Rev. 001US

July 2026

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Revision History

Revision Number	Description	Date
001US	• Initial release of the document.	July 2026

1.0 Preface

This document is an update to the specifications contained in the following table. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

1.1 Affected Documents

Document Title	Document Number/ Location
Intel® Xeon® 6900E+ Series Processors Architecture Specification	779546
Intel® Xeon® 6900E+ Series Processors Registers Specification	783269
Birch Stream-AP Platform Electrical Specification	635356
Birch Stream-AP Platform Design Guide (PDG)	635354
Birch Stream Platform BIOS Writer's Guide (BWG)	647898
Birch Stream-AP Pin List	636245

NOTE

Documents are available at https://www.intel.com/content/www/us/en/design/resource-design-center.html.

1.2 Related Documents

Document Title	Document Number/ Location
Intel® 64 and IA-32 Architectures Software Developer's Manual, Combined Volumes 1, 2A, 2B, 2C, 2D, 3A, 3B, 3C, 3D, and 4	671200[1]
ACPI Specifications	www.acpi.info[2]

NOTES

1. Document is available at https://www.intel.com/content/www/us/en/design/resource-design-center.html.
2. Document available at www.uefi.org.

1.3 Nomenclature

Errata are design defects or errors. These may cause the Intel® Xeon® 6900E+ Series Processors behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics, such as, core speed, L2 cache size, all notes associated with each S-Spec number.

QDF Number is a several-digit code used to distinguish between engineering samples. These processors are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. The NDA specification update has a processor identification information table that lists these QDF numbers and the corresponding product sample details.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE

Errata remain in the specification update throughout the product's life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so forth).

2.0 Identification Information

2.1 Component Identification via Programming Interface

The Intel® Xeon® 6900E+ Series Processors stepping can be identified by the following register contents.

Table 1. Intel® Xeon® 6900E+ Series Processors Identification

CPUID	Extended Family[1]	Extended Model[2]	Reserved	Processor Type[3]	Processor Family[4]	Processor Model[5]	Processor Stepping[6]
Bit	27:20	19:16	15:14	13:12	11:8	7:4	3:0
XDCC	0h	Dh	0h	0h	6h	Dh	1h

NOTES

1. The Extended Family, bits [27:20], is used in conjunction with the Family Code, specified as bits [11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® Pro, Pentium® 4, Intel® Core™ processor family, or the Intel® Core™ i7 family.
2. The Extended Model ID, bits [19:16] in conjunction with the Model Number, specified in bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Processor Type, specified in bit [12] indicates whether the processor is an original OEM processor, an Intel® OverDrive processor, or a dual processor (capable of being used in a dual processor system).
4. The Processor Family corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
5. The Processor Model, bits [7:4] corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
6. The Processor Stepping, bits [3:0] indicates the revision number of that model. See Component Identification via Registers for the processor stepping ID number in the CPUID information.

This location contains the CPUID, Processor Type, Family, Model, and Stepping. The CPUID field is a copy of the results in EAX[15:0] from Function 1 of the CPUID instruction. Writes to this register have no effect. Data format is hexadecimal.

To find the mapping between a processor's CPUID and its Family/Model number, see the *Intel® 64 and IA-32 Architectures Software Developer Manual Combined Volumes*.

A complete description of the processor identification and feature determination is located in Chapter 20.

When EAX is set to a value of '1,' the CPUID instruction returns the Processor Family, Extended Model ID, Processor Type, Family, Model, and Stepping together referred as the processor signature value, in the EAX register. Note that after reset, the EDX processor will report the processor signature value in both the EDX and the EAX registers.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX, and EDX general purpose registers after the CPUID instruction is executed with a 2 in the EAX register. Special uses of general purpose registers include: Accumulator for operands and results data (EAX), Pointer to data in the DS segment (EBX),Counter for string and loop operations (ECX), and I/O pointer (EDX).

The Intel® Xeon® 6900E+ Series Processors Identification can also be identified in *Intel® Xeon® 6900E+ Series Processors Registers Specification*.

Table 2. Component Identification via Capability Registers

Physical Chip	Stepping	SEGMENT, WAYNESS	CPUID	SEGMENT[1] [Bits 5:3]			WAYNESS[2] [Bits 1:0]	
				Offset [B:31, D:30, F:3] + 84h				
				5	4	3	1	0
XDCC	B	Server, 2S	0xD06D1	1	0	1	0	1

NOTES

1. Bits[5:3] SEGMENT:
   - 111: Server SP
   - 110: RSVD
   - 101: Server AP
   - 100: RSVD
   - 011: Server DE
   - 010: Server Atom
   - 001: Workstation
   - 000: HEDT

   Also, refer to CAPID5_[12:9]4 bits Sub-segment SKU for definitions.
2. Bits[1:0] WAYNESS (max wayness):
   - 00 = 1S
   - 01 = 2S
   - 10 = 4S
   - 11 = 8S
3. The Intel® Xeon® 6900E+ Series Processors Capability Registers may also be identified in *Intel® Xeon® 6900E+ Series Processors Registers Specification*.

3.0 Processor Marking and Traceability Information

The Intel® Xeon® 6900E+ Series Processors can be identified by the following register markings.

Figure 1. Processor Marking and Traceability (Example)

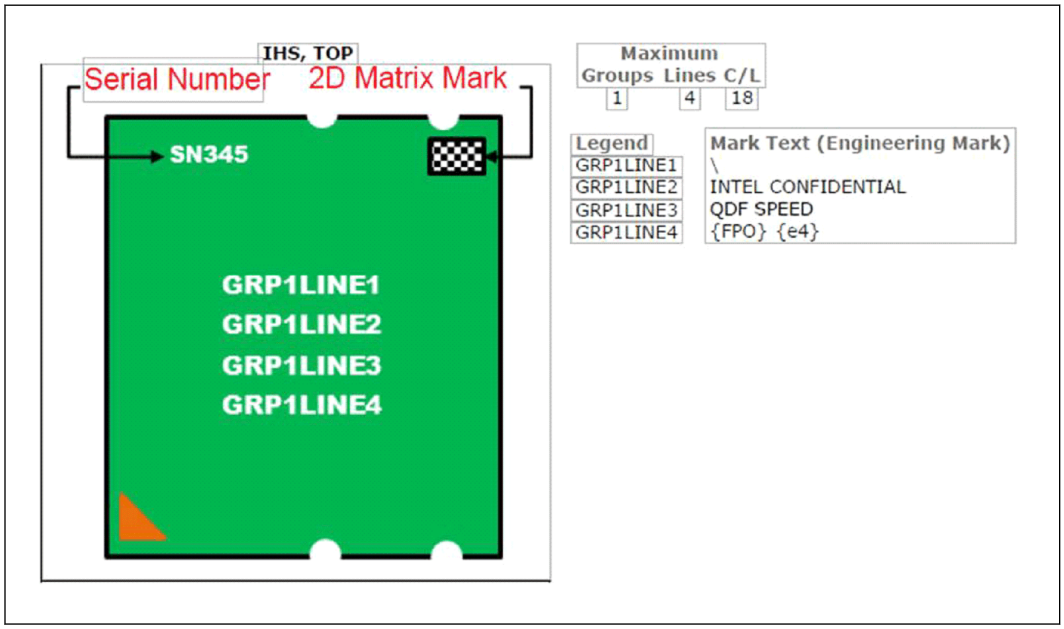

Table 3. Intel® Xeon® 6900E+ Series Processors Intel® Turbo Boost Technology Information

SKU	SSPEC	MM#	Ordering / Product Code	Cores	Cache (MB)	TDP (W)	Base Speed (GHz)	All Core Turbo (GHz)	Max Turbo Freq. (GHz)	DDR5 Speed (MT/s)	Memory Channels Supported
6990E+	SAE3X	99DK3V	PK807303B9B4E13	288	576	450	2.2	2.8	3.2	8000	12
6980E+	SAE3W	99DK3P	PK807303B9B4E14	264	528	400	2.1	2.7	3.2	8000	12
6970E+	SAE4W	99DKCH	PK807303B9B52F4	192	480	400	2.3	3	3.2	8000	12
6960E+	SAE3Z	99DK3N	PK807303B9B4E16	144	432	330	2.4	3	3.2	8000	12

Table 4. Intel® Xeon® 6900E+ Series Processors Additional Feature Information

SKU	Max. Socket Scalability	Max. Intel® UPI Ports	Intel® UPI Speed (GT/s)	Intel® QAT	Intel® DLB	Intel® IAA	Intel® DSA	Intel® TME-MK and Intel® TDX Keys	Intel® SGX Enclave Size	Reliability (10 years)	Availability (10 years)
6990E+	2S	6	24	4	4	4	4	1024	512 GB	yes	yes
6980E+	2S	6	24	4	4	4	4	1024	512 GB	yes	yes
6970E+	2S	6	24	4	4	4	4	1024	512 GB	yes	yes
6960E+	2S	6	24	4	4	4	4	1024	512 GB	yes	yes

NOTE

Intel® QAT - Intel® QuickAssist Technology

Intel® UPI - Intel® Ultra Path Interconnect

Intel® DLB - Intel® Dynamic Load Balancer

Intel® IAA - Intel® In-Memory Analytics Accelerator

Intel® DSA - Intel® Data Streaming Accelerator

Intel® TME-MK - Intel® Total Memory Encryption - Multi-Key

Intel® TDX - Intel® Trust Domain Extensions

Intel® SGX - Intel® Software Guard Extensions

4.0 Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel® Xeon® 6900E+ Series Processors product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations.

4.1 Codes Used in Summary Tables

Stepping	Description
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update will be implemented.
Planned Fix	This erratum may be fixed in a future hardware stepping, firmware, or software update.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plan to fix this erratum.

4.2 Errata Summary Table

Erratum ID / Internal Reference #	Processor C Stepping XDCC/HDCC	Title
CWF1 / 14022632661	No Fix	Intel RDT Memory Bandwidth Allocation (MBA) Cannot Throttle to Minimum Bandwidth
CWF2 / 14024373919	No Fix	System Hang When Page Request Message Issued From Discrete Device
CWF3 / 14022014815	No Fix	Intel DSA Memory Write with Incorrect Parity May Result in a System Crash
CWF4 / 14024345095	No Fix	PCIe TLP May be Lost After Link Down Event
CWF5 / 14014907791	No Fix	CHA UCNA Errors May Be Incorrectly Controlled by MC7_CTL Enable Bits
CWF6 / 14023746547	No Fix	Locked Page Split Access May Not Be Detected by UC-lock Disable if Split-lock Disable is Not Used
CWF7 / 14020785117	No Fix	Errors May Occur During TOR CrashDump
CWF8 / 22019963362	No Fix	TOR_TIMEOUT May Occur Due to RID Values Outside Range Limit
CWF9 / 14022992878	No Fix	APPP Error May Be Logged Incorrectly in Machine Check Status Register ADDRV

continued...

Erratum ID / Internal Reference #	Processor C Stepping XDCC/HDCC	Title
CWF10 / 14023454424	No Fix	S and AR Bits of MCi_STATUS Registers Unexpectedly Cleared by UCNA or CE
CWF11 / 22020041317	No Fix	Completion Timeout When Using Link IDE And Selective IDE
CWF12 / 22020610273	No Fix	Mirrored 128b ECC Mode May Not Log DRAM Address With Poison
CWF13 / 14024373537	No Fix	Unable to Access 32-bit Address MMIO Registers Out of Band
CWF14 / 14022882270	No Fix	Intel DSA and Intel IAA Devices May Cause a Machine Check
CWF15 / 14024373801	No Fix	PLR and PEM PCS_PSTATE Not Asserted or Incremented
CWF16 / 14025020928	No Fix	PCIe Infinite Recovery Loop During Link Equalization
CWF17 / 14025045018	No Fix	Incorrect B2CMI MCi_STATUS_SHADOW.CORRCOUNT Value
CWF18 / 14025264335	No Fix	Incorrect Values For CHA ALL0 And CHA ALL1
CWF19 / 14025336815	No Fix	CXL Mode Incorrectly Identifies ASPM L1 Aborts
CWF20 / 14025810731	No Fix	PCIe Root Port May Not Reduce Link Width
CWF21 / 22021466988	No Fix	SYS_RESET_N Trigger May Lead to MCA_GPSB_TIMEOUT
CWF22 / 14025793445	No Fix	Performance Monitoring Event For Memory Bound Stalls May Undercount
CWF23 / 14025920836	No Fix	PMON Unit Control Unfreeze May Cause COUNTERVALUE Registers to Overcount
CWF24 / 13014270453	No Fix	TRIG Packets May Contain ICNT Field When ICNTV Bit is Not Set
CWF25 / 14027632738	No Fix	Intel® PT Event Trace Generates CFE and FUP After VMCS/PIP Packets During VM Entry
CWF26 / 14027632994	No Fix	Intel® PT Event Trace Generates Incorrect IP For FUP Packet During VM Entry
CWF27 / 14027633025	No Fix	Intel® PT TRIG Packet Not Generated When ContextEn is 0
CWF28 / 14027633108	No Fix	Simultaneous Intel® PT TRIG and PTWRITE Packet May Result in Incorrect Trace Output
CWF29 / 14021761774	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results

Table 5. Specification Changes

Number	Specification Changes
SCHx	None for this revision of the specification update.

Table 6. Specification Clarifications

No.	Specification Clarifications
SCL1	Intel® Xeon® 6900E+ Series Processors Do Not Support CXL Snoop Filter Capability Structure

Table 7. Documentation Changes

No.	Documentation Changes
DCHx	None for this revision of the specification update.

5.0 Errata Details

CWF1. Intel RDT Memory Bandwidth Allocation (MBA) Cannot Throttle to Minimum Bandwidth

Problem: The system may not be limited to the minimum memory bandwidth possible when the maximum Intel RDT MBA delay value MSR throttle settings IA32_L2_QOS_EXT_BW_THRTL_[0..14] (at MSR address D50h...D5Eh) are configured by setting these registers to the maximum value of 90.

Implication: Due to this erratum, maximum bandwidth throttling cannot be guaranteed.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF2. System Hang When Page Request Message Issued From Discrete Device

Problem: A Page Request Message with a Last Page In Group (LPIG) field value of 0 issued from a discrete PCIe device to the processor may behave unexpectedly.

Implication: Due to this erratum, the system may hang. Root complex integrated devices are not affected by this erratum.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF3. Intel DSA Memory Write with Incorrect Parity May Result in a System Crash

Problem: When executing a copy operation, if an Intel DSA device receives a poisoned data response to a memory read request (Bus 8:11; Device: 1; Function: 0; Offset 104h, ERRUNCSTS.PTLP, bit[12]), an associated destination memory write with incorrect parity may be generated.

Implication: Due to this erratum, the memory write with incorrect parity may result in a machine check error leading to a system crash.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF4. PCIe TLP May be Lost After Link Down Event

Problem: If the first PCIe TLP received from the endpoint after a link down or hot-add event is a TLP with an LCRC error, one TLP may be lost on the link due to an incorrect Sequence Number in the NAK DLLP.

Implication: Due to this erratum, the system may log a Completion Timeout Status of 1 (ERRUNCSTS.CTE; Bus: 29, 28, 26, 5-1; Device: 9-2; Function: 0; Offset 104h; Bit 14) or Configuration Request Timeout of 1 (RPPIOSTS.CFGCTO; Bus: 29, 28, 26, 5-1; Device: 9-2; Function: 0; Offset 1ACh; Bit 2), leading to a device reset, a device (surprise) warm reset, or a failure to add the device.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF5. CHA UCNA Errors May Be Incorrectly Controlled by MC7_CTL Enable Bits

Problem: Uncorrectable Error No Action required (UCNA) errors reported in Cache Home Agent (CHA) Machine Check Banks (Bank 7) IA32_MC7_STATUS (MSR 41Dh) may be incorrectly controlled by the associated IA32_MC7_CTL (MSR 41Ch).

Implication: Due to this erratum, when IA32_MC7_CTL = 0h, the UCNA error may be logged but not signaled. When IA32_MC7_CTL = FFFFFFFFFh, the UCNA error may be logged and signaled, but may incorrectly set IA32_MC7_STATUS.EN (bit 60). Intel has not observed this erratum to affect any commercially available software.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF6. Locked Page Split Access May Not Be Detected by UC-lock Disable if Split-lock Disable is Not Used

Problem: The UC-lock disable feature (MSR_MEMORY_CTRL bit [28] (MSR 33h)) may not cause a fault (#AC(4)) for a page split lock that accesses a page with non-WB memory type if the split lock disable (MSR_MEMORY_CTRL bit [29]) is not set.

Implication: Due to this erratum, system software may not be able to fully prevent bus locks due to locks to non-WB memory unless they use the split-lock disable feature to prevent bus locks due to splits. Intel has not observed this erratum with any commercially available software.

Workaround: None identified. Software using the UC-lock disable feature should also enable the split lock disable feature.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF7. Errors May Occur During TOR CrashDump

Problem: When reading the TOR_AUX array prior to a TOR CrashDump operation, a segment of the TOR_AUX memory array may not be fully initialized, and the processor may return invalid data. As a result, a TOR_AUX_DATA_PARITY_ERR error may be logged (IA32_MCi_STATUS.MSCOD = 40h).

Implication: Due to this erratum, software analyzing a CrashDump record may not behave as expected.

Workaround: None identified. Software should ignore TOR_AUX_DATA_PARITY_ERR errors after a TOR CrashDump.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF8. TOR_TIMEOUT May Occur Due to RID Values Outside Range Limit

Problem: When Integrity and Data Encryption (IDE) is enabled, Requestor ID (RID) values that falls outside the expected RID value limits defined by the Selective IDE RID Association 1 Register (Bits [23:8] in SIDERIDA1_1, Bus: 29, 26, 4-1; Device: 9-2; Function: 0; Offset 324h) and Selective IDE RID Association 2 Register (Bits [23:8] in SIDERIDA2_1, Bus: 29, 26, 4-1; Device: 9-2; Function: 0; Offset 328h) for the PCI Express*(PCIe*) root port may lead to a TOR_TIMEOUT Machine Check Exception reported in MC7_STATUS (MSR 41Dh, MSCOD=0Ch), rather than a Completion Timeout.

Implication: Due to this erratum, a TOR_TIMEOUT may occur, which may lead to a system hang.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF9. APPP Error May Be Logged Incorrectly in Machine Check Status Register ADDRV

Problem: When the processor encounters an address parity error, it will signal an Address Parity Error (APPP) in [bit:58] of IA32_MCi_STATUS.ADDRV, the failing address in IA32_MCi_STATUS.ADDRV register may be incorrectly logged.

Implication: Due to this erratum, software that relies upon the IA32_MCi_ADDR.ADDR bits may not function as expected.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF10. S and AR Bits of MCi_STATUS Registers Unexpectedly Cleared by UCNA or CE

Problem: An Uncorrected No Action (UCNA) or Correctable Error (CE) may incorrectly clear the Signaling (S; bit 56) or Action Required (AR; bit 55) flags of IA32.MCi_STATUS registers.

Implication: Due to this erratum, software that relies on S and AR bits of IA32_MCi_STATUS registers may not function as expected.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF11. Completion Timeout When Using Link IDE And Selective IDE

Problem: When using both Link Integrity and Data Encryption (Link IDE) and Selective Integrity and Data Encryption (Selective IDE) capabilities for a PCIe port, the processor may respond with an incorrect StreamID field value in a completion packet.

Implication: Due to this erratum, an endpoint that relies upon coherent secure link StreamID field values when the Link IDE Stream State register (Bit [3:0]; Bus: 10, 14, 18, 22; Device: 0:2; Function: 0:7; offset 314h) and the Selective IDE Stream State register (Bit [3:0], Bus: 10, 14, 18, 22; Device: 0:2; Function: 0:7; offset 320h) are enabled may not function as expected and may lead to a device Completion Timeout (CTO) error.

Workaround: None identified. Software should not enable both Link IDE and Selective IDE for a PCIe port. Additional details may be found in the *Root Complex IDE Key Configuration Unit Software Programming Guide*, document number 732838.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF12. Mirrored 128b ECC Mode May Not Log DRAM Address With Poison

Problem: When a poison pattern error is detected with the 128-bit Error Correcting Code (ECC) mode and Memory Mirroring mode enabled, the DRAM address may not be logged in the RETRY_RD_ERR_LOG (Bus: 10, 14, 18, 22; Device: 0:2; Function: 0:7; Offset 2F10h + [0...3 × 4h]) register.

Implication: Due to this erratum, software that relies upon the RETRY_RD_ERR_LOG register may not function as expected.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF13. Unable to Access 32-bit Address MMIO Registers Out of Band

Problem: The processor logic incorrectly handles access requests from an out-of-band agent (such as BMC) to any MMIO registers with a 32-bit address.

Implication: Due to this erratum, out-of-band access to 32-bit address MMIO registers may result in a completion code of 90h (illegal command) with values of 0.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF14. Intel DSA and Intel IAA Devices May Cause a Machine Check

Problem: Reads returning greater than 8 from some registers of Intel DSA and Intel IAA devices will result in a fatal Machine Check Exception (MCE) logged in MC4_STATUS (MSR=419h, MSCOD=0000h, MCACOD=0x0E0Bh).

Implication: Due to this erratum, reads greater than 8 bytes will trigger a fatal MCE.

Workaround: None identified. Only software at the highest privilege level should access Intel DSA and Intel IAA devices.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF15. PLR and PEM PCS_PSTATE Not Asserted or Incremented

Problem: The PCS_PSTATE status (bit 29) in the Performance Limit Reasons (PLR) (Bus: 8; Device: 3; Function: 7; Offset: 12K+10×4×1-4d) and the Power and Performance Excursion Monitor (PEM) (Bus: 8; Device: 3; Function: 7; Offset: 44K +10×4×1-4d) will not be asserted when the Baseboard Management Controller (BMC) overrides the P-state and limits core frequency, and the PCS_PSTATE counter (ID 29) in the PEM will not be incremented and will read 0.

Implication: Due to this erratum, software that relies upon the PCS_PSTATE bits may behave unexpectedly.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF16. PCIe Infinite Recovery Loop During Link Equalization

Problem: When link equalization fails at Gen5 or Gen4, and the endpoint disables that rate, the processor may unexpectedly attempt to recover at the link partner's advertised speed resulting in an infinite recovery loop.

Implication: Due to this erratum, the PCIe link may fail to train, preventing DL-Init which causes the Data Link Layer Link Active (DLLLA, bit 13) in Link Status (LINKSTS, offset 52h) to remain unset.

Workaround: None identified. To mitigate this erratum, disable Gen5 or Gen4 per affected port to train at Gen4 or Gen3 within BIOS by using the Requested Link Speed setting.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF17. Incorrect B2CMI MCi_STATUS_SHADOW.CORRCOUNT Value

Problem: During memory mirror failover, the value in Bridge to Converged Memory Interface (B2CMI) MCi_STATUS_SHADOW.CORRCOUNT Offset 1C0h (bits 52:38) may not match the CORRECTED_ERROR_COUNT register values in IA32_MCi_STATUS (bits 52:38).

Implication: When this erratum occurs, software that relies upon the B2CMI MCi_STATUS_SHADOW.CORRCOUNT register may not function correctly.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF18. Incorrect Values For CHA ALL0 And CHA ALL1

Problem: For Out-of-Band access, the BDFs for (CHA ALL0 Bus 31; Device 14-0; Function 7-0) and (CHA ALL1 Bus 30; Device 28-14; Function 7-0) PCI Configuration Space Registers are incorrectly mapped.

Implication: Due to this erratum, BMC that relies upon the values in CHA ALL0 or CHA ALL1 may function incorrectly.

Workaround: None identified. To access the CHA ALL0 PCI Configuration Space Register, the BMC needs to use (Bus 30; Device 28-14; Function 7-0). Additionally, to access the CHA ALL1 PCI Configuration Space Register, the BMC needs to use (Bus 31; Device 14-0; Function 7-0).

Status: For the steppings affected, see the Summary Tables of Changes.

CWF19. CXL Mode Incorrectly Identifies ASPM L1 Aborts

Problem: In Compute Express Link (CXL) mode, the processor may incorrectly identify Active State Power Management (ASPM) L1 aborts as errors when the ARBMUX requests L1 and transitions to an Active State before the LTSSM reaches L1, resulting in IBSTERRRCRVSTS.RECOVCNT (bits 30:16; Offset 4E4h) overcounting.

Implication: Due to this erratum, software that relies upon the IBSTERRRCRVSTS.RECOVCNT bits may not function as expected.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF20. PCIe Root Port May Not Reduce Link Width

Problem: During a PCIe Link Width Degrade event on PCIe devices, the root port may not successfully transition to reduced link width due to a timeout in the PCIe Configuration.Linkwidth.Accept to Configuration.Lanenum.Wait state.

Implication: Due to this erratum, the PCIe root port may encounter unexpected recoveries, unexpected link width degrade attempts, uncorrectable errors, Surprise Link Down, and LTSSM errors.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF21. SYS_RESET_N Trigger May Lead to MCA_GPSB_TIMEOUT

Problem: When the SYS_RESET_N pin is triggered before the reset flow phase 5 completes, an unexpected microcode timeout may occur.

Implication: Due to this erratum, the system may hang with MCA_GPSB_TIMEOUT (IA32_MCi_STATUS.MCACOD=402h and IA32_MCi_STATUS.MSCOD=0B00hh).

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF22. Performance Monitoring Event For Memory Bound Stalls May Undercount

Problem: The Performance Monitoring events, MEM_BOUND_STALLS_LOAD (EventID: 34h) and MEM_BOUND_STALLS_IFETCH (EventID: 35h), and their subevents, will undercount the number of cycles of core initiated requests with latencies that exceed 256 cycles. A CMASK value of 255 may be used to count instances of this erratum.

Implication: Due to this erratum, software monitoring the events for Memory Bound Stalls may undercount.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF23. PMON Unit Control Unfreeze May Cause COUNTERVALUE Registers to Overcount

Problem: When the PMON Unit Control (PMONUNITCTRL) FREEZECOUNTERS (Offset: 2800h; Bit: 0) is set to 0 while the PMON GLOBALPMONFREEZE register is set to 1, the unit control may unexpectedly override the global control and unfreeze the PMONCNTR_0,1,2,3,4 COUNTERVALUE (Offsets 2808h, 2810h, 2818h, 2820h, 2828h; Bits [47:0]).

Implication: Due to this erratum, software that relies on the value of COUNTERVALUE may observe higher than expected values.

Workaround: None identified. The software should use only the unit control unfreeze when the global control freeze is set to 0.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF24. TRIG Packets May Contain ICNT Field When ICNTV Bit is Not Set

Problem: When a Intel® Processor Trace (Intel® PT) trigger tracing TRIG packet is generated following a trigger event, the TRIG packet will include the additional two-byte instruction count (ICNT) field even when the instruction count valid (ICNTV) bit (byte 1, bit 6) in the TRIG packet is not set.

Implication: Due to this erratum, trace decoding software may incorrectly decode the ICNT field as a separate packet, leading to incorrect trace decoding.

Workaround: Trace decoder software may mitigate this sighting by treating TRIG packets as always containing five bytes and ignoring the ICNT field in the last two bytes if ICNTV is not set.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF25. Intel® PT Event Trace Generates CFE and FUP After VMCS/PIP Packets During VM Entry

Problem: When the Intel® Processor Trace (Intel® PT) event trace feature is enabled, a VMLAUNCH/VMRESUME instruction will insert a Control Flow Event (CFE) packet and Flow Update Packet (FUP) packet into the trace output. These packets should be inserted before any VMCS or Paging Information Packet (PIP) packets, but are incorrectly inserted after those packets.

Implication: When this erratum occurs, the software trace decoder may be unable to properly decode the Intel® PT trace log.

Workaround: It may possible for the software trace decoder to workaround this sighting by detecting this situation and reordering the packets.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF26. Intel® PT Event Trace Generates Incorrect IP For FUP Packet During VM Entry

Problem: When the Intel® Processor Trace (Intel® PT) event trace feature is enabled, a VMLAUNCH/VMRESUME instruction will insert a Control Flow Event (CFE) alongside a Flow Update Packet (FUP) packet into the trace output. This FUP packet should include the Instruction Pointer (IP) address of the VMLAUNCH/VMRESUME instruction, but incorrectly includes the target IP of the VM entry instead.

Implication: When this erratum occurs, the software trace decoder may be unable to properly decode the Intel® PT trace log.

Workaround: It may possible for the software trace decoder to workaround this sighting by disregarding the IP included in the FUP packets after CFE VM entry packets, and binding the event to the next VMLAUNCH/VMRESUME instruction.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF27. Intel® PT TRIG Packet Not Generated When ContextEn is 0

Problem: The Intel® Processor Trace (Intel® PT) trigger tracing feature should be able to generate TRIG packets even when IA32_RTIT_STATUS [ContextEn] (MSR 571H, bit 1) is 0. Instead, TRIG packets are not generated when ContextEn is 0.

Implication: Due to this erratum, users of Intel® PT Trigger Tracing will not be able to tell from the trace that a trigger occurred outside of the main context where Intel® PT is enabled. ContextEn may be 0 due to the Intel® PT enable for the current privilege level not being set, the CR3 not matching the current CR3 filter, or being in a production enclave.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF28. Simultaneous Intel® PT TRIG and PTWRITE Packet May Result in Incorrect Trace Output

Problem: When the Intel® Processor Trace (Intel® PT) trigger tracing feature generates a TRIG packet in the same cycle as a PTWRITE instruction generates a packet, it is possible for the TRIG packet to be output between the PTWRITE header and payload.

Implication: When this erratum occurs, the software trace decoder will not correctly decode the trace.

Workaround: To avoid this erratum, software can avoid simultaneously enabling Intel® PT trigger tracing and PTWRITE.

Status: For the steppings affected, see the Summary Tables of Changes.

CWF29. Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results

Problem: The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called Cross-Modifying Code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor may see unexpected or unpredictable execution behavior from the processor that is executing the modified code.

Implication: In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the *Intel Architecture Software Developer's Manual Volume 3: System Programming Guide* including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.

Workaround: In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the section *Handling Self- and Cross-Modifying Code* in the *Intel Architecture Software Developer's Manual Volume 3: System Programming Guide*.

Status: For the steppings affected, see the Summary Tables of Changes.

6.0 Specification Changes

There are no specification changes in this specification update revision.

7.0 Specification Clarifications

SCL1. Intel® Xeon® 6900E+ Series Processors Do Not Support CXL Snoop Filter Capability Structure

Intel® Xeon® 6900E+ Series Processors do not support CXL Snoop Filter Capability Structure nor the Snoop Filter Capability registers as defined in the *Compute Express Link* (CXL*) Specification*, Revision 2.0, Section 8.2.5.15.

Figure 2. Compute Express Link* (CXL*) Specification, Revision 2.0, Section 8.2.5.15

8.2.5.15 CXL Snoop Filter Capability Structure

Offset	Register Name
0h	Snoop Filter Group ID
04h	Snoop Filter Capacity

8.2.5.15.1 Snoop Filter Group ID (Offset 0)

Bit Location	Attributes	Description
15:0	HwInit	Group ID - Uniquely identifies a snoop filter instance that is used to track CXL.cache devices below this Port. All Ports that share a single Snoop Filter instance shall set this field to the same value.
31:16	RsvdP	Reserved

8.2.5.15.2 Snoop Filter Effective Size (Offset 4)

Bit Location	Attributes	Description
31:0	HwInit	Capacity - Effective Snoop Filter Capacity representing the size of cache that can be effectively tracked by the Snoop Filter with this Group ID, in multiples of 64K.

8.0 Documentation Changes

There are no document changes in this specification update revision.