Intel® Core™ Processors (Series 3)

Specification Update

Supporting Intel® Core™ Series 3 Processors, formerly known as Wildcat Lake

Revision 003

July 2026

Document Number: 914196-003

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Revision History

Document Number	Revision Number	Description	Revision Date
914196	001	• Initial Revision	April 2026
	002	• Added Erratum: WCL034	May 2026
	003	• Added Errata: WCL035, WCL036, WCL037	July 2026

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
Intel® Core™ Series 3 Processors Datasheet, Volume 1 of 2	913965
Intel® Core™ Series 3 Processors Datasheet, Volume 2 of 2	917292

Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	874239
ACPI Specifications	www.acpi.info

Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

QDF Number – A several digit code used to distinguish between engineering samples. These processors are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. The NDA specification update has a processor identification information table that lists these QDF numbers and the corresponding product sample details.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – These describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – These include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle or until a stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Identification Information

Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 1. Component Identification

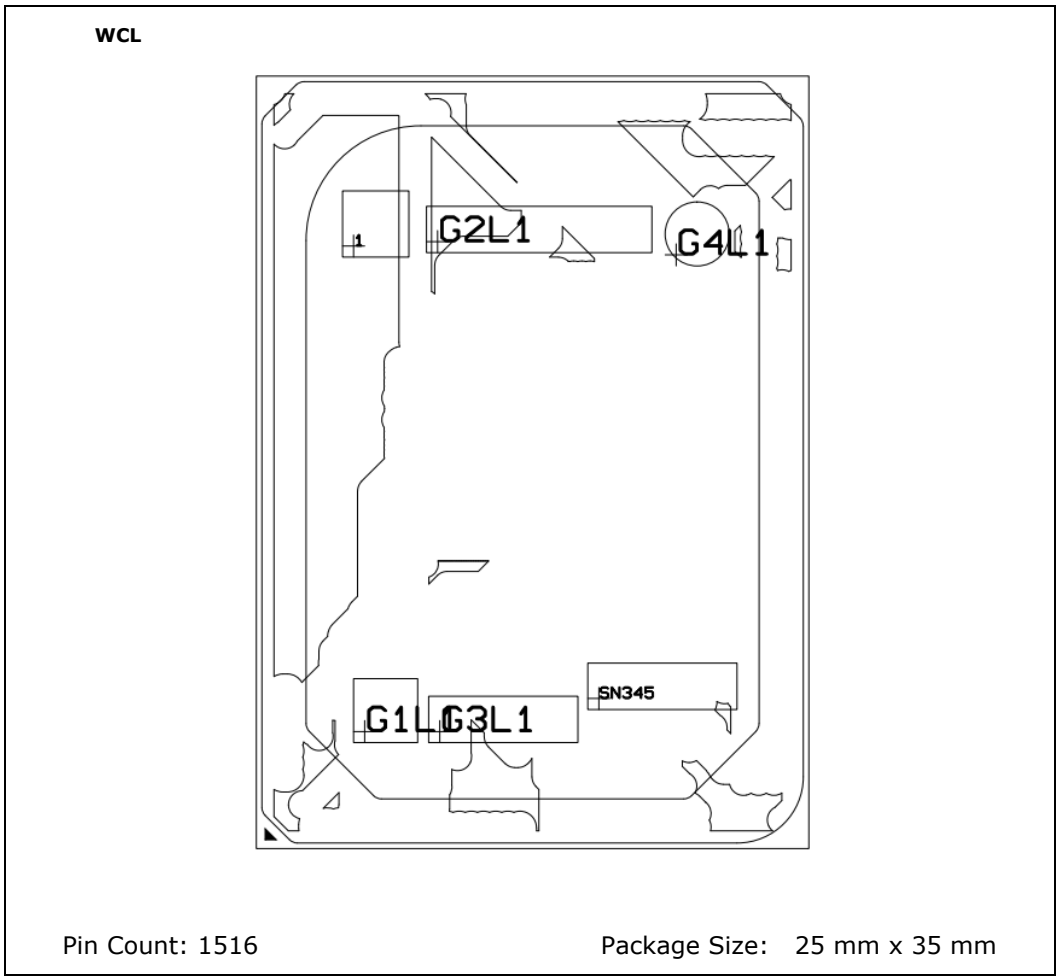
Product	Stepping	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
WCL	A1	D0651h	Reserved	0h	Dh	Reserved	0h	6h	5h	1h

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. Refer to Processor BIOS Specification for additional information. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

Component Marking Information

Figure 1. Wildcat Lake Processor Foveros Package BGA Top-Side Markings



Production (SSPEC):

SN345

G1L1: SPARK

G2L1: FPO

G3L1: SSPEC

G4L1: {ex}

Note: "1" is used to extract the unit visual ID (2D ID)

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Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed processor stepping. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank box)	This erratum is fixed or does not apply to the listed stepping or specification change does not apply to the listed stepping.

Status	Description
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

Errata Summary Table

Erratum ID	Processor Line	Title
	WCL	
WCL001	No Fix	Incorrect FROM_IP Value For an RTM Abort in BTM or BTS May be Observed
WCL002	No Fix	USB DbC or Device Mode Port When Exiting S4, S5, or G3
WCL003	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
WCL004	No Fix	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
WCL005	No Fix	DDR_DRAM_RESET_N Signal Transition Voltage Level During Power On
WCL006	No Fix	System Hang During S0ix Exit at Low Temperature and VCCPRIM_IO Low Voltage
WCL007	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
WCL008	No Fix	xHCI Controller Reset Due to Missing Link Credit From Device

Erratum ID	Processor Line	Title
	WCL	
WCL009	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
WCL010	No Fix	xHCI Unresponsive Due to Split Transaction Error
WCL011	No Fix	xHCI Out of Order ACK Due to LCRD1
WCL012	No Fix	Architectural Performance Monitoring Events For Last Level Cache Will Overcount
WCL013	No Fix	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
WCL014	No Fix	USB 2.0 Isochronous Missed Service Interval With Concurrent Bulk Traffic and Package C-States
WCL015	No Fix	Performance Monitoring Event For Memory Bound Stalls May Undercount
WCL016	No Fix	Bandwidth Allocation for USB 2.0 Periodic Devices Behind USB 3.2 Hub
WCL017	No Fix	I3C Interface Minimum Clock Timing Specifications
WCL018	No Fix	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
WCL019	No Fix	Performance Monitoring Event INT_VEC_RETIRED.MUL_256 May Undercount
WCL020	No Fix	Intel® PT Incorrect CR3-Filtering
WCL021	No Fix	Incorrect Last Branch From Value in BTS Branch Record During a Task Switch
WCL022	No Fix	Performance Monitoring Event MEMORY_ACTIVITY.STALLS_L2_MISS May Undercount
WCL023	No Fix	Performance Monitoring Event MEMORY_STALLS.L2 May Overcount
WCL024	No Fix	Certain BR_MISP_RETIRED Performance Monitoring Events May Overcount
WCL025	No Fix	LBR Event Logging IA32_LBR_x_INFO.PMCx_CNT Field May Undercount
WCL026	No Fix	Instruction Timeout VM Exit Will Not Set Guest RFLAGS.RF During #UD
WCL027	No Fix	Incorrect MSR Data Saved on WRMSRLIST VM-Exit for MSR 0h
WCL028	No Fix	Incorrect STI Blocking After ERETS When BTM/BTS Is Enabled
WCL029	No Fix	Incorrect Exception Behavior on IRET/FAR-RET With FRED Enabled
WCL030	No Fix	ICR Read May Not Generate an APIC-Access VM Exit

Erratum ID	Processor Line	Title
	WCL	
WCL031	No Fix	IAA Decompression Logic May Return Non-Deterministic Value of Bytes Completed in Completion Record
WCL032	No Fix	Remapping Hardware Does Not Perform a Reserved(0) Check in Interrupt Remap Table Entry
WCL033	No Fix	Non-Responsive USB Port After Disconnecting Full-speed Device
WCL034	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
WCL035	No Fix	LPDDR5/x VrefDQ Value JEDEC Specification Violation
WCL036	No Fix	Incorrect Guest RFLAGS.RF on VM Entry
WCL037	Fixed	System Hang Due to Insufficient P-core Voltage Ramp Rate

Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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Errata Details

WCL001	Incorrect FROM_IP Value For an RTM Abort in BTM or BTS May be Observed
Problem	During RTM (Restricted Transactional Memory) operation when branch tracing is enabled using BTM (Branch Trace Message) or BTS (Branch Trace Store), the incorrect EIP value (From_IP pointer) may be observed for an RTM abort.
Implication	Due to this erratum, the From_IP pointer may be the same as that of the immediately preceding taken branch.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL002	USB DbC or Device Mode Port When Exiting S4, S5, or G3
Problem	If a standalone xHCI controller USB port is configured in DbC mode and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1. The processor exits from S4 or S5, the port may remain in U2. 2. The port is connected to a USB 3.2 Gen 1x1 host controller when exiting from S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance Mode is disabled. 3. The port is connected to a USB 3.2 Gen 2x1 host controller when exiting from S4, S5, or G3, the port may enter an inactive state.
Implication	Due to this erratum, the processor standalone xHCI controller USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL003	xHCI USB 2.0 ISOCH Device Missed Service Interval
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets. Note: This issue has only been observed with a USB 3.2 Bulk Stream device.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL004	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
Problem	Intel® VT-d remapping hardware does perform Reserved(0) check on Page Snoop (PGSNP) field in scalable-mode Process Address ID (PASID) table entry when Snoop Control capability is defined as not available in the Extended Capability Register Offset 10h bit 7 (ECAP.SC=0)
Implication	There are no known functional implications due to this erratum. Intel has not observed this erratum with any commercially available software
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL005	DDR_DRAM_RESET_N Signal Transition Voltage Level During Power On
Problem	An unexpected transitional voltage level may be observed on the DDR_DRAM_RESET_N signal during Power-up/down sequence.
Implication	Intel has not observed any functional implications due to this erratum.
Workaround	None Identified
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL006	System Hang During S0ix Exit at Low Temperature and VCCPRIM_IO Low Voltage
Problem	When the processor operating temperature is below 5°C and the VCCPRIM_IO power rail voltage is below 1.25 V, internal wake signals timing for S0ix exit may be incorrect.
Implication	Due to this erratum, the system may hang with Machine Check Error MSCOD=PCU_MCA_MSEC_UCERR(0C02H) or hang with the CATERR# signal asserted.
Workaround	None identified
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL007	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL008	xHCI Controller Reset Due to Missing Link Credit From Device
Problem	The xHCI controller may not send LCRD (Link Credit) to the device after the link U0 state recovery is completed if a USB 3.2 device incorrectly stops sending LCRD.
Implication	When this erratum occurs, subsequence transfers from the device may not be completed and the xHCI host controller driver may initiate a host controller reset.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL009	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL010	xHCI Unresponsive Due to Split Transaction Error
Problem	When multiple USB 2.0 split transaction errors occur, the xHCI host controller may become unresponsive.
Implication	Due to this erratum, USB devices connected to the xHCI controller may not function.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL011	xHCI Out of Order ACK Due to LCRD1
Problem	A delay in the availability of LCRD1 (Link Credit 1) from a USB 3.2 hub, with two or more downstream USB 3.2 bulk endpoint devices engaged in SuperSpeedPlus concurrent transfers, may lead to the connected xHCI controller sending the ACK and Status of a transfer packet out of order.
Implication	Due to this erratum, a USB 3.2 bulk endpoint device may not respond to subsequent transfers. It may be possible for a device driver to recover the USB 3.2 device.

WCL011	xHCI Out of Order ACK Due to LCRD1
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL012	Architectural Performance Monitoring Events For Last Level Cache Will Overcount
Problem	The Performance Monitoring Event LONGEST_LAT_CACHE.REFERENCES (Event: 2EH, UMask: 4FH) and LONGEST_LAT_CACHE.MISS (Event: 2EH, UMask: 41H) will double count.
Implication	Due to this erratum, software monitoring these two events for last level cache will observe counts that are two times the actual value.
Workaround	None identified. Software may mitigate this issue by dividing the counter value by two.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL013	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
Problem	The UC-lock disable feature (MSR_MEMORY_CTRL bit [28] (MSR 33h)) may not cause a fault (#AC(4)) for a page split lock that accesses a page with non-WB memory type if the split lock disable (MSR_MEMORY_CTRL bit [29]) is not set.
Implication	Due to this erratum, system software may not be able to fully prevent bus locks due to locks to non-WB memory unless they use the split-lock disable feature to prevent bus locks due to splits. Intel has not observed this erratum with any commercially available software.
Workaround	None identified. Software using the UC-lock disable feature should also enable the split lock disable feature.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL014	USB 2.0 Isochronous Missed Service Interval With Concurrent Bulk Traffic and Package C-States
Problem	When there is concurrent USB 2.0 Isochronous IN and USB 3.2 Bulk traffic on the standalone xHCI controller, the USB 2.0 Isochronous device may not be serviced within the required service interval if the processor enters package C-State C6 or deeper state.
Implication	Due to this erratum, USB 2.0 isochronous IN devices may experience dropped packets. This issue has only been observed when using a USB 3.2 Bulk device that initiates frequent flow control.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL015	Performance Monitoring Event For Memory Bound Stalls May Undercount
Problem	The Performance Monitoring events, MEM_BOUND_STALLS_LOAD (EventID: 34h) and MEM_BOUND_STALLS_IFETCH (EventID: 35h), and their subevents, will undercount the number of cycles of core initiated requests with latencies that exceed 256 cycles. A CMASK value of 255 may be used to count instances of this erratum.
Implication	Due to this erratum, software monitoring the events for Memory Bound Stalls may undercount.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL016	Bandwidth Allocation for USB 2.0 Periodic Devices Behind USB 3.2 Hub
Problem	The xHCI controller may allocate more bandwidth than can be supported when two or more USB 2.0 periodic devices (Isochronous or Interrupt) are connected behind a USB 3.2 hub.
Implication	Due to this erratum, the xHCI controller may not service the USB 2.0 periodic devices within the required service interval. Intel has only observed missed service intervals when two USB 2.0 Isochronous cameras are connected behind a USB 3.2 Hub and are streaming at 1080p or higher resolution, sometimes resulting in video disruptions on the second camera stream.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL017	I3C Interface Minimum Clock Timing Specifications
Problem	The following clock timing specifications of Serial IO and Integrated Sensor Hub (ISH) I3C interfaces may not meet the minimum timing requirements listed in the MIPI specification version 1.0: • Serial IO and ISH: SCL and SDA fall time when operating in I2C mode for Fast Mode (400 Kbps) and Fast Mode Plus (1 Mbps) speeds. • Serial IO and ISH: SCL rise time when operating in I2C mode for Fast Mode (400 Kbps). • Serial IO: SCL low time when operating in I2C mode for Fast Mode (400 Kbps) and Fast Mode Plus (1 Mbps) speeds.
Implication	There are no known functional implications due to this erratum and Intel has not observed this erratum with any commercially available system.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL018	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
Problem	The performance monitoring events TOPDOWN.BACKEND_BOUND_SLOTS (Event A4h, UMask 02h) and IDQ_BUBBLES.* (Event 9Ch, UMask 01h) may not count when the processor is in the C0.2 power sub-state, which is entered via the TPAUSE or UWAIT instructions. This erratum also impacts the accuracy of MSR_PERF_METRICS fields Frontend Bound, Backend Bound, and Fetch Latency (MSR 329h, Bits [23:16], [31:24] and [55:48]).
Implication	Due to this erratum, these performance monitoring events and the fields in MSR_PERF_METRICS may be inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL019	Performance Monitoring Event INT_VEC_RETIRED.MUL_256 May Undercount
Problem	The performance monitoring event INT_VEC_RETIRED.MUL_256 (Event E7h, Umask 80h) may not count VPMULLQ instructions.
Implication	Due to this erratum, the performance monitoring event may report lower counts than expected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL020	Intel® PT Incorrect CR3-Filtering
Problem	When the Intel® Processor Trace (Intel® PT) CR3-filtering mechanism is enabled using the CR3Filter bit in IA32_RTIT_CTL MSR (MSR 570h, bit 7), CR3 control register bits [63:52] are not compared with the IA32_RTIT_CR3_MATCH MSR (MSR 572h) value.
Implication	Due to this erratum, software that relies upon the IA32_RTIT_CTL MSR (bit 7) may function incorrectly.
Workaround	None identified. Software may mitigate this erratum by copying the CR3 register value into IA32_RTIT_CR3_MATCH MSR.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL021	Incorrect Last Branch From Value in BTS Branch Record During a Task Switch
Problem	When branch tracing is enabled using branch trace store (BTS) during a task switch, the processor reports the linear address of the branch target in the branch record field "Last Branch from" instead of the linear address of the instruction from which branch was taken.
Implication	Due to this erratum, debug tools relying on BTS may misinterpret control flow.
Workaround	None identified. Software should avoid using BTS to determine the accuracy of branch prediction.

WCL021	Incorrect Last Branch From Value in BTS Branch Record During a Task Switch
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL022	Performance Monitoring Event MEMORY_ACTIVITY.STALLS_L2_MISS May Undercount
Problem	The performance monitoring event MEMORY_ACTIVITY.STALLS_L2_MISS (Event 47h, UMASK 05h) may undercount for cases of streaming partial loads.
Implication	Due to this erratum, performance monitoring counters may undercount values for this event and the Top-down Microarchitecture Analysis (TMA) L2_Bound may be over-estimated for streaming partial loads.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL023	Performance Monitoring Event MEMORY_STALLS.L2 May Overcount
Problem	The performance monitoring event MEMORY_STALLS.L2 (Event 46h, UMASK 02h) may overcount for cases of streaming partial loads.
Implication	Due to this erratum, performance monitoring counters may overcount for this event and the Top-down Microarchitecture Analysis (TMA) L2_Bound may be over-estimated for streaming partial loads.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL024	Certain BR_MISP_RETIRED Performance Monitoring Events May Overcount
Problem	The performance monitoring events BR_MISP_RETIRED.COND_TAKEN_FWD_COST and BR_MISP_RETIRED.COND_TAKEN_BWD_COST (Event C5h, UMaskExt 80h) may overcount when a branch misprediction happens right after the processor clears speculative instructions.
Implication	Due to this erratum, when PEBS (Processor Event-Based Sampling) is enabled and triggered on an overcount, then the instruction pointer (EventingIP) and retire latency fields may point to the wrong instruction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL025	LBR Event Logging IA32_LBR_x_INFO.PMCx_CNT Field May Undercount
Problem	Under a complex set of microarchitectural conditions, when LBR (Last Branch Record) Event Logging (EN_LBR_LOG bit 35 in IA32_PERFEVTSELx MSR (186h to 18Fh)) is enabled for performance monitoring counters, some event counts may not be logged to PMCx_CNT fields in IA32_LBR_x_INFO MSR (1200h to 121Fh).
Implication	Due to this erratum, the processor may report incorrect lower values in LBR's record data IA32_LBR_x_INFO.PMCx_CNT.

WCL025	LBR Event Logging IA32_LBR_x_INFO.PMCx_CNT Field May Undercount
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL026	Instruction Timeout VM Exit Will Not Set Guest RFLAGS.RF During #UD
Problem	When the VM-Execution Control "Instruction timeout" (bit 31) is set to 1, and a VM exit occurs with basic exit reason 75 (Instruction timeout) during the delivery of an invalid opcode (#UD) exception, the processor will not set Guest RFLAGS.RF (bit 16).
Implication	Due to this erratum, when the VMM resumes the guest at the same instruction, and an instruction breakpoint is set in the guest, it may trigger double instruction breakpoints (#DB).
Workaround	A mitigation for this erratum is for VMMs to set guest RFLAGS.RF before resuming guest execution following an instruction timeout VM exit.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL027	Incorrect MSR Data Saved on WRMSRLIST VM-Exit for MSR 0h
Problem	When both “Enable MSR-list instructions” VM-Execution control (bit 6) and the “use MSR bitmaps” VM-Execution control (bit 28) are set to 1, and if the MSR address is 0h (P5_MC_ADDR) and the corresponding bit in the write bitmap is 1, then an execution of WRMSRLIST in VMX non-root will cause a VM exit with exit qualification '0' , the same as MSR index (0h). The VMCS field MSR-data (2402h, 2403h) is set to 0 instead of the actual value read from the memory.
Implication	Due to this erratum, software that relies on the MSR-data field may incorrectly write 0 to MSR 0h.
Workaround	A mitigation for this erratum is for software to check for VM exits with exit reason 79 (WRMSRLIST) and exit qualification 0. If the MSR index is 0h, software should use the original memory operand value instead of the MSR-data field.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL028	Incorrect STI Blocking After ERETS When BTM/BTS Is Enabled
Problem	When branch trace message (BTM) or branch trace store (BTS) is enabled using IA32_DEBUGCTL MSR (1D9h, bits 7:6) and if the Event Return to Supervisor (ERETS) instruction executes with RFLAGS.IF=1 and tempCS[24] =1 (CS selector of the return context, bit 24), STI blocking (Set Interrupt Flag) may be cleared if ERETS generates a BTM/BTS trace message. As a result, interrupts may be delivered immediately after ERETS instead of being delayed until the next instruction completes.
Implication	Due to this erratum, software that relies on STI blocking after ERETS may function incorrectly when BTM or BTS is enabled.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL029	Incorrect Exception Behavior on IRET/FAR-RET With FRED Enabled
Problem	When FRED (Flexible Return and Event Delivery) transitions are enabled (CR4.FRED=1), an execution of IRET or FAR-RET to a target code segment (CS) whose selector's RPL value is greater than the CPL may generate an exception other than #GP. In addition, the processor incorrectly sets the accessed bit in the code-segment descriptor.
Implication	Due to this erratum, software that expects a #GP or expects the accessed bit to remain unchanged may function incorrectly.
Workaround	A mitigation for this erratum is for software to clear the accessed bit in the code-segment descriptor during the exception-handling flow for IRET/FAR-RET when FRED is enabled.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL030	ICR Read May Not Generate an APIC-Access VM Exit
Problem	When "virtualize APIC accesses" and "IPI virtualization" are both 1, and both "virtual-interrupt delivery" and "APIC-register virtualization" are 0, a memory-mapped read of the Interrupt Command Register (ICR) may return data from the virtual-APIC page (VICR) instead of generating an APIC-access VM exit.
Implication	Due to this erratum, software that relies on an APIC-access VM exit for ICR reads may function incorrectly.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL031	IAA Decompression Logic May Return Non-Deterministic Value of Bytes Completed in Completion Record
Problem	When an Intel® In-Memory Analytics Accelerator (IAA) device decompress operation has a non-zero Source 1 Size, and if the sum of Drop Initial Bits of Analytics Engine Configuration and State (AECS; offset 1DCh) and Ignore End Bits (Decompression Flags, bits [8:6]) is equal to Source 1 Size times 8, the operation correctly drops all the Source 1 data. However, if the operation also results in a recoverable output buffer overflow (Completion Record Status Code 0Bh), then the value of Bytes Completed in the Completion Record (bytes 4 to 7) or the value of Drop Initial Bits field in the AECS may be incorrect.
Implication	Due to this erratum, the incorrect values may lead to the subsequent decompress operation, that is, the continuation of the same job producing an incorrect result.
Workaround	None identified. It is possible for software to contain a workaround for this issue.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL032	Remapping Hardware Does Not Perform a Reserved(0) Check in Interrupt Remap Table Entry
Problem	Remapping hardware does not perform Reserved(0) check on b[127:HAW+64] of the Interrupt Remap Table Entry for a Posted Interrupt.

WCL032	Remapping Hardware Does Not Perform a Reserved(0) Check in Interrupt Remap Table Entry
Implication	Due to this erratum, system software violating VT-d architecture requirement by programming non-zero reserved values in b[127:HAW+64] of Interrupt Remap Table entry for Posted Interrupt may not fault on current processors but may fault on future processors. Intel has not observed this sighting/erratum with any commercially available system.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL033	Non-Responsive USB Port After Disconnecting Full-speed Device
Problem	Disconnecting a USB full-speed device from the USB port while the xHCI controller is in the process of sending the Start of Frame may cause the USB 2.0 functionality to become unresponsive for that specific port.
Implication	Due to this erratum, USB 2.0 devices may not be recognized on the USB port until a host controller reset occurs. Intel has only observed this behavior in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL034	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the stack pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL035	LPDDR5/x VrefDQ Value JEDEC Specification Violation
Problem	The LPDDR5/x VrefDQ value, as read from LPDDR5 Mode registers MR14 OP[6:0] and MR15 OP[6:0], is set to 360 mV when the speed is above 3200 MHz, while the LPDDR5 JEDEC specification JESD209-5C (Revision of JESD209-5B, June 2021) requires VrefDQ to be less than or equal to 180 mV.
Implication	There are no known functional implications due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL036	Incorrect Guest RFLAGS.RF on VM Entry
Problem	When the user-interrupt feature is enabled (CR4.UINTR=1) and a VM exit occurs during user-interrupt delivery due to a fault, the processor may incorrectly set the guest RFLAGS.RF (bit 16) to 1 on VM entry.
Implication	Due to this erratum, software that relies upon the guest RFLAGS.RF may function incorrectly.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

WCL037	System Hang Due to Insufficient P-core Voltage Ramp Rate
Problem	When multiple P-cores exit low power states simultaneously during intensive ring utilization, the internal P-core voltage ramp rate may be insufficient
Implication	Due to this erratum, the system may hang with Machine Check Exception INTERNAL TIMER (MCACOD=400h, MSCOD=000h).
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

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Specification Changes

None.

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Specification Clarification

None.

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Document Change

None.

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