



The Converged Vector ISA: Intel[®] Advanced Vector Extensions 10

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Revision History

Revision Number	Description	Date
1.0	Initial release of the document.	June 2023
2.0	Updated Section 1.2, "Introduction to Intel® AVX10," to remove the 32-bit mask register limitation.	December 2023
3.0	Removed references to 256-bit maximum vector register size, enumeration of vector-length support, and 256-bit instructions supporting embedded rounding.	March 2025

CHAPTER 1

CONVERGED VECTOR ISA: INTEL® ADVANCED VECTOR EXTENSIONS 10

Intel® Advanced Vector Extensions 10 (Intel® AVX10) introduces a modern vector Instruction Set Architecture (ISA) that will be supported across future Intel® processors. This new ISA includes all the richness of the Intel® Advanced Vector Extensions 512 (Intel® AVX-512) with additional features and capabilities enabling it to seamlessly run across Performance-cores and Efficient-cores, delivering performance and consistency across all platforms. It also introduces a new enumeration approach based on version, reducing the burden on the developer to check multiple feature bits for the platform. Intel AVX10 extends and enhances the capabilities of Intel AVX-512 to benefit all Intel® products and will be the vector ISA of choice moving into the future.

1.1 BACKGROUND

In 2016, Intel launched a major update to its vector instruction set with the launch of a high-performance vector ISA named Intel Advanced Vector Extensions 512 (Intel AVX-512). The Intel AVX-512 ISA included several new features and capabilities over the Intel® Advanced Vector Extensions 2 (Intel® AVX2) ISA including 512-bit vector registers, a discrete feature enumeration methodology, 16 additional vector registers, 8 mask registers, 512-bit vector length embedded rounding, and a large suite of new instructions. Over time, Intel AVX-512 evolved to include support for shorter vector length versions of instructions (128 and 256 bits) along with many additional instructions, each with its own CPUID feature flag, driving performance and capabilities for Performance-core targeted vector workloads.

The Intel® AVX family of instruction sets (Intel AVX, Intel AVX2, and Intel AVX-512) have successfully gained wide industry adoption for a variety of applications including video processing, cryptography, HPC, AI, gaming, and others. Building on this momentum, Intel is announcing the next generation Intel AVX10 as the standard for ISA, supported by future Efficient-cores (E-cores) and Performance-cores (P-cores). Intel AVX10 will enable the ecosystem to seamlessly integrate solutions across products and platforms and innovate for future generations of our products for years to come.

1.2 INTRODUCTION TO INTEL® AVX10

Intel AVX10 includes all the capabilities and features of the Intel AVX-512 ISA. In addition, this ISA supports a new enumeration scheme that reduces the number of CPUID feature flags needing to be checked for feature support. Intel AVX10 is designed to run on future Intel P-core and E-core-based processors, allowing applications to seamlessly move across platforms.

There are three motivating factors for Intel AVX10:

1. To continue to support a high performance, vector ISA with all the richness of features of the existing Intel AVX-512 ISA.
2. To create a converged vector ISA based on Intel AVX-512 that will be supported on all future Intel processors.
3. To ease the developer task of verifying CPUID feature support.

The converged version of the Intel AVX10 vector ISA will include Intel AVX-512 vector instructions with an AVX512VL feature flag and eight 64-bit mask registers. This converged version will be supported on both P-cores and E-cores. Thus, Intel AVX10 carries forward all the benefits of Intel AVX-512 from the Intel® Xeon® with P-core product lines, supporting the key instructions, vector and mask register lengths, and capabilities that have comprised the ISA to date. Future processors will continue to support all Intel AVX-512 instructions ensuring that legacy applications continue to run without impact.

1.3 ENUMERATION

The developer community has provided feedback that the current Intel AVX-512 enumeration method has become increasingly unwieldy over time. As new instructions were introduced, they were assigned a new CPUID feature flag that would need to be checked to determine processor support. As of future Intel Xeon processors with P-cores, codenamed Granite Rapids, there are expected to be more than 20 discrete Intel AVX-512 feature flags. To address this, Intel AVX10 introduces a new versioning approach to enumeration: a Vector ISA feature bit specifying Intel AVX10 support and an Intel AVX10 ISA Version Number.

The Intel AVX10 ISA Version Number will be inclusive and monotonically increasing. A developer can expect that Intel AVX10 Version N+1 will include all the features and capabilities included in Version N. With the stated goal of minimizing developer impact, a new version of the Intel AVX10 ISA can be expected to include a significant suite of new instructions and capabilities, delivering sufficient additional value to justify the associated software enablement effort. In rare cases, a discrete CPUID feature flag may be allocated for a segment-specific feature or in the case of an interim launch in between new Intel AVX10 versions.

The Intel AVX-512 ISA will be frozen as of the introduction of Intel AVX10 and all CPUID feature flags will continue to be enabled on future P-core processors for legacy support. All new subsequent vector instructions will be enumerated only as part of Intel AVX10. Apart from a few special cases, those instructions will be supported at all vector lengths.

							AVX10
				AVX512_FP16		AVX512_FP16	
				AVX512_VPOPCNTDQ, AVX512_VBMI2, VAES, GFNI, VPCLMULQDQ, AVX512_BITALG		AVX512_VPOPCNTDQ, AVX512_VBMI2, VAES, GFNI, VPCLMULQDQ, AVX512_BITALG	
				AVX512_BF16		AVX512_BF16	
				AVX512_VNNI		AVX512_VNNI	
		AVX512_VBMI, AVX512_IFMA		AVX512_VBMI, AVX512_IFMA		AVX512_VBMI, AVX512_IFMA	
AVX512F, AVX512CD, AVX512BW, AVX512DQ		AVX512F, AVX512CD, AVX512BW, AVX512DQ		AVX512F, AVX512CD, AVX512BW, AVX512DQ		AVX512F, AVX512CD, AVX512BW, AVX512DQ	
AVX/AVX2		AVX/AVX2		AVX/AVX2		AVX/AVX2	
Intel® Xeon® Scalable Processors		Intel® Core™ Processors		2nd Gen Intel® Xeon® Scalable Processors		5th Gen Intel® Xeon® Scalable Processors	
				3rd Gen Intel® Xeon® Scalable Processors for 4S/8S Servers		4th Gen Intel® Xeon® Scalable Processors	
						AVX/AVX2	
						AVX/AVX2	
						AVX/AVX2	

Figure 1-1. Intel® AVX-512 Feature Flags Across Intel® Xeon® Processor Generations vs. Intel® AVX10

1.4 PERFORMANCE BENEFITS

In addition to the previously stated usability benefits, several additional performance-based benefits of Intel AVX10 include:

- Intel AVX2-compiled applications, re-compiled to Intel AVX10, should realize performance gains without the need for additional software tuning.
- Intel AVX2 applications sensitive to vector register pressure will gain the most performance due to the 16 additional vector registers and new instructions.
- Highly-threaded vectorizable applications are likely to achieve higher aggregate throughput when running on E-core-based Intel Xeon processors or on Intel® products with performance hybrid architecture.

Existing Intel AVX-512 applications should see the same performance when compiled to Intel AVX10. Intel AVX10 will continue to deliver the best-in-class performance for AI, scientific, and other high-performance codes. New Intel® AVX10 libraries, compilers, and tool support will also be provided to help application developers realize the best achievable performance for all vector lengths.

1.5 AVAILABILITY

Intel AVX10 Version 1 will be introduced for early software enablement and supports the subset of all the Intel AVX-512 instruction set available as of future Intel Xeon processors with P-cores, codenamed Granite Rapids, that is forward compatible to Intel AVX10. This version will serve as the transition base version from Intel AVX-512 to Intel AVX10.

Intel AVX10 Version 2 will include a suite of new Intel AVX10 instructions covering new AI data types and conversions, data movement optimizations, and standards support. All new instructions will be supported at 128-, 256-, and 512-bit vector lengths with limited variances. All Intel AVX10 versions will implement the new versioning enumeration scheme.

		Intel® AVX-512	Intel® AVX10.1 (pre-enabling)	Intel® AVX10.2
		128/256/512-bit FP/Int 32 vector registers 8 mask registers 512-bit embedded rounding Embedded broadcast Scalar/SSE/AVX “promotions” Native media additions HPC additions Transcendental support Gather/Scatter Flag-based enumeration Intel® Xeon P-core only	128/256/512-bit FP/Int 32 vector registers 8 mask registers 512-bit embedded rounding Embedded broadcast Scalar/SSE/AVX “promotions” Native media additions HPC additions Transcendental support Gather/Scatter Version-based enumeration Intel® Xeon P-core only	New data movement, transforms and type instructions 128/256/512-bit FP/Int 32 vector registers 8 mask registers 512-bit embedded rounding Embedded broadcast Scalar/SSE/AVX “promotions” Native media additions HPC additions Transcendental support Gather/Scatter Version-based enumeration Supported on P-cores, E-cores
Intel® AVX	Intel® AVX2			
128/256-bit FP 16 registers NDS (and AVX128) Improved blend MASKMOV Implicit unaligned	Float16 128/256-bit FP FMA 256-bit int PERMD Gather			

Figure 1-2. Intel® ISA Families and Features

1.6 CONCLUSION

Intel AVX10 represents a major shift to supporting a high-performance vector ISA across future Intel processors. It allows the developer to maintain a single code-path that achieves high performance across all Intel platforms with the minimum of overhead checking for feature support. Future development of the Intel AVX10 ISA will continue to provide a rich, flexible, and consistent environment that optimally supports both Server and Client products.