Intel® Core™ Ultra Processors (series 2) for Edge Platforms

Datasheet Addendum

January 2025

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Revision History

Date	Revision	Description
January 2025	001	Initial release.

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1.0 Introduction

This Intel® Core™ Ultra Processors (series 2) (formerly known as Arrow Lake-S) Datasheet Addendum is to be used as supplement documentation that covers Edge platform-specific features .

Intel® Core™ Processors includes the Intel® Performance Hybrid architecture, P-Cores for performance, and E-Cores for Efficiency. Refer to Table 3 for availability in Intel processor lines.

The S-Processor Line is offered in a 2-Chip Platform that includes the Processor Die and Platform Controller Hub (PCH-S) die.

Note: This document serves as a supplementary documentation, please ensure all required specifications from the **Intel® Core™ Ultra 200S Series Processors Datasheet** and **Intel® 800 Series Chipset Family Platform Controller Hub (PCH) Datasheet** are met prior to using this document, unless specifically noted otherwise.

1.1 Terminology

Table 1. Terminology

Term	Description
BIOS	Basic Input/Output System
BL	Baseline
CLK	Clock
CMTG	Common Master Timing Generator
DP	DisplayPort
ECC	Error Correction Code
GT	Graphic Technology
HDMI	High-Definition Multimedia Interface
HW	Hardware
I/O	Input / Output
PCH-S	Platform Controller Hub-Desktop
PLL	Phase-locked Loop
PWM	Pulse Width Modulation
SoC	System on Chip
SW	Software
TDP	Processor Base Power (a.k.a Thermal Design Power)
VM	Virtual Memory
VMM	Virtual Machine Monitor
VSYNC	Vertical Reference Synchronization

1.2 Reference Documents

Table 2. Reference Document

Document	Document No./Location
Ultimate Guide for Displays in Embedded Applications	Please contact your Intel Representative

1.3 Supported Package and Die Plan

Table 3. Processor Lines Package and Die Plan

Processor Line Segment (P+E+X[e])	Die Type	Package (mm)	TDP	PCH
S-series (8+16+4)	8P + 16E	45 x 37.5	35W	PCH-S
			65W	
S-series (8+12+4)			35W	
			65W	
S-series (6+8+4)	6P + 8E		35W	
			65W	
S-series (6+4+2)			35W	
			65W	

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2.0 Graphics and Display

2.1 Genlock

2.1.1 Overview

Multichip Genlock is a feature which helps in synchronizing frames across displays connected to multiple systems. This feature ensures that all the monitors that are part of the Genlock configuration displays the same scan line of the same frame within +/- Δ pixels.

Figure 1. High Level Block Diagram - Multichip Genlock Configuration

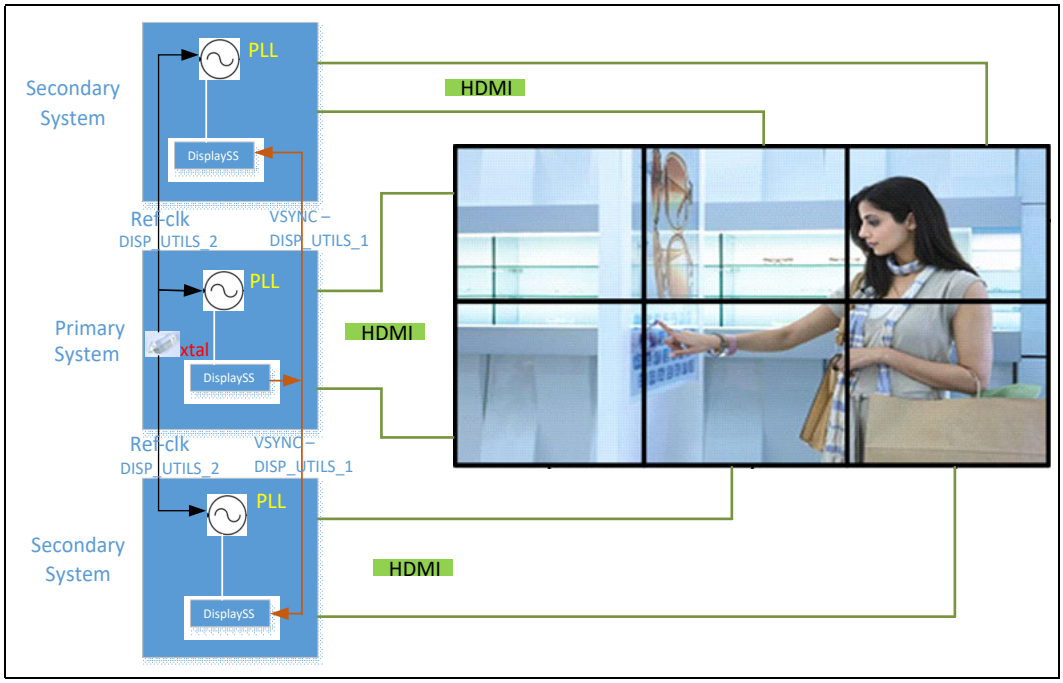


Figure 1 above illustrates a wall of 2x3 displays connected to 3 systems in a Multichip Genlock configuration, where one system acts as a genlock primary generating the clock and two other systems, as genlock secondary receiving the clock.

Each Genlock configuration allows:

- All display PLLs are running off of the same reference clock
- All displays receive their vertical reference at the same time (via a separate wire or combined with the reference clock).

Note: Having the frame start at the same time is the responsibility of this feature. Flipping the right frame across displays is the responsibility of the application software.

Genlock requires a primary-secondary topology to operate. One of the systems runs as a primary, providing the clock and vertical sync to other systems (secondary) in the configuration so that Genlock can be achieved (refer to Figure 1). Supported display interfaces for Genlock are HDMI* and DP*.

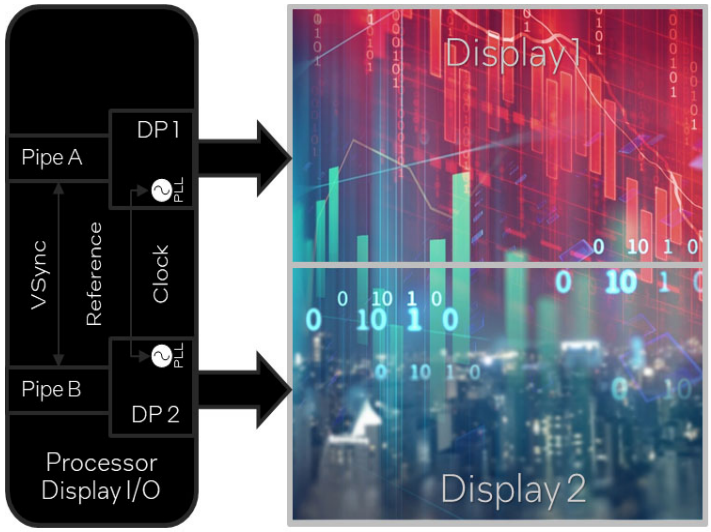
2.2 Pipelock

2.2.1 Overview

Pipelock is defined as the synchronization between ports driven by a single GPU. Genlock is defined as the synchronization between ports driven from multiple GPUs. For timing synchronization, the display hardware supports port sync, CMTG and Genlock features. For a single GPU use case, it is recommended to use (legacy) port sync for tiled DP display and Genlock for synchronization of multiple external displays.

Note: Pipelock is a sub-feature of Genlock that vsync timing of all secondary pipes under Genlock is synced on the primary pipe's timing. Pipelock is activated when enabling the Genlock as the primary pipe.

Figure 2. High Level Diagram of a Single Host iGPU Pipelock



The figure above illustrates the single host iGPU Pipelock where one of the pipes acts as a primary display, and its vsync timings are synchronized with the secondary displays. Refer to the Ultimate Guide for Displays in Embedded Applications for more details.

2.3 EDID Management/Lock Display

Windows* OS provides a way to manage EDID via monitor.inf, but its functionality is limited and does not meet the requirements of certain embedded use cases. Adding the EDID Management feature to the Intel Graphics driver is a solution to overcome these limitations. EDID Management feature includes EDID read, EDID override/remove-override and EDID lock/unlock for the monitors that are connected to the system. The Intel® Graphics Control Library interface can be used to enable these operations on the supported platforms.

- EDID read: This operation reads the monitor's EDID and uses this information to set various display configurations.
- EDID override: This operation provides the ability to manipulate the default EDID that comes with the monitor. The advantage of EDID override is that the Windows* OS can set the requested target mode on the monitor and can also recognize the monitor when it is not physically connected to the system.
- EDID lock: By default, Windows* OS triggers the Hot Plug Detect (HPD) signal when a monitor is turned off or unplugged. When two or more monitors are connected, and if one of the monitors is either turned off, malfunctioned, or unplugged, an HPD event occurs, and the Windows applications will be re-oriented resulting in a new display configuration. By design and behavior, this is triggered by the HPD signal being asserted. However, this is an undesirable behavior for some embedded use cases. EDID lock was introduced to overcome this issue. When EDID lock is enabled on a monitor, the Intel® Graphics driver ignores the HPD event, and the system retains the original display configuration regardless of the status of the locked monitor (turned off, unplugged, or malfunctioned).

Refer to the Ultimate Guide for Displays in Embedded Applications for more details.

2.4 Bezel Correction

This feature allows users to adjust the image to correct the physical monitor bezel so images that span across multiple monitors can be visually adjusted. Current versions of the Intel® Graphics Command Center now support this capability. The following figures show illustrations of how bezel correction can be used. The top illustration shows how the image will appear without enabling bezel correction. The bottom illustration shows how the image will appear after enabling bezel correction and setting the value to a desired number. Refer to the Ultimate Guide for Displays in Embedded Applications for more details.

Figure 3. Without Bezel Correction

Figure 4. With Bezel Correction

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