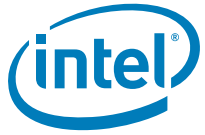
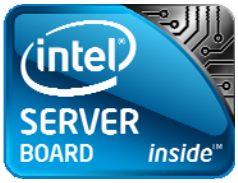


Intel® Server Board S5400SF

Technical Product Specification

Intel order number: D92944-007



Revision 2.02

May 2010

Enterprise Platforms and Services Division - Marketing

Revision History

Date	Revision Number	Modifications
September 2007	1.00	Initial release.
July 2008	2.00	▪ Updated supported CPU table. ▪ Added memory type support table. ▪ Updated password clear procedure. ▪ Updated supported BIOS POST error code table. ▪ Updated BIOS Setup Utility options section.
August 2008	2.01	Updated processor naming.
May 2010	2.02	Deleted CCC and CNCA.

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The Intel® Server Board S5400SF may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel Corporation server boards support peripheral components and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel's own chassis are designed and tested to meet the intended thermal requirements of these components when the fully integrated system is used together. It is the responsibility of the system integrator that chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

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1. Introduction

This Technical Product Specification (TPS) provides board-specific information detailing the features, functionality, and high-level architecture of the Intel® Server Board S5400SF.

In addition, design level information for specific subsystems can be obtained by ordering the External Product Specifications (EPS) or External Design Specifications (EDS) for a given subsystem. EPS and EDS documents are not publicly available. They are only made available under non-disclosure agreement (NDA) with Intel and must be ordered through your local Intel representative. See the *Reference Documents* section at the end of this document for a complete list of available documents.

The Intel® Server Board S5400SF may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Refer to the *Intel® Server Board S5400SF Specification Update* for published errata.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Server Board Overview
- Chapter 3 – Functional Architecture
- Chapter 4 – Server Management
- Chapter 5 – System BIOS
- Chapter 6 – Connector and Header Locations and Pin-outs
- Chapter 7 – Jumper Block Settings
- Chapter 8 – Intel Light-Guided Diagnostics
- Chapter 9 – Power and Environmental Specifications
- Chapter 10 – Regulatory and Certification Information
- Appendix A – Integration and Usage Tips
- Appendix B – POST Code Diagnostic LED Decoder
- Appendix C – Post Error Messages and Handling
- Appendix D – EFI Shell Commands
- Appendix E – Supported Intel® Server Chassis
- Appendix F – 1U PCI Express* Gen 2 Riser Card
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system meets the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to

determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The Intel® Server Board S5400SF is a monolithic printed circuit board with features that were designed to support the high-density High Performance Computing (HPC) server market.

2.1 Intel® Server Board S5400SF Feature Set

Feature	Description
Processors	771-pin LGA sockets supporting one or two Intel® Xeon® processors
Memory	16 Keyed DIMM slots supporting fully buffered DIMM technology (FBDIMM) memory. Only 240-pin DDR2-667 or DDR2-800 FBDIMMs are supported on this server board.
Chipset	Intel® Chipset, which includes the following components: ▪ Intel® 5400 Memory Controller Hub Chipset ▪ Intel® 6321ESB I/O Controller Hub
On-board Connectors/Headers	External I/O connections: ▪ Stacked PS/2 ports for keyboard and mouse ▪ RJ-45 Serial B port ▪ Two RJ-45 NIC connectors for 10/100/1000 Mb connections ▪ Two USB 2.0 ports ▪ Video Connector Internal connectors/headers: ▪ One USB port header, capable of providing two USB 2.0 ports ▪ One DH-10 Serial A header ▪ Six SATA ports via the Intel® 6321ESB I/O Controller Hub supporting 3 Gb/s and integrated Software (SW) RAID 0/1/10 support ▪ One 44pin (power + I/O) ATA/100 connector for optical drive support ▪ One Intel® Remote Management Module 2 (Intel® RMM2) connector (use of Intel® RMM2 is optional) ▪ One Intel® I/O Expansion Module connector supporting any of the following: o Dual GB NIC Intel® I/O Expansion Module (Optional) o External SAS Intel® I/O Expansion Module (Optional) o Infiniband* I/O Expansion Module (Optional) ▪ SSI-compliant 24-pin control panel header ▪ SSI-compliant 24-pin main power connector, supporting the ATX-12 V standard on the first 20 pins ▪ 8-pin +12 V processor power connector
System Fan Support	Six 4-pin fan headers supporting two processor fans, and up to four system fans One 26-pin custom system fan header for use in an Intel® Server Chassis
Add-in Adapter Support	One full-height riser card slot supporting PCI Express* x16 Gen 2 riser card
On-board Video	ATI* ES1000 video controller with 32 MB DDR SDRAM
On-board Hard Drive Controller	Six Intel® 6321ESB I/O Controller Hub 3 Gb/s SATA ports Intel® Embedded Server RAID Technology II with SW RAID levels 0/1/10. Optional support for SW RAID 5 with activation key.
LAN	Two 10/100/1000 Intel® 82563EB PHYs supporting Intel® I/O Acceleration Technology
System Management	Support for Intel® System Management Software 2.0 and later

2.2 Server Board Layout

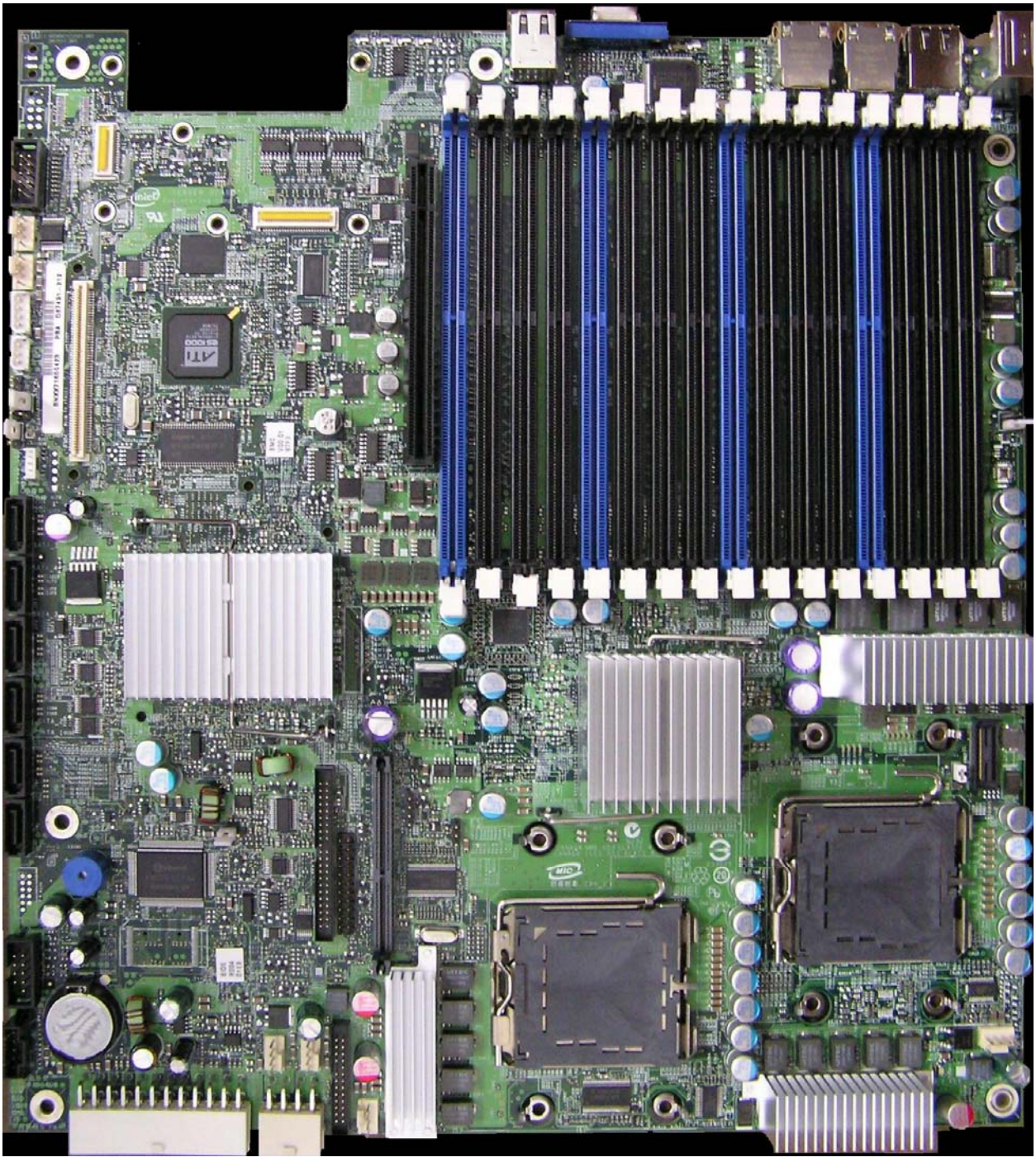


Figure 1. Server Board Layout

2.3 Connector and Component Locations

The following figure shows the board layout of the server board. Each connector and major component is identified by a letter, and a description is given below the figure.

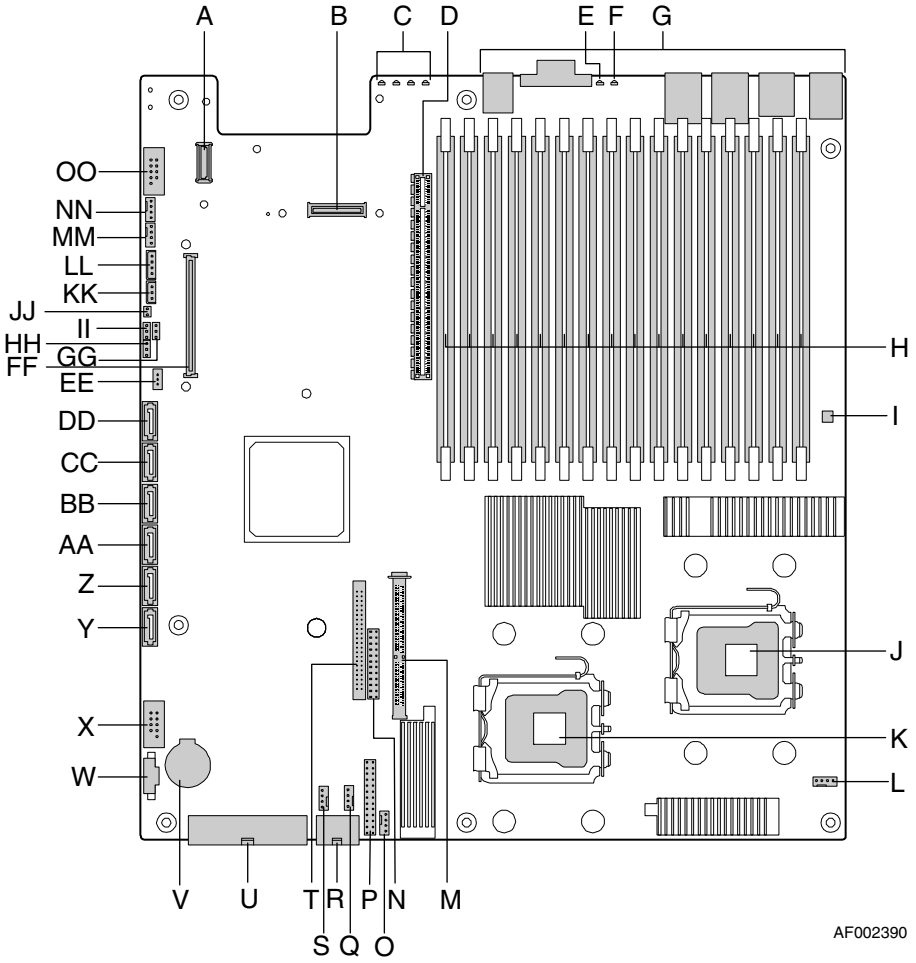
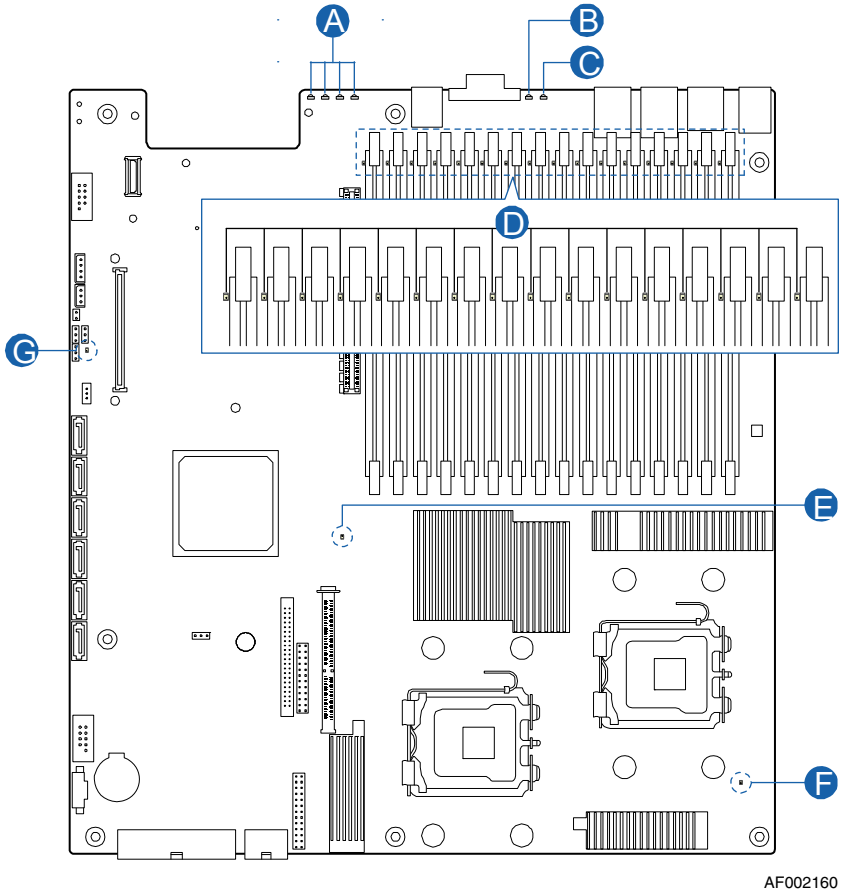


Figure 2. Components and Connector Location Diagram

Table 1. Major Components and Connectors

A	Intel® RMM2 NIC Connector	V	Battery
B	I/O Module Option Connector	W	Power Supply Management Connector
C	POST Code Diagnostic LEDs	X	Dual Port USB 2.0 Header (USB0-1)
D	PCI Express* Riser Connector (x16 Gen 2)	Y	SATA0
E	System Identification LED - Blue	Z	SATA1
F	System Status LED – Green/Amber	AA	SATA2
G	External I/O Connectors	BB	SATA3
H	FBDIMM Memory Sockets	CC	SATA4
I	Serial 'B' Port Configuration Jumper	DD	SATA5
J	Processor 1 Socket	EE	SATA SW RAID 5 Activation Key Connector
K	Processor 2 Socket	FF	Intel® Remote Management Module 2 Connector
L	Processor 1 Fan	GG	Integrated BMC FRU Update Jumper
M	Bridge Board Connector	HH	CMOS Clear Jumper
N	SSI 24-pin Control Panel Header	II	Password Clear Jumper
O	Processor 2 Fan	JJ	Chassis Intrusion Switch Header
P	Fan Board Connector	KK	3-pin IPMB Header
Q	System Fan 2	LL	4-pin IPMB Header
R	CPU Power Connector	MM	System Fan 4
S	System Fan 1	NN	System Fan 3
T	ATA-100 Optical Drive Connector (Power+IO)	OO	Serial 'A' Header
U	Main Power Connector		

2.4 Intel® Light-Guided Diagnostics LED Locations

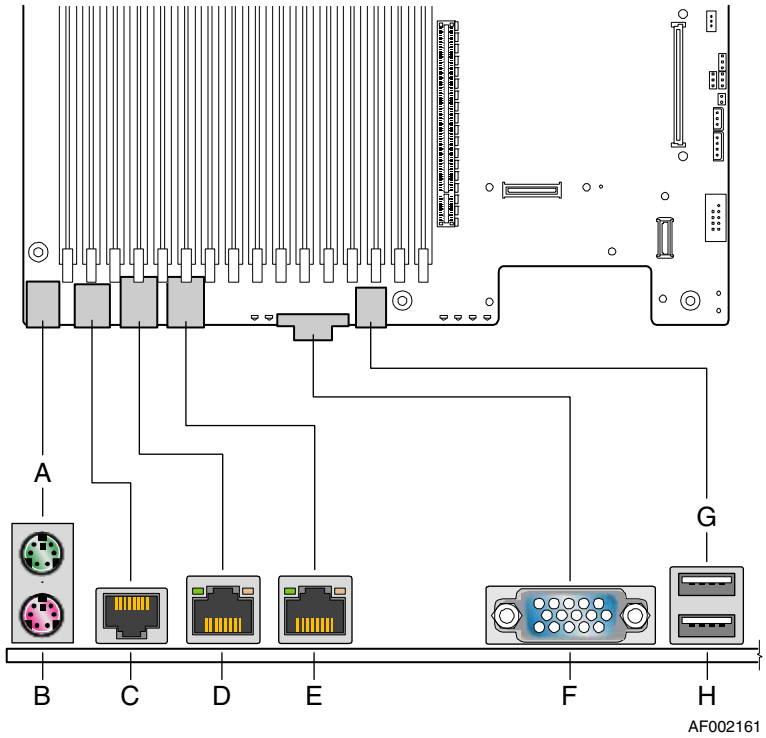


	Description		Description
A	Post Code Diagnostic LEDs	E	Processor 2 Fault LED
B	System ID LED	F	Processor 1 Fault LED
C	Status LED	G	5 V Standby LED
D	DIMM Fault LEDs		

Figure 3. Intel Light-Guided Diagnostics LED Location Diagram

2.5 External I/O Connector Locations

The drawing below shows the layout of the rear I/O components for the server board.



A	PS/2 Mouse	E	NIC port 2 (1 Gb)
B	PS/2 Keyboard	F	Video
C	Serial Port B	G	USB port 5
D	NIC port 1 (1 Gb)	H	USB port 6

Figure 4. Intel® Server Board S5400SF External I/O Layout

3. Functional Architecture

The architecture and design of the Intel® Server Board S5400SF is based on the Intel® 5400 Chipset. The chipset is designed for systems using the Intel® Xeon® processor 5000 sequence with front-side bus speeds of 1066 MHz, 1333 MHz, or 1600 MHz. The chipset is made up of two main components: the Intel® 5400 Memory Controller Hub Chipset (Intel® 5400 MCH Chipset) for the host bridge and the Intel® 6321ESB I/O Controller Hub for the I/O subsystem.

This chapter provides a high-level description of the functionality associated with each chipset component and the architectural blocks that make up this server board.

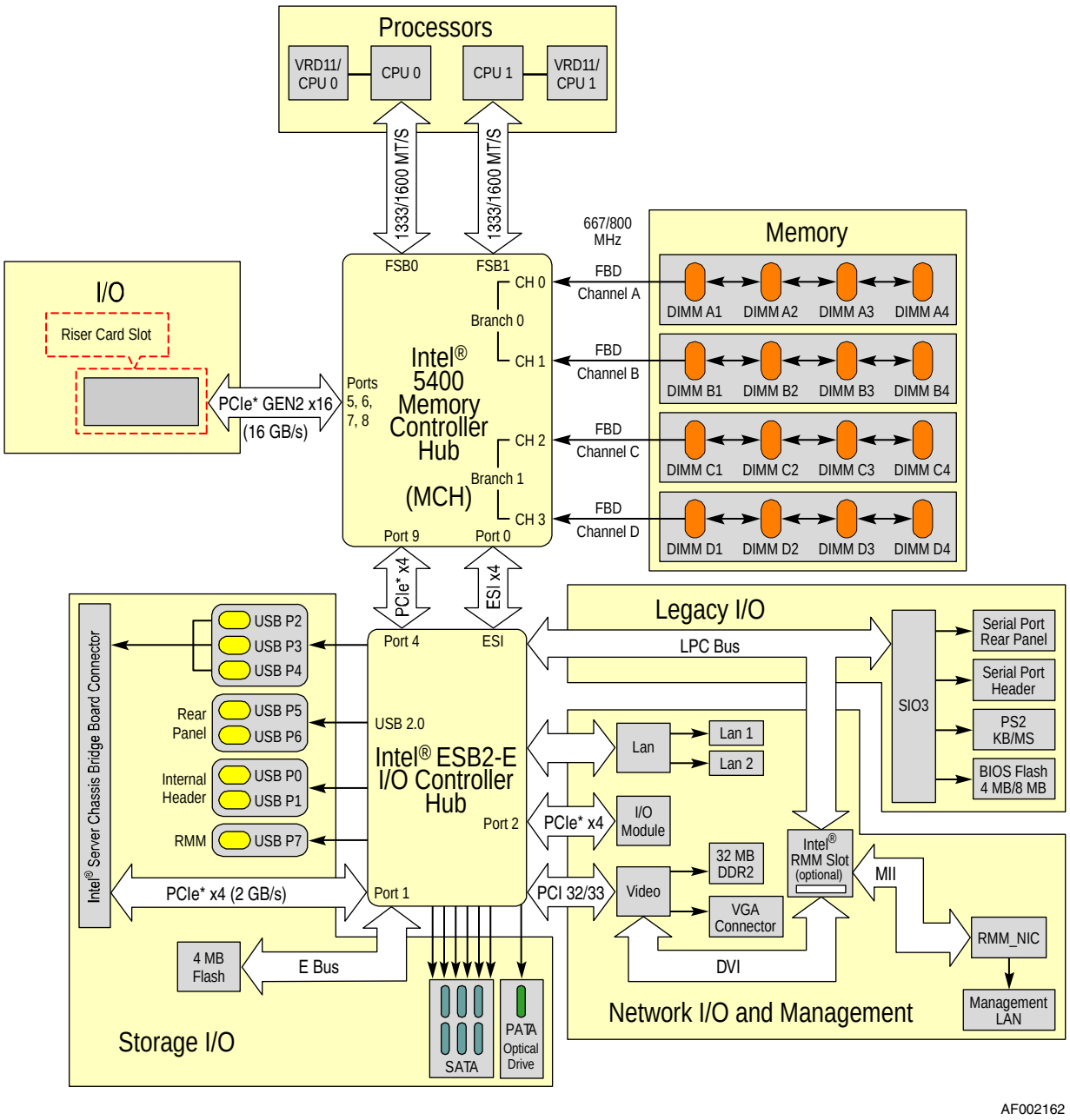


Figure 5. Server Board Functional Block Diagram

3.1 Processor Support

The Intel® Server Board S5400SF supports up to two Intel® Xeon® Processors 5000 Sequence. See

Table 2. Processor Support Matrix for a list of supported processors.

Note: Only Intel® Xeon® processors listed in

Table 2 are supported on this server board.

Support for Intel® Xeon® processor 5100 series and 5300 series is limited to Low Voltage SKUs only on this server platform.

Table 2. Processor Support Matrix

Processor Family	Core Count	System Bus Speed	Core Frequency	Cache	Watts
Intel® Xeon® processor 5138	2	1066 MHz	2.13 GHz	4 MB shared	35
Intel® Xeon® processor 5148	2	1333 MHz	2.33 GHz	4 MB shared	40
Intel® Xeon® processor L5310	4	1066 MHz	1.60 GHz	8 MB shared	50
Intel® Xeon® processor L5320	4	1066 MHz	1.86 GHz	8 MB shared	50
Intel® Xeon® processor L5335	4	1333 MHz	2.00 GHz	8 MB shared	50
Intel® Xeon® processor 5200 Series	2	All	All	6 MB shared	120 Watt or less
Intel® Xeon® processor 5400 Series	4	All	All	12 MB shared	120 Watt or less

3.1.1 Processor Population Rules

Note: Although the server board does support dual-processor configurations consisting of different processors that meet the criteria defined below, Intel does not perform validation testing of this configuation. For optimal system performance in dual-processor configurations, Intel recommends that identical processors be installed.

When using a single-processor configuration, the processor must be installed into the processor socket labeled CPU1. No terminator is required in the second processor socket when using a single-processor configuration.

When two processors are installed, the following population rules apply:

- Both processors must be of the same processor family.
- Both processors must have the same front-side bus speed.
- Both processors must have the same cache size.
- Processors with different speeds can be mixed in a system, if the prior rules are met. If this condition is detected, all processor speeds are set to the lowest common denominator (highest common speed).
- Processor stepping within a common processor family can be mixed as long as it is listed in the processor specification updates published by Intel Corporation.

The following table describes mixed processor conditions and recommended actions for all Intel® Server Boards and Systems that use the Intel® 5400 Chipset. Errors fall into one of two categories:

- **Fatal:** If the system can boot, it goes directly to the error manager, regardless of whether the “Post Error Pause” setup option is enabled or disabled.
- **Major:** If “Post Error Pause” setup option is enabled, the system goes directly to the error manager. Otherwise, the system continues to boot and no prompt is given for the error. The error is logged to the error manager.

Table 3. Mixed Processor Configurations

Error	Severity	System Action
Processor family not Identical	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the error into the system event log (SEL) ▪ Alerts the Integrated BMC of the configuration error with an IPMI command. ▪ Does not disable the processor ▪ Displays “0194: Processor family mismatch detected” message in the error manager ▪ Halts the system
Processor cache not identical	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the error into the SEL ▪ Alerts the Integrated BMC of the configuration error with an IPMI command. ▪ Does not disable the processor ▪ Displays “0192: Cache size mismatch detected” message in the error manager ▪ Halts the system
Processor frequency (speed) not identical	Major	The BIOS detects the error condition and responds as follows: ▪ Adjusts all processor frequencies to the lowest common denominator ▪ Continues to boot the system successfully If the frequencies for all processors cannot be adjusted to be the same, then the BIOS: ▪ Logs the error into the SEL ▪ Displays “0197: Processor speeds mismatched” message in the error manager ▪ Halts the system
Processor microcode missing	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the error into the SEL ▪ Alerts the Integrated BMC of the configuration error with an IPMI command. ▪ Does not disable the processor ▪ Displays “816x: Processor 0x unable to apply microcode update” message in the error manager ▪ Pauses the system for user intervention
Processor FSB speeds not identical	Fatal	The BIOS detects the error condition and responds as follows: ▪ Logs the error into the system event log (SEL) ▪ Alerts the Integrated BMC of the configuration error with an IPMI command. ▪ Does not disable the processor ▪ Displays “0195: Processor Front-side Bus speed mismatch detected” message in the error manager ▪ Halts the system

3.1.2 Multiple Processor Initialization

IA-32 processors have a microcode-based bootstrap processor (BSP) arbitration protocol. The BSP starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an application processor (AP).

The Intel® 5400 Memory Controller Hub Chipset (Intel® 5400 MCH Chipset) has two processor front-side buses (FSB), each accommodating a single dual-core or quad-core Intel® Xeon® processor. At reset, the hardware arbitration chooses one BSP from the available processor cores per FSB. However, the BIOS power-on self-test (POST) code requires only one processor for execution. This requires the BIOS to elect a system BSP using registers in the Intel® 5400 MCH Chipset. The BIOS cannot guarantee which processor will be the system BSP, only that a system BSP will be selected. In the remainder of this document, the system BSP is referred to as the BSP.

The BSP is responsible for executing the BIOS POST and preparing the server to boot the operating system. At boot time, the server is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR) driven by the programmable interrupt controller (PIC) and non-maskable interrupt (NMI)).

As part of the boot process, the BSP wakes each AP. When awakened, an AP programs its memory type range registers (MTRRs) to be identical to those of the BSP. All APs execute a halt instruction with their local interrupts disabled. If the BSP determines that an AP exists that is a lower-featured processor or that has a lower value returned by the CPUID function, the BSP switches to the lowest-featured processor in the server. The system management mode (SMM) handler expects all processors to respond to an SMI.

3.1.3 Enhanced Intel SpeedStep® Technology

Enhanced Intel SpeedStep® Technology helps reduce average system power consumption and potentially improves system acoustics by allowing the system to dynamically adjust processor voltage and core frequency.

3.1.4 Intel® Extended Memory 64 Technology (Intel® EM64T)

Intel® Xeon® processors support Intel® Extended Memory 64 Technology (EM64T). Intel® 64 architecture delivers 64-bit computing on server platforms when combined with supporting software. Intel® 64 architecture improves the performance by allowing systems to address more than 4 gigabytes (GB) of both virtual and physical memory.

The following table identifies the three Intel® EM64T operating modes.

Table 4. Intel® EM64T Operating Modes

Legacy Mode	Compatibility Mode	64-Bit Mode
32-bit operating system 32-bit applications 32-bit drivers	64-bit operating system 32-bit applications 64-bit drivers 4 GB address space GPRs are 32-bit	64-bit operating system 64-bit applications 64-bit drivers 64-bit flat virtual address space GPRs are 64-bit

Intel® EM64T operating modes are not manually selectable. The system BIOS, hardware drivers, operating system, and applications that are in use determine the operating mode in use.

In support of Intel® EM64T, the system BIOS does the following:

- Detects whether the processor is Intel® Extended Memory 64 Technology capable
- Initializes the SMBASE for each processor
- Detects the appropriate SMRAM State Save Map used by the processor
- Enables Intel® EM64T during memory initialization, if necessary

3.1.5 Execute Disable Bit Feature

The Execute Disable Bit feature (XD bit) is an enhancement to the Intel® IA-32 architecture. An IA-32 processor that supports the Execute Disable Bit feature can prevent data pages from being used by malicious software to execute code. An IA-32 processor with the Execute Disable Bit feature can provide memory protection in either of the following modes:

- Legacy protected mode if Physical Address Extension (PAE) is enabled.
- IA-32e mode when 64-bit extension technology is enabled (Entering the IA-32e mode requires enabling PAE).

The Execute Disable Bit does not introduce any new instructions. It requires operating systems to operate in a PAE-enabled environment and establish a page-granular protection policy for memory. The Execute Disable Bit can be enabled and disabled in the BIOS setup. The default behavior is enabled.

3.1.6 Multi-Core Processor Support

The BIOS does the following:

- Initializes all processor cores
- Installs all NMI handlers for all dual-core processors
- Leaves initialized AP in CLI/HLT loop
- Initializes stack for all APs

The BIOS setup provides an option to selectively enable or disable multi-core processor support. The default behavior is enabled.

The BIOS creates additional entries in the ACPI MP tables to describe the dual core processors. The SMBIOS Type 4 structure shows only the physical processors installed. It does not describe the virtual processors.

The BIOS creates entries in the *Multi-Processor Specificatio*n, Version 1.4 tables to describe dual-core processors.

3.1.7 Intel® Virtualization Technology

Intel® Virtualization Technology is designed to support multiple software environments sharing the same hardware resources. Each software environment may consist of operating system and applications. The Intel® Virtualization Technology can be enabled or disabled in the BIOS setup. The default behavior is disabled.

Note: If the setup option is changed to enable or disable the Intel® Virtualization Technology setting in the processor, the user must perform an AC power cycle for the change to take effect.

3.1.8 Platform Environmental Control Interface (PECI)

PECI is a thermal management interface that uses a single wire bus interface to provide a communication channel between an Intel® processor and an external monitoring device (PECI host controller). The PECI host controller on this server board is ADT7490*. Intel® Xeon® processors 5000 sequence provides processor temperature via the PECI interface.

The PECI feature configuration and support is controlled via the processor MSR (Model Specific Registers). All installed processors must support PECI. The BIOS polls all installed processors for PECI support. If the PECI feature is supported, then the BIOS enables PECI by programming the MSRs.

The processor temperature monitoring and management is accomplished by the Integrated BMC firmware. It is the responsibility of the Integrated BMC firmware to enable the PECI polling circuitry.

3.1.9 Common Enabling Kit (CEK) Design Support

The server board complies with Intel's Common Enabling Kit (CEK) processor mounting and heatsink retention solution. The server board ships with a CEK spring snapped onto the underside of the server board, beneath each processor socket. The heatsink attaches to the CEK, over the top of the processor and the thermal interface material (TIM). See the following figure for the stacking order of the chassis, CEK spring, server board, TIM, and heatsink.

The CEK spring is removable, allowing for the use of non-Intel heatsink retention solutions.

Note: The processor heatsink and CEK spring shown in the following figure are for reference purposes only. The actual processor heatsink and CEK solutions compatible with this generation server board may be of a different design.

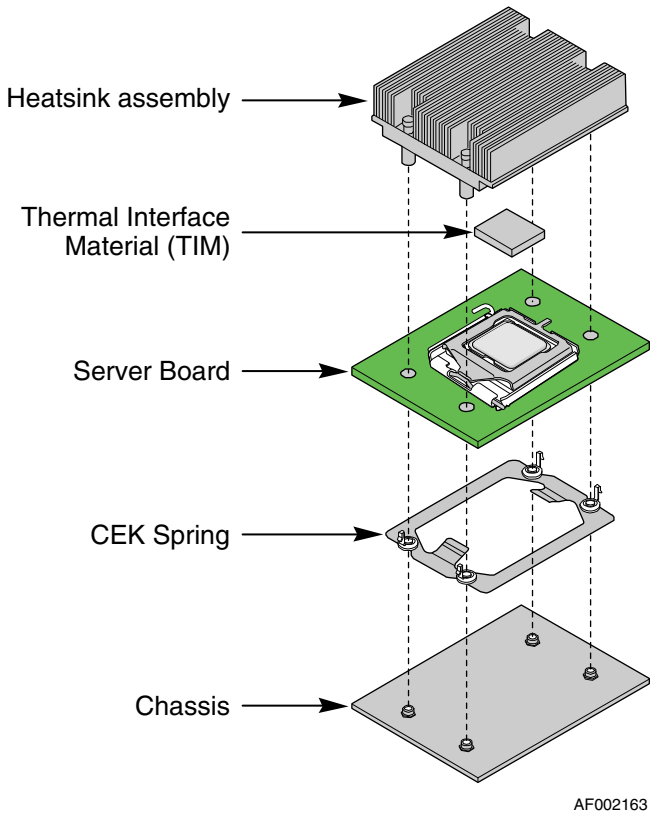


Figure 6. CEK Processor Mounting

3.2 Intel® 5400 Memory Controller Hub Chipset (Intel® 5400 MCH Chipset)

This section describes the general functionality of the memory controller hub as it is implemented on the Intel® Server Board S5400SF.

The Memory Controller Hub (MCH) is a single 1520-pin FCBGA package, which includes the following core platform functions:

- Processor Front-Side Buses
- System Memory Controller
- Enterprise Southbridge Interface
- PCI Express* Ports
- Power Management
- FBD Thermal Management
- SMBus Interface

Additional information about the MCH functionality can be obtained from the *Intel® 5400 Memory Controller Hub External Design Specification*.

3.2.1 Processor Front-Side Buses

The MCH supports two independent point-to-point processor front-side bus (FSB) interfaces. Each front-side bus is 64 bits wide. Depending on the installed processor, the interfaces operate using a 266 MHz,333 MHz, or 400 MHz clock, which is then quad pumped to support 1066 MT/s, 1333 MT/s, and 1600 MT/s transfer rates respectively. The following table provides the theoretical bandwidth and transfer rates for each type of supported processor.

Table 5. Processor Front-Side Buses

FSB Clock (Quad pumped)	FSB Transfer Rate	FSB BW
266 MHz (1066 MHz)	1066 MT/s	8 GB/s
333 MHz (1333 MHz)	1333 MT/s	10.7 GB/s
400 MHz (1600 MHz)	1600 MT/s	12.8 GB/s

The MCH supports 38-bit host addressing and decoding up to 128 GB of the processor's memory address space.

3.2.2 Snoop Filter

The MCH supports a 24 MB Snoop Filter (SF), which eliminates traffic on the snooped front-side bus of the processor being snooped. By removing snoops from the snooped bus, the full bandwidth is available for other transactions. Supporting concurrent snoops effectively reduces performance degradation attributable to multiple snoop stalls.

The Snoop Filter has the following features:

- Snoop Filter tracks total of 24 MB of processor L2 cache lines, this is equivalent to: (24 * (2^{20}) byte)/64 byte CL = 393,216 cache lines.
- The SF is configured in 4 K sets organized as a 4 DID Affinity x 24 Way x 4 K Set - Associativity array. This is equivalent to (2^{12} Sets) x 24 Way x 4 DID = 393,216 tag entries
- 4 x 24 Affinity Set - Associativity will allocate/evict entries within the 24-way corresponding to the assigned affinity group if the SF look up is a miss. Each SF look up will be based on 96-way (4x24 ways) look up.
- The size of the snoop filter Tag RAM is: 4096 sets * 4 affinities * 24 ways * 33 bits/affinity/ set/way = 1,622,016 bytes
- The size of the snoop filter Victim Ram is: 4096 sets * 4 affinities * 8 bits = 16,384 bytes
- The size of the snoop filter Random ROM is: 1024 addresses * 16 bits = 2,048 bytes
- The Snoop Filter is operated at 2x of the MCH core frequency, i.e., 533 MHz to provide 267 MLUU/s (where a Look-Up-Update operation is a read followed by a write operation to the tag).
- The maximum lookup and update bandwidth of the Snoop Filter is equal to the maximum requested bandwidth from both FSBs. The lookup and update bandwidth from I/O coherent transactions have to share the bandwidth with both FSBs per request weighted-round-robin arbitration.

- The Snoop Filter lookup latency is four SF-clocks or two MCH core clocks to support single snoop stall in an idle condition (single request issued from either bus). If both buses make requests simultaneously, the snoop-filter always selects bus 0 first. In such a scenario, bus 0 request has one snoop-stall and bus 1 request has two snoop-stalls.
- Active Way/Invalid/E/M/Pseudo-Random replacement algorithm with updates on lookups and invalidates; Invalid/Pseudo-Random replacement algorithm with updates on lookups and invalidates.
- Tag entries support a 38-bit physical address space. The MCH supports an external address space of 38 bits as well.
- ECC coverage with correction of single bit errors and detection of double bit errors (SEC-DED).
  - Invalid/Random Array does not implement ECC or parity protection. A bit failure results in the selection of the wrong victim entry and may have a minimal impact on performance. However, the coherency engine resolves the conflict and guarantee correctness.

3.2.3 System Memory Controller and Memory Subsystem

The MCH masters four fully buffered DIMM (FBDIMM) memory channels. The four memory channels are organized in to two branches. Each branch is supported by a separate memory controller. The two channels on each branch operate in lock step to increase FBD bandwidth. A branch transfers 16 bytes of payload/frame on Southbound lanes and 32 bytes of payload/frame on Northbound lanes.

The host frequency is the speed of the memory interface of the Intel® 5400 Chipset. This frequency determines the speed at which the chipset completes a memory transaction. The gear ratio determines the relative speed between the processor interface and the memory interface. The BIOS supports 667 MHz and 800 MHz FB-DIMMs, and automatically selects and configures the host frequency and gear ratio.

The following table shows the theoretical peak bandwidth of the Front-Side Bus and Memory Bus when the server board is configured with supported processor and memory configurations.

Table 6. Front-Side Bus and Memory Bus Bandwidth

FSB Clock (Quad pumped)	FSB Transfer Rate	FSB BW	FBD Channel Frequency	DRAM Clock	DRAM Transfer Rate	FBD BW per Branch
266 MHz **(1066 MHz)**	1066 MT/s	8 GB/s	3.2 GHz	266 MHz	533 MT/s	8.4 GB/s
			4 GHz	333 MHz	667 MT/s	10.6 GB/s
333 MHz **(1333 MHz)**	1333 MT/s	10.7 GB/s	3.2 GHz	266 MHz	533 MT/s	8.4 GB/s
			4 GHz	333 MHz	667 MT/s	10.6 GB/s
400 MHz **(1600 MHz)**	1600 MT/s	12.8 GB/s	3.2 GHz	266 MHz	533 MT/s	8.4 GB/s
			4 GHz	320 MHz	640 MT/s[1]	10.2 GB/s
			4.8 GHz	400 MHz	800 MT/s	12.8 GB/s

[1] In system configurations that utilize processors supporting a 1600 MHz FSB and 667 MHz FBDIMMs concurrently, the actual DRAM transer rate is 640 MT/s due to a set gear ratio inside the MCH.

Note: The use of 800 MHz FBDIMMs is only supported with Intel® Xeon® processors that support a 1600 MHz front-side bus. Using these FBDIMMs with processors that support slower front-side bus frequencies is not supported on this server board.

On the Intel® Server Board S5400SF, a pair of channels becomes a branch where Branch 0 consists of channels A and B, and Branch 1 consists of channels C and D. The first DIMM slot for each memory channel is identified in "blue" as shown in the following illustration.

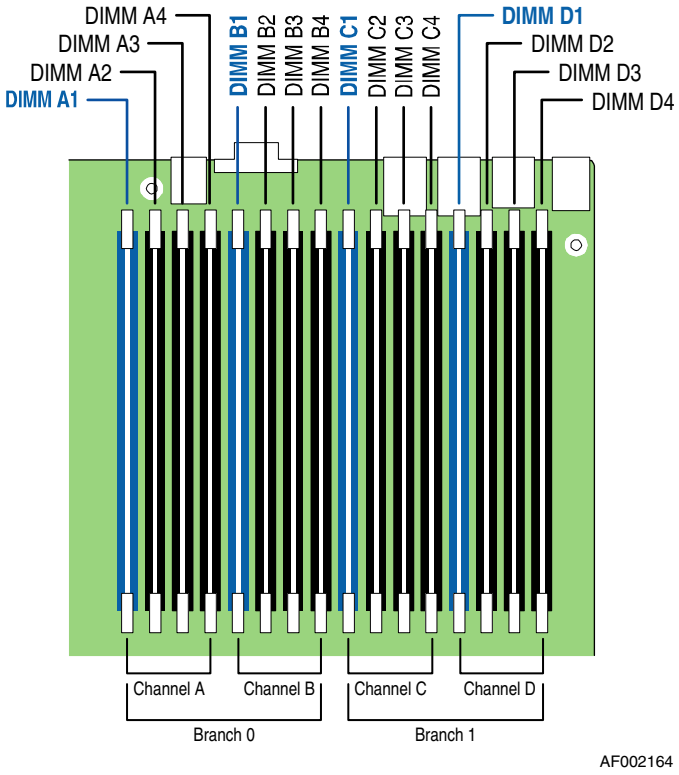


Figure 7. Memory Slot Layout

3.2.3.1 Supported Memory

The server board can support up to sixteen DDR2-667 or DDR2-800 Fully Buffered DIMMs (FBD memory). Using 8 GB DIMMs, the maximum supported memory configuration equals 128 GB of physical memory (validated).

Note: DDR2 DIMMs that are not fully buffered are NOT supported on this server board.

See the *Intel® Server Board S5400SF Tested Memory List* for a complete list of supported memory for this server board.

The following table lists the currently supported memory types:

Table 7. Supported Memory Types

FBDIMM-667 CL5 & FBDIMM-800 CL5/6 Memory Matrix						
DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# SDRAM Devices	# Address bits Row/Bank/Column	# of Ranks
512 MB	64 Mbit x 72	512 Mbit	64 Mbit x 8	9	14/10/2	1
1 GB	128 Mbit x 72	512 Mbit	64 Mbit x 8	18	14/10/2	2
1 GB	128 Mbit x 72	512 Mbit	128 Mbit x 4	18	14/11/2	1
1 GB	128 Mbit x 72	512 Mbit	128 Mbit x 8	9	14/10/3	1
2 GB	256 Mbit x 72	512 Mbit	128 Mbit x 4	36	14/11/2	2
2 GB	256 Mbit x 72	1 Gbit	256 Mbit x 4	18	14/11/3	1
2 GB	256 Mbit x 72	1 Gbit	128 Mbit x 8	18	14/10/3	2
4 GB	512 Mbit x 72	1 Gbit	256 Mbit x 4	36	14/11/3	2
4 GB	512 Mbit x 72	2 Gbit	128 Mbit x 8	36	14/3/10	4
4 GB	512 Mbit x 72	2 Gbit	512 Mbit x 4	18	13/11/2	2
4 GB	512 Mbit x 72	2 Gbit	256 Mbit x 8	18	15/3/10	2
8 GB	1 Gbit x 72	2 Gbit	512 Mbit x4	36	15/3/11	2
8 GB	1 Gbit x 72	2 Gbit	Stacked 1 Gbit x 4	18	15/3/11	2

Note: This server board has no support for Quad Rank x4 SDRAM organization FBDIMMs

3.2.3.2 DIMM Population Rules and Supported DIMM Configurations

Intel supported DIMM population configurations for this server board are shown in the following table:

Supported and Validated configuration : Slot is populated

Supported but not validated configuration : Slot is populated

Slot is not populated

Table 8. Supported DIMM Population Configurations

Branch 0								Branch 1								Sparing Possible
Channel A				Channel B				Channel C				Channel D				
DIMM_A1	DIMM_A2	DIMM_A3	DIMM_A4	DIMM_B1	DIMM_B2	DIMM_B3	DIMM_B4	DIMM_C1	DIMM_C2	DIMM_C3	DIMM_C4	DIMM_D1	DIMM_D2	DIMM_D3	DIMM_D4	
																No
																No
																No
																No
																Yes (0, 1)
																Yes (0,1)
																Yes (0, 1)

Notes:

1. Single channel mode is only tested and supported with a 512 MB x8 FBDIMM installed in DIMM Slot A1.
2. The supported memory configurations must meet the population rules defined below.
3. For best performance, the number of DIMMs installed should be balanced across both memory branches. For example, a four-DIMM configuration performs better than a two-DIMM configuration and should be installed in DIMM Slots A1, B1, C1, and D1; an eight-DIMM configuration performs better then a six-DIMM configuration.
4. Although mixed DIMM capacities between channels are supported, Intel does not validate DIMMs in mixed DIMM configurations.

The DIMM population rules for this server board are as follows:

- Within a branch, DIMMs must be populated in slot order starting with Slot 1 for each channel, followed by slot 2, then slot 3 and ending with slot 4.
- DIMMs must be populated in matching pairs across channels within a given branch. Therefore, when populating DIMM pairs, the population order would be as follows:

  A1 and B1; C1 and D1; A2 and B2; C2 and D2; A3 and B3; C3 and D3; A4 and B4; C4 and D4
- DIMMs that make up a given pair must match with respect to size, speed, and organization
- DIMM size from one DIMM pair to another can be different. However, speed and organization must be the same. For example, if DIMM pair A1 and B1 is populated with x8 1 GB DDR2-667 DIMMs, DIMM pair C1 and D1 can be populated with x8 2 GB DDR2-667 DIMMs.

3.2.3.3 Minimum Memory Configuration

The server board is capable of supporting a minimum of one installed DIMM (DIMM Slot A1). However, for system performance reasons, Intel's recommendation is that at least two DIMMs be installed, populating DIMM slots A1 and B1.

The following figure shows the recommended minimum DIMM memory configuration:

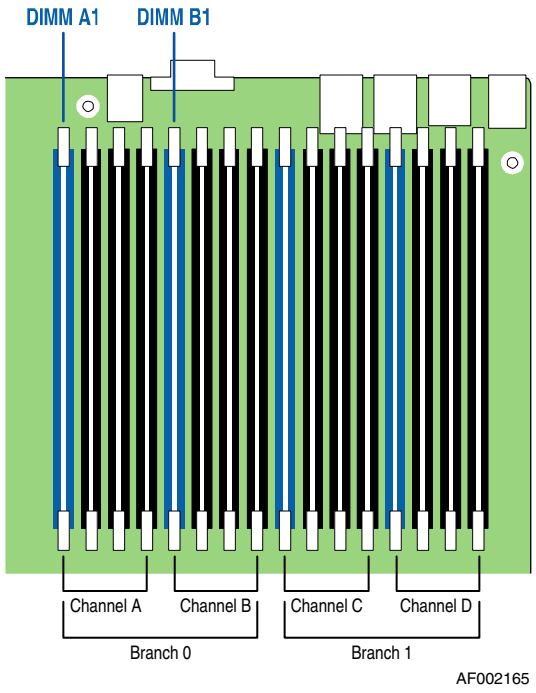


Figure 8. Recommended Minimum DIMM Memory Configuration

Note: The server board supports single DIMM mode operation. Intel only validates and supports this configuration with a single 512 MB x8 FBDIMM installed in DIMM slot A1.

3.2.3.4 Memory upgrades

The minimum memory upgrade increment is two DIMMs per branch. The DIMMs must cover the same slot position on both channels. DIMMs pairs must be identical with respect to size, speed, and organization. DIMMs that cover adjacent slot positions do not need to be identical.

When adding two DIMMs to the configuration shown in Figure 8, the DIMMs should be populated in DIMM slots C1 and D1 as shown in the following figure:

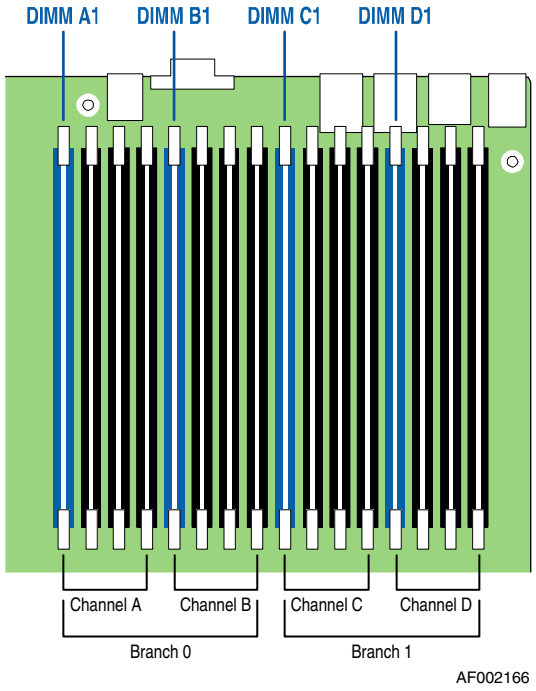


Figure 9. Recommended Four-DIMM Configuration

Functionally, DIMM slots A2 and B2 could also be populated instead of DIMM slots C1 and D1. However, the system does not achieve equivalent performance. The above figure shows the supported DIMM configuration that is recommended because it allows both memory branches from the MCH to operate independently and simultaneously. Memory bandwidth is doubled when both branches operate in parallel.

3.2.3.5 ECC Code Support

When branches operate in the dual-channel mode, the MCH supports the 18 device DRAM failure correction code (SDDC aka SECC) option for FBD. As applied by the MCH, this code has the following properties:

- Correction of any x4 or x8 DRAM device failure
- Detection of 99.986% of all single bit failures that occur in addition to a x8 DRAM failure. The MCH detects a series of failures on a specific DRAM and uses this information in addition to the information provided by the code to achieve 100% detection of these cases.
- Detection of all two wire faults on the DIMMs. This includes any pair of single bit errors.
- Detection of all permutations of 2 x4 DRAM failures.

When the branch operates in the single-channel mode, the MCH supports an 8-byte-over-32-byte Single Error Correct, Double Error Detect (SECDED+) code. It is the same ECC code that is used in the dual-channel mode, but the number of devices over which the codeword is defined is half, thereby reducing the SDDC properties to SECDED+. A single wire fault in the same device is replicated across all symbols reducing the effectiveness of the error correction. In the single DIMM mode (e.g. nine x8 devices), single wire fault (stuck at) errors or permanent full device faults cannot be corrected. This code has the following properties:

- Detection of any two bits in error within 8 bytes of data
- Correction of any single bit in error within 8 bytes of data
- Correction to any single DRAM data bus wire failure

3.2.3.6 Memory Sparing

The MCH provides DIMM sparing capabilities. DIMM Sparing is a RAS feature that places DIMMs in reserve to replace DIMMs that are failing. Spared memory configurations do not provide redundant copies of memory and the system cannot continue to operate when an uncorrectable error occurs. The purpose of memory sparing is to detect a degrading FBDIMM before it causes a system crash. Once the affected FBDIMM is isolated and removed from the set of active FBDIMMs, the system integrity is maintained by copying the data from the failed FBDIMM to the reserved FBDIMM. DIMM sparing occurs within a given channel of memory and is not supported across branches.

The DIMM sparing feature requires that the spare FBDIMM be at least the size of the largest primary FBDIMM in use. When sparing is enabled, the BIOS selects the spare automatically during POST. No manual configuration of this feature is required beyond enabling the feature in the BIOS setup. With sparing enabled, the total effective memory size is reduced by the size of the spare FBDIMM(s).

For FBDIMM sparing, the minimum population is at least two FBDIMMs on the same channel on any branch. Selecting the Memory RAS Sparing option from the BIOS setup causes the BIOS to attempt enabling the feature on both branches to begin with, but actual configuration for a given branch depends upon the population of FBDIMMs on that branch.

See Table 8 in section 1.1.1.1 for valid memory configurations that support the Memory Sparing feature.

The spare FBDIMMs do not contribute to available physical memory under normal system operation. The Effective Memory field on the BIOS Setup screen indicates this absence of memory for the sparing operation.

When a dual-ranked FBDIMM is used as a spare, the BIOS has the ability to independently select a physical rank on that FBDIMM as the spare unit and utilize the other physical rank as a normal unit. This selective sparing ensures maximization of available memory while still providing RAS.

3.2.3.7 FBD Memory Thermal Management

The Intel® 5400 MCH Chipset implements an adaptive throttling methodology to limit the number of memory requests to the FBDIMMs. This methodology is comprised of the following:

- **Activation throttling**: Consists of closed/open loop throttling of activates on the FBDIMM.
  - Closed Loop Thermal Activate Throttle Control when the temperature of the FBDIMMs increases beyond a specified threshold.
  - Open Loop Global Activate Control to limit requests when the number of activates crosses an event threshold in a large time window.
- **Electrical Throttling**: To prevent silent data corruption by limiting the number of activates per rank in a small sliding window.

3.2.3.8 BIOS Support of Memory Subsystem

The BIOS is able to configure the memory controller dynamically in accordance with the available FBDIMM population and the selected RAS (reliability, availability, serviceability) mode of operation.

3.2.3.8.1 Memory sizing and Configuration

The BIOS supports various memory module sizes and configurations. These combinations of sizes and configurations are valid only for FBDIMMs approved by Intel. The BIOS reads the Serial Presence Detect (SPD) SEEPROMs on each installed memory module to determine the size and timing characteristics of the installed memory modules (FBDIMMs). The memory-sizing algorithm then determines the cumulative size of each row of FBDIMMs. The BIOS programs the Memory Controller in the chipset accordingly, such that the range of memory accessible from the processor is mapped into the correct FBDIMM or set of FBDIMMs.

3.2.3.8.2 POST Error Codes

The range {0xE0, 0xEF} of POST codes is used for memory errors in early POST. In late POST, this range is used for reporting other system errors as follows:

- If no memory is available, the system emits a POST Diagnostic LED code 0xE1 and halts the system.
- If the BIOS cannot electrically identify and thus communicate with the AMB on an installed FBDIMM, the BIOS eventually times out and reports a POST Diagnostic LED code 0xE4. This is usually indicative of hardware failure in the serial channel on which the AMBs sit.
- If a FBDIMM or a set of FBDIMMs on the same FBD memory channel (row) fails Intel® Interconnect BIST (Intel® IBIST), or Memory Link Training, the BIOS emits a POST Diagnostic LED code 0xE6. If all of the memory fails Intel® IBIST, the system acts as if no memory is available.
- If the BIOS detects an FBDIMM with bad or corrupted SPD data, it emits a POST Diagnostic LED code 0xEB and halts the system.
- If a FBDIMM has no SPD information at all, the BIOS treats that FBDIMM slot as if no FBDIMM is present on it at all. Therefore, if this is the only FBDIMM installed in the

system, the BIOS halts with a POST Diagnostic LED code 0xE1 (no memory detected) and halts the system.

Any of the above errors causes a memory error beep code.

3.2.3.8.3 Publishing System Memory

- The BIOS displays the "Total Memory" of the system during POST if Display Logo is disabled in the BIOS setup. This is the total size of memory discovered by the BIOS during POST, and is the sum of the individual sizes of installed FBDIMMs in the system.
- The BIOS displays the "Effective Memory" of the system in the BIOS setup. The term *Effective Memory* refers to the total size of all FBDIMMs that are active (not disabled) and not used as redundant units.
- The BIOS provides the total memory of the system in the main page of the BIOS setup. This total is the same as the amount described by the first bullet above.
- If Display Logo is disabled, the BIOS displays the total system memory on the diagnostic screen at the end of POST. This total is the same as the amount described by the first bullet above.
- The BIOS provides the total amount of memory in the system by supporting the EFI Boot Service function, GetMemoryMap().
- The BIOS provides the total amount of memory in the system by supporting the INT 15h, E820h function. See the *Advanced Configuration and Power Interface Specification*, Revision 2.0 for details.

Note: Memory between 4 GB and 4 GB minus 512 MB is not accessible for use by the operating system and may be lost to the user. This area is reserved for the BIOS, APIC configuration space, and virtual video memory space. Memory is also reserved for PCI/PCI-X/PCI Express* resources. This means that if 4 GB of memory is installed, 3.5 GB or less of this memory is usable. The chipset allows the remapping of unused memory above the 4 GB address. To take advantage of this, turn on the Physical Address Extensions (PAE) in your operating system.

A region of size 0.25 GB of memory below 4 GB is always reserved for mapping chipset, processor and BIOS (flash) spaces as memory-mapped I/O regions. This region appears as a loss of memory to the operating system. In addition to this loss, the BIOS creates another reserved region for memory-mapped PCI Express* functions, including a standard 0.25 GB of standard PCI Express configuration space. This memory is reclaimed by the operating system if PAE is turned on in the operating system.

When 4 GB or more of physical memory is installed (physical memory is the memory installed as FBDIMMs), the reserved memory is lost. However, the Intel® 5400 Chipset provides a feature called *High-memory reclaim*, that allows the BIOS and the operating system to remap the lost physical memory into system memory above 4 GB (the system memory is the memory that can be seen by the processor).

The BIOS always enables high-memory reclaim if it discovers installed physical memory equal to or greater than 4 GB. For the operating system, the reclaimed memory is recoverable only when it supports and enables the PAE feature in the processor. Most operating systems support this feature. For details, see the relevant operating system manuals.

3.2.3.8.4 Memory Interleaving

In general, to optimize memory accesses, the BIOS enables *Branch Interleaving*, which allows the chipset to interleave data for successive cache-lines between the autonomous branches.

Additionally, the Intel® 5400 MCH Chipset also provides interleaving across logical memory devices called ranks. A pair of single-ranked lock-stepped FBDIMMs constitutes a memory *rank*. Interleaving effected between ranks allows the chipset to interleave cache-line data between participant ranks, and the process is called *Rank Interleaving*. The BIOS by default enables 4:1 Rank Interleaving, in which 4 ranks participate in a single cache-line access.

3.2.3.8.5 Support for Mixed Speed Memory Modules

The BIOS supports memory modules of mixed speed by automatic selection of the highest common frequency of all memory modules (FBDIMM).

To program a FBDIMM to function correctly for a given frequency, the BIOS queries each FBDIMM's Serial-presence Data (SPD) store. The SPD contains the frequency characteristics of the FBDIMM, which are measured in terms of the following parameters:

- CAS latency (CL)
- Common clock frequency
- Additive latency (AL)
- Buffer read delay (BRD)

The CAS latency and the additive latency are configurable parameters that are detected by the BIOS by reading the SPD data of the FBDIMMs. The BRD is the average inherent delay that is caused by the finite time that the AMB consumes in buffering the data read from the DRAMs before forwarding it on the Northbound (or Southbound) path.

3.2.3.9 Memory Error Handing

The BIOS classifies memory errors into the following categories:

- Correctable ECC errors: These are errors that occur between the Northbridge MCH and the DRAM memory cells and are corrected by the chipset. This correction could be the result of ECC correction, a successfully retried memory cycle, or both.
- Uncorrectable ECC errors: These are errors that occur in the memory cells and result in data corruption. The chipset's ECC engine detects these errors, but cannot correct them. These errors create a loss of data fidelity and are severe errors.
- Unrecoverable and Fatal Errors: These are errors that are outside the scope of the standard ECC engine. These errors are thermal errors, certain FBD channel errors and data path errors. These errors bring about catastrophic failure of the system.

There are two specific stages in which memory errors can occur:

- Early POST during memory discovery
- Late POST or at runtime (when the operating system is running)

During POST, the BIOS captures and reports memory BIST errors.

At runtime, the BIOS captures and reports correctable, uncorrectable, and fatal errors occurring in the memory subsystem.

3.2.3.9.1 Faulty FBDIMMs

The BIOS provides detection of a faulty or failing FBDIMM. A FBDIMM is considered faulty if it fails the memory BIST. The BIOS enables the in-built memory BIST engine in the Intel® 5400 MCH Chipset during memory initialization in POST. The Memory BIST cycle isolates failed, failing, or faulty FBDIMMs and the BIOS then marks those FBDIMMs as failed, and takes these FBDIMMs offline.

FBDIMMs can also fail during normal operation. The BIOS marks these FBDIMMs as temporarily disabled, and performs other housekeeping tasks as relevant. The Memory BIST function is run on every FBDIMM during each boot of the system.

3.2.3.9.2 Faulty Links

FBDIMM technology is a serial technology. Therefore, errors or failures can occur on the serial path between FBDIMMs. These errors are different from ECC errors, and do not necessarily occur as a result of faulty DRAM cells. The BIOS keeps track of such link-level failures.

In general, when a fatal link failure occurs, the BIOS disables all FBDIMMs on that link. If all FBDIMMs are present on the same faulty link, the BIOS generates a POST code 0xE1 to indicate that the system has no usable memory, and then halts the system. For example, if A1 through A4 and B1 through B4 is populated with 1 GB FBDIMMs, and if A3 fails, the BIOS disables both A3 and A4.

If a fatal link failure occurs during normal operation at runtime (after POST), the BIOS signals a fatal error and performs policies related to fatal error handling.

3.2.3.9.3 Error Counters and Thresholds

The BIOS handles memory errors through a variety of platform-specific policies. Each of these policies is aimed at providing comprehensive diagnostic support to the system administrator towards system recovery following the failure.

The BIOS uses error counters on the Intel® 5400 Chipset and internal software counters to track the number of single-bit correctable and multi-bit correctable errors that occur at runtime. The chipset increments the count for these counters when an error occurs. The count also decays at a given rate, programmable by the BIOS. Because of this particular nature of the counters, they are termed *leaky bucket counters*.

The leaky bucket counters provide a measurement of the frequency of errors. The BIOS configures and uses the leaky bucket counters and the decay rate such that it can be notified of a failing FBDIMM. A degrading DRAM typically generates errors faster over time, which is detected by the leaky bucket algorithm. The chipset maintains separate internal leaky bucket counters for single-bit correctable and multi-bit correctable errors respectively.

The BIOS initializes the correctable error leaky bucket counters to a value of ten for correctable ECC errors. These counters are on a per-rank basis. A rank applies to a pair of FBDIMMs on adjacent channels functioning in lock-stepped mode.

3.2.3.9.3.1 BIOS Policies on Correctable Errors

For each correctable error that occurs before the threshold is reached, the BIOS logs a "Correctable Error" SEL entry. No other action is taken, and the system continues to function normally.

When the error threshold reaches ten, the BIOS logs a SEL entry to indicate the correctable error. In addition, the following steps occur:

1. If sparing is enabled, the chipset initiates a spare fail-over to a spare FBDIMM. In all other memory configurations, future correctable errors are masked and no longer reported to the SEL.
2. The BIOS logs a "Max Threshold Reached" SEL event.
3. The BIOS sends a "DIMM Failed" event to the Integrated BMC. This causes the Integrated BMC to light the System Fault LEDs to initiate memory performance degradation and an assertion of the failed FBDIMM.
4. The BIOS lights the DIMM Fault LED for the faulty FBDIMM.

3.2.3.9.4 Multi-bit Correctable Error Counter Threshold

Due to the internal design of the chipset, the same threshold value for correctable errors also applies to the multi-bit correctable errors. However, maintaining a tolerance level of 10 for multi-bit correctable errors is undesirable because these are critical errors. Therefore, the BIOS programs the threshold for multi-bit correctable errors based on the following alternate logic:

- **Automatic retries on memory errors:** The chipset automatically performs a retry of memory reads for uncorrectable errors. If the retry results in good data, this is termed a multi-bit correctable error. If the data is still bad, then it is an uncorrectable error. Another memory error is a CRC error on the FBDIMM serial path. CRC errors are also retried in a similar manner. The retry eliminates transient errors that occur on memory packets transacted over the FBDIMM serial links between the chipset and the FBDIMMs.
- **Internal error reporting by the chipset:** The chipset records the occurrence of uncorrectable errors both at the time of the occurrence, and on the subsequent failure on retry. Both errors are independently reported to the BIOS. The BIOS reports a successful retry as "Correctable Memory Error" in the SEL regardless of whether the originating error was a CRC error or an ECC error.

3.2.3.9.5 FBD Fatal Error Threshold

In addition to standard ECC errors, the BIOS monitors FBD protocol errors reported by the chipset. FBD protocol errors cause degradation of system memory, and hence it is pointless to tolerate them to any level. The BIOS maintains an internal software counter to handle FBD errors. The threshold of this software counter is one. When the threshold is met, it is treated as an uncorrectable error and follows the same policy as outlined below.

3.2.3.9.5.1 BIOS Policies on Uncorrectable Errors

For uncorrectable errors, the BIOS logs a single "Uncorrectable Error" SEL entry. The BIOS then generates an NMI.

3.2.3.10 Memory Error Reporting

Memory errors are reported through a variety of platform-specific elements, as described in the following table.

Table 9. Memory Error Reporting Agent Summary

Platform Element	Description
Event Logging	When a memory error occurs at runtime, the BIOS logs the error into the system event log in the Integrated Baseboard Management Controller's (Integrated BMC) repository.
BIOS Diagnostic/Error Screen	At the end of POST, memory errors found during MemBIST are reported in the BIOS Error Manager.
Beep Codes	The BIOS emits a beep code when the system has no memory or when a link failure is detected during memory discovery, causing all memory to be mapped out.
BIOS Setup Screen	When FBDIMMs fail Memory BIST or RAS configuration errors occur, the FBDIMM status is captured in the Advanced > Memory screen in the BIOS setup.
DIMM Fault Indicator LEDs	Intel® server boards and systems that use the Intel® 5400 Chipset have a set of Fault Indicator LEDs on the board, one LED per DIMM socket. These LEDs are used for indicating failed/faulty FBDIMMs.
System Fault/Status LEDs	Intel® server boards and systems that use the Intel® 5400 Chipset provide a specific LED on the front panel and rear I/O Panel that indicates the state of the system. When a memory error occurs such that the performance of the memory subsystem is affected, the BIOS sends a request to the Integrated BMC to initiate a Status LED state change.
NMI Generation	The BIOS triggers/initiates an NMI to halt the system when a critical error occurs.

3.2.3.10.1 Memory BIST Error Reporting

The Error Manager screen in the BIOS captures Memory BIST failures that occurred during the current POST.

Table 10. Memory Errors Captured by Error Manager

Specific Error	Error Class	Error Code	Error Text	Description
Configuration Error	Pause	0x85F0	Memory was not configured for the selected memory RAS mode.	Failure of BIOS to configure the memory system in the selected RAS mode.
Memory BIST Failure	Pause	0x852x	DIMM_xx failed self test (BIST).	During normal Memory BIST operation in POST, the BIOS detected that DIMM_xx failed to pass Memory BIST.

Note: x = the instance number of the DIMM that failed.

3.2.3.10.2 DIMM Fault Indicator LEDs

Intel® server boards have a fault-indicator LED next to each DIMM socket. The LEDs are turned on when the FBDIMM on the adjacent DIMM socket is determined to be faulty.

The generic usage model for the DIMM Fault LEDs is as follows:

Table 11. DIMM Fault LED Behavior Summary

Error Event	Mode of Operation	Description
A FBDIMM fails Memory BIST during POST.	N/A	DIMM LED for the failing FBDIMM is turned on.
Channel Intel® IBIST failure occurs during POST.	N/A	If there are multiple FBDIMMs on that channel, all corresponding failing DIMM LEDs are turned on.
Correctable error threshold reached for a failing FBDIMM. (Ten correctable errors occur on the same FBDIMM within the limits of the error period.)	System is operating in the single-channel mode.	DIMM fault LED for the failed FBDIMM is turned on when the error count reaches the threshold (i.e, on the tenth error).
Correctable error threshold reached for a failing FBDIMM. (Ten correctable errors occur on the same FBDIMM within the limits of the error period.)	System is operating in the dual-channel mode.	DIMM fault LED for the failed FBDIMM is turned on when the error count reaches the threshold (i.e., on the tenth error).
Uncorrectable error occurs on a FBDIMM.	System is operating in the single-channel mode.	DIMM fault LED for the failed FBDIMM is turned on.
Uncorrectable error occurs on a FBDIMM.	System is operating in the dual-channel mode.	DIMM fault LEDs for the failed pair of FBDIMMs are turned on.
Fatal channel link-level or FBD fatal error occurs.	N/A	DIMM fault LEDs of all FBDIMMs present on the failing channel or branch are turned on.

Note: As indicated in the preceding table, when two FBDIMMs are operating in lthe ock-stepped mode and one of the FBDIMMs fails, the BIOS also lights the DIMM Fault LED of the companion FBDIMM. This is because the BIOS cannot isolate failures at the individual FBDIMM level in this mode.

3.3 Intel® 6321ESB I/O Controller Hub

The Intel® 6321ESB I/O Controller Hub is a multi-function device that provides four distinct functions: an I/O Controller, a PCI-X Bridge, a Gigabit Ethernet Controller, and an Integrated Baseboard Management Controller (Integrated BMC). Each function within the Intel® 6321ESB I/O Controller Hub has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller.

A primary role of the Intel® 6321ESB I/O Controller Hub is to provide the gateway to all PC-compatible I/O devices and features. The server board uses the following Intel® 6321ESB I/O Controller Hub features:

- Six-channel SATA interface with SATA Busy LED Control
- Dual GbE MAC
- Integrated Baseboard Management Controller (Integrated BMC)
- Single ATA interface, with Ultra DMA 100 capability
- Universal Serial Bus (USB) 2.0 interface

- LPC bus interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- System RTC
- General purpose I/O

This section describes the functionality of most of the listed features as they pertain to this server board. For more detail information, see the *Intel® Enterprise South Bridge 2 External Design Specification*.

3.3.1 Serial ATA Support

The Intel® 6321ESB I/O Controller Hub has an integrated Serial ATA (SATA) controller that supports independent DMA operation on six ports and supports data transfer rates of up to 3.0 Gb/s. The six SATA ports on the server board are numbered SATA-0 through SATA-5. The SATA ports can be enabled/disabled and/or configured by accessing the BIOS Setup utility during POST.

The BIOS initializes and supports SATA devices just like PATA devices. It initializes the embedded IDE controllers in the chipset and any SATA devices that are connected to these controllers. From a software standpoint, SATA controllers present the same register interface as the PATA controllers. Hot plugging of SATA drives during the boot process is not supported by the BIOS and may result in undefined behavior.

3.3.1.1 Intel® Embedded Server RAID Technology II Support

The on-board storage capability of this server board includes support for Intel® Embedded Server RAID Technology II, which provides three standard software RAID levels:

- Data striping (RAID Level 0)
- Data mirroring (RAID Level 1)
- Data striping with mirroring (RAID Level 10)

For higher performance, data striping can be used to alleviate disk bottlenecks by taking advantage of the dual independent DMA engines that each SATA port offers. Data mirroring is used for data security. Should a disk fail, a mirrored copy of the failed disk is brought on-line. There is no loss of either PCI resources (request/grant pair) or add-in card slots.

With the addition of an optional Intel® RAID Activation Key (Intel Part # AXXRAKSW5), Intel® Embedded Server RAID Technology II is also capable of providing fault tolerant data striping (software RAID Level 5), such that if a SATA hard drive should fail, the lost data can be restored on a replacement drive from the other drives that make up the RAID 5 pack.

See Figure 2 for the location of the Intel® RAID Activation Key connector location.

Intel® Embedded Server RAID Technology II functionality requires the following:

- Intel® 6321ESB I/O Controller Hub (on-board device)
- Intel® Embedded Server RAID Technology II Option ROM (on-board device)
- Intel® Application Accelerator RAID Edition drivers, most recent revision

- At least two SATA hard disk drives attached to on-board SATA connectors

Intel® Embedded Server RAID Technology II is not available in the following configurations:

- When the SATA controller is in compatible mode
- When the Intel® Embedded Server RAID Technology II has been disabled.

3.3.1.2 Intel® Embedded Server RAID Technology Option ROM

The Intel® Embedded Server RAID Technology II Option ROM provides a pre-OS user interface for the Intel® Embedded Server RAID Technology II implementation. It also provides the ability for an Intel® Embedded Server RAID Technology II volume to be used as a boot disk as well as to detect any faults in the Intel® Embedded Server RAID Technology II volume(s) attached to the Intel® RAID controller.

Refer to the *Intel Embedded Server RAID Technology II Users Guide* for complete RAID setup information.

3.3.2 Parallel ATA (PATA) Support

The integrated IDE controller of the Intel® 6321ESB I/O Controller Hub provides one IDE channel. It redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s. For this server board, the IDE channel was designed to provide slimline optical drive support to the platform. The BIOS initializes and supports ATAPI devices such as CD-ROM, CD-RW and DVD. The IDE channel is accessed through a single high-density 44-pin connector (J3G2), which provides both power and I/O signals. The ATA channel can be configured and enabled or disabled by accessing the BIOS Setup utility during POST.

Note: The IDE connector on this server board is NOT a standard 40 IDE connector. Instead, this connector has four additional power pins over and above the standard 40 I/O pins. The design intent of this connector is to provide support for a slimline optical drive only.

The BIOS supports the *ATA/ATAPI Specification*, Version 6 or later. It initializes the embedded IDE controller in the Intel® 6321ESB I/O Controller Hub and the IDE devices that are connected to these devices in accordance to the *Intel® 6321ESB I/O Controller Hub BIOS Writers Guide* The BIOS scans the IDE devices and programs the controller and the devices with their optimum timings. The IDE disk read/write services that are provided by the BIOS use the PIO mode, but the BIOS programs the necessary ultra DMA registers in the IDE controller so the operating system can use the ultra DMA modes.

3.3.3 Integrated Baseboard Management Controller (Integrated BMC)

The Integrated BMC component of the Intel® 6321ESB I/O Controller Hub is provided by an embedded ARC* controller and associated peripheral functionality that is used to provide the Integrated Baseboard Management Controller functionality that is required for IPMI-based server management. The following is a summary of the Intel® 6321ESB I/O Controller Hub management hardware features utilized by the Integrated BMC:

- ARC4 processor with 16 Kb I-cache and D-cache
- 256 KB of internal SRAM with dual ports (one for code accesses and one for all other accesses).

- Expansion bus allowing connection to an external Flash PROM (asynchronous or synchronous), SRAM, or SDRAM.
- Serial flash interface
- Five SMB ports, two that support FML (either master or slave)
- RS-232 serial port (UART)
- Cryptographic module supporting AES and RC4 encryption algorithms and SHA1 and MD5 authentication algorithms with internal DMA and raw checksum support
- Two keyboard controller style (KCS) interfaces residing on the LPC bus
- General-purpose input/output (GPIO) interface
- MAC CSR interface
- Timer interface
- Host DMA interface

3.3.4 USB 2.0 Support

The Intel® 6321ESB I/O Controller Hub contains an enhanced host controller interface that supports USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s, which is 40 times faster than full-speed USB. The I/O Controller Hub also contains four universal host controller interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The Intel® 6321ESB I/O Controller Hub supports eight USB 2.0 ports. All eight ports are capable of high-speed, full-speed, and low-speed operations. Two external connectors are located on the back edge of the server board. One internal 2x5 header is provided, capable of supporting two optional USB 2.0 ports. Three USB ports are routed through the bridge board connector providing optional USB support for a system control panel or other USB requirements. An additional USB port is dedicated to the Intel® Remote Management Module 2 (Intel® RMM2) connector.

3.3.4.1 Native USB Support

During the power-on self test (POST), the BIOS initializes and configures the USB subsystem in accordance with Chapter 14 of the *Extensible Firmware Interface Reference Specification*, Version 1.1. The BIOS is capable of initializing and using the following types of USB devices:

- USB Specification-compliant keyboards
- USB Specification-compliant mice
- USB Specification-compliant storage devices that utilize bulk-only transport mechanism

USB devices are scanned to determine if they are required for booting.

The BIOS supports USB 1.1 and USB 2.0 compliant devices and host controllers.

During the pre-boot phase, the BIOS automatically supports the hot-addition and hot-removal of USB devices. For example, if a USB device is hot-plugged, the BIOS detects the device insertion, initializes the device, and makes it available to the user. Only on-board USB controllers are initialized by the BIOS. This does not prevent the operating system from supporting any available USB controllers, including add-in cards.

3.3.4.2 Legacy USB Support

The BIOS supports PS/2 emulation of USB keyboards and mice. During POST, the BIOS initializes and configures the root hub ports and then searches for a keyboard and/or a mouse on the USB hub and then enables them.

3.3.5 System Management Bus (SMBus 2.0)

The Intel® 6321ESB I/O Controller Hub contains a SMBus host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices. Special I^2C commands are implemented. The SMBus host controller for the I/O Controller Hub provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves).

The Intel® 6321ESB I/O Controller Hub supports slave functionality, including the Host Notify protocol. The host controller supports eight command protocols of the SMBus interface: Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

See the *System Management Bus (SMBus) Specification*, Version 2.0 for more information.

3.3.6 Real-time Clock (RTC)

The Intel® 6321ESB I/O Controller Hub contains a Motorola* MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data even when the system is powered down. The RTC operates on a 32.768-KHz crystal and a separate on-board 3-V lithium battery (Panasonic* 3V CR2032 or equivalent).

The RTC supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

3.3.7 General-purpose Input/Output (GPIO)

General-purpose inputs and outputs are provided for custom system designs. The number of inputs and outputs depends on the Intel® 6321ESB I/O Controller Hub configuration. All unused GPI pins must be pulled high or low, so they are at a predefined level and do not cause problems.

3.4 PCI Subsystem

The primary I/O buses for the server board are PCI Express*. An additional PCI bus segment is also utilized from the Intel® 6321ESB I/O Controller Hub to support the on-board video controller.

The MCH utilizes general purpose PCI Express* high-speed ports to achieve superior I/O performance. The MCH PCI Express* ports are compliant with the *PCI Express* Base Specification*, Version 0.9 of Revision 2.0. The raw bit-rate per PCI Express* Gen 1 bit lane is 2.5 Gbit/s. This results in a real bandwidth per Gen 1 bit lane pair of 250 MB/s given the 8/10 encoding used to transmit data across this interface. The result is a maximum theoretical realized bandwidth on a x4 PCI Express* port of 1 GB/s in each direction. The raw bit-rate per

PCI Express* Gen 2 bit lane is 5 Gbit/s similarly with a maximum theoretical realized bandwidth of 2 GB/s in each direction. The Gen 2 speeds are only supported for the x16 high-performance PCI Express* interfaces. Each of the MCH PCI Express* ports are organized as four bi-directional bit lanes, and are referred to as a x4 port.

The following table lists the characteristics of each PCI bus segment used on this server board:

Table 12. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	On-board Device Support
Intel® 6321ESB I/O Controller Hub PCI 32/33	3.3 V	32 bit	33 MHz	PCI	Used internally for the video controller
Intel® 6321ESB I/O Controller Hub port 1	3.3 V	x4	2 GB/S	PCI Express*	Bridge Board Connector – Used as an interconnect for Intel® Server System boards supporting a SAS controller option
Intel® 6321ESB I/O Controller Hub port 2	3.3 V	x4	2 GB/S	PCI Express*	Mezzanine connector for optional Intel® I/O Expansion Module
MCH to Intel® 6321ESB I/O Controller Hub Interface – port 9 to port 4	3.3 V	x4	2 GB/s	PCI Express*	x4 PCI Express* link between MCH and Intel® 6321ESB I/O Controller Hub
MCH to Intel® 6321ESB I/O Controller Hub Interface – ESI ports	3.3 V	x4	2 GB/s	PCI Express*	ESI Link between MCH and Intel® 6321ESB I/O Controller Hub
MCH ports 5,6,7,8	3.3 V	x16	16 GB/S	PCI Express*	Full-height riser slot, x16 Gen 2 PCI Express*

3.4.1 Intel® 6321ESB I/O Controller Hub PCI32: 32-bit, 33-MHz PCI Bus Segment

All 32-bit, 33-MHz PCI I/O is directed through the Intel® 6321ESB I/O Controller Hub. The PCI32 segment is only used to provide support for the on-board 2D Graphics Accelerator: ATI* ES1000 Video Controller

3.4.2 Intel® 6321ESB I/O Controller Hub Port 1: x4 PCI Express* Bus Segment

This x4 PCI Express* segment is routed from the Intel® 6321ESB I/O Controller Hub to the bridge board connector for use by Intel® Server System boards that include a SAS controller option.

3.4.3 Intel® 6321ESB I/O Controller Hub Port 2: x4 PCI Express* Bus Segment

This x4 PCI Express* segment is routed from the Intel® 6321ESB I/O Controller Hub to the proprietary Intel® I/O Expansion Module mezzanine connector (J3B1).

3.4.4 MCH to Intel® 6321ESB I/O Controller Hub Chip-to-Chip Interface: Two x4 PCI Express* Bus Segments

The Enterprise Southbridge Interface (ESI) in the MCH is the chip-to-chip connection to the Intel® 6321ESB I/O Controller Hub. The ESI is a specialized inter-chip interface based upon the *PCI Express* Base Specification*, Revision 1.1 with special commands/features added to enhance the PCI Express* interface for enterprise applications. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic. Base functionality is completely transparent permitting current and legacy software to operate normally.

On the Intel® Server Board S5400SF, the ESI port in the MCH is combined with PCI Express* Port 9 to augment the available bandwidth to the Intel® 6321ESB I/O Controller Hub. When operating alone, the available bi-directional bandwidth to the Intel® 6321ESB I/O Controller Hub is 2 GB/s (1 GB/s in each direction). When the ESI is paired with an additional x4 PCI Express* link, the available bi-directional bandwidth to the Intel® 6321ESB I/O Controller Hub is increased to 4 GB/s.

3.4.5 MCH Ports 5-8: x16 Gen 2 PCI Express* Bus Segment

This PCI Express* bus segment combines four MCH x4 PCI Express* ports to support a high-speed x16 Gen 2 interface for the on-board riser slot capable of supporting a maximum theoretical bandwidth of 16 GB/s. The raw bit-rate per PCI Express* Gen 2 bit lane is 5 Gbit/s with a maximum theoretical realized bandwidth of 2 GB/s in each direction.

3.4.5.1 PCI Express* Riser Slot

The server board has one 164-pin Gen 2 PCI Express* riser slot. See Table 62 for the connector pin-out definition.

Note: See Appendix F for a mechanical drawing showing the dimensional data for a 1U x16 PCI Express* Gen 2 riser card as used in the Intel® Server System SR1560SF.

3.4.6 Scan Order

The BIOS assigns PCI bus numbers in a depth-first hierarchy, in accordance with the *PCI Local Bus Specification*, Revision 2.2. The bus number is incremented when the BIOS encounters a PCI-PCI bridge device. Scanning continues on the secondary side of the bridge until all subordinate buses are assigned numbers. PCI bus number assignments may vary from boot to boot with varying presence of PCI devices with PCI-PCI bridges. If a device with a bridge with a single bus behind it is inserted into a PCI bus, all subsequent PCI bus numbers below the current bus are increased by one.

The bus assignments occur once, early in the BIOS boot process, and never change during the pre-boot phase.

3.4.7 Resource Assignment

The BIOS resource manager assigns the PIC-mode interrupt for the devices that are accessed by the legacy code. The BIOS ensures the PCI BAR registers and the command registers for all devices are correctly set up to match the behavior of the legacy BIOS after booting to a legacy operating system. Any legacy code cannot make any assumption about the scan order of devices or the order in which resources are allocated to them.

In the legacy mode, the BIOS supports the INT 1Ah PCI BIOS interface calls.

3.4.8 Automatic IRQ Assignment

The BIOS automatically assigns IRQs to devices in the system for legacy compatibility. No method is provided to manually configure the IRQs for devices.

3.4.9 Legacy Option ROM Support

The legacy support code in the BIOS dispatches the legacy option ROMs in the available memory space in the address range 0C0000h-0DFFFFh and follows all the legacy rules with respect to the option ROM space. If room is available in the E segment, and both C and D segments are already used, the BIOS also shadows up to 0E7FFF. The BIOS allows the user to disable the shadowing of the on-board PCI devices.

The BIOS integrates option ROMs for the ATI* RN50 video controller, LSI* 1064e SAS controller (on select board models), AHCI ROM, Intel® 6321ESB I/O Controller Hub Ethernet ROM (if onboard), Intel® 82571EB Ethernet ROM (if onboard), and the SATA Software RAID ROM.

3.4.10 EFI PCI APIs

The BIOS provides standard PCI protocols as described in the *Extensible Firmware Interface Reference Specification*, Version 1.1.

3.4.11 Legacy PCI APIs

In the legacy mode, the system BIOS supports the INT 1Ah, AH = B1h functions as defined in the *PCI BIOS Specification*, Revision 2.1. The system BIOS supports the real mode interface.

3.5 Video Support

The server board provides an ATI* ES1000 PCI graphics accelerator, along with 32 MB of video DDR SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI* ES1000 chip contains an SVGA video controller, clock generator, 2D engine, and RAMDAC in a 359-pin BGA. One DDR SDRAM chip provides 32 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 1024 x 768 resolution in 8/16/32 bpp modes under 2D. It also supports both CRT and LCD monitors up to a 100 Hz vertical refresh rate.

Video is accessed using a standard 15-pin VGA connector found on the back edge of the server board. Video signals are also made available through the 120-pin bridge board connector, which provides signals for an optional video connector to be present on the platform's control panel. Video is routed to both the rear video connector and a control panel video connector. Video is present at both connectors simultaneously and cannot be disabled at either connector individually. Hot-plugging the video while the system is still running is supported.

On-board video can be disabled using the BIOS Setup utility or when an add-in video card is installed. The system BIOS also provides the option for dual video operation when an add-in video card is configured in the system.

3.5.1 Video Modes

The ATI* ES1000 chip supports all standard IBM* VGA modes. The following table shows the 2D modes supported for both CRT and LCD.

Table 13. Video Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support		
		8 bpp	16 bpp	32 bpp
640x480	60, 72, 75, 85, 90, 100, 120, 160, 200	Supported	Supported	Supported
800x600	60, 70, 72, 75, 85, 90, 100, 120,160	Supported	Supported	Supported
1024x768	60, 70, 72, 75,85,90,100	Supported	Supported	Supported
1152x864	43,47,60,70,75,80,85	Supported	Supported	Supported
1280x1024	60,70,74,75	Supported	Supported	Supported
1600x1200	52	Supported	Supported	Supported

3.5.2 Video Memory Interface

The memory controller subsystem of the ATI* ES1000 arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing co-processor, the display controller, the video scalar, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/co-processor drawing performance.

3.5.3 Dual Video

The BIOS supports single and dual video modes. The dual video mode is enabled by default.

In the single mode (Dual Monitor Video = Disabled), the on-board video controller is disabled when an add-in video card is detected.

In the dual mode (On-board Video = Enabled, Dual Monitor Video = Enabled), the on-board video controller is enabled and is the primary video device. The external video card is allocated resources and is considered the secondary video device. The BIOS setup provides user options to configure the feature as follows:

Table 14. BIOS setup options for video modes

On-board Video	Enabled Disabled	
Dual Monitor Video	Enabled Disabled	Grayed out if the on-board video is set to "Disabled"

3.6 Network Interface Controller (NIC)

Network interface support is provided from the built-in dual GbE MAC features of the Intel® 6321ESB I/O Controller Hub in conjunction with the Intel® 82563EB compact Physical Layer Transceiver (PHY). Together, they provide the server board with support for dual LAN ports designed for 10/100/1000 Mbps operation.

The 82563EB device is based upon proven PHY technology integrated into the Intel® Gigabit Ethernet Controllers. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The 82563EB device is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps.

Each Network Interface Controller (NIC) drives two LEDs located on each network interface connector. The link/activity LED (to the right of the connector) indicates network connection when on, and transmit/receive activity when blinking. The speed LED (to the left of the connector) indicates 1000-Mbps operation when amber, 100-Mbps operation when green, and 10-Mbps when off. The following table provides an overview of the LEDs.

Table 15. NIC Status LEDs

LED Color	LED State	NIC State
Green/Amber (Left)	Off	10 Mbps
	Green	100 Mbps
	Amber	1000 Mbps
Green (Right)	On	Active Connection
	Blinking	Transmit/Receive activity

3.6.1 Intel® I/O Acceleration Technology

Intel® I/O Acceleration Technology moves network data more efficiently through Intel® Xeon® processor 5000 sequence-based servers for improved application responsiveness across diverse operating systems and virtualized environments. Intel® I/OAT improves network application responsiveness by unleashing the power of Intel® Xeon® processors 5000 sequence through more efficient network data movement and reduced system overhead. Intel multi-port network adapters with Intel® I/OAT provide high-performance I/O for server consolidation and virtualization via stateless network acceleration that seamlessly scales across multiple ports and virtual machines. Intel® I/OAT provides safe and flexible network acceleration through tight integration into popular operating systems and virtual machine monitors, avoiding the support risks of third-party network stacks and preserving existing network requirements such as teaming and failover.

3.6.2 MAC Address Definition

Each Intel® Server Board S5400SF has four MAC addresses assigned to it at the Intel factory. During the manufacturing process, each server board has a white MAC address sticker placed on the board. The sticker displays the MAC address in both bar code and alpha numeric formats. The printed MAC address is assigned to NIC 1 on the server board. NIC 2 is assigned the NIC 1 MAC address + 1.

Two additional MAC addresses are assigned to the Integrated Baseboard Management Controller (Integrated BMC) embedded in the Intel® 6321ESB I/O Controller Hub. These MAC addresses are used by the Integrated BMC's embedded network stack to enable IPMI remote management over LAN. Integrated BMC LAN Channel 1 is assigned the NIC1 MAC address + 2, and Integrated BMC LAN Channel 2 is assigned the NIC1 MAC address + 3.

3.7 Super I/O

Legacy I/O support is provided by using a National Semiconductor* PC87427 super I/O device. This chip contains all of the necessary circuitry to support the following functions:

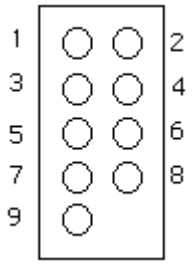
- GPIOs
- Two serial ports
- Keyboard and mouse support
- Wake up control
- System health support

3.7.1 Serial Ports

The server board provides two serial ports: an external RJ-45 serial port, and an internal DH-10 serial header.

Serial A is an optional port accessed through a 9-pin internal DH-10 header. A standard DH10 to DB9 cable can be used to direct the Serial A port to the rear of a chassis. The Serial A interface follows the standard RS-232 pin-out as defined in the following table:

Table 16. Serial A Header Pin-out

Pin	Signal Name	Serial Port A Header Pin-out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	

The rear RJ-45 Serial B port is a fully functional serial port that can support any standard serial device. Using an RJ-45 connector for a serial port allows direct support for serial port concentrators, which typically use RJ-45 connectors and are widely used in the high-density server market. For server applications that use a serial concentrator to access the system management features of the server board, a standard 8-pin CAT-5 cable from the serial concentrator is plugged directly into the rear RJ-45 serial port.

To allow support for either of two serial port configuration standards, a jumper block located directly behind the rear RJ-45 serial port must be configured appropriately according to the desired standard. For serial concentrators that require a DCD signal, the jumper block must be configured with the serial port jumper over pins 1 and 2. For serial concentrators that require a

DSR signal (Default), the jumper block must be configured with the serial port jumper over pins 3 and 4. Pin 1 on the jumper is identified by "*".

Note: By default, the rear RJ-45 serial port is configured to support a DSR signal. This configuration is compatible with the Cisco standard.

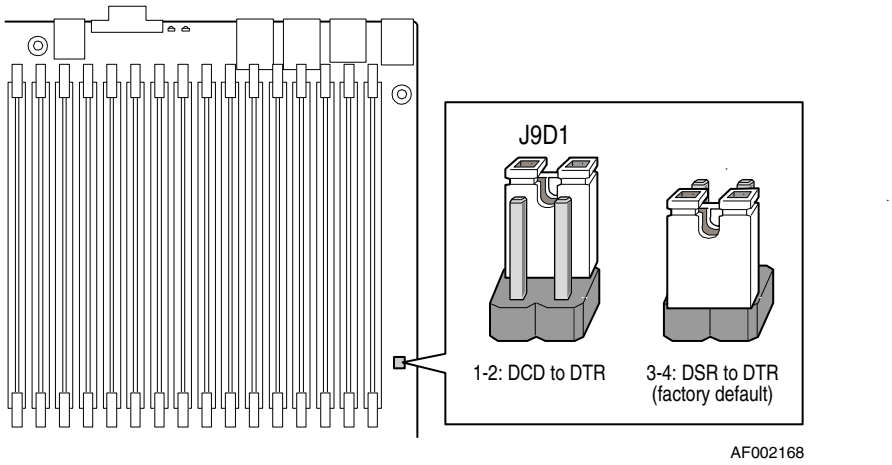


Figure 10. Serial Port Configuration Jumper Location

Pins	At system reset
1-2	Serial port is configured for DCD to DTR.
3-4	Serial port is configured for DSR to DTR (default).

For server applications that require a DB9 serial connector, an 8-pin RJ45-to-DB9 adapter must be used. The following table provides the pin-out required for the adapter to provide RS-232 support. A standard DH10-to-DB9 cable and 8-pin RJ-45 to DB9 DCD and DSR adapters are available from Intel in the Serial Port Accessory Kit (Product Code: AXXRJ45DB92).

Table 17. Rear Serial B Port Adapter Pin-out

RJ-45	Signal	Abbreviation	DB9
1	Request to Send	RTS	7
2	Data Terminal Ready	DTR	4
3	Transmitted Data	TD	3
4	Signal Ground	SGND	5
5	Ring Indicator	RI	9
6	Received Data	RD	2
7	DCD or DSR	DCD/DSR	1 or 6 (see note)
8	Clear To Send	CTS	8

Note: The RJ45-to-DB9 adapter should match the configuration of the serial device used. One of two pin-out configurations is used, depending on whether the serial device requires a DSR or DCD signal. The final adapter configuration should also match the desired pin-out of the RJ-45 connector, as it can also be configured to support either DSR or DCD.

3.7.2 Floppy Disk Controller

The server board does not support a floppy disk controller (FDC) interface. However, the system BIOS does recognize USB floppy devices.

3.7.3 Keyboard and Mouse Support

Dual stacked PS/2 ports, located on the back edge of the server board, are provided for keyboard and mouse support. Either port can support a mouse or keyboard. Neither port supports hot plugging. The system can boot without an attached keyboard or mouse. If present, the BIOS detects the keyboard during POST and displays the message “Keyboard Detected” on the POST Screen.

3.7.4 Wake-up Control

The super I/O contains functionality that allows various events to power-on and power-off the system.

3.7.5 System Health Support

The super I/O provides an interface via GPIOs for BIOS and Server Management firmware to activate the Diagnostic LEDs, the FRU fault indicator LEDs for processors, DIMMs, fans and the system status LED. Refer to Figure 3 for the location of the LEDs on the server board.

The super I/O also provides PWM fan control to the system fans, monitors tach and presence signals for the system fans, and monitors server board and control panel temperature.

4. Server Management

The server management subsystem is a major component embedded into the design of the server board. It is comprised of several communication buses, system BIOS, the Integrated Baseboard Management Controller (Integrated BMC) features of the Intel® 6321ESB I/O Controller Hub, multiple voltage and thermal sensors, and Integrated BMC Firmware. It is responsible for error management and reporting, system power control, thermal monitoring and management including system fan control, and provides system interface and monitoring features based on the *IPMI Specification,* Version 2.0.

This section provides a high level overview of the server management architecture and its features. For greater detail, the following documents should also be referenced:

- *Intel® 5400 Series Server Board BIOS External Product Specification*
- *Intel® 5400 Series Server Board Integrated Baseboard Management Controller Core External Product Specification*
- *Intel® Remote Management Module 2 Technical Product Specification*
- *Intelligent Platform Management Interface (IPMI) Specification*, Version 2.0

The following diagram provides an overview of the Server Management Bus (SMBus) architecture used on this server board:

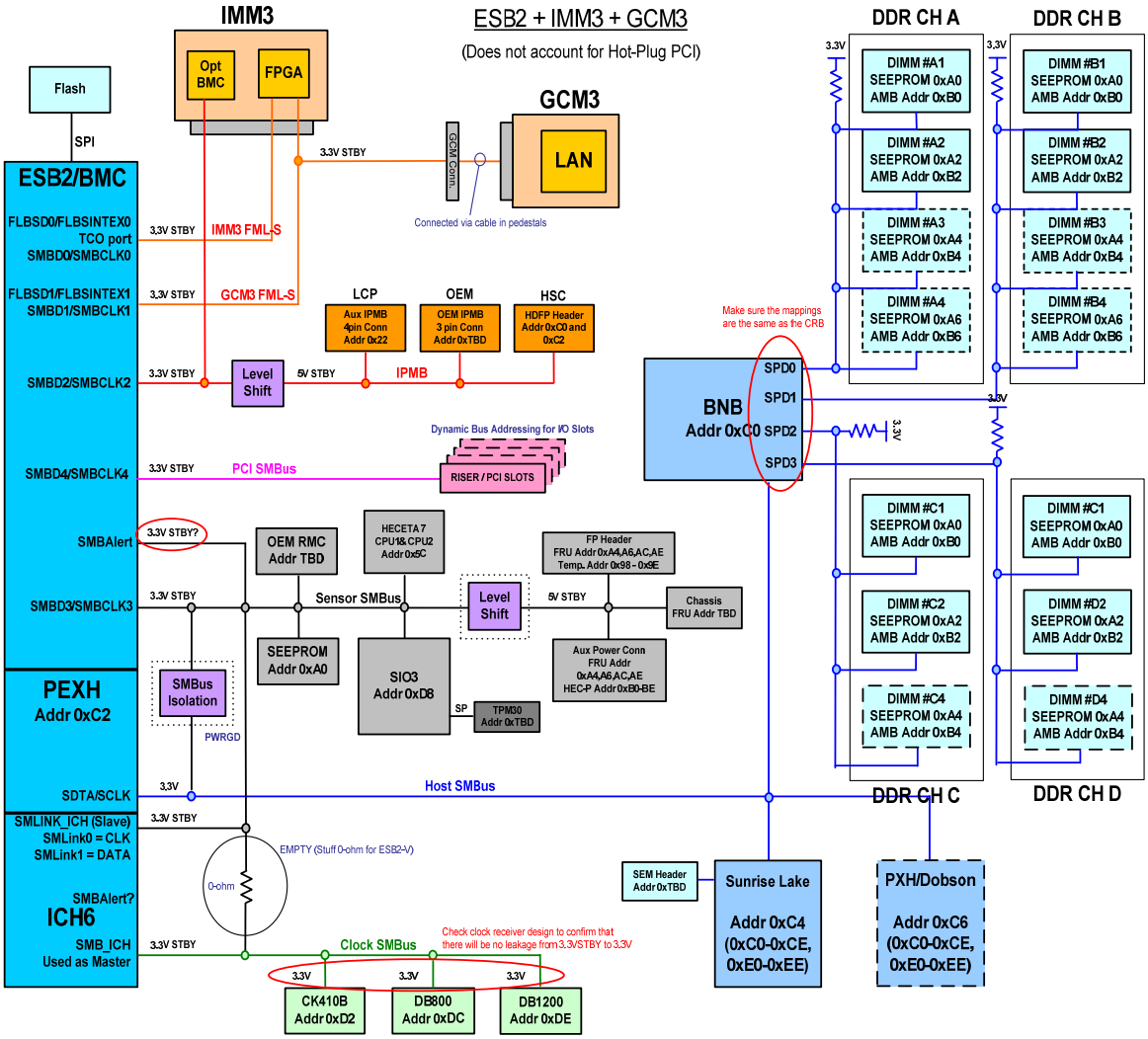


Figure 11. SMBus Block Diagram

4.1 Intel® 6321ESB I/O Controller Hub Integrated Baseboard Management Controller (Integrated BMC) Feature Set

This server board supports the following Integrated Baseboard Management Controller features of the Intel® 6321ESB I/O Controller Hub.

4.1.1 IPMI 2.0 Features

- Integrated Baseboard management controller (Integrated BMC) functionality
- Watchdog timer
- Messaging support, including support for command bridging and user/session
- Chassis device functionality, including support for power/reset control and BIOS boot flags
- Platform event trap (PET) SNMP alerts via LAN interfaces

- Platform event filtering (PEF) device functionality
- Event receiver device functionality: The Integrated BMC receives and processes events from other system subsystems.
- Field replaceable unit (FRU) inventory device functionality: The Integrated BMC supports access to system FRU devices using IPMI FRU commands.
- System event log (SEL) device functionality: The Integrated BMC supports and provides access to a SEL.
- Sensor device record (SDR) repository functionality: The Integrated BMC supports storage and access of system SDRs.
- Sensor device and sensor scanning and monitoring: The Integrated BMC provides IPMI management of system sensors. The Integrated BMC polls system sensors to monitor and report system health. These sensors include soft sensors that are used for reporting system state and events, and hardware sensor.
- IPMI interfaces
  - Host Interfaces – Includes SMS (with "receive message queue" support) and SMM interfaces.
  - Serial Interface – Direct Connect Serial (TMode only).
  - IPMB Interface.
  - LAN Interfaces – supports IPMI over LAN protocol (RMCP, RMCP+).
- Serial over LAN (SOL)
- ACPI state synchronization: The Integrated BMC tracks ACPI state changes that are provided by the BIOS.
- Integrated BMC self test: The Integrated BMC performs initialization and run-time self-tests and makes results available to external entities.

See the *IPMI Specification,* Version 2.0 for more information on these features.

4.1.2 Non-IPMI Features

This section lists non-IPMI feature support carried over from prior generation of servers.

- Fault resilient booting (FRB) support. FRB2 is supported by the watchdog timer functionality.
- Integrated BMC firmware update using firmware transfer mode operation.
- Integrated BMC on-line update: An Integrated BMC rolling update supports a redundant firmware image.
- Power state retention
- Chassis intrusion detection is supported on some systems.
- FRU fault LED support – The Integrated BMC lights the server board LEDs to indicate failed components.
- ASF POST progress queuing: The Integrated BMC queues POST messages sent from the BIOS and makes these accessible through IPMI interfaces.
- Signal testing support: The Integrated BMC provides test commands for setting or getting system signal states.

- Beep code generation: The Integrated BMC generates diagnostic beep codes for fault conditions.
- Hot-swap backplane support: The Integrated BMC pushes the power supply state to the hot-swap controller.
- System GUID storage and retrieval.
- Memory RAS: The Integrated BMC provides sensors to track the DIMM state and memory RAS redundancy state. The Integrated BMC provides IPMI OEM commands to enable the BIOS to push this information to the Integrated BMC.
- Front panel management: The Integrated BMC controls system fault and chassis ID LEDs. It supports secure lockout of certain front panel functionality. It monitors button presses. The chassis ID can be turned on from a front panel button or through a command.
- Power unit management: The Integrated BMC supports a power unit sensor. The Integrated BMC handles power-good dropout condition.
- NMI: The Integrated BMC provides commands to set/get the NMI source. It supports the generation of an NMI signal due to a watchdog timer, IPMI command, or front panel NMI button. The Integrated BMC monitors the system NMI signal.
- ARPs: The Integrated BMC can send and respond to an ARP. This is supported on Intel® 6321ESB I/O Controller Hub embedded NICs.
- DHCP: The Integrated BMC supports DHCP on Intel® 6321ESB I/O Controller Hub embedded NICs.
- SMTP: The Integrated BMC supports SMTP on Intel® 6321ESB I/O Controller Hub embedded NICs.
- Integrated BMC timeclock sync with SIO RTC: At Integrated BMC startup, the Integrated BMC reads SIO RTC and updates its internal time clock to match. The Integrated BMC updates SIO RTC if Integrated BMC internal timeclock is updated by *Set SEL Time* IPMI command.
- Chassis intrusion fan interactions: Fans go to high speed when the chassis intrusion signal is asserted. This is available only on systems that have chassis intrusion support.

4.1.3 New Features

This section lists features that are being introduced on Intel® Server Boards and systems that use the Intel® 5400 Chipset:

- Acoustic management: Improved acoustic levels are achieved by including support for CLTT and fan profiles using TControl version 2 SDRs.
- Intel® Remote Management Module 2 (Intel® RMM 2) support: The Integrated BMC supports the Intel® Remote Management Module 2 as an add-in card. This card utilizes its own ASMI NIC to provide advanced server management features that work in conjunction with the Integrated BMC. This support includes the following:
  - IPMI and IPMI OEM commands to support discovery and configuration of the Integrated BMC by Intel® RMM2.
  - Integrated BMC usage of ASMI NIC via FML (FML used as an extra NIC channel to the Integrated BMC). Integrated BMC can support IPMI over LAN and SOL using this interface.
  - Integrated BMC forwarding of event log messages to Intel® RMM2.

- Integrated BMC notification to Intel® RMM2 of select Integrated BMC status changes.

4.2 Advanced Configuration and Power Interface (ACPI)

The Integrated BMC features work with the ACPI BIOS and with the hardware features of the server board. The following sub-sections illustrate these capabilities. The following table shows the ACPI power states.

Table 18. ACPI Power States

State	Supported	Description
S0	Yes	Working
S1	Yes	Sleeping. Hardware context maintained. Typically equates to processor and chipset clocks stopped.
S2	Yes	Soft off. Typically equates to stopped clocks with processor and cache context lost.
S3	**No**	Typically equates to suspend-to-RAM. This is not supported.
S4	Yes	Non volatile sleep. Typically equates to suspend-to-disk.
S5	Yes	Soft off.

4.2.1 ACPI Power Control

The chipset implements ACPI-compatible power control. Power control requests are routed to the power button input of the chipset, allowing the ACPI-compatible power button logic in the chipset to be utilized. The Integrated BMC can block the power button signal to support secure mode features.

4.2.2 ACPI State Synchronization

The BIOS keeps the Integrated BMC synchronized with the system ACPI state. The BIOS provides the ACPI state when the server transitions between power and sleep states. It uses the SMM interface to provide the ACPI state.

4.2.3 ACPI S0 Support

The following events occur when the ACPI S0 state is entered:

- The front panel power LED is on (not controlled by the Integrated BMC).
- The fans spin at the normal speed, as determined by various sensor inputs.
- Front panel buttons work normally. Front panel lockout can be enabled.

4.2.4 ACPI S1 Sleep Support

The following events occur when the ACPI S1 state is entered:

- The front panel power LED blinks at a rate of 1 Hz with a 50% duty cycle (not controlled by the Integrated BMC).
- If enabled via the *Set ACPI Configuration Mode* command, the server board fans are set to the sleep speed, as specified in the associated OEM TControl SDR for each fan domain. Otherwise, fan control is the same as for ACPI S0 state.
- The watchdog timer is stopped.

- The power, sleep, reset, front panel NMI, and ID buttons are unprotected.

The Integrated BMC detects that the system has exited the ACPI S1 sleep state when it is notified by the BIOS SMI handler.

4.2.5 ACPI S4 Support

The following events occur when the ACPI S4 state is entered:

- The fans are stopped.
- The normal operating system boot process is not followed while exiting from hibernated state.
- The original context is maintained from hibernated to working state.
- The power, sleep, reset, front panel NMI, and ID buttons are unprotected.

4.2.6 ACPI S5 Support

The following event occurs when the ACPI S5 state is entered:

- The front panel buttons are not locked.
- The fans are stopped.
- The power-up process goes through the normal boot process.
- The power, sleep, reset, front panel NMI, and ID buttons are unprotected.
- The system's context is not preserved by the hardware. The system must be restarted to return to the working state.

4.2.7 ACPI Power State Notify

If enabled through the *Set ACPI Configuration Mode* commands, the Integrated BMC sends the system's ACPI power state changes (S0, S1, S3, S4, and S5) to other management controllers by sending the *Set ACPI Power State* command on the IPMB as indicated by their SDR management device records. The command is sent whenever there is a power state transition.

4.3 System Initialization

4.3.1 Processor TControl Setting

Processors used with the Intel® Server Boards and systems that use the Intel® 5400 Chipset implement a feature called Tcontrol. Tcontrol provides a processor-specific value that can be used to adjust the fan control behavior to achieve optimum cooling and acoustics. These values are not directly accessible by the Integrated BMC. The BIOS reads these values during POST and communicates processor Tcontrol values to the Integrated BMC. The Integrated BMC uses these values to adjust the hardware configuration appropriately.

4.3.2 Fault Resilient Booting (FRB)

Fault resilient booting (FRB) is a set of BIOS and Integrated BMC algorithms and hardware support that, under certain conditions, allows a multiprocessor system to boot even if the bootstrap processor (BSP) fails. The FRB algorithms detect BSP failure, disable the failed processor, and reset the server with a different processor as the BSP. Only FRB2 is supported, using watchdog timer commands.

4.3.2.1 Watchdog Timer Timeout Reason Bits

To implement FRB2, during POST the BIOS determines whether a Integrated BMC watchdog timer timeout occurred on the previous boot attempt. If it finds that a watchdog timeout did occur, it determines whether that timeout was an FRB2 timeout, a system management software (SMS) timeout, or an intentional, timed hard reset.

The timeout-reason bits implemented by the Integrated BMC watchdog are maintained by the Integrated BMC across system resets and DC power cycles, but not across AC power cycles.

4.3.2.2 Fault Resilient Booting 2 (FRB2)

FRB2 refers to the FRB algorithm that provides for detection of system failures, such as hangs during POST. The BIOS uses the Integrated BMC watchdog timer to back up its operation during POST. The BIOS configures the watchdog timer to indicate that the BIOS is using the timer for the FRB2 phase of the boot operation.

After the BIOS has identified and saved the BSP information, it sets the FRB2 timer use bit and loads the watchdog timer with the new timeout interval.

If the watchdog timer expires while the watchdog use bit is set to FRB2, the Integrated BMC (if so configured) logs a watchdog expiration event showing the FRB2 timeout in the event data bytes. If the BIOS has set the watchdog timeout action as reset, the Integrated BMC then hard resets the system.

The BIOS is responsible for disabling the FRB2 timeout before initiating the option ROM scan and before displaying a request for a boot password. If the processor fails and causes an FRB2 timeout, the Integrated BMC resets the system.

As part of its normal operation, the BIOS obtains the watchdog expiration status from the Integrated BMC. If this status shows an FRB2 timeout expiration, the BIOS creates an entry in the system event log (SEL) that indicates an FRB2 failure. In the OEM bytes entry in the event log, the entry includes the last POST code generated during the previous boot attempt in the OEM bytes of the event entry. FRB2 failure is not reflected in the processor status sensor value.

Although an FRB2 failure causes events to be logged into the SEL, there is no effect on the front panel LEDs.

4.3.3 Boot Control Support

The Integrated BMC supports the IPMI 2.0 boot control feature. This feature allows the boot device and boot parameters to be managed remotely.

4.4 Integrated Front Panel User Interface

The Integrated BMC in the Intel® 6321ESB I/O Controller Hub incorporates the front panel interface functionality and supports an SSI EB compliant model. The indicators on the Intel® 6321ESB I/O Controller Hub supported front panels are LEDs. They may be single or bicolor, depending on the supported model.

4.4.1 Power LED

The green power LED is active when system DC power is on. The power LED is controlled by the BIOS. The power LED reflects a combination of the state of system (DC) power and the system ACPI state. The following table shows the states that can be assumed.

Table 19. Power LED Indicator States

State	ACPI	Power LED
Power off	No	Off
Power on	No	Solid on
S4/S5	Yes	Off
S1 Sleep	Yes	~1 Hz blink
S0	Yes	Solid on

4.4.2 System Status LED

Note: The system status LED state shows the state for the current, most severe fault. For example, if there was a critical fault due to one source and a non-critical fault due to another source, the system status LED state would be solid on (the state for the critical fault).
The system status LED is a bicolor LED. Green (status) is used to show a normal operation state or a degraded operation. Amber (fault) shows the system hardware state and overrides the green status.

The Integrated BMC-detected state and the state from other controllers, such as the SAS/SATA hot-swap controller state, is included in the LED state. For fault states that are monitored by the Integrated BMC sensors, the contribution to the LED state follows the associated sensor state, with the priority going to the most critical state that is currently asserted.

When the server is powered down (transitions to the DC-off state or S5), the Integrated BMC is still on standby power and retains the sensor and front panel status LED state established prior to the power-down event.

The following table maps the system state to the LED state:

Table 20. System Status LED Indicator States

Color	State	System Status	Description
Green	Solid on	Ok	System ready
Green	~1 Hz blink	Degraded	System degraded: BIOS detected 1. Unable to use all of the installed memory (more than one DIMM installed).[1] 2. Correctable errors over a threshold of ten and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spare DIMMs indicating a redundancy lost condition. The c\Corresponding DIMM LED should light up.[1] 3. In a mirrored configuration, when memory mirroring takes place and system loses memory redundancy. This is not covered by (2).[1] 4. PCI Express* correctable link errors. Integrated BMC detected 1. Redundancy loss such as power supply or fan. Applies only if the associated platform subsystem has redundancy capabilities. 2. CPU disabled – if there are two CPUs and one CPU is disabled. 3. Fan alarm – Fan failure. Number of operational fans should be more than the minimum number needed to cool the system. 4. Non-critical threshold crossed – Temperature, voltage, power nozzle, power gauge, and PROCHOT[2] (Therm Ctrl) sensors. 5. Battery failure. 6. Predictive failure when the system has redundant power supplies.
Amber	~1 Hz blink	Non-Fatal	Non-fatal alarm – system is likely to fail: BIOS Detected 1. In the non-sparing and non-mirroring mode if the threshold of ten correctable errors is crossed within the window[1]. 2. PCI Express* uncorrectable link errors. Integrated BMC Detected 1. Critical threshold crossed – Voltage, temperature, power nozzle, power gauge, and PROCHOT (Therm Ctrl) sensors. 2. VRD Hot asserted 3. Minimum number of fans to cool the system are not present or have failed

Color	State	System Status	Description
Amber	Solid on	Fatal	Fatal alarm – system has failed or shutdown: BIOS Detected 1. DIMM failure when there is one DIMM present and no good memory is .present[1]. 2. Run-time memory uncorrectable error in a non-redundant mode[1]. 3. CPU configuration error (for instance, processor stepping mismatch). Integrated BMC Detected 1. CPU IERR signal asserted. 2. CPU 1 is missing. 3. CPU THERMTRIP. 4. No power good – power fault. 5. Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present).
Off	N/A	Not ready	AC power off

Note:

1. BIOS detects these conditions and sends a *Set Fault Indication* command to the Integrated BMC to provide the contribution to the system status LED.
2. Support for upper non-critical limit is not provided in the default SDR configuration. However if a user does enable this threshold in the SDR, then the system status LED should behave as described.

4.4.3 Chassis ID LED

The chassis ID LED provides a visual indication of a system being serviced. The state of the chassis ID LED is affected as follows:

- Toggled by the chassis ID button
- Controlled by the *Chassis Identify* command (IPMI)
- Controlled by the *Chassis Identify LED* command (OEM)

Table 21. Chassis ID LED Indicator States

State	LED State
Identify active via button	Solid on
Identify active via command	~1 Hz blink
Off	Off

There is no precedence or lock-out mechanism for the control sources. When a new request arrives, all previous requests are terminated. For example, if the chassis ID LED is blinking and the chassis ID button is pressed, then the chassis ID LED changes to solid on. If the button is pressed again, with no intervening commands, the chassis ID LED turns off.

4.4.4 Front Panel/Chassis Inputs

The Integrated BMC monitors the front panel switches and other chassis signals. The front panel input buttons are momentary contact switches that are debounced by the Integrated BMC processor firmware. The debounce time is 50 ms; the signal must be in a constant low state for 50 ms before it is treated as asserted.

4.4.4.1 Chassis Intrusion

Some systems support chassis intrusion detection. On systems that support chassis intrusion detection, the Integrated BMC monitors the state of the *Chassis Intrusion* signal and makes the status of the signal available via the *Get Chassis Status* command and the *Physical Security* sensor state. If enabled, a chassis intrusion state change causes the Integrated BMC to generate a *Physical Security* sensor event message with a *General Chassis Intrusion* offset (00h).

The Integrated BMC boosts all fans when the chassis intrusion signal is active. This provides sufficient cooling when a technician has the cover removed while servicing the system. Fans return to their previous level when the chassis intrusion signal is no longer active.

4.4.4.2 Reset Button

An assertion of the *Front Panel Reset* signal to the Integrated BMC causes the system to start the reset and reboot process, as long as the Integrated BMC has not locked out this input. This assertion is immediate and without the cooperation of any software or operating system running on the system.

4.4.4.3 Diagnostic Interrupt (Front Panel NMI)

As stated in the *IPMI Specification,* Version 2.0, a diagnostic interrupt is a non-maskable interrupt (NMI) or signal for generating diagnostic traces and 'core dumps' from the operating system. For Intel® server boards, this is an NMI.

The diagnostic interrupt button is connected to the Integrated BMC through the front panel connector. Pressing the diagnostic interrupt button causes the Integrated BMC to do the following:

- Generate a *Critical Event* sensor event message with a *Front Panel NMI/Diagnostic interrupt* offset (00h), if enabled.
- Set the OEM 1 (40h) bit in the message flags. The message flags can be read with the *Get Message Flags* command and cleared with the *Clear Message Flags* command.
- Set bit 0 in NMI source 1. This information can be retrieved with the *Get NMI Source* command.
- Generate a system NMI pulse.

Once an NMI has been generated by the Integrated BMC, the Integrated BMC does not generate another NMI until the system has been reset or powered down.

The Integrated BMC automatically clears the OEM 1 message flag and NMI sources whenever it detects a system reset, or is itself reset. The diagnostic interrupt button is not disabled or otherwise affected when the system is in secure mode, although the *Set Secure Mode Options* command can be used to block the use of this button.

4.4.4.4 Chassis Identify

The front panel chassis identify button toggles the state of the chassis ID LED. If the LED is off, then pushing the ID button lights the LED. It remains lit until the button is pushed again or until a *Chassis Identify* or a *Chassis Identify LED* command is received to change the state of the LED.

4.4.5 Secure Mode and Front Panel Lock-out Operation

The secure mode feature allows the front panel buttons to be protected against unauthorized use or access. The secure mode is enabled and controlled via the *Set Secure Mode Options* command.

When secure mode is enabled and active and a protected front panel button is pressed, a Secure Mode Violation event is generated – specifically asserting the *Secure Mode Violation Attempt* offset (00h) of the Integrated BMC's *Security Violation Attempt* sensor. The secure mode state is cleared by the following:

- Whenever AC power or system power is applied
- When a system reset occurs
- When a Integrated BMC reset occurs

The secure mode state includes the bits that specify the actions that are to be taken when the secure mode is active, and the *Force Secure Mode On* bit.

The *Set Secure Mode Options* command allows specific front panel buttons to be protected regardless of the secure mode state. This protection includes blocking the buttons and generating secure mode violation events if one of the buttons is pressed when in the secure mode state. See the command definition for details. Support is available only for protecting the front panel power and reset buttons as a unit; these buttons cannot be individually locked.

The set of buttons that is protected when Secure Mode is active varies, depending on the system ACPI power state.

Table 22. Secure Mode vs. ACPI State

ACPI State	Power Button	Reset Button	Diagnostic Interrupt Button (Front Panel NMI)	ID Button
S0	Protected	Protected	Unprotected	Unprotected
S1	Unprotected	Unprotected	Unprotected	Unprotected
S4/S5	Unprotected	Unprotected	Unprotected	Unprotected

4.5 Platform Control

This server board has embedded platform control that is capable of automatically adjusting system performance and system acoustic levels.

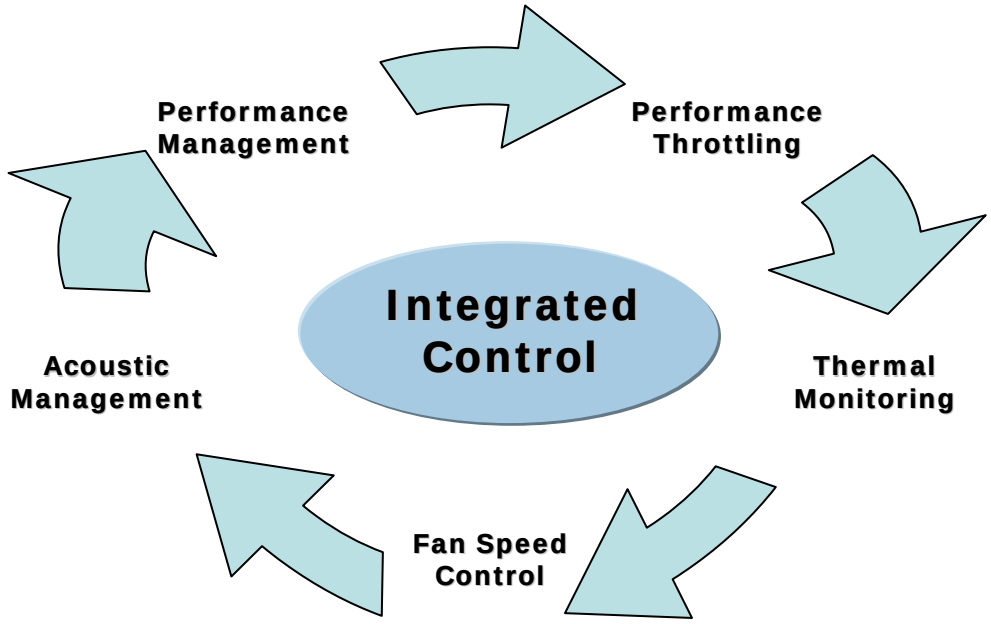


Figure 12. Platform Control

4.5.1 Overview

The platform components used to implement platform control include:

- Integrated Baseboard Management Controller functions of the Intel® 6321ESB I/O Controller Hub
- LM94 Sensor Monitoring Chip
- Platform Sensors
- Variable Speed System Fans
- System BIOS
- Integrated BMC Firmware
- Sensor Data Records as loaded by the FRUSDR Utility
- FBDIMM type
- Processor type

Platform control optimizes system performance and acoustics levels through:

- Performance Management
- Performance Throttling
- Thermal Monitoring
- Fan Speed Control
- Acoustics Management

Memory throttling is a feature of the Intel® 5400 Chipset to prevent FBDIMM memory from overheating. If the performance of the installed FBDIMMs approaches their supported thermal limit for a given platform, the system BIOS initiates memory throttling. This manages memory performance by limiting bandwidth to the DIMMs, therefore capping the power consumption and preventing the DIMMs from overheating.

Two different memory throttling mechanisms are supported on this server board:

- Closed Loop Thermal Throttling (CLTT)
- Open Loop Throughput Throttling (OLTT)

The system BIOS determines which mechanism to implement based on the following flow chart:

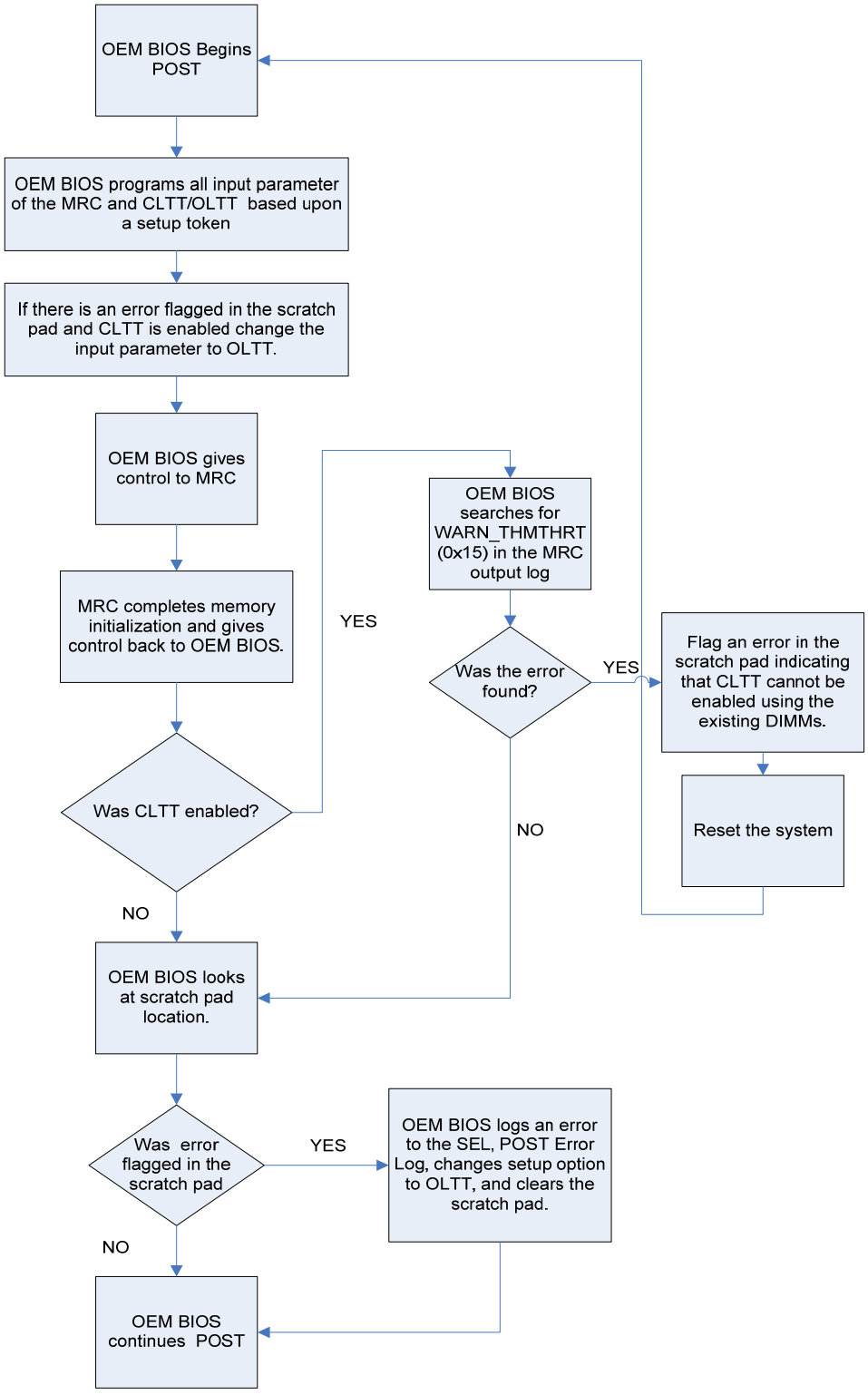


Figure 13. Memory throtting mechanisms implemented flow through the system BIOS

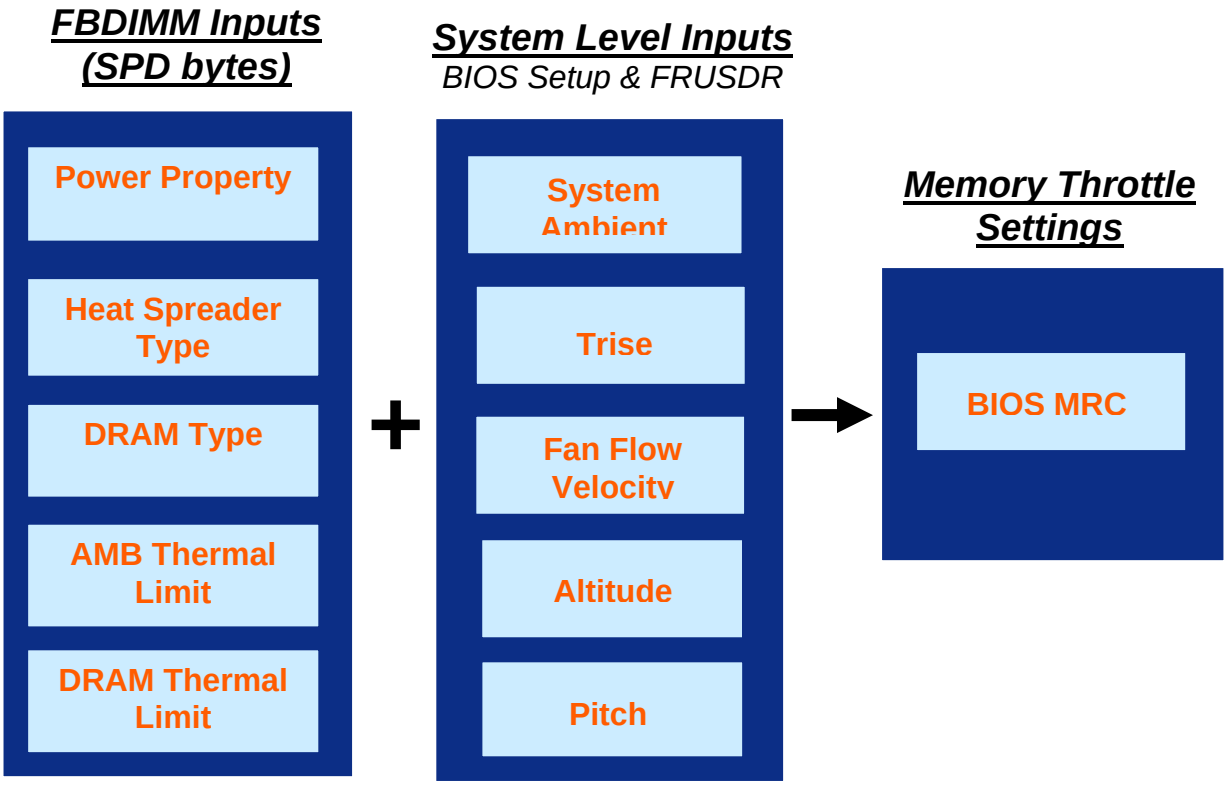


Figure 14. Memory Throttle Settings Inputs

The following sections describe the functionality of each platform control mechanism:

4.5.2 FBDIMM Closed Loop Thermal Throttling (CLTT)

Closed Loop Memory throttling (CLTT) is a feature of the Intel chipset to prevent FBDIMM memory from overheating. This is a temperature based throttling feature. If the temperature of the installed FBDIMMs approaches their thermal limit, the system BIOS initiates memory throttling. This manages memory performance by limiting bandwidth to the DIMMs, therefore capping the power consumption and preventing the DIMMs from overheating. By default, the BIOS configures the system to support CLTT if it detects that there are functional AMB thermal sensors present on all installed DIMMs. In the CLTT mode, the system fans run slower to meet the acoustic limits for the given platform but this mode also allows the fans to ramp up as needed to maintain the parts within temperature specifications under high stress levels.

In a similar way to OLTT, the system BIOS utilizes a Memory Reference Code (MRC) throttling algorithm to maximize memory bandwidth for a given configuration. The MRC code relies on Serial Presence Detect (SPD) data read from the installed DIMMs. Closed Loop Thermal Throttling is autonomous and internal to the MCH hardware and the throttling algorithm always throttles the minimum amount required to prevent the part from overheating.

Note: CLTT is the Intel preferred platform control mechanism as it provides the best memory bandwidth performance while providing the lowest system fan acoustics. CLTT is supported by default when FBDIMMs are installed with functional AMB thermal sensors.

4.5.3 FBDIMM Open Loop Throughput Throttling (OLTT)

Open Loop Throughput Throttling (OLTT) is based on a hardware bandwidth count and works by preventing the bandwidth from exceeding the throttling settings programmed into the MCH registers. The system BIOS automatically selects OLTT as the memory throttling mechanism if it detects that one or more installed DIMMs do not have a functional AMB thermal sensor. Once the system BIOS enables OLTT, it utilizes a Memory Reference Code (MRC) throttling algorithm to maximize memory bandwidth for a given configuration. The MRC code relies on Serial Presence Detect (SPD) data read from the installed DIMMs as well as system level data as set through the FRUSDR utility.

4.5.4 Fan Speed Control

System fan speed is controlled by the Integrated Baseboard Management Controller (Integrated BMC) functions of the Intel® 6321ESB I/O Controller Hub chip. During normal system operation, the Integrated BMC retrieves information from the BIOS and monitors several platform thermal sensors to determine the required fan speeds.

In order to provide the proper fan speed control for a given system configuration, the Integrated BMC must have the appropriate platform data programmed. Platform configuration data is programmed using the FRUSDR utility during the system integration process and by the system BIOS during runtime.

4.5.4.1 System Configuration Using the FRUSDR Utility

The Field Replaceable Unit and Sensor Data Record Update utility (FRUSDR utility) is a program used to write platform-specific configuration data to NVRAM on the server board. It allows the user to select the supported chassis (Intel or non-Intel) and platform chassis configuration that is being used. Based on the input provided, the FRUSDR writes sensor data specific to the configuration to NVRAM for the Integrated BMC controller to read each time the system is powered on.

4.5.4.2 Fan Speed Control from Integrated BMC and BIOS Inputs

Using the data programmed to the NVRAM by the FRUSDR utility, the Integrated BMC is configured to monitor and control the appropriate platform sensors and system fans each time the system is powered on. After power-on, the Integrated BMC uses additional data provided to it by the system BIOS to determine how the system fans should be controlled.

The BIOS provides data to the Integrated BMC about the fan profile (Acoustics Mode [CLTT Default] or Performance Mode [OLTT Default]) for which the platform is set up and the Altitude setting that the platform is configured to support. Only the Altitude setting is a configurable option in the BIOS setup. The BIOS also uses parameters retrieved from the thermal sensor data records (SDR) to configure the system for memory throttling and fan speed control. If the BIOS fails to get the thermal SDRs, then it uses the Memory Reference Code (MRC) default settings for the memory throttling settings. Each operating mode has a predefined profile for

which specific platform targets are configured, which in turn determines how the system fans operate to meet those targets. Platform profile targets are determined by the type of platform that is selected when running the FRUSDR utility.

4.6 Standard Fan Management

The Integrated BMC controls and monitors the system fans. For each fan, there is a fan speed sensor that provides fan failure detection. Some systems also provide fan presence detection in which the Integrated BMC maps into per-fan presence sensors.

It is possible for the Integrated BMC to control the speed of some fans. Controllable fans are divided into fan domains in which there is a separate fan speed control for each domain and a separate fan control policy configurable for each domain. Two or more fans tied to a common fan domain cannot be controlled independently. For the Intel® Server Board S5400SF, there are four fan domains, which control four system fan connectors and two CPU fan connectors. The following table identifies the association of the on-board fan connectors to a specific fan domain.

Table 23. Fan Domain Identification Table

Fan Connector	Fan Domain Name	Fan Domain Controller
System Fan 1 (J3K2)	FAN_IO_PWM	87427 SIO Controller
System Fan 2 (J3K3)	FAN_IO_PWM	87427 SIO Controller
System Fan 3 (J1B3)	FAN_MEM_PWM	87427 SIO Controller
System Fan 4 (J1C1)	FAN_MEM_PWM	87427 SIO Controller
CPU 1 Fan (J9K1)	FAN_PWM_CPU1	LM94
CPU 2 Fan (J4K1)	FAN_PWM_CPU2	LM94
FAN Board Connector[1]	FAN_IO_PWM; FAN_PWM_CPU1; FAN_PWM_CPU2	87427 SIO Controller LM94

[1] For the pin-out definition, see Chapter 6.

A fan domain can have a set of temperature and fan sensors associated with it. These are used to determine the current fan domain state. A fan domain has three states: sleep, nominal, and boost. The sleep and boost states have fixed but configurable (via OEM SDRs) fan speeds associated with them. The nominal state has a variable speed determined by the fan domain policy. An OEM SDR record is used to configure the fan domain policy.

Fan domain state is controlled by several factors (states in order of precedence, high to low):

Boost

- Associated fan in a critical or non-recoverable state (non-redundant fan configuration).
- Fan domain is in an *insufficient resources* redundancy state (redundant fan configuration).
- Any temperature sensor in a critical or non-recoverable state, with the exception of Processor Thermal Control Monitoring sensor (ProcHot) or VRD Over-Temperature (VRDHot) sensor.

Sleep

No boost conditions, system in ACPI S1 sleep state, and Integrated BMC configured to transition fan domains to sleep state via the *Set ACPI Configuration Mode* command.

Nominal

It is possible to configure a fan domain's nominal fan speed to be either static (fixed value) or controlled by the state of one or more associated temperature sensors. OEM SDR records are used to configure which temperature sensors are associated with which fan control domains as well as the relationship (algorithm) between the temperature and fan speed control (PWM) value. Multiple OEM SDRs may reference/control the same fan control domain and multiple OEM SDRs may reference the same temperature sensors. The PWM value for the given domain is computed using one or more instances of a stepwise linear algorithm and a clamp algorithm. The transition from one computed nominal fan speed (PWM value) to a new one is ramped over time to minimize audible transitions. The ramp rate is configurable via the OEM SDR.

For more information about fan management, refer to the *Intel® 5400 Series Server Board Integrated Baseboard Management Controller Core External Product Specification*.

4.7 Private Management I²C Buses

The Integrated BMC controls multiple private I^2C buses. The Integrated BMC is the sole master on these buses. External agents must use the Integrated BMC's *Master Write/Read I^2C* command if they require direct communication with a device on any of these buses. In general, only FRU devices are accessible in this manner. Sensor devices should not be directly accessed by Integrated BMC clients.

4.8 Integrated BMC Messaging Interfaces

This section provides a high-level overview of some of the supported Integrated BMC communication interfaces, which include the following:

- Host SMS Interface via low pin count (LPC)/keyboard controller style (KCS) interface
- Host SMM Interface via low pin count (LPC)/keyboard controller style (KCS) interface
- Intelligent platform management bus (IPMB) I^2C interface
- PCI SMBus
- Emergency management port (EMP) using the IPMI over Serial/Modem protocols for serial remote access.
- LAN interface using the IPMI-over-LAN protocols

Refer to the *Intel® 5400 Series Server Board Integrated Baseboard Management Controller Core External Product Specification* for more information.

4.8.1 LPC/KCS Interface

The Integrated BMC has three 8042 keyboard controller style (KCS) interface ports as described in the *IPMI Specification,* Version 2.0. These interfaces are mapped into the host I/O space and accessed via the chipset low pin count (LPC) bus.

4.8.2 Server Management Software (SMS) Interface

The SMS interface is the Integrated BMC host interface. The Integrated BMC implements the SMS KCS interface as described in the *IPMI Specification,* Version 2.0.

4.8.3 Server Management Mode (SMM) Interface

The SMM interface is a KCS interface that is used by the BIOS when interface response time is a concern, such as with the BIOS SMI handler. The Integrated BMC gives this interface priority over other communication interfaces.

4.8.4 IPMB Communication Interface

The IPMB is a communication protocol that utilizes the 100 KB/s version of an I^2C bus as its physical medium. For more information on I^2C specifications, refer to *The I^2C Bus and How to Use It* document*.* The IPMB implementation in the Integrated BMC is compliant with the *IPMB v1.0,* Revision 1.0*.*

4.8.5 Emergency Management Port (EMP) Interface

The emergency management port (EMP) interface is the Intel implementation of the IPMI 2.0: IPMI over Serial/Modem feature. The primary goal of providing an out-of-band RS-232 connection is to give system administrators the ability to access low-level server management firmware functions by using commonly available tools. To make it easy to use and to provide high-compatibility with LAN and IPMB protocols, this protocol design adopts some features of both protocols.

4.8.6 LAN Interface

The Integrated BMC implements both the IPMI 1.5 and IPMI 2.0 messaging models. These provide out-of-band local area network (LAN) communication between the Integrated BMC and the external world.

The Integrated BMC supports a maximum of three LAN interfaces:

- Two of the LAN interfaces utilize the embedded Intel® 6321ESB I/O Controller Hub NICs (one channel per embedded NIC).
- One LAN interface utilizes an optional external NIC known as the Intel® Remote Management Module 2 (Intel® RMM2) NIC. Use of this NIC requires the installation of the optional Intel® RMM2 add-in card.

See the *IPMI Specification,* Version 2.0 for details on the IPMI-over-LAN protocol.

Run-time determination of LAN channel capabilities can be determined both by standard IPMI defined mechanisms and by an OEM configuration parameter that defines advanced feature support.

4.9 Event Filtering and Alerting

The Integrated BMC implements most of the IPMI 2.0 alerting features. The following features are supported:

- PEF
- Alert-over-LAN

4.9.1 Platform Event Filtering

The Integrated BMC monitors system health and logs failure events into the SEL. Platform event filtering provides a configurable mechanism to allow events to trigger alert actions. PEF provides a flexible, general mechanism that enables the Integrated BMC to perform selectable actions triggered by a configurable set of system events. The Integrated BMC supports the following PEF actions:

- Power off
- Power cycle
- Reset
- Diagnostic interrupt
- OEM action
- Alerts

See the *IPMI Specification,* Version 2.0 for additional details of PEF operation.

4.9.2 Alert-over-LAN

Platform event trap (PET) alerts, standard and advanced, are supported over a LAN. Alert-over-LAN is used to notify remote system management application about PEF-selected events, regardless of the state of the server's operating system. LAN alerts can be sent over any of the LAN channels supported by a system, modulo the specific channel capabilities. The Integrated BMC implements the following three OEM PEF parameters associated with platform event trap alerts over the LAN:

- *PET OEM String* (parameter 96)
  This string, if defined, is included as part of the PET packet OEM data field.
- *Infinite Retry Alert Behavior* (parameter 97)
  A byte value where if equal to 1, indicates that alert-over-LAN should retry alerts until they succeed.
- *UTC Offset* (parameter 98)
  This parameter provides a value for the UTC offset field in the PET packet.

The alert-over-LAN resource size is LAN Alert Destination Count = 4. See the *IPMI Specification,* Version 2.0 for additional details on PET alerts.

4.9.3 Factory Default Event Filters

A maximum of 20 PEF table entries are supported. The following table describes the 12 factory-preconfigured event filters. The remaining 8 entries are software configurable. Each PEF entry contains 22 bytes of data for a maximum table size of 440 bytes.

Table 24. Factory Default Event Filters

Event Filter Number	Offset Mask	Events
1	Non-critical, critical and non-recoverable	Temperature sensor out of range
2	Non-critical, critical and non-recoverable	Voltage sensor out of range
3	Non-critical, critical and non-recoverable	Fan failure
4	General chassis intrusion	Chassis intrusion (security violation)
5	Failure and predictive failure	Power supply failure
6	Uncorrectable ECC	BIOS
7	POST error	BIOS: POST code error
8	FRB1, FRB2, and FRB3	Not supported
9	–	Reserved (no source for fatal NMI)
10	Power down, power cycle, and reset	Watchdog timer
11	OEM system boot event	System restart (reboot)
12	–	Reserved (not preconfigured; reserved for future use)

4.9.4 Alert Policies

An alert policy is associated with each PEF entry and it determines whether the alert is a dial page or a PPP alert, and over which IPMI channel the alert is to be sent. There is a maximum of 20 alert policy entries. There are no preconfigured entries in the alert policy table because the destination types and alerts may vary by user. Each entry in the alert policy table contains 4 bytes for a maximum table size of 80 bytes.

4.10 Watchdog Timer

The Integrated BMC implements a fully IPMI 2.0-compatible watchdog timer. See the *IPMI Specification,* Version 2.0 for details. The NMI/diagnostic interrupt specified for an IPMI 2.0 watchdog timer is associated with an NMI on IA-32 systems. A watchdog pre-timeout SMI (or equivalent signal assertion) is not supported.

4.11 System Event Log (SEL)

The Integrated BMC implements the logical system event log as specified in the *Intelligent Platform Management Interface Specification,* Version 2.0*.* The SEL is accessible via all communication transports. This way out-of-band interfaces can access SEL information even while the server is down.

The Integrated BMC allocates 65,536 bytes (64 KB) of non-volatile storage space for storing system events. Each system log record is padded with an extra four-byte timestamp that indicates when the record is deleted, making each SEL record 20 bytes in size. There can be up to 3,276 SEL records stored at a time. An attempt to add a SEL record after 3,276 records are stored results in a failure, and the out-of-space completion code is returned.

4.12 Sensor Data Record (SDR) Repository

The Integrated BMC implements the logical sensor data record (SDR) repository as specified in the *Intelligent Platform Management Interface Specification,* Version 2.0. The SDR repository is accessible via all communication transports. This way out-of-band interfaces can access SDR repository information evn while the system is down.

The Integrated BMC allocates 65,536 bytes (64 KB) of non-volatile storage space for the SDR.

4.13 Field Replaceable Unit (FRU) Inventory Device

The Integrated BMC implements the interface for logical FRU inventory devices as specified in the *Intelligent Platform Management Interface Specification*, Version 2.0. This functionality provides commands used for accessing and managing the FRU inventory information. These commands can be delivered via all interfaces.

The Integrated BMC provides FRU device command access to its own FRU device, and to the FRU devices throughout the server. The FRU device ID mapping for a specific server board is defined in the appendix. The Integrated BMC controls the mapping of the FRU device ID to the physical device. In accordance with the *IPMI Specification*, FRU device 0 is always located on the server board.

4.14 Non-maskable Interrupt (NMI)

On IA-32 systems, the Integrated BMC has specific monitoring and signal generation functionality in regards to the NMI signal. When a diagnostic interrupt (also referred to as front panel diagnostic interrupt or NMI/diagnostic interrupt) is generated by the Integrated BMC, the actual signal that is pulsed is the NMI signal. A front panel diagnostic interrupt sensor is used to log SEL events for assertion of the diagnostic interrupt.

4.15 General Sensor Behavior

4.15.1 Sensor Initialization

As part of the Integrated BMC initialization, upon application of standby power or Integrated BMC reset, the Integrated BMC enables a subset of its sensors. This is done prior to loading any SDRs. This allows some amount of sensor functionality even if there are no SDRs present. Subsequent loading of SDRs may change the configuration of these sensors.

The sensors that are enabled independently of an SDR load include processor status sensors.

4.15.2 Sensor Re-arm

All sensors (manual and auto re-arm) that show an asserted event status generate a de-assertion SEL event when the sensor is re-armed, provided that the associated SDR is configured to enable a de-assertion event for that condition. This applies regardless of whether the sensor is re-armed by an IPMI command, the Integrated BMC Initialization agent, or due to sensor-specific re-arm trigger events (for instance, insertion of a hot-swap fan should re-arm an associated manual re-arm fan tach sensor). This behavior applies regardless of whether the sensor is a threshold/analog sensor or a discrete sensor.

If the condition that caused the original assertion is no longer present at the time the re-arm occurs, then the entire sequence is as follows:

1. Failure condition occurs and Integrated BMC logs an assertion event.
2. Sensor is re-armed.
3. Integrated BMC clears sensor status and generates a de-assertion event.
4. Sensor is put into “Init in progress” state until sensor is polled again or otherwise updated.
5. Sensor is polled and the “Init in progress” state is cleared.

If the condition that caused the original assertion is present at the time the re-arm occurs, then the entire sequence is as follows:

1. Failure condition occurs and Integrated BMC logs an assertion event.
2. Sensor is re-armed
3. Integrated BMC clears sensor status and generates a de-assertion event.
4. Sensor is put into “Init in progress” state until sensor is polled again or otherwise updated.
5. Sensor is polled, the failure detected, and the Integrated BMC logs an assertion event.

All auto re-arm sensors that show an asserted event status generate a de-assertion SEL event at the time the Integrated BMC detects that the condition causing the original assertion is no longer present and the associated SDR is configured to enable a de-assertion event for that condition.

4.16 Processor Sensors

The Integrated BMC provides IPMI sensors for processors and associated components, such as voltage regulators and fans. Most of these sensors are implemented on a per-processor basis.

Table 25. Processor Sensors

Sensor Type	Per-Proc Socket	Description
Processor Status	Yes	Processor presence and fault state
Processor Temperature	Yes	Temperature from processor itself
Processor VRD Over-temperature Indication	Yes	Discrete sensor that indicates a processor VRD has crossed an upper operating temperature threshold
Processor Voltage	Yes	Threshold sensor for voltage from processor voltage regulator
Processor Voltage Limit Fault	Yes	Discrete sensor that indicates a processor voltage is out of range
Processor Fan Speed	Yes	Speed of processor fan (not always present)
Processor Thermal Control (ProcHot)	Yes	Percentage of time a processor is throttling due to thermal conditions
CPU Population Error	No	Improper socket population. This means slot 1 is empty.

4.16.1 Processor Status Sensors

The Integrated BMC provides an IPMI sensor of type ‘processor’ for monitoring status information for each processor slot. With the exception of the processor presence offset, if an

event state (sensor offset) has been asserted, it remains asserted until one of the following occurs:

- A *Rearm Sensor Events* command is executed for that processor status sensor.
- A *Processor Retest* command is executed. The BIOS sends this command to the Integrated BMC as a result of a user choosing the *Processor Retest* option from the BIOS Setup screen.
- AC power cycle occurs. This will only clear persistent bits of the sensor if the processor is not present.

DC power-on and system resets do not re-arm processor status sensors.

Table 26. Requirements for Processor Status

Offset	Processor Status	Detected By	Persistent
0	IERR	Integrated BMC	–
1	Thermal trip	Integrated BMC	X
2	FRB1/BIST failure	Not supported	–
3	FRB2/Hang in POST failure	BIOS[1]	–
4	FRB3/Processor startup/initialization failure (CPU fails to start)	Not supported	–
5	Configuration error (for instance, stepping mismatch)	BIOS	–
6	SM BIOS uncorrectable CPU-complex error	Not supported	–
7	Processor presence detected	Integrated BMC	–
8	Processor disabled	N/A	–
9	Terminator presence detected	Not supported	–

Note 1: Fault is not reflected in the processor status sensor.

4.16.2 Processor VRD Over-temperature Sensor

This sensor monitors a signal that indicates whether or not a processor VRD is running over the temperature threshold. The state of this signal is not an input into the system fan control subsystem. However, it is an input into the National Semiconductor LM94* device, which in turn asserts the associated ProcHot signal and effectively lowers the VRD temperature. This relationship is 1:1, i.e, if VRD-hot is asserted, then ProcHot asserts.

4.16.3 ThermalTrip Monitoring

The Integrated BMC is responsible for persistently retaining ThermalTrip history for each processor. This history tracks whether the processor has had a ThermalTrip since the last processor sensor re-arm or retest.

When a ThermalTrip occurs, the system hardware automatically attempts to power down the server. Before the system is allowed to power down, the Integrated BMC polls the ThermalTrip status for each processor, at which point the power down sequence continues. If the Integrated BMC detects that a ThermalTrip occurred, then it sets the ThermalTrip offset for the applicable processor status sensor. As this bit is persistent across AC cycles, the Integrated BMC logs thermal trip events every AC cycle until the processor is manually re-armed.

4.16.4 Internal Error (IERR) Monitoring

The Integrated BMC monitors the IERR signal from each processor and maps this to the IERR offset of the associated processor status sensor.

4.16.5 Dynamic Processor Voltage Monitoring

Processors used on Intel® server boards and systems that use the Intel® 5400 Chipset support dynamic operating states in which the processor VIDs can change under program control or due to operating conditions. It is not feasible for the Integrated BMC to dynamically alter voltage thresholds for direct monitoring of the processor voltages. However, the LM94 device supports dynamic monitoring. The Integrated BMC reads a status register from the LM94 device, which indicates if the processor voltage is within acceptable limits. This status is reflected in the *Processor Voltage Limit Fault* sensors (one per processor).

The Integrated BMC provides threshold type sensors for reading the processor voltages. SEL logging and other fault notification is handled by the *Processor Voltage Limit Fault* sensors rather than the threshold sensors.

4.16.6 Processor Temperature Monitoring

Processors used on Intel® server boards and systems that use the Intel® 5400 Chipset are multi-core and have one physical temperature sensor per core. The type of physical temperature sensor provided is processor-specific digital Thermal Sensor.

4.16.7 Processor Thermal Control Monitoring (ProcHot)

The Integrated BMC monitors processor thermal control monitoring for each processor. This functionality is provided by an LM94 device which provides a reading of the percentage of time that the processor *ProcHot* signal is asserted over a given measurement window (set to 5.8 seconds).

The Integrated BMC implements this as a threshold sensor (IPMI sensor type is ‘processor’, sensor name is “Therm Ctrl %”) on a per-processor basis. This sensor supports one threshold (the upper-critical) and it is set for 50% by default in the SDRs.

4.16.8 CPU Population Error Sensor

The only processor population check that the Integrated BMC performs is to verify that a processor is installed in socket 1. The hardware does not allow the server to power up if a processor is not installed in this socket.

At Integrated BMC initialization, the CPU Population Error sensor is first set to a de-asserted state. The Integrated BMC then checks for CPU population errors and sets the new value accordingly. If an error is detected and the SDR is so configured, a SEL event is logged. The Integrated BMC checks for this fault condition and updates the sensor state at each attempt to DC power on the system. At each DC power-on attempt, a beep code is generated if this fault is detected.

This sensor is an auto-re-arm sensor but is not re-armed at system DC power-on or for system resets. The correct way to clear this sensor state is to correct the problem by doing the following:

1. AC powering down the server.
2. Installing a processor into slot 1.
3. AC powering on the server.

4.17 Intel® Remote Management Module 2 (Intel RMM2) Support

The server board includes a high-density 120-pin Intel® RMM2 connector at location J1C2 providing support for the Intel® Remote Management Module 2 (Intel® RMM2) server management card. This is a second generation server management option that provides keyboard, video, mouse (KVM) redirection capability and other advanced server management functionality. In support of the Intel® RMM2 card, the server board also includes a Intel® RMM2 NIC connector at location J1B2, providing the Intel® RMM2 card with a dedicated management network interface with IPMI-Over-LAN and Serial-Over-LAN support.

Refer to the *Intel® Remote Management Module 2 Technical Product Specification* for more information.

5. System BIOS

The BIOS is implemented as firmware that resides in a 4 MB Intel® 28F320C3B flash ROM part. It provides hardware-specific initialization algorithms and standard PC-compatible basic input/output (I/O) services, and standard Intel® Server Board features. The Flash ROM also contains firmware for the on-board Ethernet and Video devices. These images are supplied by the device manufacturers and are not specified in this document.

The BIOS implementation is based on the Intel® Platform Innovation Framework for EFI architecture and is compliant with all Intel Platform Innovation Framework for EFI architecture specifications specified in the *Extensible Firmware Interface Reference Specification*, *Version 1.1*.

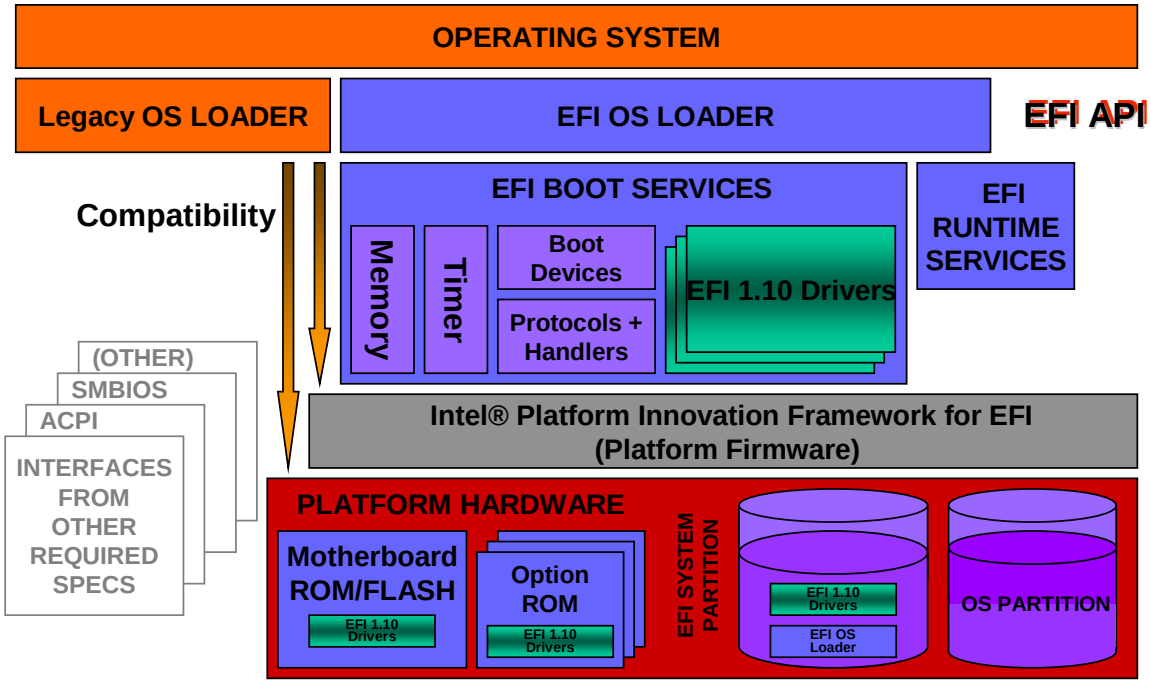


Figure 15. EFI architecture

5.1 BIOS Identification String

The BIOS Identification string is used to uniquely identify the revision of the BIOS being used on the server. The string is formatted as follows:

S5400.86B.01.00.0003.051220071200

Where:

S5400 = Board Family ID
86B = Intel OEMID
01 = Major Revision Number

00 = Minor Revision Number
0003 = Build ID
05122007 = Build date using MMDDYY format
1200 = Build time using HHMM format

The Board ID is available in the SMBIOS type 2 structure in which the phase of the BIOS can be determined by the release notes associated with the image. The board ID is also available in the BIOS setup. The BIOS ID is available in the setup and in the SMBIOS type 0 structure.

5.2 BIOS User Interface

5.2.1 Logo/Diagnostic Screen

The Logo/Diagnostic Screen may be displayed in one of the following forms:

- If Quiet Boot is enabled in the BIOS setup, a logo splash screen is displayed. By default Quiet Boot is enabled in the BIOS Setup. If the logo is displayed during POST, pressing <Esc> hides the logo and displays the diagnostic screen.
- If a logo is not present in the flash ROM, or if Quiet Boot is disabled in the system configuration, the summary and diagnostic screen is displayed.

The diagnostic screen consists of the following information:

- BIOS ID
- Platform name
- Total memory detected (Total size of all installed FBDIMMs)
- Processor information (Intel branded string, speed, and number of physical processors identified)
- Flash bank being booted from
- Types of keyboards detected if plugged in (PS/2 and/or USB)
- Types of mouse devices detected if plugged in (PS/2 and/or USB)

5.2.2 BIOS Setup Utility

The BIOS Setup utility is a text-based utility that allows the user to configure the system and view current settings and environment information for the platform devices. The Setup utility controls the platform's built-in devices, the boot manager, and error manager.

The BIOS Setup interface consists of a number of pages or screens. Each page contains information or links to other pages. The Advanced tab in the setup displays a list of general categories as links. These links lead to pages containing a specific category’s configuration.

The following sections describe the look and behavior for the platform setup.

5.2.2.1 Operation

The BIOS setup has the following features:

- **Localization:** The BIOS setup uses the Unicode standard and is capable of displaying setup forms in all languages currently included in the Unicode standard. The Intel® server board BIOS is only available in English.
- **Console Redirection:** The BIOS setup is functional via console redirection over various terminal emulation standards. This may limit some functionality for compatibility, e.g., usage of colors or some keys or key sequences or support of pointing devices.

5.2.2.2 Setup Page Layout

The setup page layout is sectioned into functional areas. Each occupies a specific area of the screen and has dedicated functionality. The following table lists and describes each functional area:

Table 27. BIOS Setup Page Layout

Functional Area	Description
Title Bar	The title bar is located at the top of the screen and displays the title of the form (page) the user is currently viewing. It may also display navigational information.
Setup Item List	The Setup Item List is a set of controllable and informational items. Each item in the list occupies the left column of the screen. A Setup Item may also open a new window with more options for that functionality on the board.
Item Specific Help Area	The Item Specific Help area is located on the right side of the screen and contains help text for the highlighted Setup Item. Help information may include the meaning and usage of the item, allowable values, effects of the options, etc.
Keyboard Command Bar	The Keyboard Command Bar is located at the bottom right of the screen and continuously displays help for keyboard special keys and navigation keys.

5.2.2.3 Entering BIOS Setup

To enter the BIOS Setup, press <F2> during boot time when the OEM or Intel logo is displayed. When Quiet Boot is disabled , the following message is displayed on the diagnostics screen:

```
Press <F2> to enter setup.
```

When the setup is entered, the Main screen is displayed. However, serious errors cause the system to the Error Manager screen instead of the Main screen.

5.2.2.4 Keyboard Commands

The bottom right portion of the Setup screen provides a list of commands that are used to navigate through the Setup utility. These commands are displayed at all times.

Each Setup menu page contains a number of features. Each feature is associated with a value field, except those used for informative purposes. Each value field contains user-selectable (configurable) parameters. Depending on the security option chosen and in effect by the

password, a menu feature's value may or may not be changed. If a value cannot be changed, its field is made inaccessible and appears grayed out.

Table 28. BIOS Setup: Keyboard Command Bar

Key	Option	Description
<Enter>	Execute Command	The <Enter> key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the <Enter> key selects the currently highlighted item, undoes the pick list, and returns the focus to the parent menu.
<Esc>	Exit	The <Esc> key provides a mechanism for backing out of any field. When the <Esc> key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the <Esc> key is pressed in any sub-menu, the parent menu is re-entered. When the <Esc> key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If "No" is selected and the <Enter> key is pressed, or if the <Esc> key is pressed, the user is returned to the screen displayed before <Esc> was pressed, without affecting any existing settings. If "Yes" is selected and the <Enter> key is pressed, setup is exited and the BIOS returns to the main System Options menu screen.
	Select Item	The up arrow is used to select the previous value in a pick list, or the previous option in a menu item's option list. The selected item must then be activated by pressing the <Enter> key.
	Select Item	The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the <Enter> key.
	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.
<Tab>	Select Field	The <Tab> key is used to move between fields. For example, <Tab> can be used to move from hours to minutes in the time item in the main menu.
-	Change Value	The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list.
+	Change Value	The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboards, but have the same effect.
<F9>	Setup Defaults	Pressing <F9> causes the following to appear: Load Optimized Defaults? Yes No If "Yes" is highlighted and <Enter> is pressed, all Setup fields are set to their default values. If "No" is highlighted and <Enter> is pressed, or if the <Esc> key is pressed, the user is returned to where they were before <F9> was pressed without affecting any existing field values

Key	Option	Description
<F10>	Save and Exit	Pressing <F10> causes the following message to appear: Save configuration and reset? Yes No If "Yes" is highlighted and <Enter> is pressed, all changes are saved and the Setup is exited. If "No" is highlighted and <Enter> is pressed, or the <Esc> key is pressed, the user is returned to where they were before <F10> was pressed without affecting any existing values.

5.2.2.5 Menu Selection Bar

The Menu Selection Bar is located at the top of the BIOS Setup Utility screen. It displays the major menu selections available to the user. By using the left and right arrow keys, the user can select the menus listed here. Some menus are hidden and become available by scrolling off the left or right of the current selections.

5.2.3 Server Platform Setup Utility Screens

The following sections describe the screens available for the configuration of a server platform. In these sections, tables are used to describe the contents of each screen. These tables follow the following guidelines:

- The Setup Item, Options, and Help Text columns in the tables document the text and values that are also displayed on the BIOS Setup screens.
- In the Options column**,** the default values are displayed in bold. These values are not displayed in bold on the BIOS Setup screen. The bold text in this document is to serve as a reference point.
- The Comments column provides additional information where it may be helpful. This information does not appear on the BIOS Setup screens.
- Information that is enclosed in brackets (< >) in the screen shots identifies text that can vary, depending on the option(s) installed. For example <Current Date> is replaced by the actual current date.
- Information that is enclosed in square brackets ([ ]) in the tables identifies areas where the user needs to type in text instead of selecting from a provided option.
- Whenever information is changed (except Date and Time), the systems requires a save and reboot to take place. Pressing <ESC> discards the changes and boots the system according to the boot order set from the last boot.

5.2.3.1 Main Screen

The Main screen is the screen that is first displayed when the BIOS Setup is entered, unless an error has occurred. If an error has occurred, the Error Manager screen is displayed instead.

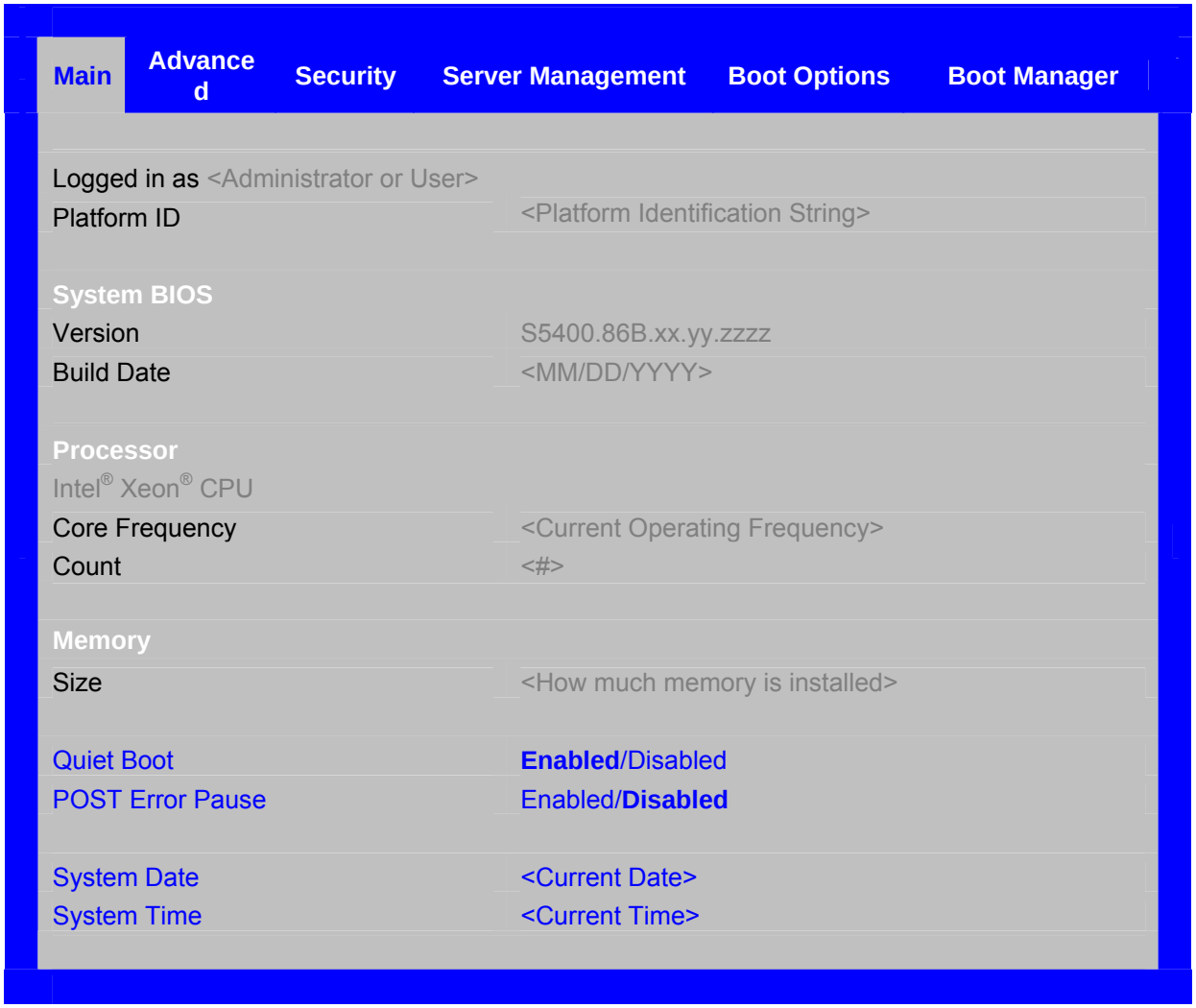


Figure 16. Setup Utility — Main Screen Display

Table 29. Setup Utility — Main Screen Fields

Setup Item	Options	Help Text	Comments
Logged in as			**Information only**. Displays password level that setup is running in: Administrator or User. With no passwords set, Administrator is the default mode.
Platform ID			**Information only**. Displays the Platform ID. (example: S5400SF)
System BIOS			
Version			**Information only**. Displays the current BIOS version. xx = major version yy = minor version zzzz = build number
Build Date			**Information only**. Displays the current BIOS build date.
Processor			
<ID string from the Processor>			**Information only**. Displays Intel processor name and the speed of the CPU. This information is retrieved from the processor.
Core Frequency			**Information only**. Displays the current speed of the boot processor in GHz or MHz.
Count			**Information only**. Number of physical processors detected.
Memory			
Size			**Information only**. Displays the total physical memory installed in the system, in MB or GB. The term physical memory indicates the total memory discovered in the form of installed FBDIMMs.
Quiet Boot	**Enabled** Disabled	[Enabled] – Display the logo screen during POST. [Disabled] – Display the diagnostic screen during POST.	
POST Error Pause	Enabled **Disabled**	[Enabled] – Go to the Error Manager for critical POST errors. [Disabled] – Attempt to boot and do not go to the Error Manager for critical POST errors.	If enabled, the POST error pause takes the system to the error manager to review the errors when major errors occur. Minor and Fatal error displays are not affected by this setting.
System Date	[Day of week MM/DD/YYYY]	System Date has configurable fields for Month, Day, and Year. Use [Enter] or [Tab] key to select the next field. Use [+] or [-] key to modify the selected field.	

Setup Item	Options	Help Text	Comments
System Time	[HH:MM:SS]	System Time has configurable fields for Hours, Minutes, and Seconds. Hours are in 24-hour format. Use [Enter] or [Tab] key to select the next field. Use [+] or [-] key to modify the selected field.	

5.2.3.2 Advanced Screen

The Advanced screen provides an access point to configure several options. On this screen, the user selects the option that is to be configured. Configurations are performed on the selected screen, and not directly on the Advanced screen.

To access this screen from the Main screen, press the right arrow until the Advanced screen is chosen.

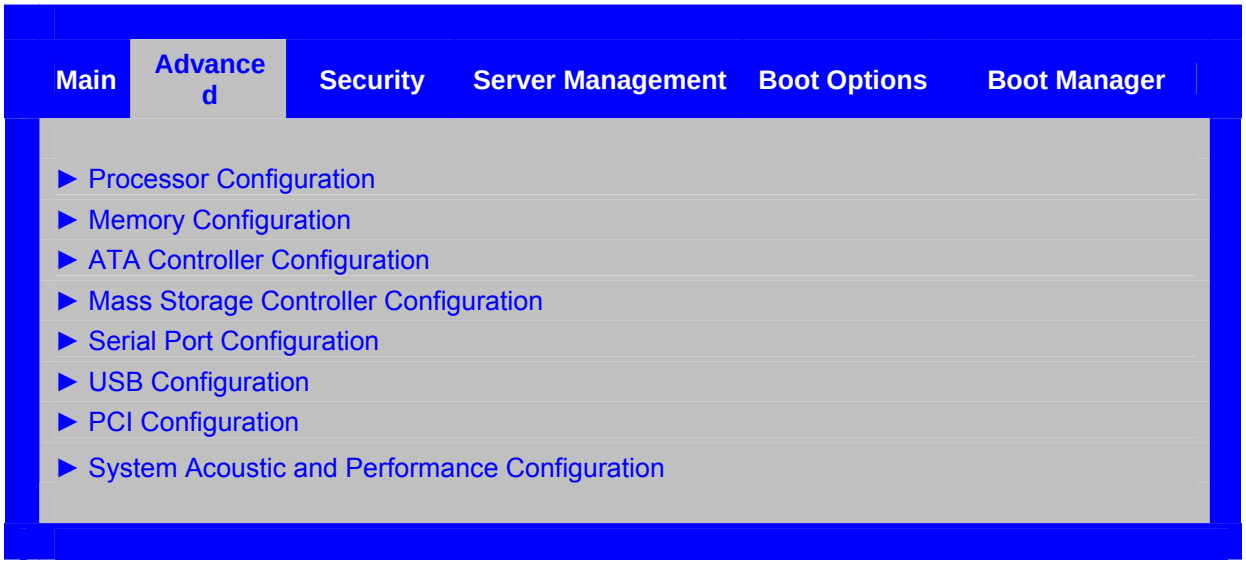


Figure 17. Setup Utility — Advanced Screen Display

Table 30. Setup Utility — Advanced Screen Display Fields

Setup Item	Options	Help Text	Comments
Processor Configuration		View/Configure processor information and settings.	
Memory Configuration		View/Configure memory information and settings.	
ATA Controller Configuration		View/Configure ATA Controller information and settings.	
Mass Storage Controller Configuration		View/Configure mass storage controller information and settings.	
Serial Port Configuration		View/Configure serial port information and settings.	
USB Configuration		View/Configure USB information and settings.	
PCI Configuration		View/Configure PCI information and settings.	
System Acoustic and Performance Configuration		View/Configure system acoustic and performance information and settings.	

5.2.3.2.1 Processor Screen

The Processor screen allows the user to view the processor core frequency, system bus frequency, and enable or disable several processor options. This screen also allows the user to view information about a specific processor.

To access this screen from the Main screen, choose Advanced > Processor.

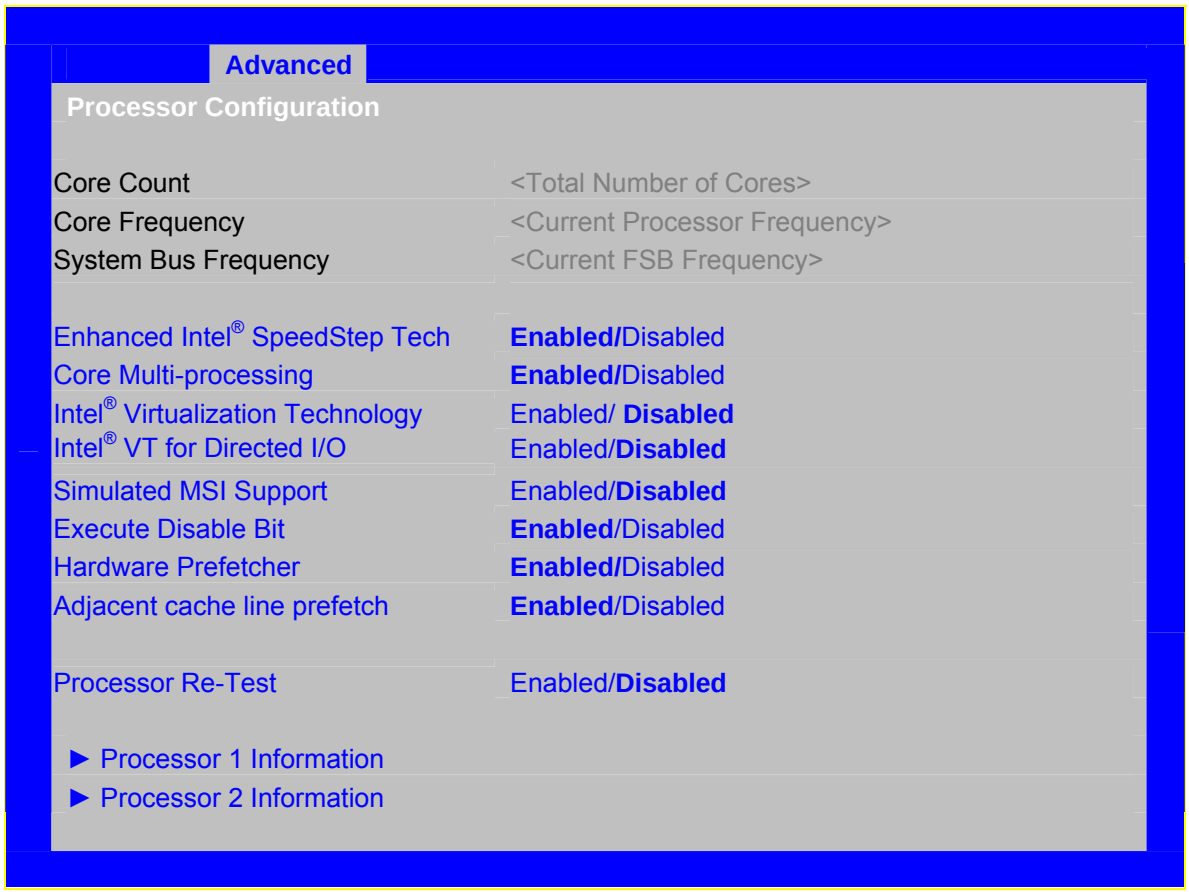


Figure 18. Setup Utility — Processor Configuration Screen Display

Table 31. Setup Utility — Processor Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Core Count			**Information only**. Total number of processor cores in the system.
Core Frequency			**Information only**. Frequency at which processors currently run.
System Bus Frequency			**Information only**. Current frequency of the processor front-side bus.
Enhanced Intel® SpeedStep Technology	**Enabled** Disabled	Enhanced Intel SpeedStep® Technology allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production. Contact your OS vendor regarding OS support of this feature.	

Setup Item	Options	Help Text	Comments
Core Multi-processing	**Enabled** Disabled	Core Multi-processing sets the state of logical processor cores in a package. [Disabled] sets only logical processor core 0 as enabled in each processor package. **Note:** If disabled, Hyper-Threading Technology will also be automatically disabled."	
Intel® Virtualization Technology	Enabled **Disabled**	Intel® Virtualization Technology allows a platform to run multiple operating systems and applications in independent partitions. **Note**: A change to this option requires the system to be powered off and then back on before the setting takes effect.	
Intel® Virtualization Technology for Directed I/O	Enabled **Disabled**	Enable/Disable the Intel® Virtualization Technology for Directed I/O. Report the I/O device assignment to VMM through DMAR ACPI Tables.	When Intel® VT is disabled, this option is hidden.
Simulated MSI Support	Enabled **Disabled**	Enable or Disable simulation of Message Signaled Interrupt (MSI) support. This feature can be enabled in the case where there is no OS support for Message Signaled Interrupts.	
Execute Disable Bit	**Enabled** Disabled	Execute Disable Bit can help prevent certain classes of malicious buffer overflow attacks. Contact your OS vendor regarding OS support of this feature.	
Hardware Prefetcher	**Enabled** Disabled	Hardware Prefetcher is a speculative prefetch unit within the processor(s). **Note:** Modifying this setting may affect system performance.	
Adjacent Cache Line Prefetch	**Enabled** Disabled	[Enabled] - Cache lines are fetched in pairs (even line + odd line). [Disabled] - Only the current cache line required is fetched. **Note:** Modifying this setting may affect system performance.	
Processor Retest	Enabled **Disabled**	Activate and retest all processors during next boot only. **Note:** This option automatically resets to [Disabled] on the next boot, after all processors are retested.	
Processor 1 Information		View Processor 1 information	Select to view information about processor 1. This takes the user to a different screen.
Processor 2 Information		View Processor 2 information	Select to view information about processor 2. This takes the user to a different screen.

5.2.3.2.1.1 Processor # Information Screen

The Processor # Information screen provides a place for the user to view information about a specific processor.

To access this screen from the Main screen, select Advanced > Processor > Processor # Information, where # is the processor number you want to see.

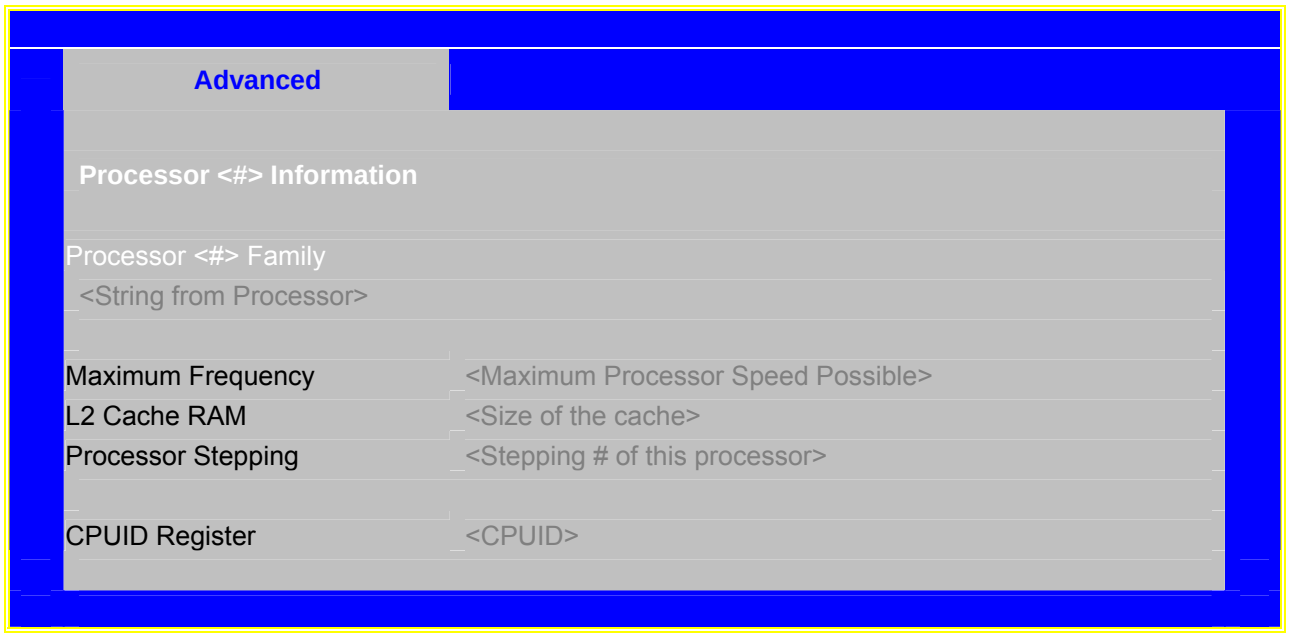


Figure 19. Setup Utility — Specific Processor Information Screen Display

Table 32. Setup Utility — Specific Processor Information Screen Fields

Setup Item	Options	Help Text	Comments
Processor <#> Family			Information only. Identifies the family or generation of the processor.
Maximum Frequency			Information only. Maximum frequency the processor core supports.
L2 Cache RAM			Information only. Size of the processor L2 cache.
Processor Stepping			Information only. Stepping number of the processor.
CPUID Register			Information only. CPUID register value identifies details about the processor family, model, and stepping.

5.2.3.2.2 Memory Screen

The Memory screen allows the user to view details about the system memory FBDIMMs that are installed. This screen also allows the user to open the Configure Memory RAS and Performance screen.

To access this screen from the Main screen, choose Advanced > Memory.

Note: The following screenshot is for reference purposes only. The actual BIOS setup screen accurately reflects the number of DIMM slots found on the server board.

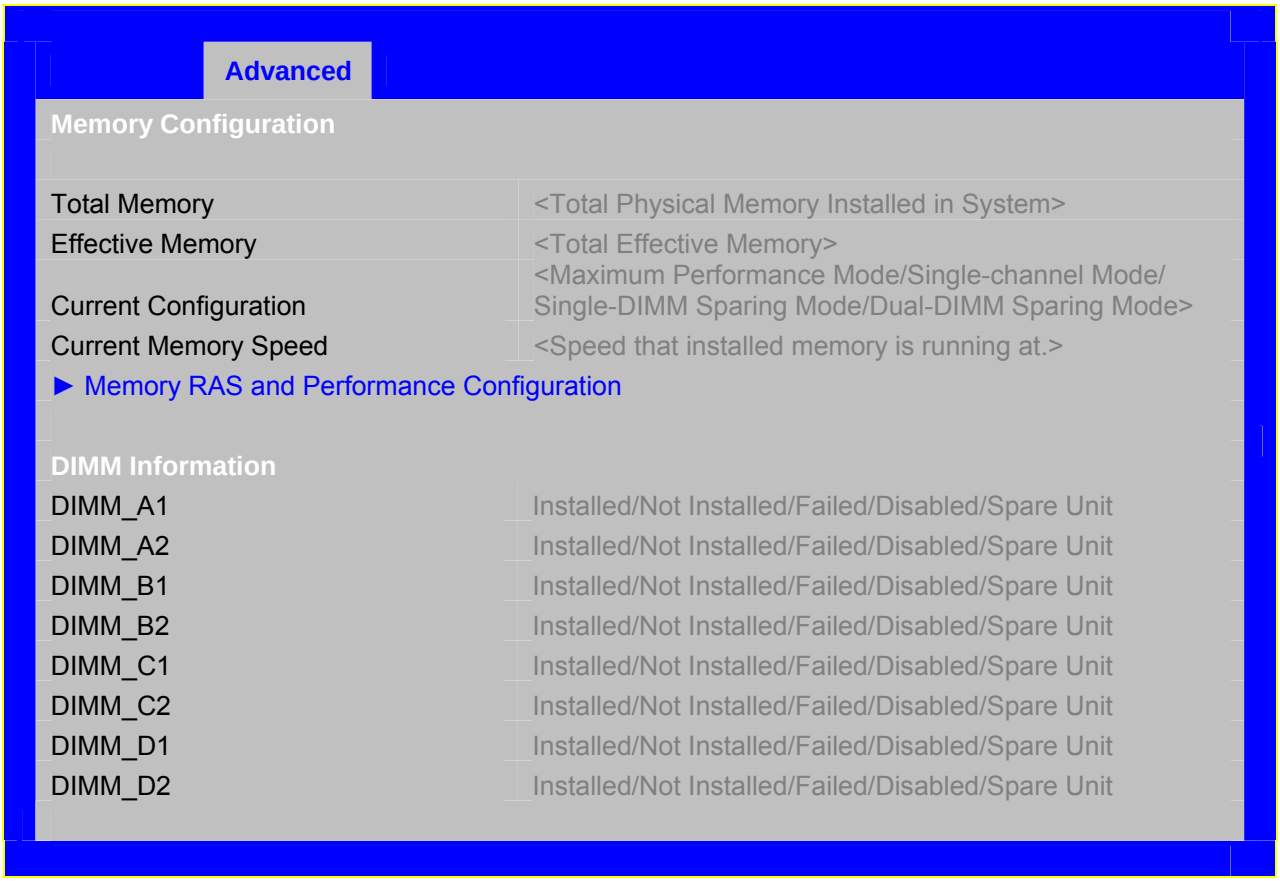


Figure 20. Setup Utility — Memory Configuration Screen Display

Table 33. Setup Utility — Memory Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Total Memory			**Information only.** The amount of memory available in the system in the form of installed FBDIMMs, in units of MB or GB.
Effective Memory			**Information only.** The amount of memory effective in MB or GB. The Effective Memory is the difference between Total Physical Memory and the sum of all memory reserved for internal usage, RAS redundancy and SMRAM. This difference includes the sum of all FBDIMMs that failed Memory BIST during POST, or were disabled by the BIOS during memory discovery phase in order to optimize memory configuration.
Current Configuration			**Information only**. Displays one of the following: **Maximum Performance Mode**: System memory is configured for optimal performance and efficiency and no RAS is enabled. **Single-Channel Mode**: System memory is functioning in a special, reduced efficiency mode.
Current Memory Speed			**Information only**. Displays speed the memory is running at.
Memory RAS and Performance Configuration		Configure memory RAS (Reliability, Availability, and Serviceability) and view current memory performance information and settings.	Select to configure the memory RAS and performance. This takes the user to a different screen.
DIMM_#			Displays the state of each DIMM socket present on the board. Each DIMM socket field reflects one of the following possible states: **Installed:** There is a FBDIMM installed in this slot. **Not Installed:** There is no FBDIMM installed in this slot. **Disabled:** The FBDIMM installed in this slot has been disabled by the BIOS in order to optimize memory configuration. **Failed:** The FBDIMM installed in this slot is faulty/malfunctioning. **Spare Unit:** The FBDIMM is functioning as a spare unit for memory RAS purposes.

5.2.3.2.2.1 Memory RAS and Performance Configuration Screen

The Configure Memory RAS and Performance screen provides fields to customize several memory configuration options, such as whether to use Memory Sparing.

To access this screen from the Main screen, choose Advanced > Memory > Configure Memory RAS and Performance.

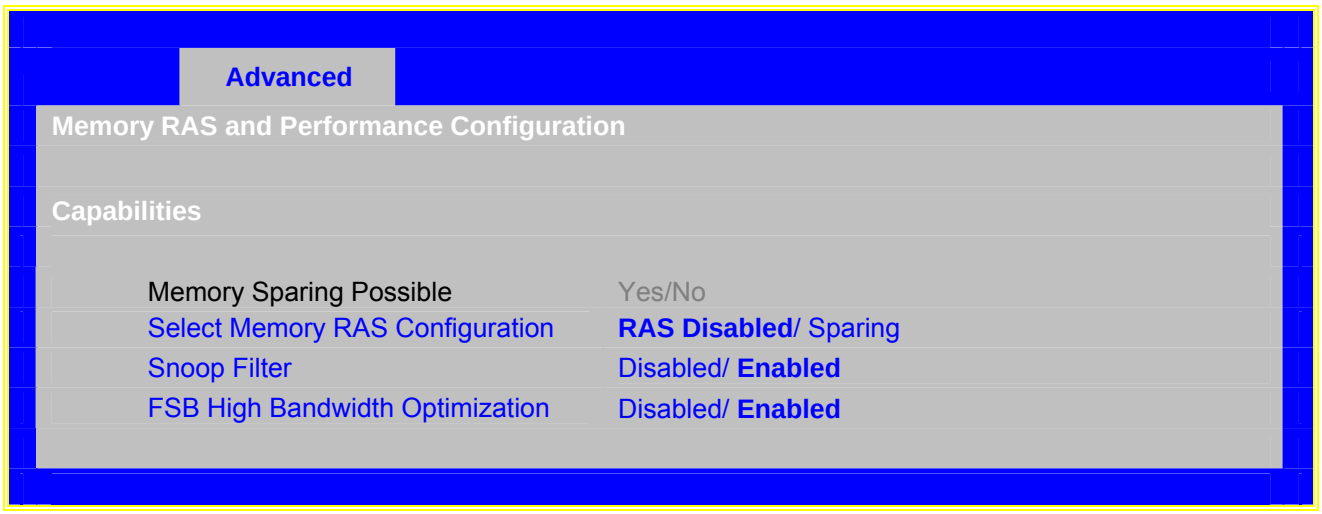


Figure 21. Setup Utility — Configure RAS and Performance Screen Display

Table 34. Setup Utility — Configure RAS and Performance Screen Fields

Setup Item	Options	Help Text	Comments
Memory Sparing Possible	Yes/No		**Information only**
Select Memory RAS Configuration	**RAS Disabled**/ Sparing	Available modes depend on the current memory population. [RAS Disabled] - Optimizes system performance. [Sparing] - Improves reliability by reserving memory for use as a replacement in the event of DIMM failure.	Provides options for configuring the Memory RAS. The BIOS dynamically configures this menu to display only those RAS modes that can be supported with the current layout and positioning of the FBDIMMs on the board. If no RAS mode is possible for the current FBDIMM configuration/layout, this setup item is not provided. **RAS Disabled**: This is the default in the normal mode of operation. In this mode, Memory RAS is not supported. **Sparing**: This option is available and displayed only when the FBDIMM population can support memory sparing.

Setup Item	Options	Help Text	Comments
Snoop Filter	**Enabled** Disabled	The Snoop Filter component monitors and controls the data transactions between memory and the processor(s).	
FSB High Bandwidth Optimization	**Enabled** Disabled	[Enabled] – Optimize Front-Side Bus for higher bandwidth when 1333 MHz FSB or faster processor(s) are installed. **Note**: Some applications benefit from this option. [Enabled].	Information only. This option is set to enabled always.

5.2.3.2.3 ATA Controller Screen

The ATA Controller screen provides fields to configure PATA and SATA hard disk drives. It also provides information on the hard disk drives that are installed.

To access this screen from the Main screen, choose Advanced > ATA Controller.

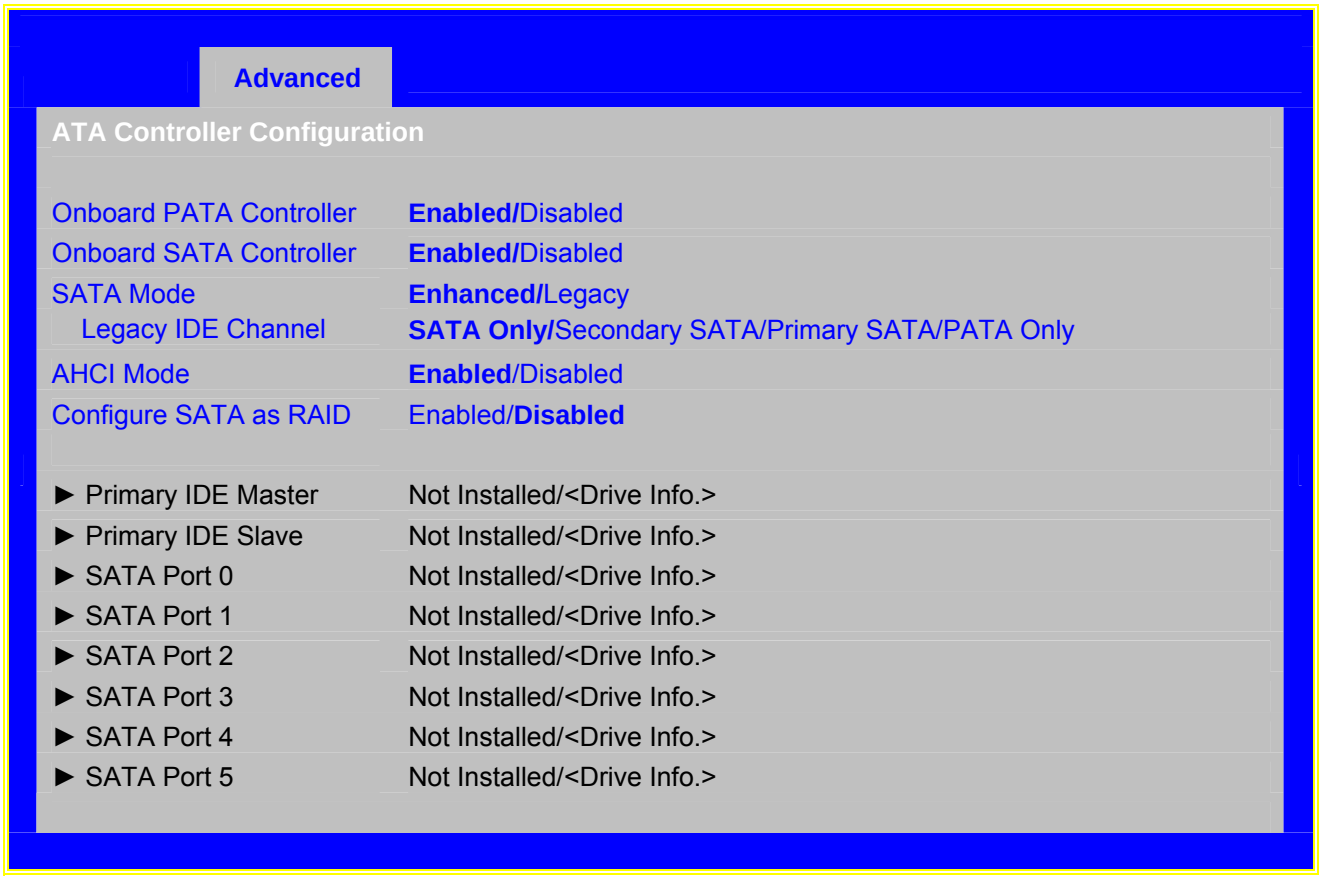


Figure 22. Setup Utility — ATA Controller Configuration Screen Display

Table 35. Setup Utility — ATA Controller Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Onboard PATA Controller	**Enabled** Disabled	Onboard Parallel ATA (PATA) controller.	
Onboard SATA Controller	**Enabled** Disabled	Onboard Serial ATA (SATA) controller.	When enabled, the SATA controller can be configured in IDE, RAID, or AHCI Mode. RAID and AHCI modes are mutually exclusive.
SATA Mode	**Enhanced** Legacy	[Enhanced] - Configures all SATA ports as individual ports. This is also known as the native mode. [Legacy] - Configures SATA ports to be primary and/or secondary channels. This is also known as the compatibility mode.	In the Legacy Mode, the BIOS can enumerate only four drives. It provides four options to choose a mix of SATA and PATA drives (see Legacy IDE Channel option below). In the Enhanced Mode, the BIOS is not limited to legacy PATA four-drive limitations, and can enumerate the two PATA drives and four SATA drives (totaling six drives) regardless of the AHCI mode, and can list/boot to the remaining two SATA drives as well with AHCI support. AHCI and RAID Modes are supported only when SATA Mode is selected as “Enhanced”.
Legacy IDE Channel	**SATA Only** Secondary SATA Primary SATA PATA Only	[SATA Only] - Master/slave for primary are SATA port 0/2. Master/slave for secondary are port 1/3. [Secondary SATA] - Master/slave for primary are PATA. Master/slave for secondary are SATA port 1/3. [Primary SATA] - Master/slave for primary are SATA port 0/2. Master/slave for secondary they are PATA. [PATA Only] - Master/slave for primary are PATA. SATA ports are disabled.	This item is displayed only when Legacy is chosen for the SATA Mode.

Setup Item	Options	Help Text	Comments
AHCI Mode	Enabled **Disabled**	Advanced Host Controller Interface (AHCI) option ROM will enumerate all AHCI devices connected to the SATA ports. Contact your OS vendor regarding OS support of this feature.	This item is unavailable if the SATA mode is "Legacy" or if the RAID Mode is selected. When AHCI is enabled: ▪ The identification and configuration is left to the AHCI Option ROM. Only devices supported by the AHCI Option ROM are displayed in the setup (SATA HDD and SATA CD-ROM). Other devices are available in the OS after their drivers are loaded. ▪ SATA 4 and SATA 5 appear in the HDD information listing.
Configure SATA as RAID	Enabled **Disabled**	SATA controller will be in RAID mode and the Intel® RAID for Serial ATA option ROM will execute.	This item is unavailable when the AHCI mode is enabled. This mode can be selected only when the SATA controller is in Enhanced Mode. When this mode is enabled, no SATA drive information is displayed.
Primary IDE Master	<Not Installed/Drive information>		**Information only**
Primary IDE Slave	< Not Installed/Drive information>		**Information only**
SATA Port 0	< Not Installed/Drive information>		**Information only**. Unavailable when the RAID Mode is enabled.
SATA Port 1	< Not Installed/Drive information>		**Information only**. This field is unavailable when the RAID Mode is enabled.
SATA Port 2	< Not Installed/Drive information>		**Information only**. This field is unavailable when the RAID Mode is enabled.
SATA Port 3	< Not Installed/Drive information>		I**nformation only**. This field is unavailable when the RAID Mode is enabled.
SATA Port 4	< Not Installed/Drive information>		**Information only**; This field is only available when the AHCI Mode is enabled.
SATA Port 5	< Not Installed/Drive information>		**Information only**; This field is only available when the AHCI Mode is enabled.

5.2.3.2.4 Mass Storage Controller Screen

The Mass Storage screen provides fields to configure when a SAS controller is present on the server board, midplane or backplane of an Intel® system.

To access this screen from the Main menu, choose Advanced > Mass Storage.

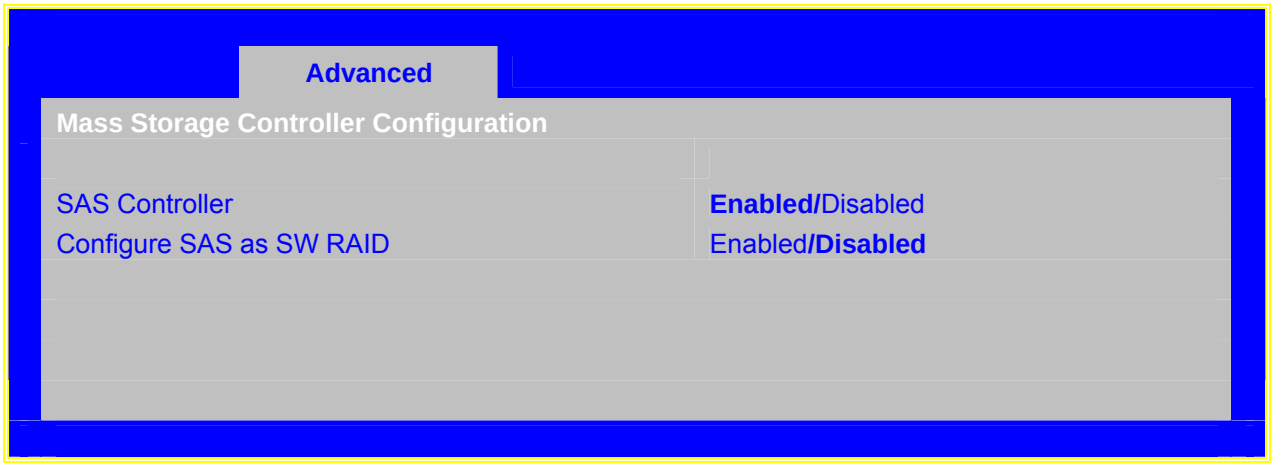


Figure 23. Setup Utility — Mass Storage Controller Configuration Screen Display

Table 36. Setup Utility — Mass Storage Controller Configuration Screen Fields

Setup Item	Options	Help Text	Comments
SAS Controller	Enabled Disabled	Enable or Disable the on-board Serial Attached SCSI (SAS) Controller.	
Configure SAS as SW RAID	Enabled Disabled	SAS ports are configured for Intel® Embedded Server RAID Technology.	This item is unavailable if the device is disabled.

5.2.3.2.5 Serial Ports Screen

The Serial Ports screen provides fields to configure the Serial A [COM 1] and Serial B [COM2] ports.

To access this screen from the Main screen, choose Advanced > Serial Port.

Figure 24. Setup Utility — Serial Port Configuration Screen Display

Table 37. Setup Utility — Serial Ports Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Serial A Enable	**Enabled** Disabled	Enable or Disable Serial port A.	
Address	**3F8h** 2F8h 3E8h 2E8h	Select Serial port A base I/O address.	
IRQ	3 **4**	Select Serial port A base interrupt request (IRQ) line.	
Serial B Enable	**Enabled** Disabled	Enable or Disable Serial port B.	
Address	3F8h **2F8h** 3E8h 2E8h	Select Serial port B base I/O address.	
IRQ	**3** 4	Select Serial port B base interrupt request (IRQ) line.	

5.2.3.2.6 USB Configuration Screen

The USB Configuration screen provides fields to configure the USB controller options.

To access this screen from the Main screen, choose Advanced > USB Configuration.

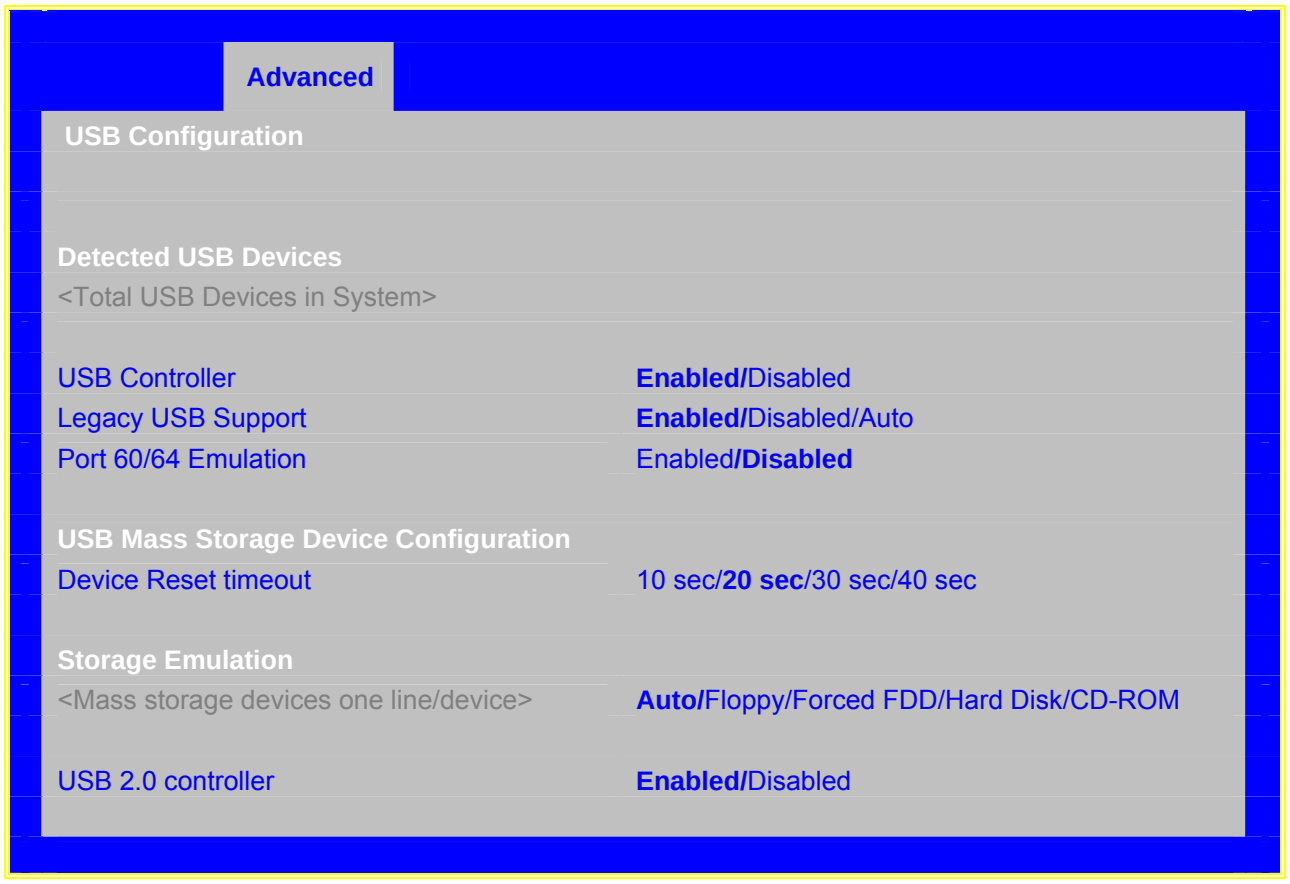


Figure 25. Setup Utility — USB Controller Configuration Screen Display

Table 38. Setup Utility — USB Controller Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Detected USB Devices			Information only: shows number of USB devices in system
USB Controller	Enabled Disabled	[Enabled] - All on-board USB controllers are turned on and made accessible by the OS. [Disabled] - All on-board USB controllers are turned off and made inaccessible by the OS.	
Legacy USB Support	Enabled Disabled Auto	PS/2 emulation for USB keyboard and USB mouse devices. [Auto] - Legacy USB support is enabled if a USB device is attached.	
Port 60/64 Emulation	Enabled Disabled	I/O port 60h/64h emulation support. Note: This may be needed for legacy USB keyboard support when using an OS that is USB unaware.	
Device Reset timeout	10 sec 20 sec 30 sec 40 sec	USB Mass storage device Start Unit command timeout.	
Storage Emulation			Header for next line.
One line for each mass storage device in system	Auto Floppy Forced FDD Hard Disk CD-ROM	[Auto] - USB devices less than 530 MB is emulated as a floppy. [Forced FDD] - HDD formatted drive is emulated as FDD (e.g., ZIP drive).	This setup screen can show a maximum of eight devices on this screen. If more than eight devices are installed in the system, the 'USB Devices Enabled' shows the correct count, but only the first eight devices can be displayed here.
USB 2.0 controller	Enabled Disabled	On-board USB ports is enabled to support USB 2.0 mode. Contact your OS vendor regarding OS support of this feature.	

5.2.3.2.7 PCI Screen

The PCI Screen provides fields to configure PCI add-in cards, the on-board NIC controllers, and video options.

To access this screen from the Main screen, choose Advanced > PCI.

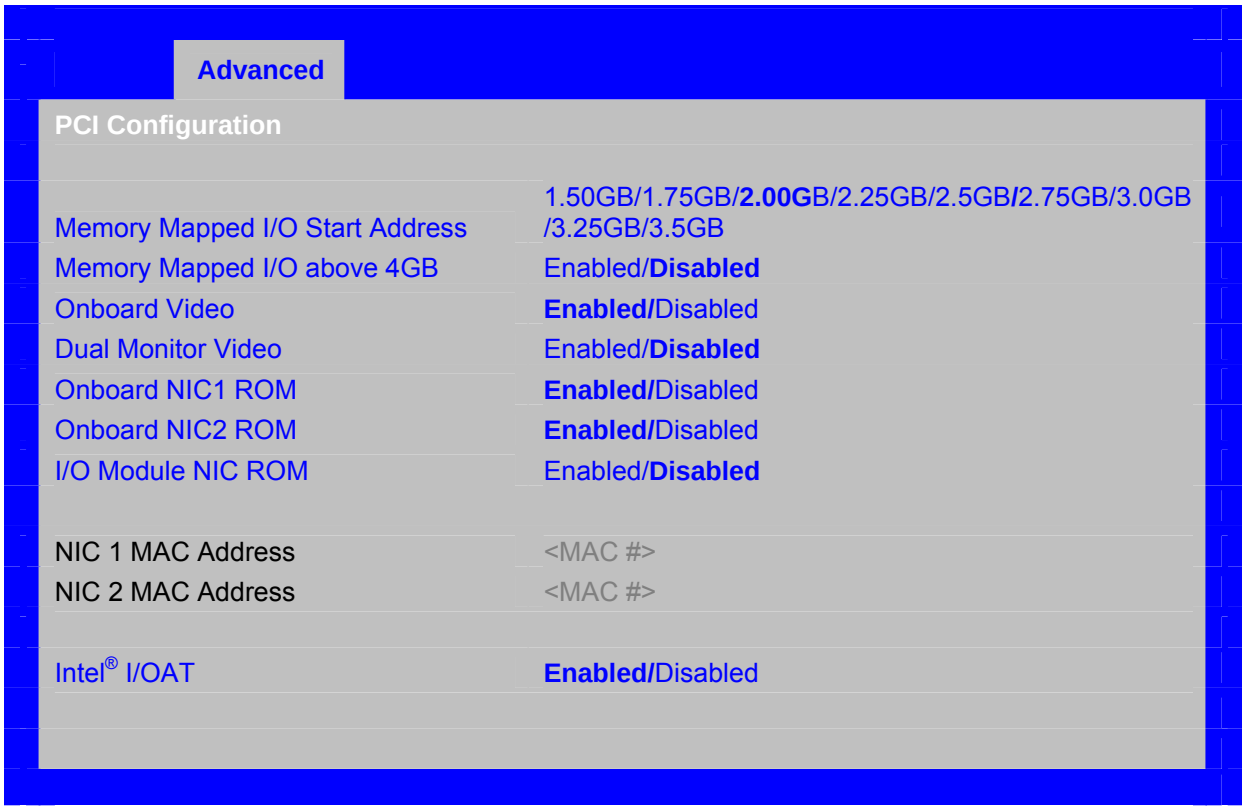


Figure 26. Setup Utility — PCI Configuration Screen Display

Table 39. Setup Utility — PCI Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Memory Mapped I/O Start Address	1.5GB 1.75GB **2.00GB** 2.25GB 2.5GB 2.75GB 3.00GB 3.25GB 3.50GB	Select the start of the reserved memory region for PCI memory mapped I/O space that ends at 4 GB. **Warning:** Depending on the system configuration, this option may impact the amount of system memory detected by an OS without Physical Address Extension (PAE) support.	For all PAE (Physical Address Extension) aware Operating Systems, 2.5 GB should be selected. The system remaps memory and the OS detects all memory installed in the system. If the installed OS does not support PAE, the maximum memory size detected is linked to the setup option selected. For example, if 2.5 GB is selected, only 2.5 GB is detected by the OS.
Memory Mapped I/O above 4GB	Enabled **Disabled**	Enable or disable memory mapped I/O of 64-bit PCI devices to 4 GB or greater address space.	

Setup Item	Options	Help Text	Comments
Onboard Video	**Enabled** Disabled	On-board video controller. **Warning:** The system video is completely disabled if this option is disabled and an add-in video adapter is not installed.	When disabled, the system requires an add-in video card in order for video to be seen.
Dual Monitor Video	Enabled **Disabled**	Both the on-board video controller and an add-in video adapter are enabled for system video. The on-board video controller is the primary video device.	
Onboard NIC ROM	**Enabled** Disabled	Load the embedded option ROM for the on-board network controllers. **Warning:** If [Disabled] is selected, NIC1 and NIC2 can not be used to boot or wake the system.	
I/O Module NIC ROM	Enabled **Disabled**	Load the embedded option ROM for the on-board network controller on the I/O module.	Option only displays when a optional Dual GigE I/O Module is Installed
NIC 1 MAC Address	No entry allowed		**Information only**. 12 hex digits of the MAC address.
NIC 2 MAC Address	No entry allowed		**Information only**. 12 hex digits of the MAC address.
Intel® I/OAT	Enabled **Disabled**	Intel® I/O Acceleration Technology 2 (I/OAT2) accelerates TCP/IP processing for on-board NICs, delivers data-movement efficiencies across the entire server platform, and minimizes system overhead.	

5.2.3.2.8 System Acoustic and Performance Configuration

The System Acoustic and Performance Configuration screen provides fields to configure the thermal characteristics of the system.

To access this screen from the Main screen, choose Advanced > System Acoustic and Performance Configuration.

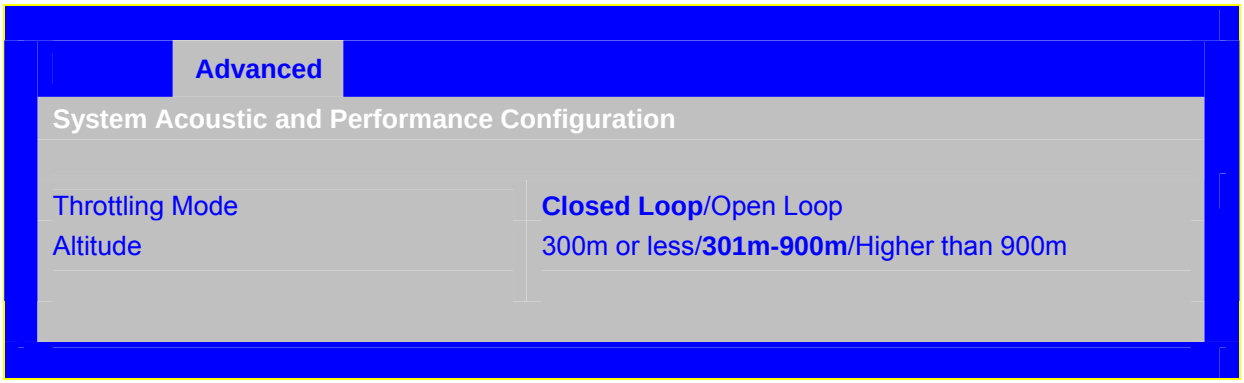


Figure 27. Setup Utility — System Acoustic and Performance Configuration

Table 40. Setup Utility — System Acoustic and Performance Configuration Screeen Fields

Setup Item	Options	Help Text	Comments
Throttling Mode	Closed Loop Open Loop	Open Loop does not rely on a thermal sensor on the board and sets up a static level which equates in a fixed bandwidth. Closed Loop will allow the system to achieve higher performance by monitoring system temps and adjusting bandwidth.	When CLTT fails, Throttling Mode defaults to OLTT. Profile is Performance for OLTT.
Altitude	300m or less 301m-900m Higher than 900m	[300m or less] (980ft or less) Optimal performance setting near sea level. [301m - 900m] (980ft - 2950ft) Optimal performance setting at moderate elevation. [Higher than 900m] (Higher than 2950ft) Optimal performance setting at high elevation.	Available only if CLTT failed and running in OLTT throttling mode.

5.2.3.3 Security Screen

The Security screen provides fields to enable and set the user and administrative password and to lock out the front panel buttons so they cannot be used.

To access this screen from the Main screen, choose Security.

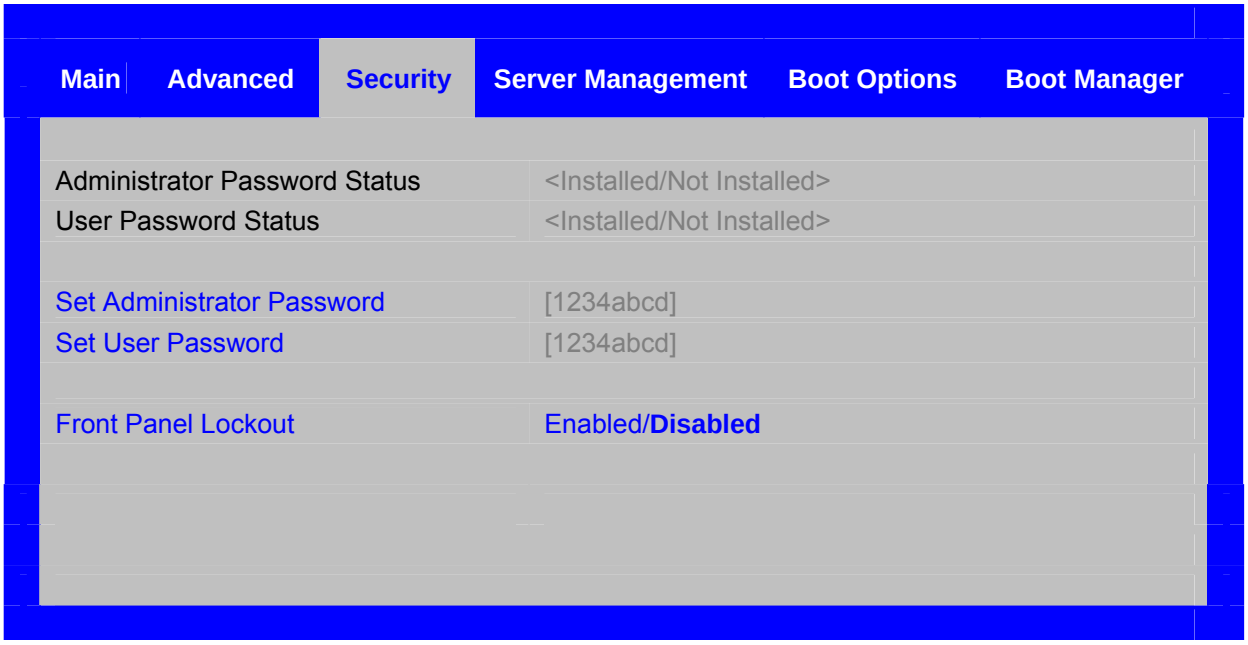


Figure 28. Setup Utility — Security Configuration Screen Display

Table 41. Setup Utility — Security Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Administrator Password Status	<Installed Not Installed>		Information only. Indicates the status of the administrator password.
User Password Status	<Installed Not Installed>		Information only. Indicates the status of the user password.
Set Administrator Password	[123abcd]	Administrator password is used to control change access in the BIOS Setup utility. Only alphanumeric characters can be used. Maximum length is 7 characters. It is case sensitive. Note: Administrator password must be set in order to use the user account.	This option is only to control access to setup. Administrator has full access to all setup items. Clearing the Administrator password also clears the user password.
Set User Password	[123abcd]	User password is used to control entry access to the BIOS Setup utility. Only alphanumeric characters can be used. Maximum length is 7 characters. It is case sensitive. Note: Removing the administrator password also automatically removes the user password.	Available only if the Administrator Password is installed. This option only protects the setup. The user password only has limited access to setup items.
Front Panel Lockout	Enabled Disabled	Locks the power button and reset button on the system's front panel. If [Enabled] is selected, power and reset must be controlled via a system management interface.	

5.2.3.4 Server Management Screen

The Server Management screen provides fields to configure several server management features. It also provides an access point to the screens for configuring console redirection and displaying system information.

To access this screen from the Main screen, choose Server Management.

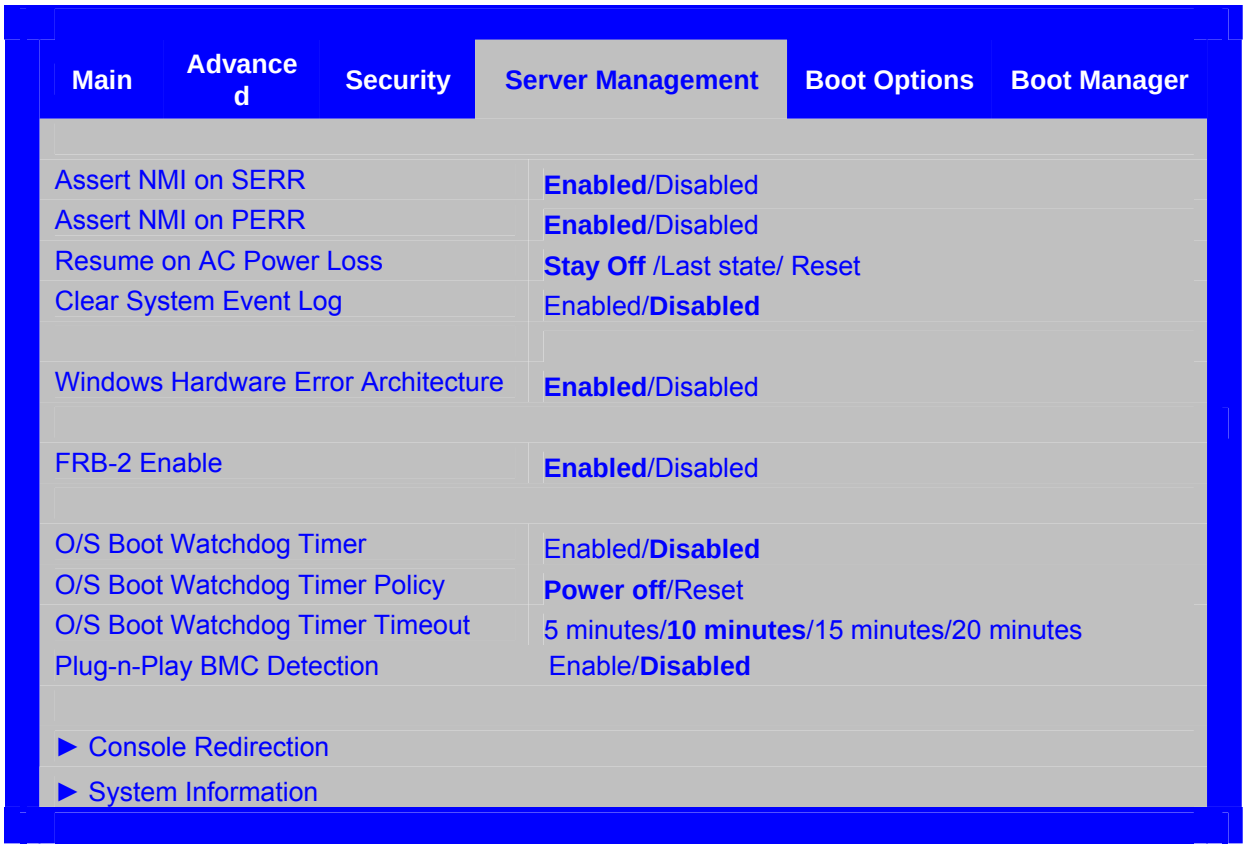


Figure 29. Setup Utility — Server Management Configuration Screen Display

Table 42. Setup Utility — Server Management Configuration Screen Fields

Setup Item	Options	Help Text	Comments
Assert NMI on SERR	**Enabled** Disabled	On SERR, generate an NMI and log an error. **Note:** Enabled must be selected for the Assert NMI on PERR setup option to be visible.	
Assert NMI on PERR	**Enabled** Disabled	On PERR, generate an NMI and log an error. **Note:** This option is only active if the Assert NMI on SERR option is Enabled.	
Resume on AC Power Loss	**Stay Off** Last state Reset	System action to take on AC power loss recovery. [Stay Off] - System stays off. [Last State] - System returns to the same state before the AC power loss. [Reset] - System powers on.	
Clear System Event Log	Enabled **Disabled**	Clears the System Event Log. All current entries are lost. **Note**: This option is reset to [Disabled] after a reboot.	
Windows Hardware Error Architecture	**Enabled** Disabled	During HW errors, in addition to the BIOS SMI Error Handlers, OS Error Handlers are signaled.	

Setup Item	Options	Help Text	Comments
FRB-2 Enable	**Enabled** Disabled	Fault Resilient Boot (FRB). The BIOS programs the Integrated BMC watchdog timer for approximately 6 minutes. If the BIOS does not complete POST before the timer expires, the Integrated BMC resets the system.	
O/S Boot Watchdog Timer	Enabled **Disabled**	The BIOS programs the watchdog timer with the timeout value selected. If the OS does not complete booting before the timer expires, the Integrated BMC resets the system and an error is logged. Requires OS support or Intel® System Management Software.	
O/S Boot Watchdog Timer Policy	**Power Off** Reset	If the OS watchdog timer is enabled, this is the system action taken if the watchdog timer expires. [Reset] - System performs a reset. [Power Off] - System powers off.	
O/S Boot Watchdog Timer Timeout	5 minutes **10 minutes** 15 minutes 20 minutes	If the OS watchdog timer is enabled, this is the timeout value BIOS uses to configure the watchdog timer.	
Plug-n-Play BMC Detection	Enabled **Disabled**	If enabled, Integrated BMC is detectable by operating systems that support plug and play loading of an IPMI driver. Do not enable if your OS does not support this driver.	
Console Redirection		View/Configure console redirection information and settings.	Takes user to Console Redirection Screen.
System Information		View system information.	Takes user to System Information Screen.

5.2.3.4.1 Console Redirection Screen

The Console Redirection screen provides a way to enable or disable console redirection and to configure the connection options for this feature.

To access this screen from the Main screen, choose Server Management > Console Redirection.

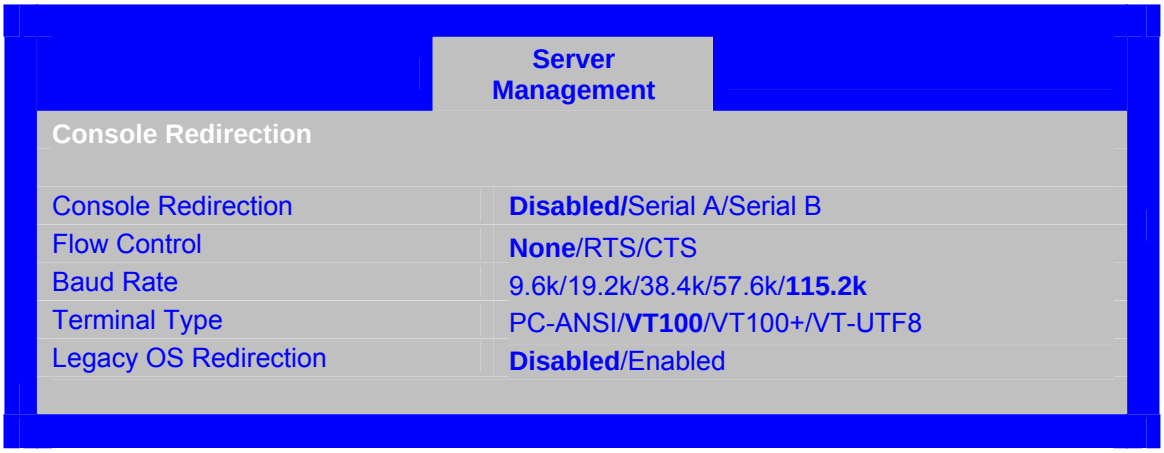


Figure 30. Setup Utility — Console Redirection Screen Display

Table 43. Setup Utility — Console Redirection Configuration Fields

Setup Item	Options	Help Text	Comments
Console Redirection	Disabled Serial A Serial B	Console redirection allows a serial port to be used for server management tasks. [Disabled] - No console redirection. [Serial Port A] - Configure serial port A for console redirection. [Serial Port B] - Configure serial port B for console redirection. Enabling this option disables display of the Quiet Boot logo screen during POST.	
Flow Control	None RTS/CTS	Flow control is the handshake protocol. Setting must match the remote terminal application. [None] - Configure for no flow control. [RTS/CTS] - Configure for hardware flow control.	
Baud Rate	9600 19.2K 38.4K 57.6K 115.2K	Serial port transmission speed. Setting must match the remote terminal application.	
Terminal Type	PC-ANSI VT100 VT100+ VT-UTF8	Character formatting used for console redirection. Setting must match the remote terminal application.	
Legacy OS Redirection	Disabled Enabled	This option enables legacy OS redirection (i.e., DOS) on the serial port. If it is enabled, the associated serial port is hidden from the legacy OS.	

5.2.3.5 Server Management System Information Screen

The Server Management System Information screen allows the user to view part numbers, serial numbers, and firmware revisions.

To access this screen from the Main screen, choose Server Management > System Information.

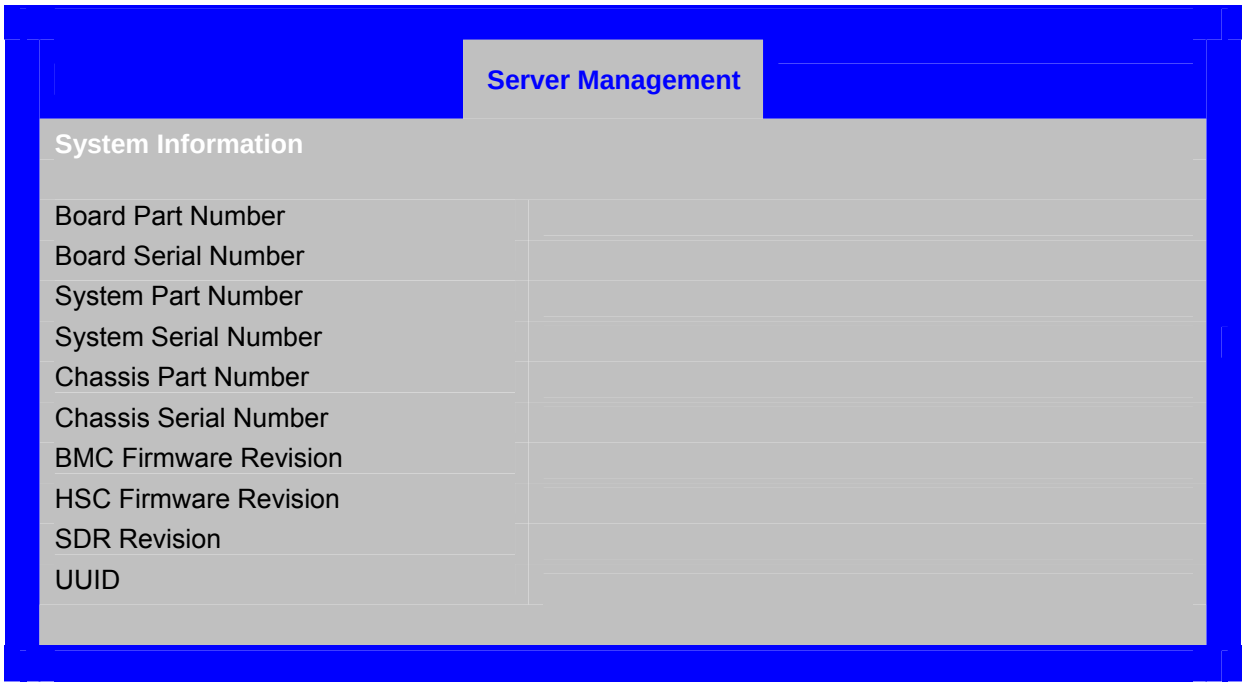


Figure 31. Setup Utility — Server Management System Information Screen Display

Table 44. Setup Utility — Server Management System Information Fields

Setup Item	Options	Help Text	Comments
Board Part Number			Information Only
Board Serial Number			Information Only
System Part Number			Information Only
System Serial Number			Information Only
Chassis Part Number			Information Only
Chassis Serial Number			Information Only
BMC Firmware Revision			Information Only
HSC Firmware Revision			Information Only
SDR Revision			Information Only
UUID			Information Only

5.2.3.6 Boot Options Screen

The Boot Options screen displays any bootable media encountered during POST, and allows the user to configure desired boot device.

To access this screen from the Main screen, choose Boot Options.

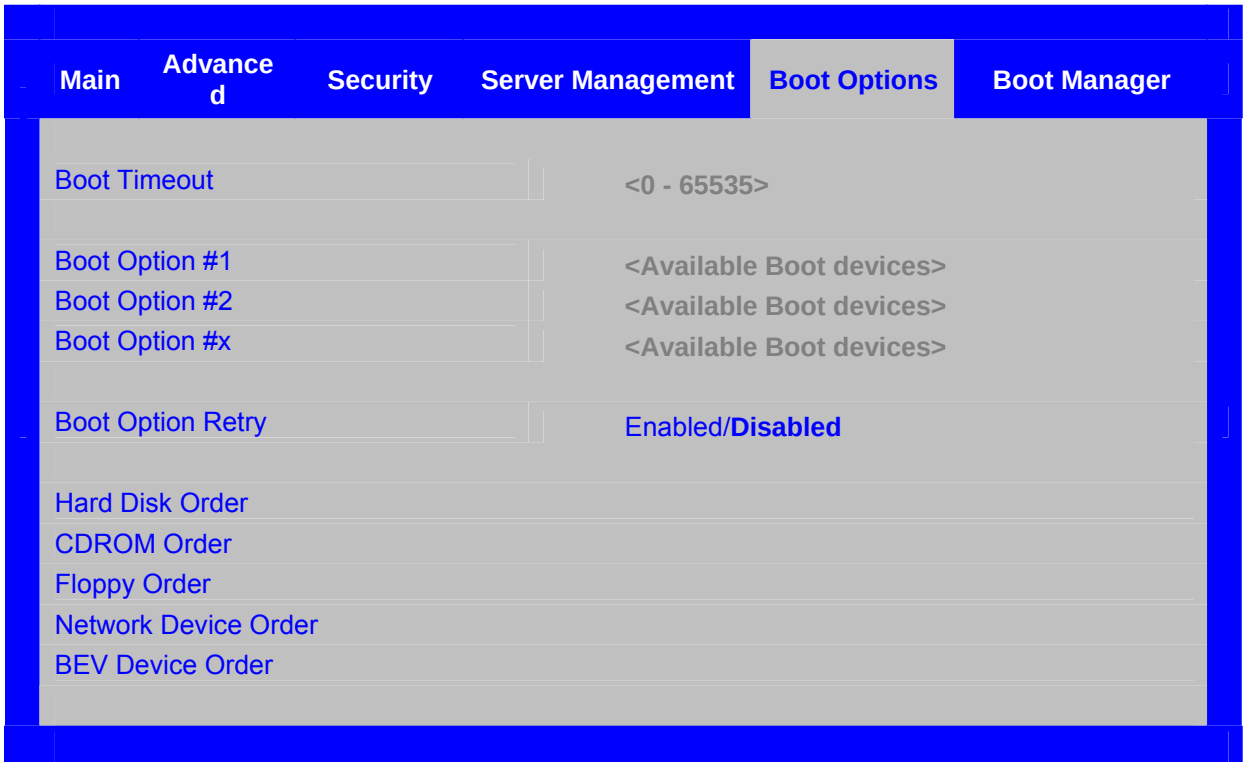


Figure 32. Setup Utility — Boot Options Screen Display

Table 45. Setup Utility — Boot Options Screen Fields

Setup Item	Options	Help Text	Comments
Boot Timeout	**0** - 65535	The number of seconds BIOS pauses at the end of POST to allow the user to press the [F2] key for entering the BIOS Setup utility. Valid values are 0-65535. Zero is the default. A value of 65535 causes the system to go to the Boot Manager menu and wait for user input for every system boot.	After entering the desired timeout, press enter to register that timeout value to the system. These settings are in seconds.
Boot Option #x	Available boot devices.	Set system boot order by selecting the boot option for this position.	**Note:** The EFI Shell boot option can only be set as the first or last boot option in the list.
Boot Option Retry	Enabled **Disabled**	This continually retries non-EFI based boot options without waiting for user input.	
Hard Disk Order		Set hard disk boot order by selecting the boot option for this position.	Appears when more than one hard disk drive is available in the system.
CDROM Order		Set CD-ROM boot order by selecting the boot option for this position.	Appears when more than one CD-ROM drive is available in the system.

Setup Item	Options	Help Text	Comments
Floppy Order		Set floppy disk boot order by selecting the boot option for this position.	Appears when more than one floppy drive is available in the system.
Network Device Order		Set network device boot order by selecting the boot option for this position. Add-in or on-board network devices with a PXE option ROM are two examples of network boot devices.	Appears when more than one of these devices is available in the system.
BEV Device Order		Set the Bootstrap Entry Vector (BEV) device boot order by selecting the boot option for this position. BEV devices require their own proprietary method to load an OS using a bootable option ROM. BEV devices are typically found on remote program load devices.	Appears when more than one of these devices is available in the system.

5.2.3.6.1 Hard Disk Order Screen

The Hard Disk Order screen allows the user to control the hard disks.

To access this screen from the Main screen, choose Boot Options > Hard Disk Order.

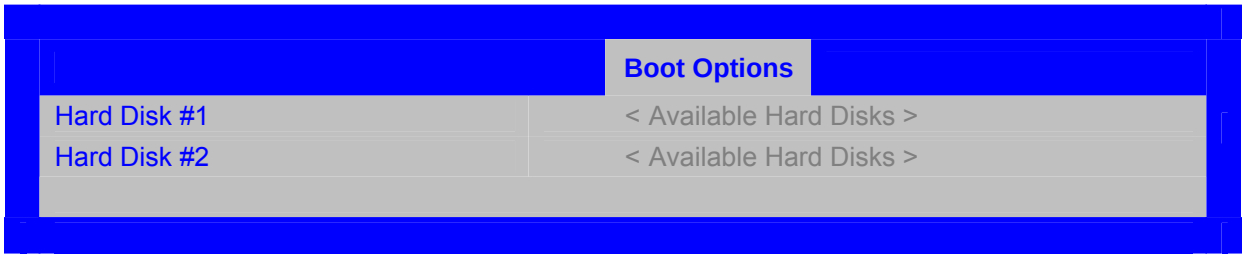


Figure 33. Setup Utility — Hard Disk Order Screen Display

Table 46. Setup Utility — Hard Disk Order Fields

Setup Item	Options	Help Text	Comments
Hard Disk #1	Available hard disks	Set hard disk boot order by selecting the boot option for this position.	
Hard Disk #2	Available hard disks	Set hard disk boot order by selecting the boot option for this position.	

5.2.3.6.2 CDROM Order Screen

The CDROM Order screen allows the user to control the CD-ROM devices.

To access this screen from the Main screen, choose Boot Options > CDROM Order.

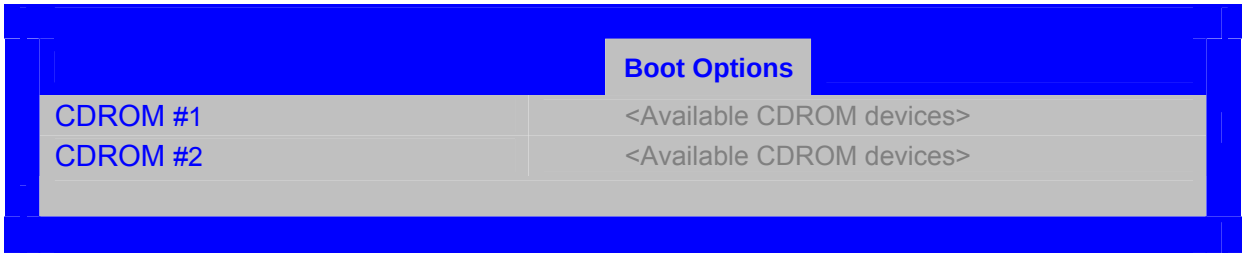


Figure 34. Setup Utility — CDROM Order Screen Display

Table 47. Setup Utility — CDROM Order Fields

Setup Item	Options	Help Text	Comments
CDROM #1	Available CDROM devices	Set CDROM boot order by selecting the boot option for this position.	
CDROM #2	Available CDROM devices	Set CDROM boot order by selecting the boot option for this position.	

5.2.3.6.3 Floppy Order Screen

The Floppy Order screen allows the user to control the floppy drives.

To access this screen from the Main screen, choose Boot Options > Floppy Order.

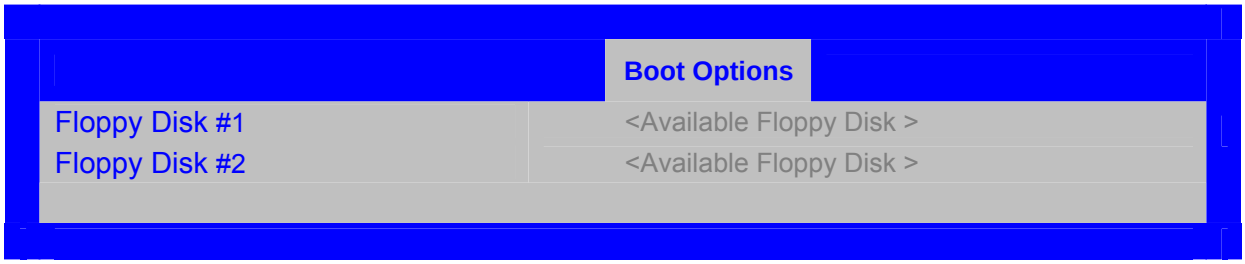


Figure 35. Setup Utility — Floppy Order Screen Display

Table 48. Setup Utility — Floppy Order Fields

Setup Item	Options	Help Text	Comments
Floppy Disk #1	Available floppy disk	Set floppy disk boot order by selecting the boot option for this position.	
Floppy Disk #2	Available floppy disk	Set floppy disk boot order by selecting the boot option for this position.	

5.2.3.6.4 Network Device Order Screen

The Network Device Order screen allows the user to control the network bootable devices.

To access this screen from the Main screen, choose Boot Options > Network Device Order.

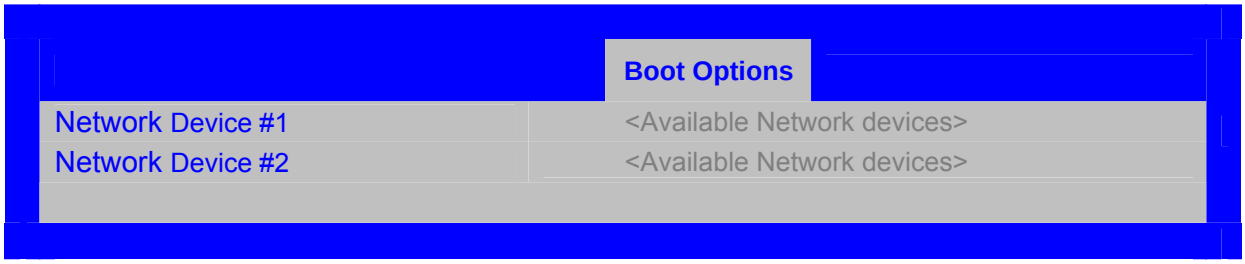


Figure 36. Setup Utility — Network Device Order Screen Display

Table 49. Setup Utility — Network Device Order Fields

Setup Item	Options	Help Text	Comments
Network Device #1	Available network devices	Set network device boot order by selecting the boot option for this position. Add-in or onboard network devices with a PXE option ROM are two examples of network boot devices.	
Network Device #2	Available network devices	Set network device boot order by selecting the boot option for this position. Add-in or onboard network devices with a PXE option ROM are two examples of network boot devices.	

5.2.3.6.5 BEV Device Order Screen

The BEV Device Order screen allows the user to control the BEV bootable devices.

To access this screen from the Main screen, choose Boot Options > BEV Device Order.

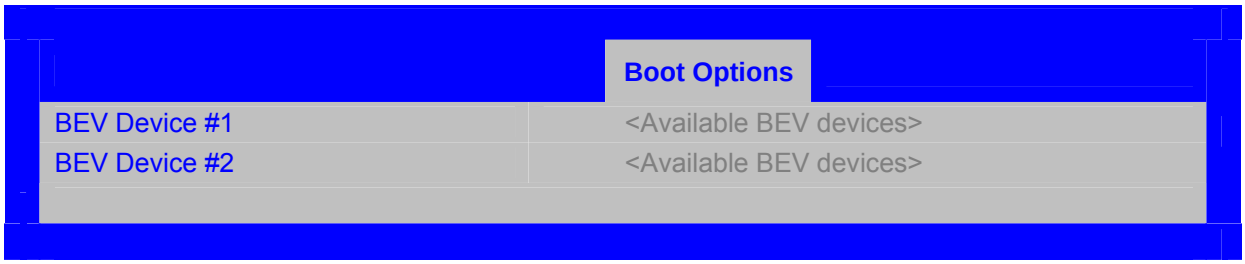


Figure 37. Setup Utility — BEV Device Order Screen Display

Table 50. Setup Utility — BEV Device Order Fields

Setup Item	Options	Help Text	Comments
BEV Device #1	Available BEV devices	Set the Bootstrap Entry Vector (BEV) device boot order by selecting the boot option for this position. BEV devices require their own proprietary method to load an OS using a bootable option ROM. BEV devices are typically found on remote program load devices.	
BEV Device #2	Available BEV devices	Set the Bootstrap Entry Vector (BEV) device boot order by selecting the boot option for this position. BEV devices require their own proprietary method to load an OS using a bootable option ROM. BEV devices are typically found on remote program load devices.	

5.2.3.7 Boot Manager Screen

The Boot Manager screen displays a list of devices available for booting, and allows the user to select a boot device for immediately booting the system.

To access this screen from the Main screen, choose Boot Manager.

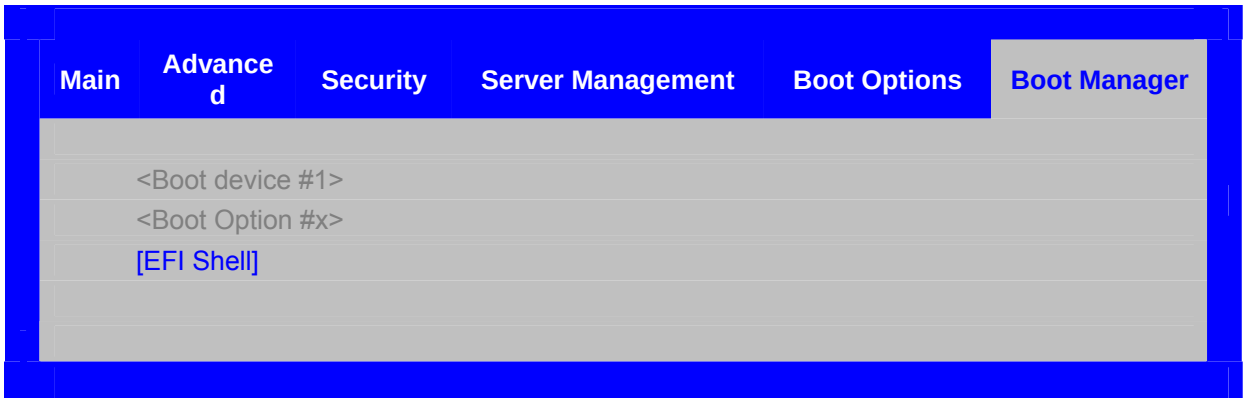


Figure 38. Setup Utility — Boot Manager Screen Display

Table 51. Setup Utility — Boot Manager Screen Fields

Setup Item	Options	Help Text	Comments
Launch EFI Shell		Select this option to boot now. Note: This list is not the system boot option order. Use the Boot Options menu to view and configure the system boot option order.	
Boot Device #x		Select this option to boot now. Note: This list is not the system boot option order. Use the Boot Options menu to view and configure the system boot option order.	

5.2.3.8 Error Manager Screen

The Error Manager screen displays any errors encountered during POST.

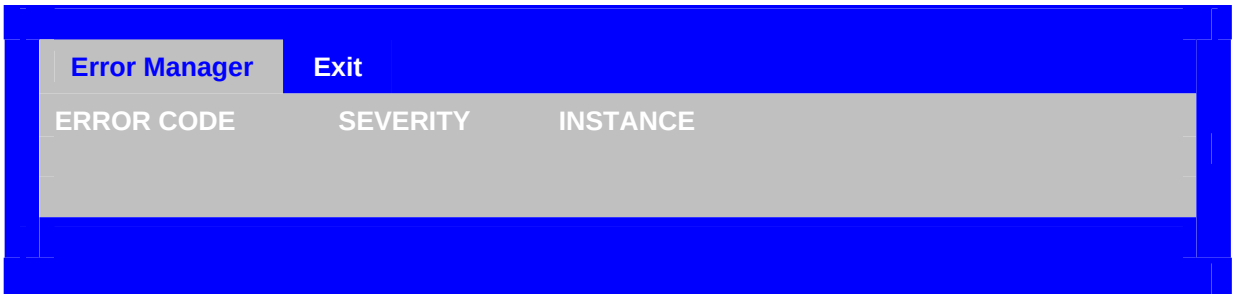


Figure 39. Setup Utility — Error Manager Screen Display

Table 52. Setup Utility — Error Manager Screen Fields

Setup Item	Options	Help Text	Comments
Displays System Errors			Information only. Displays errors that occurred during this POST.

5.2.3.9 Exit Screen

The Exit screen allows the user to choose whether to save or discard the configuration changes made on the other screens. It also provides a method to restore the server to the factory defaults or to save or restore a set of user-defined default values. If Load Default Values is selected, the default settings, noted in bold in the tables in this chapter, are applied. If Load User Default Values is selected, the system is restored to the default values that the user saved earlier, instead of being restored to the factory defaults.

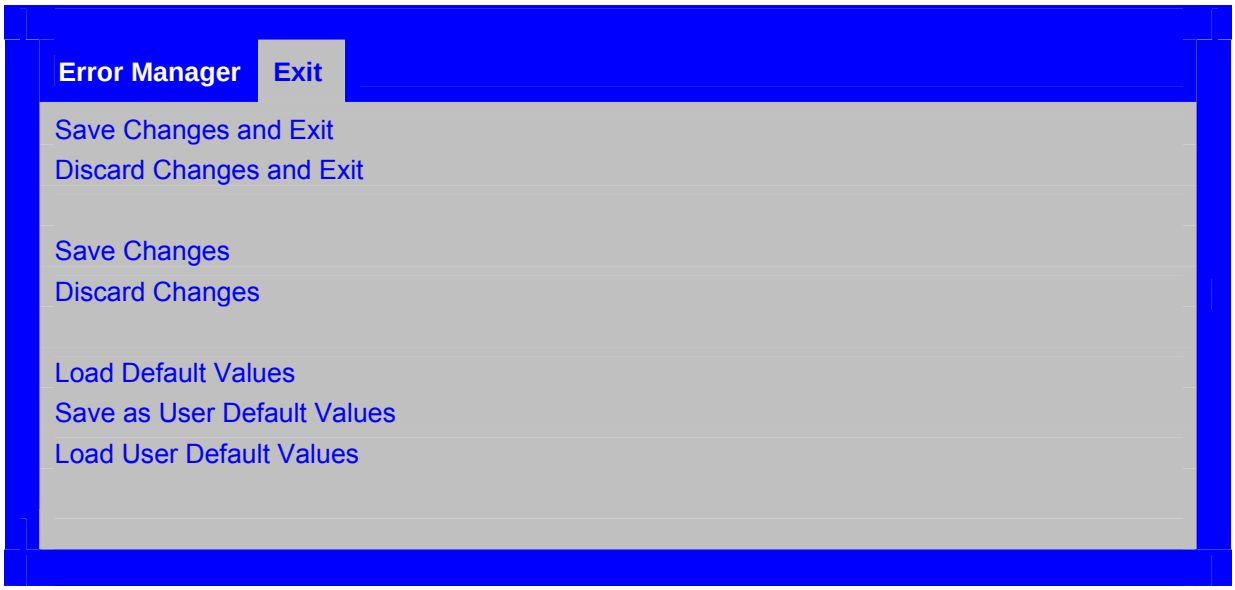


Figure 40. Setup Utility — Exit Screen Display

Table 53. Setup Utility — Exit Screen Fields

Setup Item	Help Text	Comments
Save Changes and Exit	Exit BIOS Setup utility after saving changes. The system reboots if required. The [F10] key can also be used.	User is prompted for confirmation only if any of the setup fields were modified.
Discard Changes and Exit	Exit BIOS Setup utility without saving changes. The [Esc] key can also be used.	User is prompted for confirmation only if any of the setup fields were modified.
Save Changes	Save changes without exiting the BIOS Setup utility. Note: Saved changes may require a system reboot before taking effect.	User is prompted for confirmation only if any of the setup fields were modified.
Discard Changes	Discard changes made since the last save changes operation was performed.	User is prompted for confirmation only if any of the setup fields were modified.
Load Default Values	Load factory default values for all BIOS Setup utility options. The [F9] key can also be used.	User is prompted for confirmation.
Save as User Default Values	Save current BIOS Setup utility values as custom user default values. If needed, the user default values can be restored via the Load User Default Values option below. Note: Clearing CMOS or NVRAM causes the user default values to be reset to the factory default values.	User is prompted for confirmation.
Load User Default Values	Load user default values.	User is prompted for confirmation.

5.3 Loading BIOS Defaults

Different mechanisms exist for resetting the system configuration to the default values. When a request to reset the system configuration is detected, the BIOS loads the default system configuration values during the next POST. The request to reset the system to the defaults can be generated in the following ways:

- By pressing <F9> from within the BIOS Setup utility.
- By moving the clear system configuration jumper. See section 7.1.1 for complete CMOS Clear instructions.

5.4 Rolling BIOS

The Rolling BIOS feature provides the ability to update the BIOS in a fault tolerant way. If the updated (new) BIOS is found to be non-functional for any reason, the system can still be booted by rolling back to the previous, healthy BIOS.

All Intel® Server Boards and Systems that use the Intel® 5400 Chipset have 4 MB of flash space for the system BIOS. This flash is divided into 2 banks of 2 MB each. One of the banks is called upper bank and the other is called lower bank. The BIOS can reside in either or both of these banks. The BIOS area from which the system boots at any point in time is called the “Primary BIOS Partition”. The other BIOS area (also called the backup area) is called the “Secondary BIOS Partition”. All BIOS updates are made only to the “Secondary BIOS Partition”.

Note: The primary and secondary BIOS partitions are logical partitions on a 4 MB system flash. They can reside on either of the two physical banks.

The BIOS relies on specialized hardware and additional flash space for a Rolling BIOS and One Boot Flash Update. The BIOS Select Jumper is used to direct the behavior of the BIOS once the online update is performed. The BIOS Select jumper has two modes.

- 2-3 Normal Operation (Default)
- 1-2 Recovery Mode

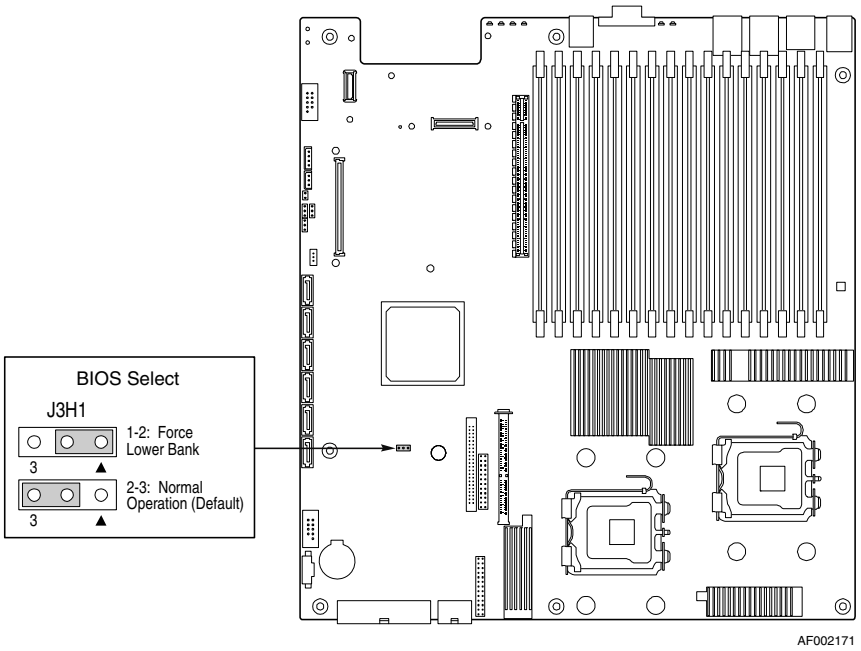


Figure 41. BIOS Select Jumper Position

BIOS updates can be made with the BIOS Select jumper in either of the two positions. The behavior of the system in either of these modes is described below.

5.4.1 BIOS Select Jumper in Normal Mode (Jumper pins 2-3 connected)

In the normal mode, the new BIOS image is updated onto the secondary partition and is validated. If the validation is successful, the BIOS uses specialized hardware to notify the system to boot from the new BIOS, and resets the system. The new BIOS begins to boot. If the boot is successful, the BIOS update is complete. If the new BIOS fails to boot successfully, a timer is started and the system rolls back to the previous, healthy BIOS image.

1. Boot the system with the jumper covering pins 2 and 3.
2. Update the BIOS using iFlash or the Intel® One Flash Update (Intel® OFU) utility.
3. Reset the system.
4. The current BIOS validates and then boots from the new BIOS.
5. If the new BIOS fails, roll back occurs and the system boots with the old BIOS.

5.4.2 BIOS Select Jumper in Recovery Mode (Jumper pins 1-2 connected)

To update the primary BIOS image, move the recovery jumper to force the BIOS to boot from the secondary partition of the flash.

1. Boot the system with the jumper covering pins 1 and 2.
2. Update the BIOS using iFlash or the Intel® OFU utility.
3. Reset the system.

4. The system boots from the old BIOS.
5. If the new BIOS needs to be used, power off the system and move the jumper to cover pins 2 and 3, then power on the system.
6. If the new BIOS is healthy, the system boots with the new BIOS.

   or

   If the BIOS is corrupted or incompatible, the system does **not** roll back to the healthy BIOS. The user should power down the system, move the jumper to cover pins 1 and 2, power up the server to boot to the older BIOS.

5.4.3 BIOS Recovery

Rolling BIOS is the only form of BIOS Recovery for Intel server boards and systems that use the Intel® 5400 Chipset. As discussed in the previous section, any BIOS update that fails to boot causes the system to automatically roll back to the older, known-good BIOS.

Under some circumstances, a user may choose to force a roll back to the older BIOS. A manual roll back can be forced by moving the BIOS Select jumper on the server board from the normal position (covering pins 2 and 3) to the recovery position (covering pins 1 and 2). If a usable BIOS exists on the secondary partition, the system boots. If the system fails to boot, the user must manually move the jumper back to the normal position to boot the system from the primary partition. When the jumper is covering pins 1 and 2, the BIOS does not automatically perform a roll back.

BIOS updates are supported when the BIOS Select jumper is covering either pins 1 and 2, or pins 2 and 3. However, normal BIOS updates should be done with the BIOS Select jumper in the normal position (covering pins 2 and 3). The validation and switch to the BIOS on the secondary partition occurs only if the BIOS Select jumper is in the normal position. When the BIOS Select jumper is covering pins 1 and 2, the BIOS update occurs but the server does not boot to the new BIOS until the user moves the BIOS Select jumper to the normal position.

BIOS updates with the BIOS Select jumper in the recovery position may be required under the following scenarios:

- **Initial Conditions:** BIOS2 (the new BIOS) is in the active partition and BIOS1 (the old BIOS) is in the secondary partition.
- **Trigger Conditions:**
  - The user successfully updates the BIOS from BIOS1 to BIOS2. The BIOS2 image is valid and boots successfully, so the primary BIOS makes the switch from BIOS1 to BIOS2. The user then learns that BIOS2 does not provide the required functionality and wants to return the server to BIOS1.
  - The user changes the system configuration and BIOS2 stops working in some manner. The user wants to try booting from BIOS1 to see if the results are different.
  - The user downloads and flashes in BIOS2. BIOS2 passes the basic checks and boots, but is not a functional BIOS.
  - A power failure occurs during the update from BIOS1 to BIOS2. BIOS2 in the secondary partition passes the basic checks and the server boots from it. However,

the BIOS does not have working code.

Under each of these cases, the user finds that the BIOS is no longer functional. The user should first try to clear the CMOS to return to a default configuration. If clearing the CMOS does not correct the issues, the user can perform a recovery by moving the BIOS Select jumper to cover pins 1 and 2 to boot to the previous version of the BIOS.

5.4.3.1 Recovery Flow

The steps to perform a BIOS recovery are as follow:

1. Move the BIOS Select jumper to cover pins 1 and 2. This causes the other BIOS image to run. If the other BIOS is good, the system boots to the operating system.
2. Update the BIOS.
3. Power down the server.
4. Remove power sources to the server (unplug it)
5. Move the BIOS Select jumper back to the normal position.
6. Plug in the server.
7. Power the server on.

Accesses to the reset vector are directed to the new BIOS. If it is good, the system boots and the recovery is complete.

5.5 OEM Binary

A firmware volume is reserved for OEMs. The OEM firmware volume is used to contain the OEM logo and is updated independently of other firmware volumes. The OEM firmware volume hosts a firmware file system. The size of the OEM firmware volume is 192 KB.

5.5.1 Splash Logo

The OEM firmware volume can include the OEM splash logo. If an OEM logo is located in the firmware volume, it is used in place of the standard Intel logo. The logo file can be identified based on the file name.

The logo file must follow the standard framework format for graphical images. The size must not exceed 800 x 512 pixels. The number of colors cannot exceed 256, although the actual number of colors may be much fewer due to image size constraints.

6. Connector/Header Locations and Pin-outs

6.1 Board Connector Information

The following section provides detailed information regarding all connectors, headers and jumpers on the server board. The following table lists all connector types available on the board and the corresponding reference designators printed on the silkscreen.

Table 54. Board Connector Matrix

Connector	Quantity	On-board Silk Screen Reference Designators	Connector Type	Pin Count
Power supply	3	J3K5 J3K4 J1K1	CPU Power Main Power P/S Aux	8 24 5
CPU	2	J8H1, J5J1	CPU Sockets	771
Main Memory	16	J4E1,J5E1,J6E1,J6E2,J7E2,J7E3,J8E2,J8E3, J5E2, J5E3, J6E3, J7E1, J7E4, J8E1, J9E1, J9E2	DIMM Sockets	240
Riser Slot	1	J4B1	Card Edge	164
Bridge Board Connector	1	J4G1	Card Edge	120
Intel® RMM2	1	J1C2	Mezzanine	120
Intel® RMM2 NIC	1	J1B2	Mezzanine	30
Intel® I/O Expansion Module	1	J3B1	Mezzanine	50
SATA RAID Key	1	J1D5	Key Holder	3
IDE (I/O + Power)	1	J3G2	Shrouded Header	44
SSI System Fans #1, #2, #3, & #4	4	J3K2, J3K3, J1B3, J1C1	Header	4
SSI CPU Fans	2	J4K1, J9K1	Header	4
Intel® Server System Fans	1	J3k1	Shrouded Header	26
Battery	1	BT1J1	Battery Holder	3
Keyboard/Mouse	1	J9A1	PS/2, stacked	12
Rear USB	2	J5A1	External	4
Serial Port A	1	J1B1	Header	9
Serial Port B	1	J9A2	External, RJ-45	10
Video connector	1	J6A1	External, D-Sub	15
LAN connector 10/100/1000	2	JA8A1, JA8A2	External LAN connector with built-in magnetic	14
SSI Control Panel	1	J3H2	Header	24
Internal USB	1	J1J1	Header	10
Intrusion detect	1	J1D1	Header	2
Serial ATA	6	J1H1,J1G2,J1G1,J1F2,J1F1,J1E2	Header	7
LCP/AUX IPMB	1	J1C3	Header	4
IPMB	1	J1C4	Header	3

Connector	Quantity	On-board Silk Screen Reference Designators	Connector Type	Pin Count
System Recovery Setting Jumpers	3	J1D2, J1D3, J1D4	Jumper	3

6.2 Power Connectors

The main power supply connection is obtained using an SSI-compliant 2x12 pin connector (J3K4). In addition, there are two additional power related connectors:

- One SSI-compliant 2x4 pin power connector (J3K5) providing support for additional 12 V.
- One SSI-compliant 1x5 pin connector (J1K1) providing I^2C monitoring of the power supply.

The following tables define the connector pin-outs:

Table 55. Power Connector Pin-out (J3K4)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3 VDC	Orange	13	+3.3 VDC	Orange
2	+3.3 VDC	Orange	14	-12 VDC	Blue
3	GND	Black	15	GND	Black
4	+5 VDC	Red	16	PS_ON#	Green
5	GND	Black	17	GND	Black
6	+5 VDC	Red	18	GND	Black
7	GND	Black	19	GND	Black
8	PWR_OK	Gray	20	RSVD_(-5V)	White
9	5 VSB	Purple	21	+5 VDC	Red
10	+12 VDC	Yellow	22	+5 VDC	Red
11	+12 VDC	Yellow	23	+5 VDC	Red
12	+3.3 VDC	Orange	24	GND	Black

Table 56. 12 V Power Connector Pin-out (J3K5)

Pin	Signal	Color
1	GND	Black
2	GND	Black
3	GND	Black
4	GND	Black
5	+12Vdc	Yellow/Black
6	+12Vdc	Yellow/Black
7	+12Vdc	Yellow/Black
8	+12Vdc	Yellow/Black

Table 57. Power Supply Signal Connector Pin-out (J1K1)

Pin	Signal	Color
1	SMB_CLK_ESB_FP_PWR_R	Orange
2	SMB_DAT_ESB_FP_PWR_R	Black
3	SMB_ALRT_3_ESB_R	Red
4	3.3V SENSE-	Yellow
5	3.3V SENSE+	Green

6.3 System Management Headers

6.3.1 Intel® Remote Management Module 2 (Intel® RMM2) Connector (J1C2)

A 120-pin Intel® RMM2 Connector (J1C2) is included on the server board for sole support of the optional Intel® Remote Management Module 2. There is no support for third-party ASMI cards on this server board.

Note: Only the Intel® Remote Management Module 2 (Intel Product Code: AXXRMM2) is supported with this server board.

Table 58. Intel® RMM2 Connector Pin-out (J1C2)

Pin	Signal Name	Pin	Signal Name
1	Reserved - NC	2	GND
3	ESB_PLT_RST_G1_N	4	Reserved - NC
5	GND	6	Reserved - NC
7	Reserved - NC	8	GND
9	Reserved - NC	10	GND
11	GND	12	Reserved - NC
13	GND	14	IRQ_SERIAL_R
15	USB_ESB_P7P	16	GND
17	USB_ESB_P7N	18	GND
19	GND	20	Reserved - NC
21	P3V3	22	Reserved - NC
23	LPC_LAD<0>	24	GND
25	LPC_LAD<1>	26	LPC_FRAME_N
27	P3V3	28	LPC_LAD<2>
29	LPC_LCLK	30	LPC_LAD<3>
31	P3V3	32	P3V3
33	SMB_1_3V3SB_MS_DAT	34	SMB_IPMB_3V3SB_DAT
35	SMB_1_3V3SB_SL_DAT	36	SMB_IPMB_3V3SB_CLK
37	SMB_1_3V3SB_MS_CLK	38	SMB_0_3V3SB_MS_CLK
39	SMB_1_3V3SB_INT	40	SMB_0_3V3SB_INT
41	P3V3_AUX	42	SMB_0_3V3SB_MS_DAT
43	SPB_IMM_DSR_N	44	SMB_0_3V3SB_SL_DAT
45	SPB_IMM_RTS_N	46	P3V3_AUX

Pin	Signal Name	Pin	Signal Name
47	SPB_IMM_CTS_N	48	FM_IMM_PRESENT_N
49	SPB_IMM_DCD_N	50	SPB_IMM_DTR_N
51	SPB_RI_N	52	SPB_IMM_SIN
53	SPB_IMM_SOUT	54	P3V3_AUX
55	P3V3_AUX	56	V_LCDDATA7
57	V_LCDCNTL3	56	V_LCDDATA6
59	P3V3_AUX	60	V_LCDDATA5
61	Reserved - NC	62	V_LCDDATA4
63	Reserved - NC	64	V_LCDDATA3
65	GND	66	V_LCDCNTL1
67	V_LCDCNTL0	68	GND
69	Reserved - NC	70	V_LCDDATA15
71	GND	72	V_LCDDATA714
73	V_LCDDATA23	74	V_LCDDATA13
75	V_LCDDATA22	76	V_LCDDATA12
77	V_LCDDATA21	78	V_LCDDATA11
79	V_LCDDATA20	80	GND
81	V_LCDDATA19	82	V_LCDCNTL2
83	GND	84	V_DVO_DDC_SDA
85	FM_MAN_LAN_TYPE1	86	V_DVO_DDC_SCL
87	FM_MAN_LAN_TYPE1	88	RST_PS_PWRGD
89	Reserved - NC	90	Reserved - NC
91	Reserved - NC	92	Reserved - NC
93	MII_MDC_RMII_SPARE	94	Reserved - NC
95	MII_COL_RMIIB_RXER	96	GND
97	GND	98	MII_CRS_RMIIB_CRS
99	MII_TXER_RMIIB_TXEN	100	MII_TXCLK_RMIIB_RXCLK
101	MII_MDIO_RMIIB_PRESENT	102	GND
103	GND	104	MII_TXD3_RMIIB_TXD1
105	MII_RXD3_RMIIB_RXD1	106	MII_TXD2_RMIIB_TXD0
107	MII_RXD2_RMIIB_RXD0	108	GND
109	GND	110	MII_TXD1_RMIIA_TXD1
111	MII_RXD1_RMIIA_RXD1	112	MII_TXD0_RMIIA_TXD0
113	MII_RXD0_RMIIA_RXD0	114	GND
115	GND	116	MII_TXEN_RMIIA_TXEN
117	MII_RXCLK	118	MII_RXER_RMIIA_TXER
119	MII_RXDV_RMIIA_CRS	120	GND

6.3.2 Intel® RMM2 NIC Connector (J1B2)

The server board provides an internal 30-pin mezzanine style connector (J1B2) to accommodate a proprietary form factor Intel® RMM2 NIC module. The following table details the pin-out of the Intel® RMM2 NIC module connector.

Table 59. 30-pin Intel® RMM2 NIC Module Connector Pin-out (J1B2)

Pin	Signal Name	Pin	Signal Name
1	FM_MAN_LAN_TYPE2	2	MII_MDC_RMII_SPARE
3	FM_MAN_LAN_TYPE1	4	MII_COL_RMIIB_RXER
5	GND	6	GND
7	MII_TXCLK_RMIIB_RXCLK	8	MII_TXER_RMIIB_TXEN
9	MII_CRS_RMIIB_CRS	10	MII_MDIO_RMIIB_PRESENT
11	GND	12	GND
13	MII_TXD2_RMIIB_TXD0	14	MII_RXD3_RMIIB_RXD1
15	MII_TXD1_RMIIA_TXD1	16	MII_RXD3_RMIIB_RXD0
17	GND	18	GND
19	MII_TXD3_RMIIB_TXD1	20	MII_RXD1_RMIIA_RXD1
21	MII_TXD0_RMIIA_TXD0	22	MII_RXD0_RMIIA_RXD0
23	GND	24	GND
25	MII_TXEN_RMIIA_TXEN	26	MII_RXCLK
27	P3V3_AUX	28	P3V3_AUX
29	MII_RXER_RMIIA_RXER	30	MII_RXDV_RMIIA_CRS

6.3.3 IPMB Headers (J1C3, J1C4)

Table 60. IPMB Header Pin-out (J1C3)

Pin	Signal Name	Description
1	SMB_IPMB_5VSB_DAT	BMC IMB 5V Standby Data Line
2	GND	Ground
3	SMB_IPMB_5VSB_CLK	BMC IMB 5V Standby Clock Line
4	P5V_STBY	+5V Standby Power

Table 61. IPMB Header Pin-out (J1C4)

Pin	Signal Name	Description
1	SMB_IPMB_5VSB_DAT	BMC IMB 5V Standby Data Line
2	GND	
3	SMB_IPMB_5VSB_CLK	BMC IMB 5V Standby Clock Line

6.4 Riser Card Slot

The server board has one riser card slot capable of supporting PCI Express* x16 Gen 2 riser card. The following table shows the pin-out for this riser slot.

Table 62. Riser Card Slot Pin-out (J4B1)

Pin-Side B	PCI Spec Signal	Pin-Side A	PCI Spec Signal
82	RSVD	82	GND
81	PRSNT2#	81	HSIN15
80	GND	80	HSIP15
79	HSON15	79	GND
78	HSOP15	78	GND
77	GND	77	HSIN14
76	GND	76	HSIP14
75	HSON14	75	GND
74	HSOP14	74	GND
73	GND	73	HSIN13
72	GND	72	HSIP13
71	HSON13	71	GND
70	HSOP13	70	GND
69	GND	69	HSIN12
68	GND	68	HSIP12
67	HSON12	67	GND
66	HSOP12	66	GND
65	GND	65	HSIN11
64	GND	64	HSIP11
63	HSON11	63	GND
62	HSOP11	62	GND
61	GND	61	HSIN10
60	GND	60	HSIP10
59	HSON10	59	GND
58	HSOP10	58	GND
57	GND	57	HSIN9
56	GND	56	HSIP9
55	HSON9	55	GND
54	HSOP9	54	GND
53	GND	53	HSIN8
52	GND	52	HSIP8
51	HSON8	51	GND
50	HSOP8	50	RSVD
49	GND	49	GND
48	PRSNT2#	48	HSIN7
47	GND	47	HSIP7
46	HSON7	46	GND

Pin-Side B	PCI Spec Signal	Pin-Side A	PCI Spec Signal
45	HSOP7	45	GND
44	GND	44	HSIN6
43	GND	43	HSIP6
42	HSON6	42	GND
41	HSOP6	41	GND
40	GND	40	HSIN5
39	GND	39	HSIP5
38	HSON5	38	GND
37	HSOP5	37	GND
36	GND	36	HSIN4
35	GND	35	HSIP4
34	HSON4	34	GND
33	HSOP4	33	RSVD
32	GND	32	RSVD
31	PRSNT2#	31	GND
30	RSVD	30	HSIN3
29	GND	29	HSIP3
28	HSON3	28	GND
27	HSOP3	27	GND
26	GND	26	HSIN2
25	GND	25	HSIP2
24	HSON2	24	GND
23	HSOP2	23	GND
22	GND	22	HSIN1
21	GND	21	HSIP1
20	HSON1	20	GND
19	HSOP1	19	RSVD
18	GND	18	GND
17	PRSNT2#	17	HSIN0
16	GND	16	HSIP0
15	HSON0	15	GND
14	HSOP0	14	REFCLK-
13	GND	13	REFCLK+
12	RSVD	12	GND
KEY		KEY	
KEY		KEY	
11	WAKE#	11	PWRGD
10	3.3V AUX	10	3.3V
9	JTAG1	9	3.3V
8	3.3V	8	JTAG5
7	GND	7	JTAG4
6	SMDAT	6	JTAG3
5	SMCLK	5	JTAG2
4	GND	4	GND

Pin-Side B	PCI Spec Signal	Pin-Side A	PCI Spec Signal
3	RSVD	3	12V
2	12V	2	12V
1	12V	1	PRSNT1#

6.5 SSI Control Panel Connector (J3H2)

The server board provides a 24-pin SSI control panel connector (J3H2) for use with non-Intel chassis. The following table provides the pin-out for this connector.

Table 63. SSI Standard 24-pin Control Panel Connector Pin-out (J3H2)

Pin	Signal Name	Pin	Signal Name
1	P3V3_STBY	2	P3V3_STBY
3	Key	4	P5V_STBY
5	FP_PWR_LED	6	FP_ID_LED
7	P3V3	8	LED_STATUS_GREEN
9	HDD_LED_ACT	10	LED_STATUS_AMBER
11	FP_PWR_BTN	12	NIC1_ACT_LED
13	GND	14	NIC1_LINK_LED
15	BMC Reset Button	16	SMB_SN_3V3SB_DAT
17	GND	18	SMB_SN_3V3SB_CLK
19	FP_ID_BTN	20	FP_CHASSIS_INTRU
21	TEMP_SENSOR	22	NIC2_ACT_LED
23	FP_NMI_BTN	24	NIC2_LINK_LED

The system BIOS combined with the Integrated BMC provide the functionality of the various supported control panel buttons and LEDs. The following sections describe the supported functionality of each control panel feature.

Note: Control panel features are also routed through the bridge board connector at location J4G1, as is implemented in Intel® Server Systems configured using a bridge board and a hot-swap backplane.

6.5.1 Power Button

The BIOS supports a front control panel power button. Pressing the power button initiates a request that the Integrated BMC forwards to the ACPI power state machines in the chipset. It is monitored by the Integrated BMC and does not directly control power on the power supply.

- **Power Button — Off to On**
  The Integrated BMC monitors the power button and the wake-up event signals from the chipset. A transition from either source results in the Integrated BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The hardware receives the power good and reset signals from the Integrated BMC and then transitions to an ON state.

- **Power Button — On to Off (operating system absent)**
  The System Control Interrupt (SCI) is masked. The BIOS sets up the power button event to generate an SMI and checks the power button status bit in the ACPI hardware registers when an SMI occurs. If the status bit is set, the BIOS sets the ACPI power state of the machine in the chipset to the OFF state. The Integrated BMC monitors power state signals from the chipset and de-asserts PS_PWR_ON to the power supply. As a safety mechanism, the Integrated BMC automatically powers off the system in 4 to 5 seconds if the BIOS fails to service the request.
- **Power Button — On to Off (operating system present)**
  If an ACPI operating system is running, pressing the power button switch generates a request to the operating system via SCI to shut down the system. The operating system retains control of the system and operating system policy determines the sleep state into which the system transitions, if any. Otherwise, the BIOS turns off the system.

6.5.2 Reset Button

The platform supports a front control panel reset button. Pressing the reset button initiates a request that is forwarded by the Integrated BMC to the chipset. The BIOS does not affect the behavior of the reset button.

6.5.3 NMI Button

The BIOS supports a front control panel NMI button. The NMI button may not be provided on all front panel designs. Pressing the NMI button initiates a request that causes the Integrated BMC to generate an NMI (non-maskable interrupt). The NMI is captured by the BIOS during boot services time, and by the operating system during runtime. During boot services time, the BIOS halts the system upon detection of the NMI.

6.5.4 Chassis Identify Button

The front panel chassis identify button toggles the state of the chassis ID LED. If the LED is off, then pushing the ID button lights the LED. It remains lit until the button is pushed again or until a *Chassis Identify* or a *Chassis Identify LED* command is received to change the state of the LED.

6.5.5 Power LED

The green power LED is active when system DC power is on. The power LED is controlled by the BIOS. The power LED reflects a combination of the state of system (DC) power and the system ACPI state. The following table shows the states that can be assumed.

Table 64. Power LED Indicator States

State	ACPI	Power LED
Power off	No	Off
Power on	No	Solid on
S4/S5	Yes	Off
S1 Sleep	Yes	~1 Hz blink
S0	Yes	Solid on

6.5.6 System Status LED

Note: The system status LED state shows the state for the current, most severe fault. For example, if there was a critical fault due to one source and a non-critical fault due to another source, the system status LED state would be solid on (the state for the critical fault).

The system status LED is a bicolor LED. Green (status) is used to show a normal operation state or a degraded operation. Amber (fault) shows the system hardware state and overrides the green status.

The Integrated BMC-detected state and the state from other controllers, such as the SCSI/SATA hot-swap controller state, is included in the LED state. For fault states that are monitored by the Integrated BMC sensors, the contribution to the LED state follows the associated sensor state, with the priority going to the most critical state that is currently asserted.

When the server is powered down (transitions to the DC-off state or S5), the Integrated BMC is still on standby power and retains the sensor and front panel status LED state established prior to the power-down event.

The following table maps the system state to the LED state:

Table 65. System Status LED Indicator States

Color	State	System Status	Description
Green	Solid on	Ok	System ready
Green	~1 Hz blink	Degraded	System degraded: <u>BIOS detected</u> 1. Unable to use all of the installed memory (more than one DIMM installed).[1] 2. Correctable errors over a threshold of ten and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spare DIMMs indicating a redundancy lost condition. The corresponding DIMM LED should light up.[1] 3. In a mirrored configuration, when memory mirroring takes place and system loses memory redundancy. This is not covered by (2). [1] 4. PCI Express* correctable link errors. <u>Integrated BMC detected</u> 1. Redundancy loss such as power supply or fan. Applies only if the associated platform subsystem has redundancy capabilities. 2. CPU disabled – if there are two CPUs and one CPU is disabled 3. Fan alarm – Fan failure. Number of operational fans should be more than the minimum number needed to cool the system. 4. Non-critical threshold crossed – Temperature, voltage, power nozzle, power gauge, and PROCHOT[2] (Therm Ctrl) sensors. 5. Battery failure 6. Predictive failure when the system has redundant power supplies

Color	State	System Status	Description
Amber	~1 Hz blink	Non-Fatal	Non-fatal alarm – system is likely to fail: BIOS Detected 1. In a non-sparing and non-mirroring mode if the threshold of ten correctable errors is crossed within the window[1]. 2. PCI Express* uncorrectable link errors. Integrated BMC Detected 1. Critical threshold crossed – Voltage, temperature, power nozzle, power gauge, and PROCHOT (Therm Ctrl) sensors. 2. VRD Hot asserted 3. Minimum number of fans to cool the system are not present or have failed.
Amber	Solid on	Fatal	Fatal alarm – system has failed or shutdown: BIOS Detected 1. DIMM failure when there is one DIMM present and no good memory is present[1]. 2. Run-time memory uncorrectable error in a non-redundant mode[1]. 3. CPU configuration error (for instance, processor stepping mismatch). Integrated BMC Detected 1. CPU IERR signal asserted. 2. CPU 1 is missing. 3. CPU THERMTRIP. 4. No power good – power fault. 5. Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present).
Off	N/A	Not ready	AC power off

Note:

1. BIOS detects these conditions and sends a *Set Fault Indication* command to the Integrated BMC to provide a contribution to the system status LED.
2. Support for upper non-critical limit is not provided in default SDR configuration. However if a user does enable this threshold in the SDR, then the system status LED should behave as described.

6.5.7 Chassis ID LED

The chassis ID LED provides a visual indication of a system being serviced. The state of the chassis ID LED is affected by the following:

- It is toggled by the chassis ID button.
- It can be controlled by the *Chassis Identify* command (IPMI).
- It can be controlled by the *Chassis Identify LED* command (OEM).

Table 66. Chassis ID LED Indicator States

State	LED State
Identify active via button	Solid on
Identify active via command	~1 Hz blink
Off	Off

There is no precedence or lock-out mechanism for the control sources. When a new request arrives, all previous requests are terminated. For example, if the chassis ID LED is blinking and the chassis ID button is pressed, then the chassis ID LED changes to solid on. If the button is pressed again with no intervening commands, the chassis ID LED turns off.

6.6 Bridge Board Connector (J4G1)

For use in the supported Intel® Server Chassis, the server board provides a 120-pin high-density bridge board connector (J4G1) to route control panel, midplane, and backplane signals from the server board to the specified system board. The following table provides the pin-outs for this connector.

Table 67. 120-pin Bridgeboard Connector Pin-out (J4G1)

Pin	Signal Name	Pin	Signal Name
A1	SMB_HOST_3V3_CLK	B1	GND
A2	SMB_HOST_3V3_DAT	B2	PE1_ESB_TXN_C<3>
A3	FM_BRIDGE_PRESENT_N	B3	PE1_ESB_TXP_C<3>
A4	GND	B4	GND
A5	PE1_ESB_RXN_C<3>	B5	PE_WAKE_N
A6	PE1_ESB_RXP_C<3>	B6	GND
A7	GND	B7	PE1_ESB_TXN_C<2>
A8	FM_FAN_D_PRSNT6	B8	PE1_ESB_TXP_C<2>
A9	GND	B9	GND
A10	PE1_ESB_RXN_C<2>	B10	FM_FAN_D_PRSNT5
A11	PE1_ESB_RXP_C<2>	B11	GND
A12	GND	B12	PE1_ESB_TXN_C<1>
A13	FM_FAN_D_PRSNT4	B13	PE1_ESB_TXP_C<1>
A14	GND	B14	GND
A15	PE1_ESB_RXN_C<1>	B15	RST_MP_PWRGD
A16	PE1_ESB_RXP_C<1>	B16	GND
A17	GND	B17	PE1_ESB_TXN_C<0>
A18	FM_RAID_PRESENT	B18	PE1_ESB_TXP_C<0>
A19	GND	B19	GND
A20	PE1_ESB_RXN_C<0>	B20	FM_RAID_MODE
A21	PE1_ESB_RXP_C<0>	B21	GND
A22	GND	B22	CLK_100M_SRLAKE_N
A23	FM_FAN_D_PRSNT1	B23	CLK_100M_SRLAKE_P
A24	FM_FAN_D_PRSNT3	B24	GND
A25	FM_FAN_D_PRSNT2	B25	SGPIO_DATAOUT1_R
A26	GND	B26	SGPIO_DATAOUT0_R
A27	USB_ESB_P4P	B27	SGPIO_LOAD_R
A28	USB_ESB_P4N	B28	SGPIO_CLOCK_N
A29	GND	B29	GND
A30	USB_ESB_OC_N<4>	B30	USB_ESB_P2P
A31	USB_ESB_OC_N<3>	B31	USB_ESB_P2N
A32	GND	B32	GND
A33	USB_ESB_P3P	B33	USB_ESB_OC_N<2>
A34	USB_ESB_P3N	B34	NIC1_LINK_LED_N
A35	GND	B35	NIC1_ACT_LED_N
A36	FP_NMI_BTN_N	B36	LED_STATUS_GREEN_R1

Pin	Signal Name	Pin	Signal Name
KEY		KEY	
A37	BMC_RST_BTN_N	B37	NIC2_LINK_LED_N
A38	FP_PWR_BTN_N	B38	NIC2_ACT_LED_N
A39	FP_ID_BTN	B39	LED_STATUS_AMBER_R1
A40	GND	B40	GND
A41	SMB_IPMB_ 5VSB_SDA	B41	SMB_SN_3V3SB_DAT_BUF
A42	SMB_IPMB_ 5VSB_CLK	B42	SMB_SN_3V3SB_CLK_BUF
A43	GND	B43	GND
A44	LED_ HDD_ACTIVITY_N	B44	V_IO_HSYNC2_BUF_FP
A45	P3V3	B45	V_IO_VSYNC2_BUF_FP
A46	FP_PWR_LED_N_R	B46	GND
A47	P3V3_STBY	B47	V_IO_BLUE_CONN_FP
A48	FP_ID_LED_R1_N	B48	V_IO_GREEN_CONN_FP
A49	FM_SIO_TEMP_SENSOR	B49	V_IO_RED_CONN_FP
A50	LED_FAN3_FAULT	B50	GND
A51	LED_FAN2_FAULT	B51	LED_FAN10_FAULT
A52	LED_FAN1_FAULT	B52	LED_FAN5_FAULT
A53	FAN_PWM_CPU1	B53	LED_FAN4_FAULT
A54	GND	B54	FAN_IO_PWM
A55	FAN_PWM_CPU2	B55	GND
A56	PCI_FAN_TACH9	B56	PCI_FAN_TACH10
A57	FAN_TACH7	B57	FAN_TACH8
A58	FAN_TACH5	B58	FAN_TACH6
A59	FAN_TACH3_H7	B59	FAN_TACH4_H7
A60	FAN_TACH1_H7	B60	FAN_TACH2_H7

6.7 I/O Connector Pin-out Definition

6.7.1 VGA Connector (J6A1)

The following table details the pin-out definition of the VGA connector (J6A1).

Table 68. VGA Connector Pin-out (J6A1)

Pin	Signal Name	Description
1	V_IO_R_CONN	Red (analog color signal R)
2	V_IO_G_CONN	Green (analog color signal G)
3	V_IO_B_CONN	Blue (analog color signal B)
4	TP_VID_CONN_B4	No connection
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	TP_VID_CONN_B9	No Connection
10	GND	Ground
11	TP_VID_CONN_B11	No connection
12	V_IO_DDCDAT	DDCDAT
13	V_IO_HSYNC_CONN	HSYNC (horizontal sync)
14	V_IO_VSYNC_CONN	VSYNC (vertical sync)
15	V_IO_DDCCLK	DDCCLK

6.7.2 NIC Connectors

The server board provides two RJ-45 NIC connectors oriented side by side on the back edge of the board (JA8A1, JA8A2). The pin-out for each connector is identical and is defined in the following table.

Table 69. RJ-45 10/100/1000 NIC Connector Pin-out (JA8A1, JA8A2)

Pin	Signal Name
1	GND
2	P1V8_NIC
3	NIC_MDI3P
4	NIC_MDI3N
5	NIC_MDI2P
6	NIC_MDI2N
7	NIC_MDI1P
8	NIC_MDI1N
9	NIC_MDI0P
10	NIC_MDI0N
11 (D1)	NIC_LINKA_1000_N (LED)
12 (D2)	NIC_LINKA_100_N (LED)
13 (D3)	NIC_ACT_LED_N
14	NIC_LINK_LED_N
15	GND
16	GND

6.7.3 IDE Connector (J3G2)

The server board includes an IDE connector to access the single IDE channel from the Intel® 6321ESB I/O Controller Hub. The design intent for this connector is to provide IDE support for a single slimline optical drive, such as CD-ROM or DVD. The connector is not a standard 40-pin IDE connector, instead it has 44 pins providing support for both power and I/O signals. The pin-out for this connector is defined in the following table.

Table 70. 44-pin IDE Connector Pin-out (J3G2)

Pin	Signal Name	Pin	Signal Name
1	ESB_PLT_RST_IDE_N	2	GND
3	RIDE_DD_7	4	RIDE_DD_8
5	RIDE_DD_6	6	RIDE_DD_9
7	RIDE_DD_5	8	RIDE_DD_10
9	RIDE_DD_4	10	RIDE_DD_11
11	RIDE_DD_3	12	RIDE_DD_12
13	RIDE_DD_2	14	RIDE_DD_13
15	RIDE_DD_1	16	RIDE_DD_14
17	RIDE_DD_0	18	RIDE_DD_15
19	GND	20	KEY
21	RIDE_DDREQ	22	GND
23	RIDE_DIOW_N	24	GND
25	RIDE_DIOR_N	26	GND
27	RIDE_PIORDY	28	GND

Pin	Signal Name	Pin	Signal Name
29	RIDE_DDACK_N	30	GND
31	IRQ_IDE	32	TP_PIDE_32
33	RIDE_DA1	34	IDE_PRI_CBLSNS
35	RIDE_DA0	36	RIDE_DA2
37	RIDE_DCS1_N	38	RIDE_DCS3_N
39	LED_IDE_N	40	GND
41	P5V	42	P5V
43	GND	44	GND

6.7.4 Intel® I/O Expansion Module Connector (J3B1)

The server board provides an internal 50-pin mezzanine style connector (J3B1) to accommodate proprietary form factor Intel® I/O Expansion Modules, which expand the I/O capabilities of the server board without sacrificing an add-in slot from the riser cards. There are three I/O modules for use on this server board: external 4-port SAS module, dual Gb NIC module, and Infiniband* module. For more information on the supported I/O modules, please refer to the *Intel® Server Board S500PAL/S5000XAL I/O Module Hardware Specification*.

The following table details the pin-out of the Intel® I/O Expansion Module connector.

Table 71. 50-pin Intel® I/O Expansion Module Connector Pin-out (J3B1)

Pin	Signal Name	Pin	Signal Name
1	P3V3_AUX	2	P3V3_AUX
3	PE_RST_IO_MODULE_N	4	GND
5	GND	6	PE2_ESB_RXP_C<0>
7	GND	8	PE2_ESB_RXN_C<0>
9	PE2_ESB_TXP_C<0>	10	GND
11	PE2_ESB_TXN_C<0>	12	GND
13	GND	14	PE2_ESB_RXP_C<1>
15	GND	16	PE2_ESB_RXN_C<1>
17	PE2_ESB_TXP_C<1>	18	GND
19	PE2_ESB_TXN_C<1>	20	GND
21	GND	22	PE2_ESB_RXP_C<2>
22	GND	24	PE2_ESB_RXN_C<2>
25	PE2_ESB_TXP_C<2>	26	GND
27	PE2_ESB_TXN_C<2>	28	GND
29	GND	30	PE2_ESB_RXP_C<3>
31	GND	32	PE2_ESB_RXN_C<3>
33	PE2_ESB_TXP_C<3>	34	GND
35	PE2_ESB_TXN_C<3>	36	GND
37	GND	38	CLK_100M_LP_PCIE_SLOT3_P
39	GND	40	CLK_100M_LP_PCIE_SLOT3_N
41	PE_WAKE_N	42	GND
43	P3V3	44	P3V3
45	P3V3	46	P3V3
47	P3V3	48	P3V3
49	P3V3	50	P3V3

6.7.5 SATA Connectors

The server board provides six Serial ATA (SATA) connectors: SATA-0 (J1H1), SATA-1 (J1G2), SATA-2 (J1G1), SATA-3 (J1F2), SATA-4 (J1F1), and SATA-5 (J1E2), for use with an internal SATA backplane. The pin configuration for each connector is identical and is defined in the following table.

Table 72. SATA Connector Pin-out (J1H1, J1G2, J1G1, J1F2, J1F1, J1E2)

Pin	Signal Name	Description
1	GND	Ground
2	SATA#_TX_P_C	Positive side of transmit differential pair
3	SATA#_TX_N_C	Negative side of transmit differential pair
4	GND	Ground
5	SATA#_RX_N_C	Negative side of Receive differential pair
6	SATA#_RX_P_C	Positive side of Receive differential pair
7	GND	Ground

6.7.6 Serial Port Connectors

The server board provides one external RJ-45 Serial 'B' port (J9A2) and one internal 9-pin Serial 'A' port header (J1B1). The following tables define the pin-outs for each.

Table 73. External RJ-45 Serial 'B' Port Pin-out (J9A2)

Pin	Signal Name	Description
1	SPB_RTS	RTS (request to send)
2	SPB_DTR	DTR (Data terminal ready)
3	SPB_OUT_N	TXD (Transmit data)
4	GND	Ground
5	SPB_RI	RI (Ring Indicate)
6	SPB_SIN_N	RXD (receive data)
7	SPB_DSR _DCD	Data Set Ready/Data Carrier Detect [1]
8	SPB_CTS	CTS (clear to send)

Note: A jumper block on the server board determines whether DSR or DCD is routed to pin 7. The board has the jumper block configured with DSR enabled at production.

Table 74. Internal 9-pin Serial 'A' Header Pin-out (J1B1)

Pin	Signal Name	Description
1	SPA_DCD	DCD (carrier detect)
2	SPA_DSR	DSR (data set ready)
3	SPA_SIN_L	RXD (receive data)
4	SPA_RTS	RTS (request to send)
5	SPA_SOUT_N	TXD (Transmit data)
6	SPA_CTS	CTS (clear to send)
7	SPA_DTR	DTR (Data terminal ready)
8	SPA_RI	RI (Ring Indicate)
9	GND	Ground

6.7.7 Keyboard and Mouse Connector

Two stacked PS/2 ports (J9A1) are provided to support both a keyboard and a mouse. Either PS/2 port can support a mouse or keyboard. The following table details the pin-out of the PS/2 connector.

Table 75. Stacked PS/2 Keyboard and Mouse Port Pin-out (J9A1)

Pin	Signal Name	Description
1	KB_DATA_F	Keyboard Data
2	TP_PS2_2	Test point – keyboard
3	GND	Ground
4	P5V_KB_F	Keyboard/mouse power
5	KB_CLK_F	Keyboard Clock
6	TP_PS2_6	Test point – keyboard/mouse
7	MS_DAT_F	Mouse Data
8	TP_PS2_8	Test point – keyboard/mouse
9	GND	Ground
10	P5V_KB_F	Keyboard/mouse power
11	MS_CLK_F	Mouse Clock
12	TP_PS2_12	Test point – keyboard/mouse
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground

6.7.8 USB 2.0 Connectors

The following table details the pin-out of the externally stacked USB connectors found on the back edge of the server board:

Table 76. External USB Connector Pin-out (J5A1)

Pin	Signal Name	Description
1	USB_OC5_FB_1	USB_Port5_PWR
2	USB_P5N_FB_2	DATAL0_Port5 (Differential data line paired with DATAH0)
3	USB_P5P_FB_3	DATAH0_Port5 (Differential data line paired with DATAL0)
4	GND	Ground
5	USB_OC6_FB_5	USB_Port6_PWR
6	USB_P6N_FB_6	DATAL0_Port6 (Differential data line paired with DATAH0)
7	USB_P6P_FB_7	DATAH0_Port6 (Differential data line paired with DATAL0)
8	GND	Ground

One 2x5 header on the server board (J1J1) provides an option to support two additional USB 2.0 ports. The pin-out of the connector is detailed in the following table.

Table 77. Internal USB Connector Pin-out (J1J1)

Pin	Signal Name	Description
1	P5V_USB2_VBUS0	USB Power (Ports 0,1)
2	P5V_USB2_VBUS1	USB Power (Ports 0,1)
3	USB_ESB_P0N_CONN	USB Port 0 Negative Signal
4	USB_ESB_P1N_CONN	USB Port 0 Positive Signal
5	USB_ESB_P0P_CONN	USB Port 1 Negative Signal
6	USB_ESB_P1P_CONN	USB Port 1 Positive Signal
7	Ground	
8	Ground	
9	--	No Pin
10	TP_USB_ESB_NC	TEST POINT

6.8 Fan Headers

The server board incorporates three system fan circuits, which support a total of six SSI-compliant 4-pin fan connectors.

- Two fan connectors are designated as processor cooling fans: CPU1 Fan (J9K1) and CPU2 Fan (J4K1). These connectors can support CPU fans that draw a maximum of 1.2 Amps each.
- Two system fan connectors can be found towards the front edge of the server board near the CPU power connector: System Fan 1 (J3K2), System Fan 2 (J3K3). The system fan connectors are capable of supporting a maximum fan load of 3.5 Amps each.
- Two additional fan connectors are located on the edge of the server board near the RMM connector: System Fan 3 (J1B3) and System Fan 4 (J1C1).

The pin configuration for each fan connector is identical and is defined in the following table:

Table 78. SSI Fan Connector Pin-out (J9K1,J4K1,J3K2,J3K3,J1B3,J1C1)

Pin	Signal Name	Type	Description
1	Ground	GND	GROUND is the power supply ground.
2	12V	Power	Power supply 12 V.
3	Fan Tach	Out	FAN_TACH signal is connected to the Integrated BMC to monitor the fan speed.
4	Fan PWM	In	FAN_PWM signal to control fan speed.

When the server board is integrated into an Intel fixed hard drive server chassis, system fan monitoring is supported through a custom 26-pin connector with the following pin-out.

Table 79. Server board-to-System Fan Board Connector (J3K1) Pin-out (Intel® Chassis Only)

Pin Definition	Pin #		Pin Definition
FAN_PWM_CPU1	1	2	FAN_PWM_CPU2
FM_FAN_D_PRSNT1_N	3	4	FAN_IO_PWM
FM_FAN_D_PRSNT3_N	5	6	FM_FAN_D_PRSNT2_N
FM_FAN_D_PRSNT5_N	7	8	FM_FAN_D_PRSNT4_N
Empty – Connector Key	9	10	LED_FAN1_FAULT
LED_FAN2_FAULT	11	12	LED_FAN3_FAULT

Pin Definition	Pin #		Pin Definition
LED_FAN4_FAULT	13	14	LED_FAN5_FAULT
FAN_TACH1_H7	15	16	FAN_TACH2_H7
FAN_TACH3_H7	17	18	FAN_TACH4_H7
FAN_TACH5	19	20	FAN_TACH6
FAN_TACH7	21	22	FAN_TACH8
PCI_FAN_TACH9	23	24	CONN_PIN24_R
PCI_FAN_TACH10	25	26	FM_SIO_TEMP_SENSOR

Note: Intel Corporation server boards support peripheral components and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel's own chassis are designed and tested to meet the intended thermal requirements of these components when the fully integrated system is used together. It is the responsibility of the system integrator that chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits

6.9 Chassis Intrusion Switch Header

For systems that require chassis intrusion detection, the server board provides a 2-pin chassis intrusion switch header. The header is located above the password clear jumper on the edge of the server board.

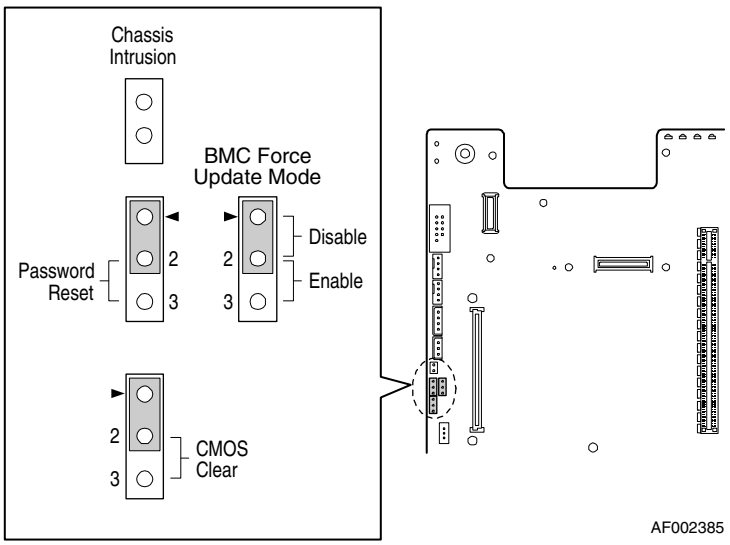


Figure 42. Chassis Intrusion Switch Header Location

The Integrated BMC monitors the state of the *Chassis Intrusion* signal and makes the status of the signal available via the *Get Chassis Status* command and the *Physical Security* sensor state. If enabled, a chassis intrusion state change causes the Integrated BMC to generate a *Physical Security* sensor event message with a *General Chassis Intrusion* offset (00h).

7. Jumper Block Settings

The server board has several 2-pin and 3-pin jumper blocks that can be used to configure, protect, or recover specific features of the server board. Pin 1 on each jumper block is denoted by an "*" or "▼".

7.1 Recovery Jumper Blocks

Table 80. Recovery Jumpers

Jumper Name	Pins	At system reset
BMC Force Update	1-2	Integrated BMC Firmware Force Update Mode – Disabled **(Default)**
	2-3	Integrated BMC Firmware Force Update Mode – Enabled
Password Clear	1-2	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	If these pins are jumpered, administrator and user passwords are cleared immediately. These pins should not be jumpered for normal operation.
CMOS Clear	1-2	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	If these pins are jumpered, the CMOS settings are cleared immediately. These pins should not be jumpered for normal operation.

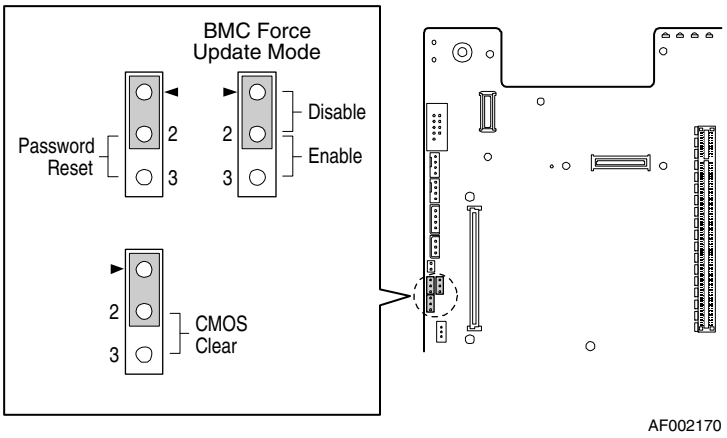


Figure 43. Recovery Jumper Blocks

7.1.1 System Administrator/User Password Reset Procedure

In the event that the System Administrator and/or User password that are set up in the BIOS Setup utility are lost or forgotten, the server board provides a Password Reset Jumper to clear both passwords. The following procedure outlines the usage model.

To reset the password, perform the following steps:

1. Power down the server; do not remove AC power.
2. Open the server and move the jumper from the default operating position (pins1-2) to the “reset” position (pins 2-3).
3. Power up the server.
4. The password is now cleared.
5. Power down the server; do not remove AC power.
6. Move the jumper back to the default position (pins 1-2) and close the server system.
7. The password can be reset by going into the BIOS setup.

7.1.2 CMOS Clear Procedure

To clear the CMOS, perform the following steps:

1. Power down the server; do not remove AC power.
2. Open the server and move the jumper from the default operating position (pins 1-2) to the “clear” position (pins 2-3).
3. Wait 5 seconds.
4. Move the jumper back to the default position (pins 1-2).
5. Close the server system and power up the server.
6. CMOS is now cleared and can be reset by going into the BIOS setup.

Note: Removing AC power before performing the CMOS clear operation causes the system to automatically power up and immediately power down after the procedure is followed and AC power is re-applied. Should this occur, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power up the system and proceed to the <F2> BIOS Setup utility to reset desired settings.

7.1.3 Integrated BMC Force Update Procedure

When performing a standard Integrated BMC firmware update procedure, the update utility places the Integrated BMC into an update mode, allowing the firmware to load safely onto the flash device. In the unlikely event that the Integrated BMC firmware update process fails due to the Integrated BMC not being in the proper update state, the server board provides a BMC Force Update jumper, which forces the Integrated BMC into the proper update state. The following procedure should be following in the event the standard Integrated BMC firmware update process fails.

1. Power down the server and remove AC power.
2. Open the server and move the jumper from the default operating position (pins 1-2) to the “enabled” position (pins 2-3).
3. Close the server system and reconnect AC power and power up the server.
4. Perform the standard Integrated BMC firmware update procedure as documented in README.TXT file that is included in the given Integrated BMC Firmware Update package.

After successful completion of the firmware update process, the firmware update utility may generate an error stating that the Integrated BMC is still in update mode.

5. Power down and remove AC power.
6. Open the server and move the jumper from the “enabled” position (pins 2-3) to the “disabled” position (pins 1-2).
7. Close the server system and reconnect AC power and power up the server.

Note: Normal Integrated BMC functionality is disabled with the Integrated BMC force update jumper set to the “enabled” position. The server should never be run with the Integrated BMC force update jumper set in this position and should only be used when the standard firmware update process fails. This jumper should remain in the default disabled position when the server is running normally.

7.2 BIOS Select Jumper

The jumper block at J3H1, located just to the left of the SSI control panel header, is used to select the BIOS image to which the system boots. Pin 1 on the jumper is identified with a ‘▼’. This jumper should only be moved if you wish to force the BIOS to boot to the secondary bank, which may hold a different version of the BIOS.

The rolling BIOS feature of the server board automatically alternates the boot BIOS to the secondary bank in the event the BIOS image in the primary bank is corrupted and cannot boot for any reason.

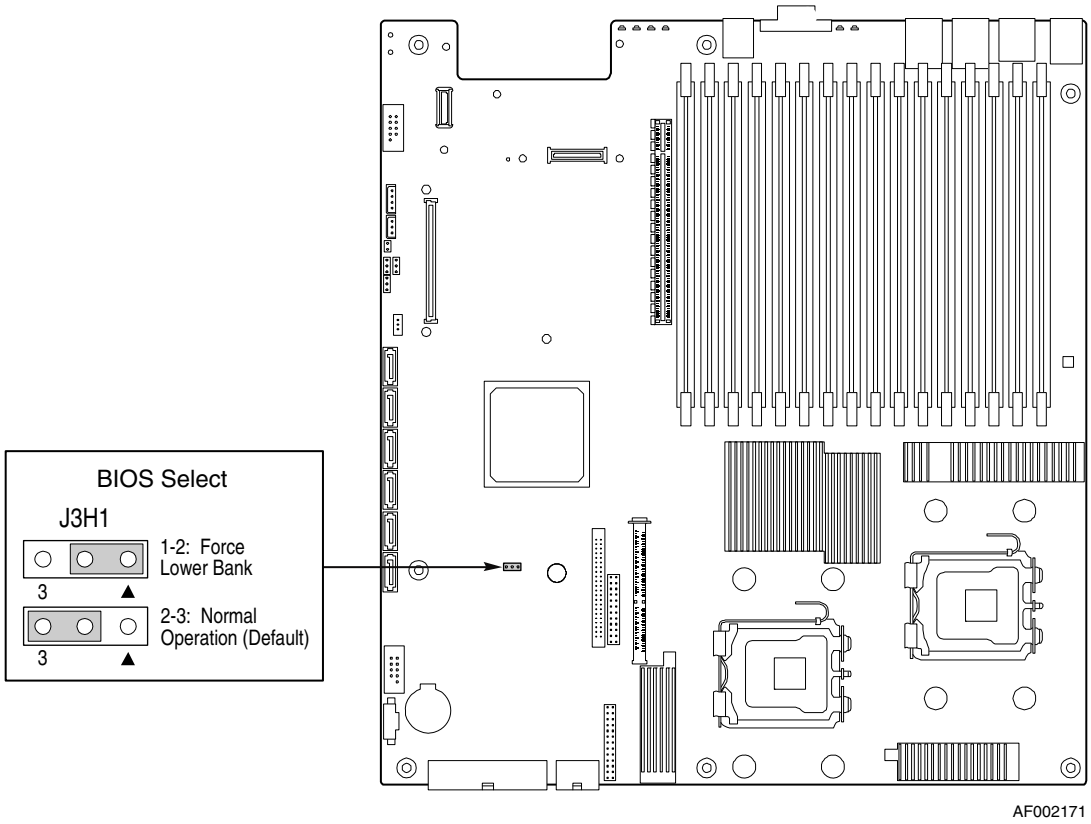


Figure 44. BIOS Select Jumper (J3H1)

Pins	At system reset
1-2	Force BIOS to bank 0
2-3	System is configured for normal operation (Default)

Note:

1. When performing the BIOS update procedure, the BIOS select jumper must be set to its default position (pins 2-3).

7.3 External RJ-45 Serial Port Jumper Block

The jumper block J9D1, located directly behind the external RJ-45 serial port, is used to configure either a DSR or a DCD signal to the connector.

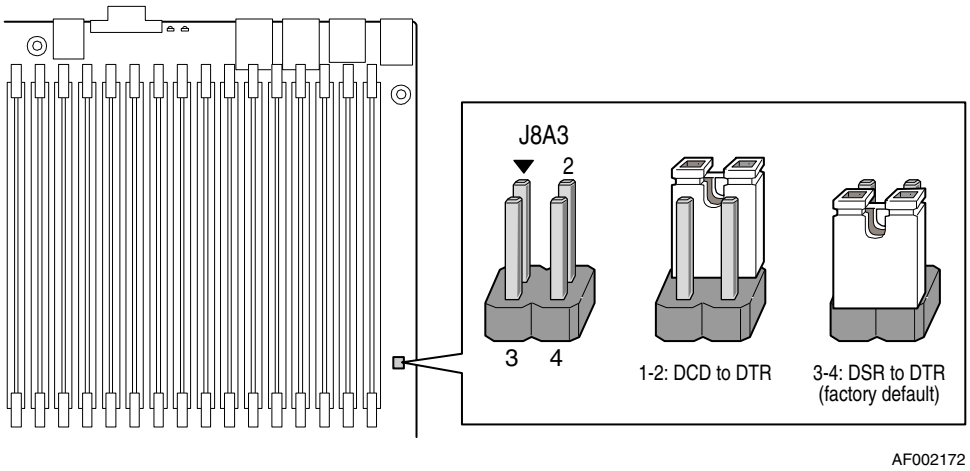


Figure 45. External RJ-45 Serial Port Configuration Jumper

8. Intel® Light-Guided Diagnostics

The server board has several on-board diagnostic LEDs to assist in troubleshooting board-level issues. Functionality of the on-board LEDs is owned by the Integrated BMC and system BIOS. Many of the LEDs are controlled via the SIO. The Integrated BMC and the BIOS use a chip-specific method to avoid contention when accessing the SIO-based LEDs.

This section shows where each LED is located and provides a high level usage description.

8.1 5-Volt Standby LED

Several server management features of this server board require that a 5 volt standby voltage be supplied from the power supply. The Integrated BMC within the Intel® 6321ESB I/O Controller Hub, on-board NICs, and optional Intel® RMM2 are some of the features and components that require that this voltage be present when the system is “Off”.

The LED located just below the system recovery jumper block labeled “5V STBY” is illuminated when AC power is applied to the platform and 5 Volt standby voltage is supplied to the server board by the power supply.

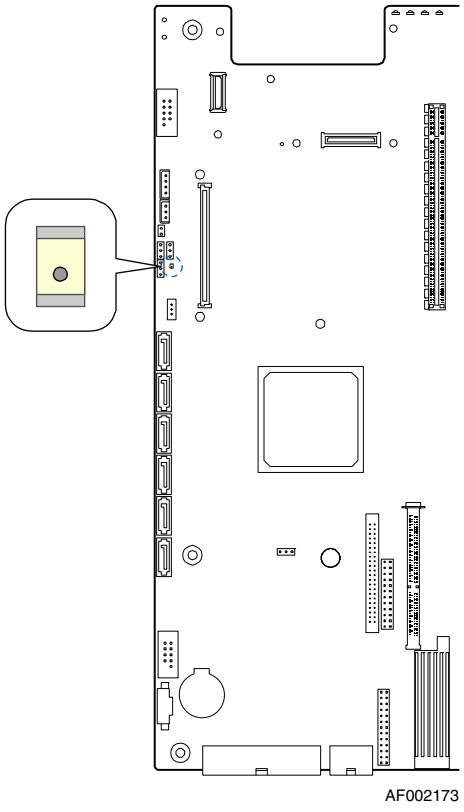


Figure 46. 5V Standby Status LED Location

8.2 System ID LED and System Status LED

The server board provides LEDs for both System ID and System Status.

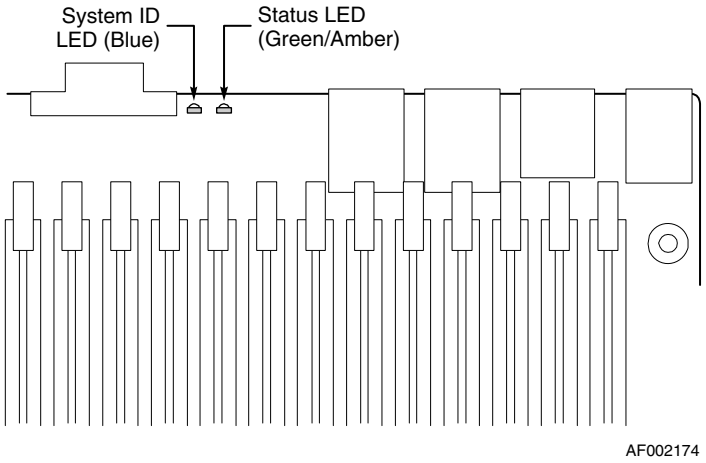


Figure 47. System ID LED and System Status LED Locations.

The blue "System ID" LED can be illuminated using one of the following mechanisms:

- By pressing the system ID button on the system control panel, the ID LED displays a solid blue color until the button is pressed again.
- By issuing the appropriate hex IPMI "Chassis Identify" value, the ID LED either blinks blue for 15 seconds and turns off or blinks indefinitely until the appropriate hex IPMI Chassis Identify value is issued to turn it off.

The bi-color System Status LED operates as described in the following table:

Table 81. System Status LED Operation

Color	State	Criticality	Description
Off	N/A	Not ready	AC power off
Green/ Amber	Alternating Blink	Not ready	Pre DC Power On – 15-20 second Integrated BMC Initialization when AC is applied to the server. Control Panel buttons are disabled until Integrated BMC initialization is completed.
Green	Solid on	System OK	System booted and ready.
Green	Blink	Degraded	System degraded: 1. Unable to use all of the installed memory (more than one DIMM installed). 2. Correctable errors over a threshold of ten and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spare DIMMs indicating a redundancy lost condition. The corresponding DIMM LED should light up. 3. In a mirrored configuration, when memory mirroring takes place and system loses memory redundancy. This is not covered by (2). 4. Redundancy loss such as power supply or fan. This does not

Color	State	Criticality	Description
			apply to non-redundant subsystems. 5. PCI Express* link errors 6. CPU failure/disabled – if there are two processors and one of them fails 7. Fan alarm – Fan failure. Number of operational fans should be more than minimum number needed to cool the system 8. Non-critical threshold crossed – Temperature and voltage
Amber	Blink	Non-critical	Non-fatal alarm – system is likely to fail: 1. Critical voltage threshold crossed 2. VRD hot asserted 3. Minimum number of fans to cool the system are not present or have failed 4. In a non-sparing and non-mirroring mode if the threshold of ten correctable errors is crossed within the window
Amber	Solid on	Critical, non-recoverable	Fatal alarm – system has failed or shut down: 1. DIMM failure when there is one DIMM present and no good memory is present 2. Run-time memory uncorrectable error in the non-redundant mode 3. IERR signal asserted 4. Processor 1 missing 5. Temperature (CPU ThermTrip, memory TempHi, critical threshold crossed). 6. No power good – power fault. 7. Processor configuration error (for instance, processor stepping mismatch).

8.2.1 System Status LED – Integrated BMC Initialization

When the AC power is first applied to the system and 5 V-STBY is present, the Integrated BMC controller on the server board requires 5 -10 seconds to initialize. During this time, the system status LED blinks alternating between amber and green, and the power button functionality of the control panel is disabled preventing the server from powering up. Once Integrated BMC initialization has completed, the status LED stops blinking and the power button functionality is restored and can be used to turn on the server.

8.3 DIMM Fault LEDs

The server board provides a memory fault LED for each DIMM slot. The DIMM fault LED is illuminated when the system BIOS disables the specified DIMM after it reaches a specified number of given failures or if specific critical DIMM failures are detected. For details describing DIMM Fault LED operation, see section 3.2.3.10.2.

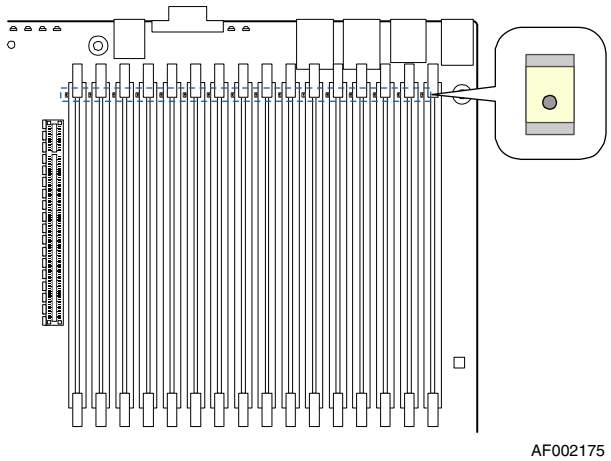


Figure 48. DIMM Fault LED Locations

8.4 Processor Fault LED

The server board provides a processor fault LED for each of the two processor sockets. These LEDs illuminate when a CPU is disabled or a CPU configuration error is detected.

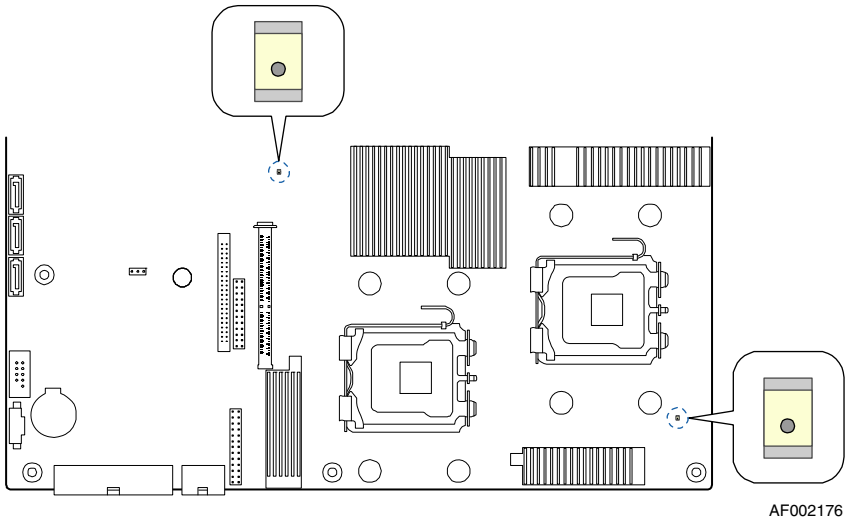


Figure 49. Processor Fault LED Location

8.5 Fan Fault LEDs

There is a fan fault LED associated with each fan header. The Integrated BMC lights a fan fault LED if the associated fan tach sensor has a lower critical threshold event status asserted. Fan tach sensors are manual re-arm sensors, therefore once the lower critical threshold has been crossed, the LED remains lit until the sensor is re-armed. These sensors are re-armed at system DC power-on and system reset.

8.6 Post Code Diagnostic LEDs

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, BIOS displays the given POST code to the POST code diagnostic LEDs found on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, the diagnostic LEDs can be used to identify the last POST process to be executed. See Appendix C for a complete description of how these LEDs are read, and for a list of all supported POST codes.

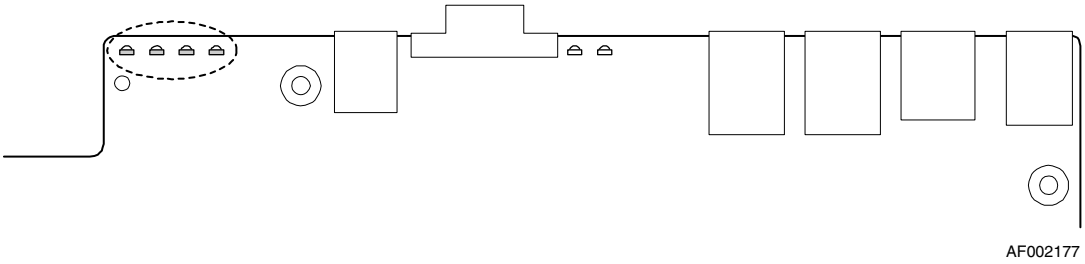


Figure 50. POST Code Diagnostic LED Location

9. Power and Environmental Specifications

9.1 Intel® Server Board S5400SF Design Specifications

Operation of the server board at conditions beyond those shown in the following table may cause permanent damage to the server board. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 82: Server Board Design Specifications

Operating Temperature	0º C to 55º C 1 (32º F to 131º F)
Non-Operating Temperature	-40º C to 70º C (-40º F to 158º F)
DC Voltage	± 5% of all nominal voltages
Shock (Unpackaged)	Trapezoidal, 50 g, 170 inches/sec
Shock (Packaged) < 20 lbs ≥ 20 to < 40 ≥ 40 to < 80 ≥ 80 to < 100 ≥100 to < 120 ≥120	 36 inches 30 inches 24 inches 18 inches 12 inches 9 inches
Vibration (Unpackaged)	5 Hz to 500 Hz 3.13 g RMS random

Note: Chassis design must provide proper airflow to avoid exceeding the Intel® Xeon® Processor 5000 Sequence maximum case temperature.

Disclaimer Note: Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system meets the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

9.2 Server Board Power Requirements

This section provides power supply design guidelines for a system using the Intel® Server Board S5400SF, including voltage and current specifications, and power supply on/off sequencing characteristics. The following figure shows the power distribution implemented on this server board.

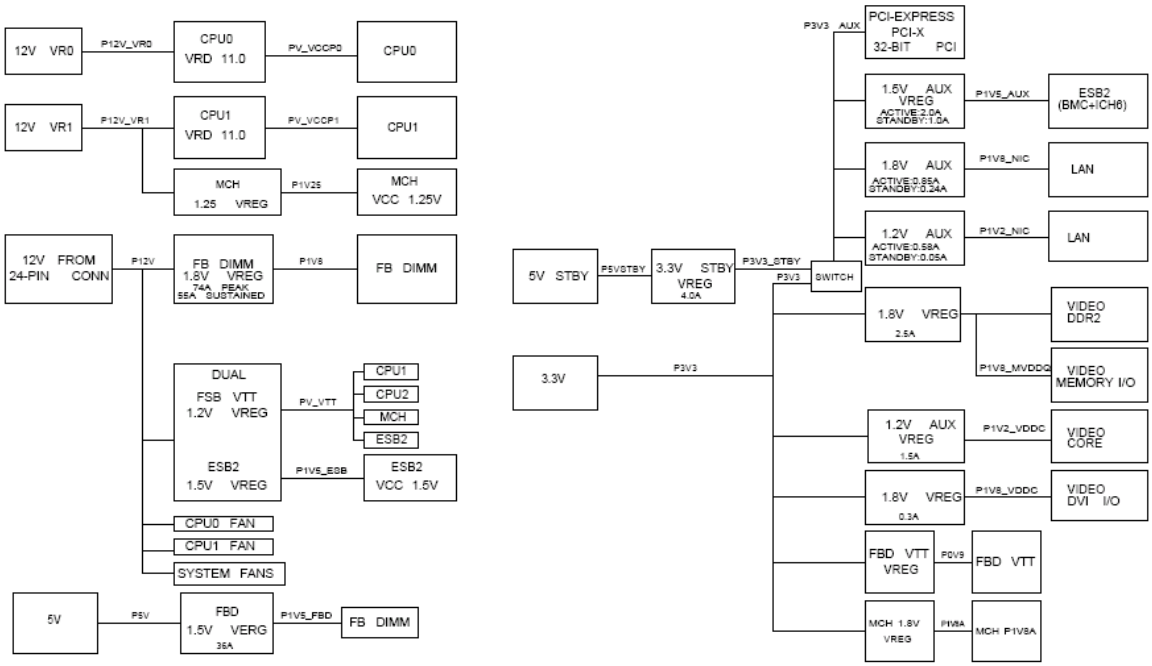


Figure 51. Power Distribution Block Diagram

9.2.1 Processor Power Support

The server board supports the Thermal Design Point (TDP) guideline for Intel® Xeon® Processors 5000 Sequence. The Flexible Motherboard (FMB) guidelines has also been followed to help determine the suggested thermal and current design values for anticipating future processor needs. The following table provides maximum values for Icc, TDP power and T_{CASE} for the Intel® Xeon® Processor 5000 Sequence family supported on this server board.

Table 83. Intel® Xeon® Processor 5000 Sequence TDP Guidelines per processor

TDP Power	Max TCASE	Icc MAX
130 W	70° C	150 A

Note: These values are for reference only. The Intel® Xeon® Processor 5000 Sequence datasheet contains the actual specifications for the processor. If the values found in the Intel® Xeon® Processor 5000 Sequence datasheet are different than those published here, the Intel® Xeon® Processor 5000 Sequence datasheet values supersede these and should be used.

9.2.2 Power Supply DC Output Requirements

This section is for reference purposes only. Its intent is to provide guidance to system architects planning to use the Intel® Server Board S5400SF in a custom chassis for which a power supply is to be determined. The contents of this section specify the power supply requirements Intel used to develop a 600 Watt power supply for its 1U server platform. The values used to determine a custom chassis power supply is dependent on the intended system configuration to be supported.

The combined power of all outputs does not exceed the rated output power of the power supply. The power supply must meet both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 84. 600 W Load Ratings

Voltage	Minimum Continuous	Maximum Continuous	Peak
+3.3 V	1.5 A	20 A	
+5 V	1.0 A	24 A	
+12 V1	0.5 A	16 A	18 A
+12 V2	0.5 A	16 A	18 A
+12 V3	0.5 A	16 A	
+12 V4	0.5 A	16 A	
-12 V	0 A	0.5 A	
+5 VSB	0.1 A	3.0 A	3.5 A

Notes:

1. Maximum continuous total DC output power should not exceed 600 W.
2. Peak load on the combined 12 V output should not exceed 49 A.
3. Maximum continuous load on the combined 12 V output should not exceed 44 A.
4. Peak total DC output power should not exceed 650 W.
5. Peak power and current loading should be supported for a minimum of 12 seconds.
6. Combined 3.3 V and 5 V power should not exceed 150 W.

9.2.3 Power-on Loading

The power supply should operate at lighter load conditions when the system first powers on. Under these conditions, the voltage regulation limits are relaxed. The power-on loading and voltage regulation requirements are listed in the following table.

Time duration is 1 second during power on.

Table 85. Power-on Loading Range

Voltage	Minimum Continuous	Maximum Continuous	Peak
+3.3 V	0 A	7 A	
+5 V	0 A	5 A	
+12 V1	Total combined minimum current for 12 V1, 12 V2, 12 V3, and 12 V4 is 0.4 A	5 A	7 A
+12 V2		5 A	7 A
+12 V3		6 A	
+12 V4		5 A	
-12 V	0 A	0.5 A	
+5 VSB	0.1 A	3.0 A	3.5 A

9.2.4 Grounding

The grounds of the power supply output connector pins provide the power return path. The output connector ground pins should be connected to safety ground (power supply enclosure). This grounding is well designed to ensure passing the maximum allowed common mode noise levels.

The power supply is provided with a reliable protective earth ground. All secondary circuits are connected to protective earth ground. Resistance of the ground returns to chassis does not exceed 1.0 m□. This path may be used to carry DC current.

9.2.5 Standby Outputs

The 5 VSB output is present when an AC input greater than the power supply turn-on voltage is applied.

9.2.6 Remote Sense

The power supply has remote sense return (ReturnS) to regulate out ground drops for all output voltages: +3.3 V, +5 V, +12 V1, +12 V2, +12 V3, -12 V, and 5 VSB. The power supply uses remote sense (3.3 VS) to regulate out drops in the system for the +3.3 V output.

The +5 V, +12 V1, +12 V2, +12 V3, –12 V and 5 VSB outputs only use remote sense referenced to the ReturnS signal. The remote sense input impedance to the power supply must be greater than 200 □ on 3.3 VS and 5 VS. This is the value of the resistor connecting the remote sense to the output voltage internal to the power supply.

The remote sense must be able to regulate out a minimum of a 200 mV drop on the +3.3 V output. The remote sense return (ReturnS) must be able to regulate out a minimum of a 200 mV drop in the power ground return. The current in any remote sense line shall be less than 5 mA to prevent voltage sensing errors.

The power supply must operate within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

9.2.7 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise.

Table 86. Voltage Regulation Limits

Parameter	Tolerance	Minimum	Normal	Maximum	Units
+ 3.3 V	- 5%/+5%	+3.14	+3.30	+3.46	V_{rms}
+ 5 V	- 5%/+5%	+4.75	+5.00	+5.25	V_{rms}
+ 12 V1,2,3,4	- 5%/+5%	+11.40	+12.00	+12.60	V_{rms}
- 12 V	- 10%/+10%	-10.80	-12.00	-13.20	V_{rms}
+ 5 VSB	- 5%/+5%	+4.75	+5.00	+5.25	V_{rms}

9.2.8 Dynamic Loading

The output voltages remain within limits for the step loading and capacitive loading specified in the following table. The load transient repetition rate is tested between 50 Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The step load may occur anywhere within the minimum load to the maximum load conditions.

Table 87. Transient Load Requirements

Output	Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load
+3.3 V	5.0 A	0.25 A/ sec	250 F
+5 V	6.0 A	0.25 A/ sec	400 F
12 V1 +12 V2 + 12 V3 +12 V4	28.0 A	0.25 A/ sec	2200 F [1,2]
+5 VSB	0.5 A	0.25 A/ sec	20 F

Notes:
1. Step loads on each 12 V output may happen simultaneously.
2. The +12 V should be tested with 2200 F evenly split between the four +12 V rails.

9.2.9 Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 88. Capacitive Loading Conditions

Output	Minimum	Maximum	Units
+3.3V	250	6,800	F
+5V	400	4,700	F
+12V1,2,3,4	500 each	11,000	F
-12V	1	350	F
+5VSB	20	350	F

9.2.10 Closed-Loop Stability

The power supply is unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of 45 degrees phase margin and -10dB-gain margin is required. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

9.2.11 Common Mode Noise

The common mode noise on any output does not exceed 350 mV pk-pk over the frequency band of 10 Hz to 30 MHz.

1. The measurement is made across a 100 Ω resistor between each of the DC outputs, including ground, at the DC power connector and chassis ground (power subsystem enclosure).

2. The test setup uses an FET probe such as Tektronix* model P6046 or equivalent.

9.2.12 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in the following table. This is measured over a bandwidth of 0 Hz to 20 MHz at the power supply output connectors. A 10 □F tantalum capacitor in parallel with a 0.1 □F ceramic capacitor are placed at the point of measurement.

Table 89. Ripple and Noise

+3.3 V	+5 V	+12 V1/2/3/4	-12 V	+5 VSB
50 mVp-p	50 mVp-p	120 mVp-p	120 mVp-p	50 mVp-p

9.2.13 Soft Starting

The power supply contains a control circuit that provides a monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions. The rise time of 5 VSB is from 1.0 ms to 25 ms and the turn on/off is monotonic.

9.2.14 Timing Requirements

The timing requirements for the power supply operation are as follows:

- The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70 ms, except for 5 VSB, in which case it is allowed to rise from 1.0 to 25 ms.
- The +3.3 V, +5 V and +12 V output voltages should start to rise approximately at the same time.
- All outputs must rise monotonically.
- The +5 V output needs to be greater than the +3.3 V output during any point of the voltage rise.
- The +5 V output must never be greater than the +3.3 V output by more than 2.25 V.
- Each output voltage should reach regulation within 50 ms (T_{vout_on}) of each other during turn on of the power supply.
- Each output voltage should fall out of regulation within 400 msec (T_{vout_off}) of each other during turn off.

Figure 52 and Figure 53 show the timing requirements for the power supply being turned on and off via the AC input with PSON held low, and the PSON signal with the AC input applied.

Table 90. Output Voltage Timing

Item	Description	Minimum	Maximum	Units
T_{vout_rise}	Output voltage rise time from each main output.	5.0	70 [1]	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		700	msec

Note:

1. The 5VSB output voltage rise time should be from 1.0 ms to 25.0 ms.

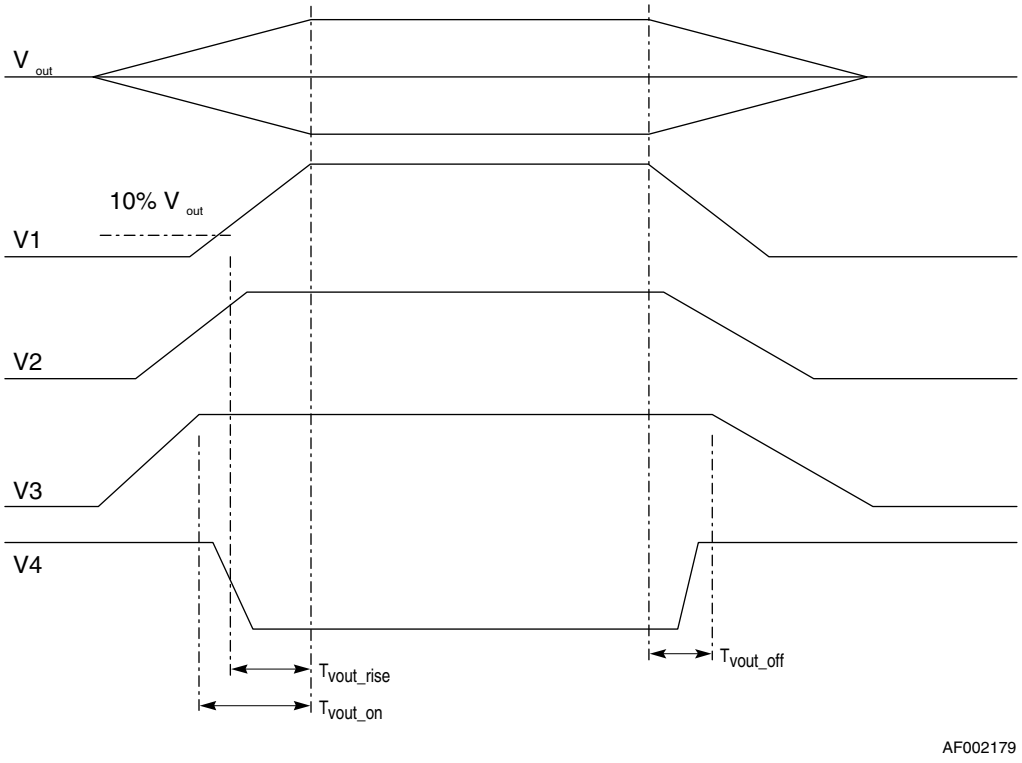


Figure 52. Output Voltage Timing

Table 91. Turn On/Off Timing

Item	Description	Minimum	Maximum	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5 VSB being within regulation.		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Duration for which all output voltages stay within regulation after loss of AC. Measured at 60% of maximum load.	21		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK. Measured at 60% of maximum load.	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# de-active to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3 V, 5 V, 12 V, -12 V) dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec
T_{5VSB_holdup}	Duration for which the 5 VSB output voltage stays within regulation after loss of AC.	70		msec

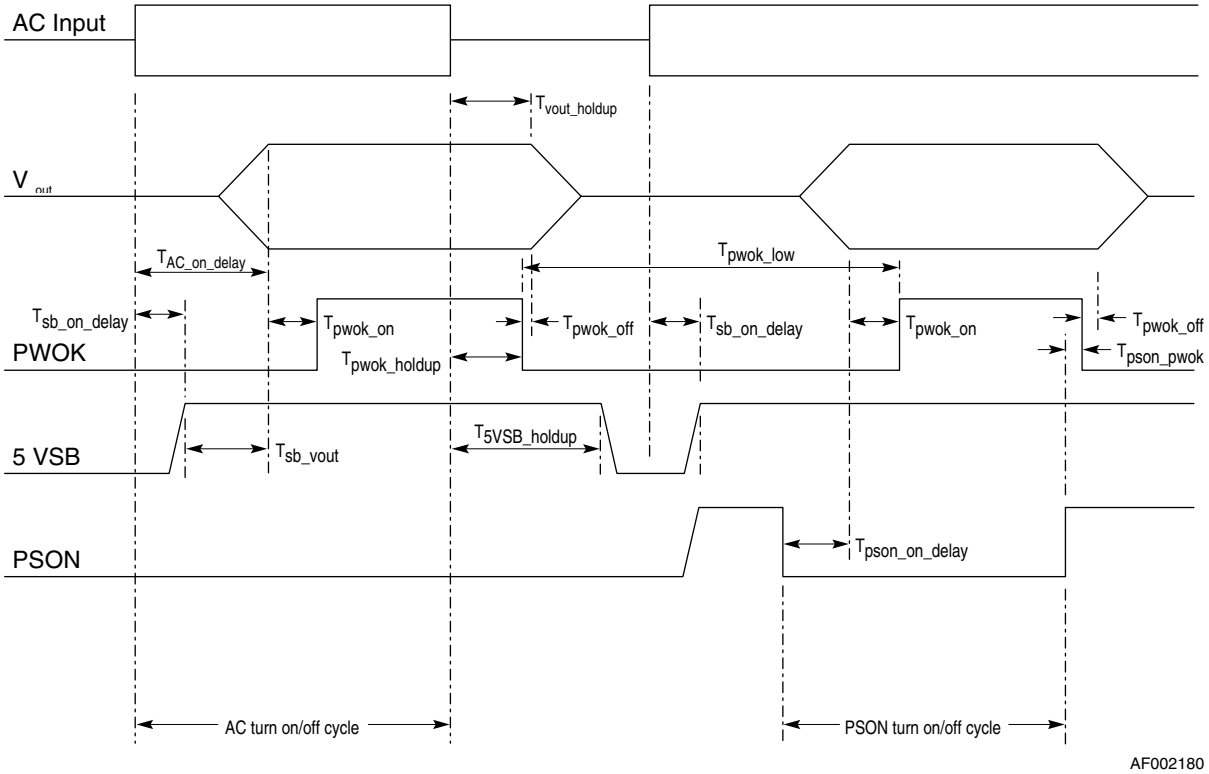


Figure 53. Turn On/Off Timing (Power Supply Signals)

9.2.15 Residual Voltage Immunity in Standby Mode

The power supply is immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500 mV. There is no additional heat generated, or stress of any internal components with this voltage applied to any individual output and all outputs simultaneously. It also does not trip the power supply protection circuits during turn on.

Residual voltage at the power supply outputs for a no-load condition does not exceed 100 mV when AC voltage is applied and the PSON# signal is de-asserted.

10. Regulatory and Certification Information

10.1 Product Regulatory Compliance

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation. This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

10.1.1 Product Safety Compliance

The server board complies with the following safety requirements:

- UL 60950 Recognition (USA)
- CE Declaration to EU Low Voltage Directive 93/68/EEC (Europe – EN60950)
- IEC60950 (International)
- CB Certificate and Report, IEC60950 (report to include all country national deviations)
- CSA 60950 Certification (Canada) or cUL

10.1.2 Product EMC Compliance – Class A Compliance

Note: This product requires complying with Class A EMC requirements.

- FCC – Part 15 Emissions (USA) Verification
- CISPR 22 – Emissions (International)
- EN55022 - Emissions (Europe)
- EN61000-4-2 – ESD (Europe)

10.1.3 Certifications/Registrations/Declarations

- UL Certification (US/Canada)
- CB Certification (International)
- CE Declaration of Conformity (CENELEC Europe)
- FCC/ICES-003 Class A Attestation (USA/Canada)
- C-Tick Declaration of Conformity (Australia)
- MED Declaration of Conformity (New Zealand)
- BSMI Declaration (Taiwan)
- RRL Certification (Korea)

10.1.4 Product Ecology Requirements

Intel has a system in place to restrict the use of banned substances in accordance with world wide product ecology regulatory requirements. Suppliers Declarations of Conformity to the banned substances must be obtained from all suppliers, and a Material Declaration Data Sheet

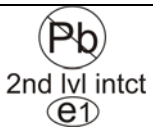
(MDDS) must be produced to illustrate compliance. Due verification of random materials is required as a screening/audit to verify suppliers declarations.

The server board complies with the following ecology regulatory requirements:

- All materials, parts and subassemblies must not contain restricted materials as defined in Intel's Environmental Product Content Specification of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm.
- Europe - European Directive 2002/95/EC - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below.
- Quantity limit of 0.1% by mass (1000 PPM) for Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE)
- Quantity limit of 0.01% by mass (100 PPM) for Cadmium
- China RoHS
- All plastic parts that weigh >25 gm shall be marked with the ISO11469 requirements for recycling. Example >PC/ABS<
- EU Packaging Directive
- German Green Dot
- Japan Recycling

10.1.5 Product Regulatory Compliance Markings

Regulatory Compliance	Region	Marking
UL Mark	USA/Canada	c UL us E139761
CE Mark	Europe	CE
EMC Mark	Canada	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A
BSMI Marking	Taiwan	D33025
		警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策
Ctick Marking	Australia/New Zealand	N232
RRL MIC Mark	Korea	MIC 인증번호: CPU-X38ML (A)
Country of Origin Marking (Marked on packaging label)	Exporting Requirements	Made in xxxxx

Regulatory Compliance	Region	Marking
PB Free Marking	Environmental Requirements	
China RoHS Marking	China	
China Recycling Package Marking (Marked on packaging label)	China	
Other Recycling Package Marking (Marked on packaging label)	Environmental Requirements	

10.2 Electromagnetic Compatibility Notices

10.2.1 FCC (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by taking one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class A or B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

10.2.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe B prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:
This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

10.2.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

10.2.4 VCCI (Japan)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

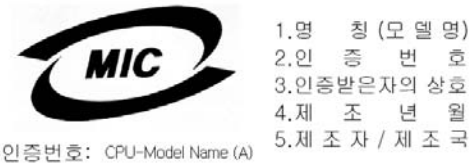
English translation of the notice above:
This is a Class B product based on the standard of the Voluntary Control Council for Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

10.2.5 Taiwan Declaration of Conformity (BSMI)

警告使用者：
這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策

The BSMI Certification Marking and EMC warning is located on the outside rear area of the product.

10.2.5.1 Korean Compliance (RRL)



English translation of the notice above:

1. Type of Equipment (Model Name): On License and Product
2. Certification No.: On RRL certificate. Obtain certificate from local Intel representative
3. Name of Certification Recipient: Intel Corporation
4. Date of Manufacturer: Refer to date code on product
5. Manufacturer/Nation: Intel Corporation/Refer to country of origin marked on product

Appendix A: Integration and Usage Tips

- When adding or removing components or peripherals from the server board, AC power must be removed. With AC power plugged into the server board, 5-volt standby is still present even though the server board is powered off.
- Processors must be installed in order. CPU 1 is located near the edge of the server board and must be populated to operate the board.
- On the back edge of the server board are four diagnostic LEDs, which display a sequence of red, green, or amber POST codes during the boot process. If the server board hangs during POST, the LEDs display the last POST event in process before the server board hung.
- Only Fully Buffered DIMMs (FBDIMMs) are supported on this server board. For a list of supported memory for this server board, see the *Intel® Server Board S5400SF Tested Memory List*.
- For a list of Intel supported operating systems, add-in cards, and peripherals for this server board, see the *Intel® Server Board S5400SF Tested Hardware and OS List*.
- For best performance, the number of DIMMs installed should be balanced across both memory branches. For example, a four-DIMM configuration performs better than a two-DIMM configuration and should be installed in DIMM Slots A1, B1, C1, and D1; an eight-DIMM configuration performs better then a six-DIMM configuration.
- 800 MHz FBDIMMs can only be used in a system configured with Intel® Xeon® processors that support a 1600 MHz front-side bus.
- The IDE connector on this server board is NOT a standard 40-pin IDE connector. Instead, this connector has additional 4 power pins over and above the standard 40 I/O pins. The design intent of this connector is to provide support for a slimline optical drive only.
- Removing AC power before performing the CMOS clear operation causes the system to automatically power up and immediately power down after the procedure is followed and AC power is re-applied. Should this occur, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power up the system and proceed to the <F2> BIOS setup utility to reset desired settings.
- Normal Integrated BMC functionality is disabled with the Integrated BMC force update jumper set to the “enabled” position (pins 2-3). The server should never be run with the Integrated BMC force update jumper set in this position and should only be used when the standard firmware update process fails. This jumper should remain in the default (disabled) position (pins 1-2) when the server is running normally.
- When performing the BIOS update procedure, the BIOS select jumper must be set to its default position (pins 2-3).
- To access the embedded EFI shell, boot the system to the BIOS Setup utility by pressing the F2 key when prompted during POST. From the BIOS Setup utility Main menu, tab over to the Boot Manager menu and select EFI Shell.

Appendix B: POST Code Diagnostic LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the given POST code to the POST Code Diagnostic LEDs found on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, the Diagnostic LEDs can be used to identify the last POST process to be executed.

Each POST code is represented by a combination of colors from the four LEDs. The LEDs are capable of displaying three colors: green, red, and amber. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. Each bit in the upper nibble is represented by a red LED and each bit in the lower nibble is represented by a green LED. If both bits are set in the upper and lower nibbles, then both red and green LEDs are lit, resulting in an amber color. If both bits are clear, then the LED is off.

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

- red bits = 1010b = Ah
- green bits = 1100b = Ch

Since the red bits correspond to the upper nibble and the green bits correspond to the lower nibble, the two are concatenated to be ACh.

Table 92: POST Progress Code LED Example

	8h		4h		2h		1h	
LEDs	Red	Green	Red	Green	Red	Green	Red	Green
ACh	1	1	0	1	1	0	0	0
Result	Amber		Green		Red		Off	
	MSB						LSB	

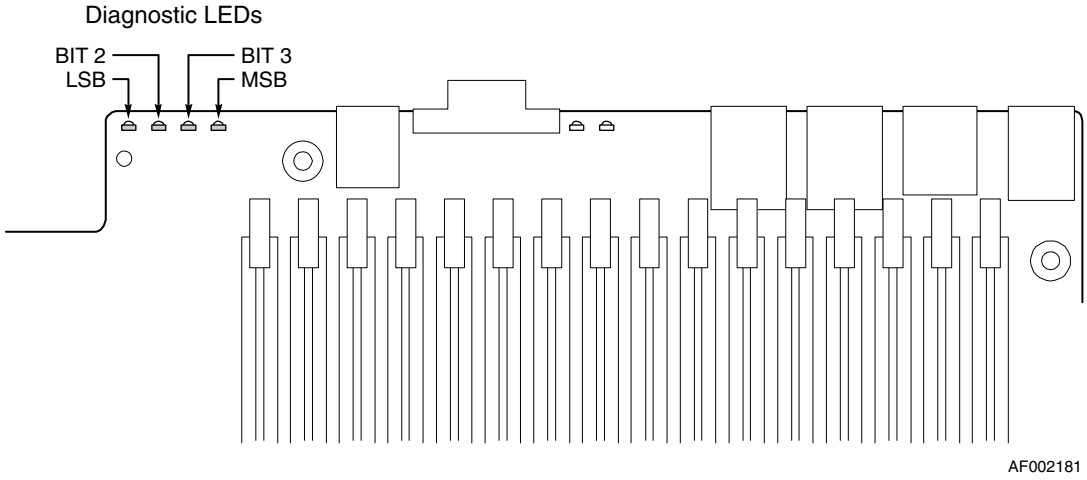


Figure 54. Diagnostic LED Placement Diagram

Table 93. Diagnostic LED POST Code Decoder

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
Host Processor					
0x10h	Off	off	off	R	Power-on initialization of the host processor (bootstrap processor)
0x11h	Off	Off	Off	A	Host processor cache initialization (including AP)
0x12h	Off	Off	G	R	Starting application processor initialization
0x13h	Off	Off	G	A	SMM initialization
Chipset					
0x21h	OFF	OFF	R	G	Initializing a chipset component
Memory					
0x22h	OFF	OFF	A	OFF	Reading configuration data from the memory (SPD on DIMM)
0x23h	OFF	OFF	A	G	Detecting presence of memory
0x24h	OFF	G	R	OFF	Programming timing parameters in the memory controller
0x25h	OFF	G	R	G	Configuring memory parameters in the memory controller
0x26h	OFF	G	A	OFF	Optimizing memory controller settings
0x27h	OFF	G	A	G	Initializing memory, such as ECC init
0x28h	G	OFF	R	OFF	Testing memory
PCI Bus					
0x50h	OFF	R	OFF	R	Enumerating PCI buses
0x51h	OFF	R	OFF	A	Allocating resources to PCI buses
0x52h	OFF	R	G	R	Hot-plug PCI controller initialization
0x53h	OFF	R	G	A	Reserved for PCI bus
0x54h	OFF	A	OFF	R	Reserved for PCI bus
0x55h	OFF	A	OFF	A	Reserved for PCI bus
0x56h	OFF	A	G	R	Reserved for PCI bus
0x57h	OFF	A	G	A	Reserved for PCI bus
USB					
0x58h	G	R	OFF	R	Resetting USB bus
0x59h	G	R	OFF	A	Reserved for USB devices
ATA/ATAPI/SATA					
0x5Ah	G	R	G	R	Resetting PATA/SATA bus and all devices
0x5Bh	G	R	G	A	Reserved for ATA
SMBus					
0x5Ch	G	A	OFF	R	Resetting SMBus
0x5Dh	G	A	OFF	A	Reserved for SMBus
Local Console					
0x70h	OFF	R	R	R	Resetting the video controller (VGA)
0x71h	OFF	R	R	A	Disabling the video controller (VGA)
0x72h	OFF	R	A	R	Enabling the video controller (VGA)
Remote Console					
0x78h	G	R	R	R	Resetting the console controller

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
0x79h	G	R	R	A	Disabling the console controller
0x7Ah	G	R	A	R	Enabling the console controller
Keyboard (PS/2 or USB)					
0x90h	R	OFF	OFF	R	Resetting the keyboard
0x91h	R	OFF	OFF	A	Disabling the keyboard
0x92h	R	OFF	G	R	Detecting the presence of the keyboard
0x93h	R	OFF	G	A	Enabling the keyboard
0x94h	R	G	OFF	R	Clearing keyboard input buffer
0x95h	R	G	OFF	A	Instructing keyboard controller to run Self Test (PS/2 only)
Mouse (PS/2 or USB)					
0x98h	A	OFF	OFF	R	Resetting the mouse
0x99h	A	OFF	OFF	A	Detecting the mouse
0x9Ah	A	OFF	G	R	Detecting the presence of mouse
0x9Bh	A	OFF	G	A	Enabling the mouse
Fixed Media					
0xB0h	R	OFF	R	R	Resetting fixed media device
0xB1h	R	OFF	R	A	Disabling fixed media device
0xB2h	R	OFF	A	R	Detecting presence of a fixed media device (IDE hard drive detection, etc.)
0xB3h	R	OFF	A	A	Enabling/configuring a fixed media device
Removable Media					
0xB8h	A	OFF	R	R	Resetting removable media device
0xB9h	A	OFF	R	A	Disabling removable media device
0xBAh	A	OFF	A	R	Detecting presence of a removable media device (IDE CDROM detection, etc.)
0xBCh	A	G	R	R	Enabling/configuring a removable media device
Boot Device Selection					
0xD0	R	R	OFF	R	Trying boot device selection
0xD1	R	R	OFF	A	Trying boot device selection
0xD2	R	R	G	R	Trying boot device selection
0xD3	R	R	G	A	Trying boot device selection
0xD4	R	A	OFF	R	Trying boot device selection
0xD5	R	A	OFF	A	Trying boot device selection
0xD6	R	A	G	R	Trying boot device selection
0xD7	R	A	G	A	Trying boot device selection
0xD8	A	R	OFF	R	Trying boot device selection
0xD9	A	R	OFF	A	Trying boot device selection
0XDA	A	R	G	R	Trying boot device selection
0xDB	A	R	G	A	Trying boot device selection
0xDC	A	A	OFF	R	Trying boot device selection
0xDE	A	A	G	R	Trying boot device selection

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
0xDF	A	A	G	A	Trying boot device selection
Pre-EFI Initialization (PEI) Core					
0xE0h	R	R	R	OFF	Started dispatching early initialization modules (PEIM)
0xE2h	R	R	A	OFF	Initial memory found, configured, and installed correctly
0xE1h	R	R	R	G	Reserved for initialization module use (PEIM)
0xE3h	R	R	A	G	Reserved for initialization module use (PEIM)
Driver Execution Environment (DXE) Core					
0xE4h	R	A	R	OFF	Entered EFI driver execution phase (DXE)
0xE5h	R	A	R	G	Started dispatching drivers
0xE6h	R	A	A	OFF	Started connecting drivers
DXE Drivers					
0xE7h	R	A	A	G	Waiting for user input
0xE8h	A	R	R	OFF	Checking password
0xE9h	A	R	R	G	Entering the BIOS setup
0xEAh	A	R	A	OFF	Flash Update
0xEEh	A	A	A	OFF	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	A	A	A	G	Unrecoverable boot failure/S3 resume failure
Runtime Phase/EFI Operating System Boot					
0xF4h	R	A	R	R	Entering Sleep state
0xF5h	R	A	R	A	Exiting Sleep state
0xF8h	A	R	R	R	Operating system has requested EFI to close boot services (ExitBootServices ( ) has been called)
0xF9h	A	R	R	A	Operating system has switched to virtual address mode (SetVirtualAddressMap ( ) has been called)
0xFAh	A	R	A	R	Operating system has requested the system to reset (ResetSystem () has been called)
Pre-EFI Initialization Module (PEIM)/Recovery					
0x30h	OFF	OFF	R	R	Crisis recovery has been initiated because of a user request
0x31h	OFF	OFF	R	A	Crisis recovery has been initiated by software (corrupt flash)
0x34h	OFF	G	R	R	Loading crisis recovery capsule
0x35h	OFF	G	R	A	Handing off control to the crisis recovery capsule
0x3Fh	G	G	A	A	Unable to complete crisis recovery.

Appendix C: POST Error Messages and Handling

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware that is being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

- **Minor:** The message is displayed on the screen or in the Error Manager. The system will continue booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.
- **Major:** The message is displayed in the Error Manager screen, and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error, where the user can take immediate corrective action or choose to continue booting.
- **Fatal:** The message is displayed in the Error Manager screen, and an error is logged to the SEL. The system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

Table 94. POST Error Messages and Handling

Error Code	Error Message	Response
12	CMOS date/time not set	Major
141	PCI resource conflict	Major
146	Insufficient memory to shadow PCI ROM	Major
194	CPUID, processor family are different	Fatal
195	Front-side bus mismatch	Major
197	Processor speeds mismatched	Major
5220	CMOS/NVRAM configuration cleared	Major
5221	Passwords cleared by jumper	Major
8110	Processor 01 internal error (IERR) on last boot	Major
8111	Processor 02 internal error (IERR) on last boot	Major
8120	Processor 01 thermal trip error on last boot	Major
8121	Processor 02 thermal trip error on last boot	Major
8130	Processor 01 disabled	Major
8131	Processor 02 disabled	Major
8160	Processor 01 unable to apply BIOS update	Major
8161	Processor 02 unable to apply BIOS update	Major
8170	Processor 01 failed Self Test (BIST).	Major
8171	Processor 02 failed Self Test (BIST).	Major
8190	Watchdog timer failed on last boot	Major
8198	Operating system boot watchdog timer expired on last boot	Major
8300	Integrated Baseboard management controller failed self-test	Major
84F2	Integrated Baseboard management controller failed to respond	Major
84F2	Integrated Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor

Error Code	Error Message	Response
85FD	Memory component could not be configured in the selected RAS mode.	Major
8520	DIMM_A1 failed Self Test (BIST).	Major
8521	DIMM_A2 failed Self Test (BIST).	Major
8522	DIMM_A3 failed Self Test (BIST).	Major
8523	DIMM_A4 failed Self Test (BIST).	Major
8524	DIMM_B1 failed Self Test (BIST).	Major
8525	DIMM_B2 failed Self Test (BIST).	Major
8526	DIMM_B3 failed Self Test (BIST).	Major
8527	DIMM_B4 failed Self Test (BIST).	Major
8528	DIMM_C1 failed Self Test (BIST).	Major
8529	DIMM_C2 failed Self Test (BIST).	Major
852A	DIMM_C3 failed Self Test (BIST).	Major
852B	DIMM_C4 failed Self Test (BIST).	Major
852C	DIMM_D1 failed Self Test (BIST).	Major
852D	DIMM_D2 failed Self Test (BIST).	Major
852E	DIMM_D3 failed Self Test (BIST).	Major
852F	DIMM_D4 failed Self Test (BIST).	Major
8580	DIMM_A1 Correctable ECC error encountered.	Minor/Major after 10
8581	DIMM_A2 Correctable ECC error encountered.	Minor/Major after 10
8582	DIMM_A3 Correctable ECC error encountered.	Minor/Major after 10
8583	DIMM_A4 Correctable ECC error encountered.	Minor/Major after 10
8584	DIMM_B1 Correctable ECC error encountered.	Minor/Major after 10
8585	DIMM_B2 Correctable ECC error encountered.	Minor/Major after 10
8586	DIMM_B3 Correctable ECC error encountered.	Minor/Major after 10
8587	DIMM_B4 Correctable ECC error encountered.	Minor/Major after 10
8588	DIMM_C1 Correctable ECC error encountered.	Minor/Major after 10
8589	DIMM_C2 Correctable ECC error encountered.	Minor/Major after 10
858A	DIMM_C3 Correctable ECC error encountered.	Minor/Major after 10
858B	DIMM_C4 Correctable ECC error encountered.	Minor/Major after 10
858C	DIMM_D1 Correctable ECC error encountered.	Minor/Major after 10
858D	DIMM_D2 Correctable ECC error encountered.	Minor/Major after 10
858E	DIMM_D3 Correctable ECC error encountered.	Minor/Major after 10
858F	DIMM_D4 Correctable ECC error encountered.	Minor/Major after 10
85A0	DIMM_A1 Uncorrectable ECC error encountered.	Major
85A1	DIMM_A2 Uncorrectable ECC error encountered.	Major
85A2	DIMM_A3 Uncorrectable ECC error encountered.	Major
85A3	DIMM_A4 Uncorrectable ECC error encountered.	Major
85A4	DIMM_B1 Uncorrectable ECC error encountered.	Major
85A5	DIMM_B2 Uncorrectable ECC error encountered.	Major
85A6	DIMM_B3 Uncorrectable ECC error encountered.	Major
85A7	DIMM_B4 Uncorrectable ECC error encountered.	Major
85A8	DIMM_C1 Uncorrectable ECC error encountered.	Major
85A9	DIMM_C2 Uncorrectable ECC error encountered.	Major
85AA	DIMM_C3 Uncorrectable ECC error encountered.	Major
85AB	DIMM_C4 Uncorrectable ECC error encountered.	Major
85AC	DIMM_D1 Uncorrectable ECC error encountered.	Major
85AD	DIMM_D2 Uncorrectable ECC error encountered.	Major
85AE	DIMM_D3 Uncorrectable ECC error encountered.	Major
85AF	DIMM_D4 Uncorrectable ECC error encountered.	Major
8601	Override jumper is set to force boot from lower alternate BIOS bank of flash ROM	Minor
8602	WatchDog timer expired (secondary BIOS may be bad!)	Minor
8603	Secondary BIOS checksum fail	Minor
8604	Chipset Reclaim of non critical variables complete.	Minor
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major

POST Error Beep Codes

The following table lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user visible code on POST progress LEDs.

Table 95. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error		System halted because a fatal error related to the memory was detected.
6	BIOS rolling back error		The system has detected a corrupted BIOS in the flash part, and is rolling back to the last good BIOS.

The Integrated BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time the problem is discovered, such as on each power-up attempt, but are not sounded continuously. Codes that are common across all Intel® Server Boards and systems that use the Intel® 5400 Chipset are listed in the following table. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 96. Integrated BMC Beep Codes

Code	Reason for Beep	Associated Sensors	Supported?
1-5-2-1	CPU: Empty slot/population error – Processor slot 1 is not populated.	CPU Population Error	Yes
1-5-2-2	CPU: No processors (terminators only)	N/A	No
1-5-2-3	CPU: Configuration error (e.g., VID mismatch)	N/A	No
1-5-2-4	CPU: Configuration error (e.g., BSEL mismatch)	N/A	No
1-5-4-2	Power fault: DC power unexpectedly lost (power good dropout)	Power Unit – power unit failure offset	Yes
1-5-4-3	Chipset control failure	N/A	No
1-5-4-4	Power control fault	Power Unit – soft power control failure offset	Yes

Appendix D: EFI Shell Commands

The embedded EFI Shell must be accessed when running any of the system update utilities or Platform Confidence Test (PCT). The embedded EFI Shell can be accessed by booting the system and entering the BIOS Setup utility (F2) during POST. From the BIOS Setup utility Main menu, tab over to the Boot Manager menu and select EFI Shell.

The following is a list of supported EFI Shell commands. Most shell commands can be invoked from the EFI shell prompt. However there are several commands that are only available for use from within batch script files. The following table lists all the commands and provides more details on each command. The “Batch-only” column indicates if the command is only available from within script files.

Table 97. EFI Shell Commands

Command	Batch-only	Description
alias	No	Displays, creates, or deletes aliases in the EFI shell
attrib	No	Displays or changes the attributes of files or directories
bcfg	No	Displays/modifies the driver/boot configuration
break	No	Executes a debugger break point
cd	No	Displays or changes the current directory
cls	No	Clears the standard output with an optional background color
comp	No	Compares the contents of two files
connect	No	Binds an EFI driver to a device and starts the driver
cp	No	Copies one or more files/directories to another location
date	No	Displays the current date or sets the date in the system
dblk	No	Displays the contents of blocks from a block device
devices	No	Displays the list of devices being managed by EFI drivers
devtree	No	Displays the tree of devices that follow the EFI Driver Model
dh	No	Displays the handles in the EFI environment
disconnect	No	Disconnects one or more drivers from a device
dmem	No	Displays the contents of memory
dmpstore	No	Displays all NVRAM variables
drivers	No	Displays the list of drivers that follow the EFI Driver Model
drvcfg	No	Invokes the Driver Configuration Protocol
drvdiag	No	Invokes the Driver Diagnostics Protocol
echo	No	Displays messages or turns command echoing on or off
edit	No	Edits an ASCII or UNICODE file in full screen.
EfiCompress	No	Compress a file
EfiDecompress	No	Decompress a file
err	No	Displays or changes the error level

Command	Batch-only	Description
exit	No	Exits the EFI Shell
for/endfor	Yes	Executes commands for each item in a set of items
getmtc	No	Displays the current monotonic counter value
goto	Yes	Makes batch file execution jump to another location
guid	No	Displays all the GUIDs in the EFI environment
help	No	Displays commands list or verbose help of a command
hexedit	No	Edits with hex mode in full screen
If/endif	Yes	Executes commands in specified conditions
load	No	Loads EFI drivers
LoadBmp	No	Displays a Bitmap file onto the screen
LoadPciRom	No	Loads a PCI Option ROM image from a file
ls	No	Displays a list of files and subdirectories in a directory
map	No	Displays or defines mappings
memmap	No	Displays the memory map
mkdir	No	Creates one or more directories
mm	No	Displays or modifies MEM/IO/PCI
mode	No	Displays or changes the mode of the console output device
mount	No	Mounts a file system on a block device
mv	No	Moves one or more files/directories to destination
OpenInfo	No	Displays the protocols on a handle and the agents
pause	No	Prints a message and suspends for keyboard input
pci	No	Displays PCI devices or PCI function configuration space
reconnect	No	Reconnects one or more drivers from a device
reset	No	Resets the system
rm	No	Deletes one or more files or directories
set	No	Displays, creates, changes or deletes EFI environment variables
setsize	No	Sets the size of a file
stall	No	Stalls the processor for some microseconds
time	No	Displays the current time or sets the time of the system
touch	No	Sets the time and date of a file to the current time and date
type	No	Displays the contents of a file
unload	No	Unloads a protocol image
ver	No	Displays the version information
vol	No	Displays volume information of the file system

Appendix E: Supported Intel® Server Chassis

The Intel® Server Board S5400SF is supported in the following Intel high-density rack mount server chassis: Intel® Server Chassis SR1560.

More details can be found by referencing the *Intel® Server System SR1560SF Technical Product Specification* (TPS).

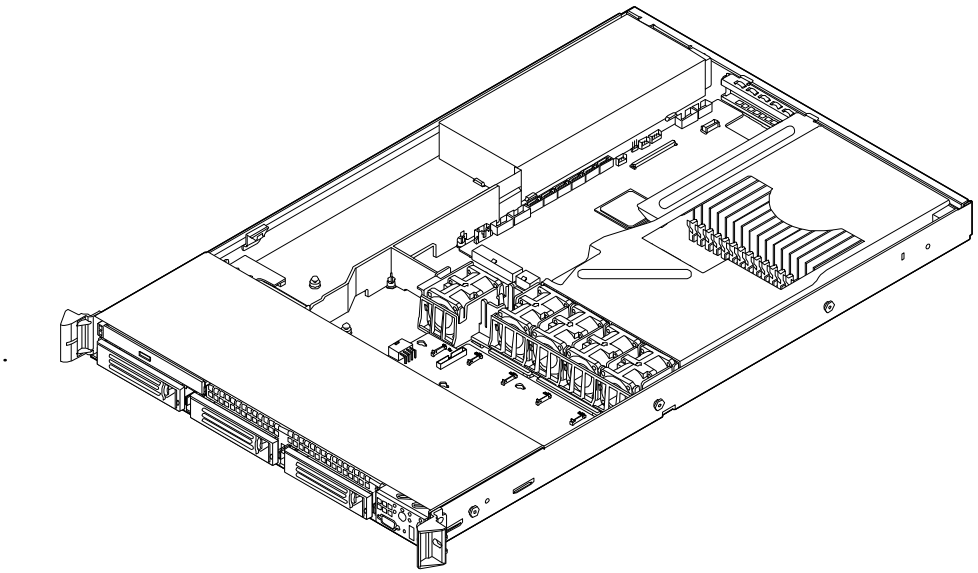


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Figure 55. 1U – Intel® Server System SR1560SF Overview

Intel® Server System SR1560SF feature set:

- 1U rack mount server chassis
- 600 Watt non-redundant power supply
- Fixed mount or hot-swap hard drive configuration options
  - Option to support up to two fixed mount SATA hard disk drives
  - Options to support up to three hot swap SAS or SATA hard disk drives
- One PCI Express* Gen 2 riser card with one x16 PCI Express* slot
- Drive bay to support one slimline optical drive
- Five non-redundant dual-rotor high-speed managed system fans

Appendix F: 1U PCI Express* Gen 2 Riser Card

As used in the Intel® Server System SR1560SF, Intel makes a 1U PCI Express* Gen 2 x16 riser card available for this server board. The following mechanical drawing is for reference purposes only.

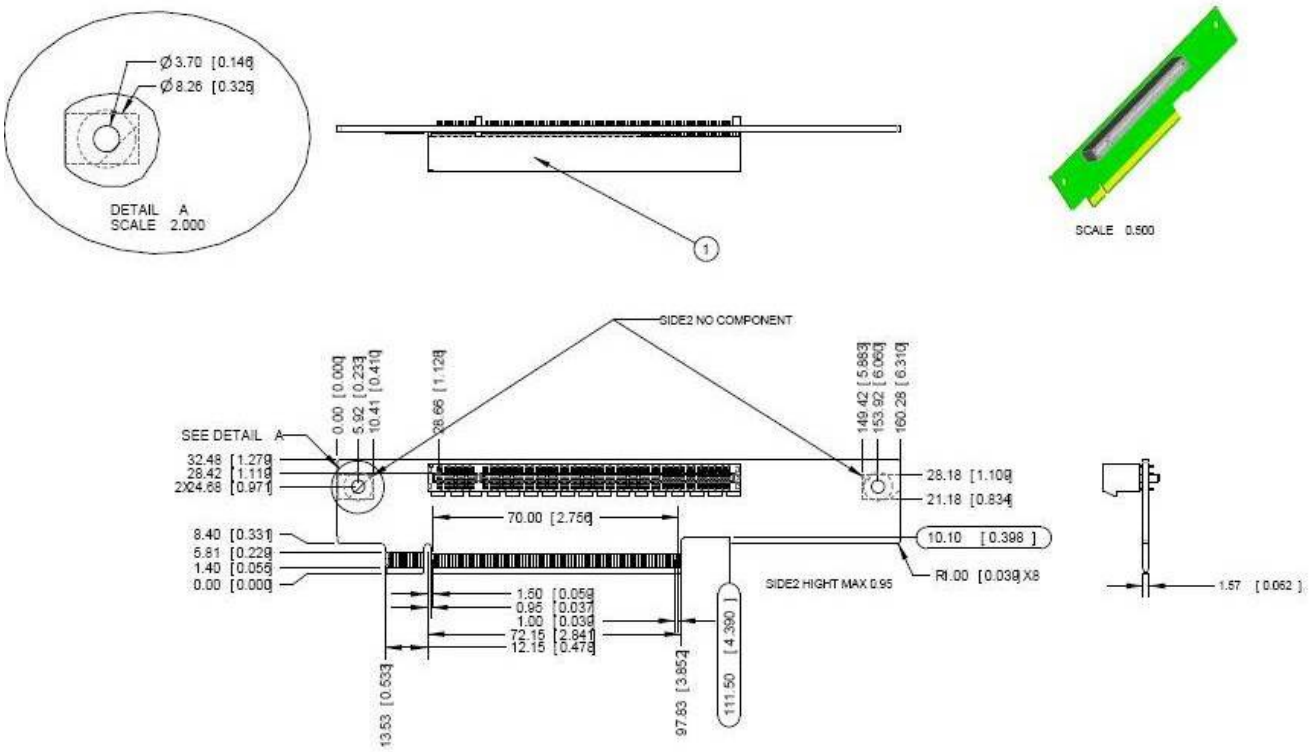

Figure 56. 1U PCI Express* Gen 2 Riser Card Mechanical Drawing

Glossary

This appendix contains important terms used in this document. For ease of use, numeric entries are listed first (e.g., “82460GX”) followed by alpha entries (e.g., “AGP 4x”). Acronyms are followed by non-acronyms.

Term	Definition
ACPI	Advanced Configuration and Power Interface
AES	Advanced Encryption Standard
AL	Additive latency
AMB	Advanced Memory Buffer
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
ATA	Advanced Technology Attachment
ATAPI	Advanced Technology Attachment Packet Interface
BEV	Bootstrap Entry Vector
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
BRD	Buffer read delay
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
Byte	8-bit quantity.
CAS	Content Addressable Storage
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CL	CAS latency
CLTT	Closed Loop Thermal Throttling
CMOS	Complementary Metal-oxide Semiconductor In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
CRC	Cyclic Redundancy Code
CRT	Cathode Ray Tube
DHCP	Dynamic Host Configuration Protocol
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2-E	Enterprise South Bridge 2

Term	Definition
ESI	Enterprise South Bridge Interface
FBD	Fully Buffered DIMM
FCBGA	Flip Chip Ball Grid Array
FMB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FRUSDR	Field Replaceable Unit and Sensor Data Record
FSB	Front-Side Bus
GB	1024 MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
GUID	Globally Unique Identifier
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IDE	Integrated
IERR	Internal Error
IFB	I/O and Firmware Bridge
INTR	Interrupt
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
IRQ	Interrupt Request
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
MDDS	Material Declaration Data Sheet

Term	Definition
MRC	Memory Reference Code
ms	milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Non-maskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
OLTT	Open Loop Throughput Throttling
PAE	Physical Address Extension
PATA	Parallel ATA
PCT	Platform Confidence Test
PECI	Platform Environmental Control Interface
PEF	Platform Event Filtering
PEP	Platform Event Paging
PET	Platform event trap
PIA	Platform Information Area (This feature configures the firmware for the platform hardware)
PIC	Programmable Interrupt Controller
PIO	Programmable Input/Output
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PROM	Programmable Read-Only Memory
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RAMDAC	Random Access Memory Digital-to-Analog Converter
RAS	Reliability, Availability, and Serviceability
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
RMM2	Remote Management Module – Second generation
RMM2 NIC	Remote Management Module – Second generation dedicated management NIC
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SCI	System Control Interrupt
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SF	Snoop Filter
SHA1	Secure Hash Algorithm Version 1.0

Term	Definition
SIO	Server Input/Output
SMB	Server Management BIOS
SMBus	System Management Bus
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt)
SMM	Server Management Mode
SMS	Server Management Software
SMTP	Simple Mail Transfer Protocol
SNMP	Simple Network Management Protocol
SRAM	Static Random Access Memory
SPD	Serial Presence Detect
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinate
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity
ZIF	Zero Insertion Force

Reference Documents

See the following documents for additional information:

- *Intel® 5400 Series Server Board BIOS External Product Specification*
- *Intel® 5400 Series Server Board Integrated Baseboard Management Controller External Product Specification*
- *Intel® 5400 Memory Controller Hub External Design Specification*
- *Intel® Enterprise South Bridge 2 (ESB2-E) External Design Specification*
- *Intel® Remote Management Module 2 Technical Product Specification*
- TEB 2.11 – Thin Electronics Bay (1U/2U Rack Optimized)
- EPS 1U Entry Level Power Supply – 1U non-redundant – Intel® 5400 Chipset Server Board Family
- Design and Evaluation of Snoop Filters for Web Servers (Intel Corporation)