White Paper

Altera® FPGAs
Soft Embedded Processors

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An Intel Company

Altera® Extends its Multi-Platform RISC-V Support by Partnering with Prominent RISC-V Tools Provider, Ashling

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Why Altera?

- Pioneer in the processor industry with a wide portfolio including Intel® x86 processors, FPGAs, RISC-V IP
- Nios® V processor, Altera's next generation RISC-V processor for Altera® FPGAs provides increased performance and access to an expansive and growing ecosystem
- Intel Foundry Services (IFS) is the only foundry to offer IP optimized for all three of the industry's leading ISAs: Intel x86, Arm, and RISC-V

Why Ashling?

- Leading, global provider of Embedded Development Tools & Services
- Robust RISC-V IDE, Compiler, and Unified Debugger
- Supports Agilex™, Stratix® 10, Arria® 10, Cyclone® 10 GX devices, and more

Executive Summary

In the case of FPGAs, one or more soft-core processors can be instantiated in the device's programmable fabric, allowing designers to add programmable microcontroller and/or microprocessor cores to their designs.

The performance of FPGA-based soft processors is becoming increasingly important in embedded markets. Embedded applications in markets like industrial and military that run complex workloads need the ability to have multiple high-performance soft processors that support easy-to-use tools to accelerate software development.

RISC-V meets the performance needs of these markets as well as providing a path to consistent technology block or intellectual property (IP) block upgrades and access to industry-leading tools. The growing RISC-V ecosystem also brings broad software compatibility, better tool and compiler support, and a standard debug environment.

By migrating the soft processor used in Altera® FPGAs to an open standard—and by partnering with prominent RISC-V solutions provider Ashling—Altera provides users with access to a diverse ecosystem of modern Integrated Development Environments (IDEs), compilers, debuggers, and operating systems.

Altera RISC-V Strategy

Altera creates high-capacity and high-performance FPGAs. These devices offer a wide variety of options, including configurable embedded SRAM, high-speed transceivers, high-speed input/outputs (I/Os), logic blocks, and routing. Built-in IP-blocks combined with outstanding software tools lower FPGA development time, power, and cost.

In February 2022, Altera became an active member of the RISC-V International global open hardware standards organization. The open RISC-V ecosystem provides open modular building blocks that are essential for modern computing. In joining RISC-V, Altera has taken on leadership activities, expanding the RISC-V ecosystem potential for all industry stakeholders.

As part of its RISC-V strategy, Altera is joining forces with leading partners in the RISC-V ecosystem, including Ashling, Andes Technology, Esperanto Technologies, SiFive, and Ventana Micro Systems.

Altera is planning investments that will strengthen the RISC-V ecosystem as well as help drive further adoption of RISC-V. These investments will help disruptive RISC-V companies innovate faster through Altera by collaborating on the following activities and more:

- Technology co-optimization
- Prioritizing wafer shuttles
- Supporting customer designs
- Building development boards

Evolving Software Infrastructure

For example, Altera plans to offer a range of validated RISC-V-based cores that are performance-optimized for different market segments. By partnering with leading providers, Altera will optimize IP blocks for Altera process technologies to ensure that RISC-V runs best on Intel® silicon across all types of cores, from embedded to high performance. Three types of RISC-V offerings will be made available:

- Partner products manufactured on Intel technologies.
- RISC-V cores licensed as differentiated IP blocks.
- RISC-V chiplet building blocks that leverage Altera's advanced packaging and high-speed chip-to-chip interfaces.

Altera's investment in RISC-V will enable acceleration of the development of open RISC-V blocks and other deliverables together with the RISC-V community. Additionally, Intel Foundry Services (IFS) will sponsor an open-source software development platform that allows for freedom in experimentation, including partners across the ecosystem, universities, and consortia. This IFS strategy will provide a broad range of technology optimized for Altera process technologies. IFS is the only foundry to offer technology optimized for all three of the industry's leading ISAs: x86, Arm, and RISC-V, and Altera has already seen strong demand from foundry customers to support more RISC-V IP block offerings.

Value of RISC-V for FPGA Customers

RISC-V is an open-source hardware ISA that began in 2010. Unlike most other ISAs, RISC-V is provided under open-source licenses. The RISC-V instruction set specification defines both 32-bit and 64-bit address space variants. The instruction set is variable-width and extensible and is designed to address a wide range of use cases.

In addition to being an open-source ISA, RISC-V's success can be attributed to the fact it has been designed from the ground up for modularity, extensibility, stability, efficiency, and performance. RISC-V is a "clean-slate" design with no legacy-based or backwards-compatibility-based limitations or restrictions. This allows RISC-V to pave the way for the future of open computing design freedom and innovation. Thanks to the involvement of multiple participants, RISC-V is fostering many innovations with multiple open-source architecture implementations available today.

Commercial enterprises require ISAs to be stable for products that are deployed for many years. To address this issue, the RISC-V Foundation was formed in 2015 to own, maintain, and publish RISC-V's definition. To better reflect its role, this nonprofit organization changed its name to RISC-V International in 2020.

RISC-V is seeing exponential growth. As reported by RISC-V International[1], "RISC-V commitments and investments continue to skyrocket with RISC-V membership growing 130% in 2021 to 2,478 members including 18 Premier level members." With billions of chips already deployed, RISC-V has seen widespread commercial adoption across industries and implementations, from embedded automotive to hyperscale artificial intelligence (AI), from 5G to high-performance computing (HPC), and beyond.

The open-source nature of RISC-V is enabling a new era of processor innovation through open standard collaboration. Multiple participants are fostering implementation innovation, resulting in the rapid emergence of a broad, open-source ecosystem that includes sophisticated hardware design and verification tools, a rich suite of software development tools, operating system (OS), and real-time operating system (RTOS) ports, etc. The proliferation of hard-core and soft-core RISC-V processors greatly facilitates the porting of applications between different implementations and the maintaining of applications over time. The world is poised to see an explosion of applications that are developed from the ground up to take full advantage of the RISC-V architecture.

In the case of FPGAs, one or more soft-core processors can be instantiated in the device's programmable fabric, thereby allowing designers to add programmable microcontroller and/or microprocessor cores to their designs. Similarly, with respect to Altera's system-on-chip (SoC) FPGAs in which one, two, or four Arm hard-core processors are implemented directly in the silicon, additional soft-core processors can be instantiated in the device's programmable fabric if required.

Since its introduction in 2004, Altera's 32-bit Nios® II processor has been the soft-core processor of choice for designers using Altera's FPGAs and SoC FPGAs. Over the years, the Nios II processor has accumulated a large ecosystem of developers, tools, software, and software IP-blocks.

Now, Altera has launched the next generation of soft-core processors for Altera FPGAs, the Nios V processor, which is based on the open-source RISC-V ISA. The first member of the Nios V processor family is the Nios V/m microcontroller. Altera plans to add additional Nios V processor variants, including a general-purpose version, an application-class version, and a Linux-capable version, where the latter will be a 64-bit processor capable of running a Linux kernel. Altera will also be adding support for a wide range of operating systems, including Zephyr, FreeRTOS, and Linux.

Leveraging RISC-V in Nios processors promises to dramatically expand the extensive, existing Nios ecosystem, delivering even greater flexibility and performance to developers of FPGA-based systems. Nios V processors use the same simple design flow as Nios II processors and are available in the Quartus® Prime Pro Edition Software. Of particular interest to the creators of existing Nios II-processor based designs is that they can be quickly and easily ported to the Nios V processor.

Nios V soft-core processors offer increased performance compared to existing soft-core processors due to architectural upgrades within the RISC-V ISA. Another key advantage of RISC-V is software portability and stability. For example, developers can start a design in an FPGA with a soft-core version of a RISC-V, and any software written to run on the initial soft RISC-V core can be run on any other RISC-V core in the future.

Another very important RISC-V benefit has been a rapid emergence of a broad, open-source ecosystem, including hardware design and verification tools, software development tools (e.g., compilers, debuggers), OS, RTOS ports, and more.

One example of Altera's commitment to RISC-V has been to provide a complete open-source tools solution to its FPGA customers by partnering with prominent RISC-V tool vendor and RISC-V International member, Ashling, for their ***RiscFree* IDE*** and Unified Debugger.

Value of RiscFree for FPGA Customers

Today's SoC and System-in-Package (SiP) designs are becoming increasingly complex as chip designers pack more and more features onto a single device and into a single package in order to meet market demands for additional features, higher performance, and lower power-consumption. As process technology improvements reach their limits, designers are continuing the move to multi-core designs. Furthermore, they are integrating multiple heterogeneous processor architectures—such as RISC-V, Arm, and x86—onto a single SoC or SiP.

A major factor contributing to the success of RISC-V is that different companies and entities can use the ISA as the basis for their own unique and differentiated implementations, such as different data widths, pipeline depths, and pipelining architectures. This allows RISC-V processors to be presented in a wide range of incarnations, from 32-bit FPGA-based soft-cores for microcontroller applications on the Edge, to 64-bit SoC-based hard-cores for HPC applications in the Cloud.

Ashling's ***RiscFree*** IDE and Unified Debugger supports the entire gamut of RISC-V realizations. Since its introduction, the ***RiscFree*** toolchain has been steadily building market share within the embedded tools market, and it is particularly strong in the RISC-V market with its ease-of-use, broad functionality, and plug-in architecture.

RiscFree provides added value to customers by providing a fully open-source multi-core—both homogeneous and heterogeneous—debug solution from within a single software environment using a single debug probe for these devices. ***RiscFree*** provides the same added value to FPGA customers with full support for Nios V processor.

In the case of Altera FPGAs, ***RiscFree*** includes an open-source, Eclipse-based IDE, Compiler, Debugger, and Trace. The single-shot installer works "out-of-the-box" to provide ***RiscFree*** software development and debug support for all 32-bit and 64-bit Nios V soft-core processors based on the RISC-V ISA.

In addition to custom integration and support for extensions to the Nios V processor, ***RiscFree*** supports Agilex™, Stratix® 10, Arria® 10, and Cyclone® 10 GX devices, with more families to follow.

Value of the Ashling and Altera Partnership

Ashling has been a leading provider of embedded development tools and services since 1982 and has over thirty years' experience in developing tools for embedded systems engineers. As a long-term member of RISC-V International, Ashling has been working closely on the evolution of RISC-V with a particular emphasis on standards for debug and trace standards. As vice-chair of the Trace committee, Ashling was involved in putting together the first standards defining RISC-V real-time trace.

Its partnership with Ashling ensures that Altera has a provider of tools that address all of its Nios V processor tool needs, including a full open-source toolchain with IDE, compiler, debugger, and trace support for Nios V processor and Arm processor.

Both companies have planned a long-term engagement, so as the Nios V processor family of devices grows and expands, the toolchain will also evolve to ensure full support for new devices and features.

Joint engineering co-operation between the Ashling and Altera teams ensures tightly coupled integration between the Ashling software development and Altera FPGA development toolchains, for example:

- Project Manager and Build Manager include Make and CMake support with rapid import, build, and debug of Quartus software-created application frameworks.
- The Nios V GCC compiler toolchain is fully integrated into the ***RiscFree*** IDE with support for the **newlib** and **picolibc** runtime libraries using the Nios V processor HAL API for hardware access.
- ***RiscFree*** provides runtime debug with support for the FPGA Download Cable II (USB Blaster II), register visualization for both Nios V and Arm processor cores, and real-time trace (both on-chip and off-chip) support for both Nios V and Arm processor cores.
- ***RiscFree*** also provides debug awareness for a wide range of OS and RTOS solutions, including Zephyr, FreeRTOS, uC/OS-II, and a full target (multi-core/multi-hart) Linux kernel, along with device driver and application debug support.
- ***RiscFree*** supports custom instructions and extensions for the Nios V processor.

In many development environments that feature a mix of Arm and RISC-V processor cores (both hard- and/or soft-cores), it is necessary to employ multiple debuggers—one for the Arm processors and one for the RISC-V processors. By comparison, a single instance of ***RiscFree*** supports the debugging any number of heterogeneous or homogeneous cores; for example, the simultaneous debug for Altera FPGA Arm hard-core and Nios V soft-core processors.

Altera vs. the Competition

Most competitive solutions offer only closed-source, proprietary solutions. Altera provides full access to the open-source RISC-V ecosystem. This enables RISC-V development now and deployment later into Altera FPGAs.

With Ashling and its ***RiscFree*** IDE and Unified Debugger, Altera is an open ecosystem partner that supports the complete custom logic across all Altera FPGAs with easy-to-use open-source tools that are now available to its RISC-V developers.

Summary

In addition to supplying the world with industry-leading microprocessors, Altera also creates state-of-the-art FPGAs. FPGAs can be configured to perform multiple functions, including one or more soft-core processors. The performance of these soft processors is becoming increasingly important in embedded markets.

RISC-V is an open-source hardware ISA. The RISC-V definition is a "clean-slate" design with no legacy-based or backwards-compatibility-based limitations or restrictions that have been designed from the ground up for modularity, extensibility, stability, efficiency, and performance. As a result, RISC-V is seeing exponential growth.

Altera joined the RISC-V International global open hardware standards organization, adopting a leadership role with the goal of expanding the RISC-V ecosystem potential for all industry stakeholders.

Altera has launched the next generation of soft-core processors for Altera FPGAs, the Nios V processor, which is based on the open-source RISC-V ISA.

Altera is partnering with Ashling, which is a long-term member of RISC-V International. Ashling's ***RiscFree*** IDE and Unified Debugger supports the entire gamut of RISC-V realizations. Since its introduction, the ***RiscFree*** toolchain has seen usage in the embedded tools market, including the RISC-V market with its ease-of-use, broad functionality, and plug-in architecture.

Ashling's ***RiscFree*** provides added value to Altera's FPGA customers by providing a fully open-source multi-core—both homogeneous and heterogeneous—debug solution from within a single software environment using a single debug probe for these devices.

Altera is planning further investments that will strengthen the RISC-V ecosystem and drive further adoption of RISC-V. These investments will help disruptive RISC-V companies innovate faster through Altera by collaborating on technology co-optimization, prioritizing wafer shuttles, supporting customer designs, building development boards, and evolving software infrastructure.

References

1 RISC-V Celebrates Incredible Year of Growth and Progress, Ratifying Multiple Technical Specifications, Launching New Education Programs, and Accelerating Broad Industry Adoption - Kim McMahon

Additional Resources

Agilex FPGA and SoC FPGA web page:
https://www.intel.com/content/www/us/en/products/details/fpga/agilex.html

Ashling RiscFree website:
https://www.ashling.com/ashling-riscfree/

Nios V Processors web page:
https://www.intel.com/content/www/us/en/products/details/fpga/nios-processor/v.html

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