



Intel® Core™ Ultra Processors (Series 2)

Specification Update

Supporting Intel® Core™ Ultra 200S, 200HX, 200H, and 200U Series Processors, formerly known as Arrow Lake.

Supporting Intel® Core™ Ultra 200S Plus, Intel Core® Ultra™ 200HX Plus Series Processors, formerly known as Arrow Lake Refresh.

Revision 024

October 2026



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Revision History

Document Number	Revision Number	Description	Revision Date
834774	001	Initial Revision – Includes errata ARL001-ARL018	October 2024
	002	Added Erratum: ARL019	November 2024
	003	Added Errata: ARL020 , ARL021 , ARL022 Removed Erratum ARL003	December 2024
	004	Added S 6+8, HX, H and U series processors Added Errata: ARL023 , ARL024 , ARL025 , ARL026 , ARL027	January 2025
	005	Added Erratum: ARL028	February 2025
	006	Added Errata: ARL029 , ARL030 , ARL031 , ARL032 , ARL033 Updated Erratum: ARL001	March 2025
	007	Added Erratum: ARL034 Updated Erratum: ARL032 Removed Erratum: ARL014 Updated CPUID Table	April 2025
	008	Added Errata: ARL035 , ARL036 , ARL037	May 2025
	009	Added Errata: ARL039 , ARL040	June 2025
	010	Added Errata: ARL041 , ARL042 , ARL043 , ARL044 , ARL045 , ARL046 , ARL047 , ARL048	July 2025
	011	Added Errata: ARL049 , ARL050 , ARL051 Updated Errata: ARL042 , ARL047 Updated CPUID Table	September 2025
	012	Added Errata: ARL052 , ARL053 , ARL054 Updated Erratum: ARL037	October 2025
	013	Added Errata: ARL055 , ARL056 , ARL057 Updated Erratum: ARL039	November 2025
	014	Added Errata: ARL058 , ARL059 , ARL060 , ARL061	December 2025
	015	Added Errata: ARL062 , ARL063 , ARL064 , ARL065	January 2026
	016	Added Errata: ARL066 , ARL067	February 2026
	017	Initial revision for Intel Core® Ultra™ 200HX Plus, 200S Plus series processors	March 2026
	018	Added Errata: ARL068 , ARL069 , ARL070	April 2026
	019	Added Erratum: ARL071	May 2026
	020	Added Errata: ARL072 , ARL073	June 2026



Document Number	Revision Number	Description	Revision Date
	021	Added Erratum: ARL074	July 2026
	022	Added Erratum: ARL075	August 2026
	023	Added Erratum: ARL076	September 2026
	024	Added Errata: ARL077 , ARL078 , ARL079 Removed Errata: ARL072, ARL073	October 2026

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1 Preface

This document is an update to the specifications contained in the documents listed in the following [Affected Documents/Related Documents](#) table. It is a compilation of device and document errata and specification clarifications and changes and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® Core™ Ultra 200S and 200HX Series Processor Datasheet, Volume 1 of 2	832586
Intel® Core™ Ultra 200S and 200HX Series Processor Datasheet, Volume 2 of 2	834966
Intel® Core™ Ultra 200H and 200U Series Processor Datasheet, Volume 1 of 2	842704
Intel® Core™ Ultra 200H and 200U Series Processor Datasheet, Volume 2 of 2	844261

1.2 Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/profducts/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

1.3 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – These describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – These include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle or until a stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.)



2 Identification Information

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 2-1. Component Identification

Product	Stepping	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
ARL-S 8P+16E	B0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h
ARL-S 6P+8E	B0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h
ARL-HX 8P+16E	B0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h
ARL-H 6P+8E	A1	C0652h	Reserved	00h	Ch	Reserved	0h	6h	5h	2h
ARL-U 2P+8E	A0	B0650h	Reserved	00h	Bh	Reserved	0h	6h	5h	0h
ARL-S Plus 8P+16E	B0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h
ARL-HX Plus 8P+16E	B0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. Refer to Processor BIOS Specification for additional information. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID

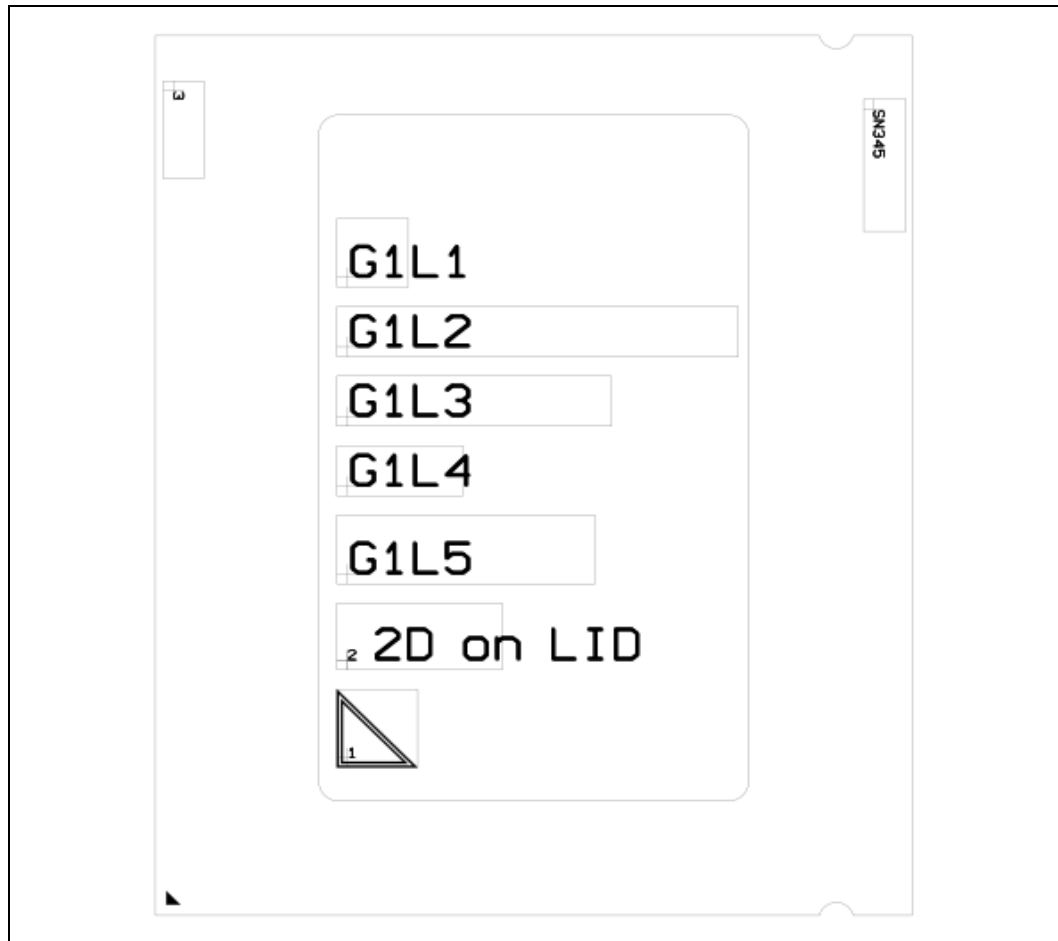
Identification Information

value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

2.2 Component Marking Information

Figure 2-1. S/S Plus-Series Chip Package LGA Top-Side Markings



Pin Count: 1851

Package Size (width x height): 37.5mm x 45mm

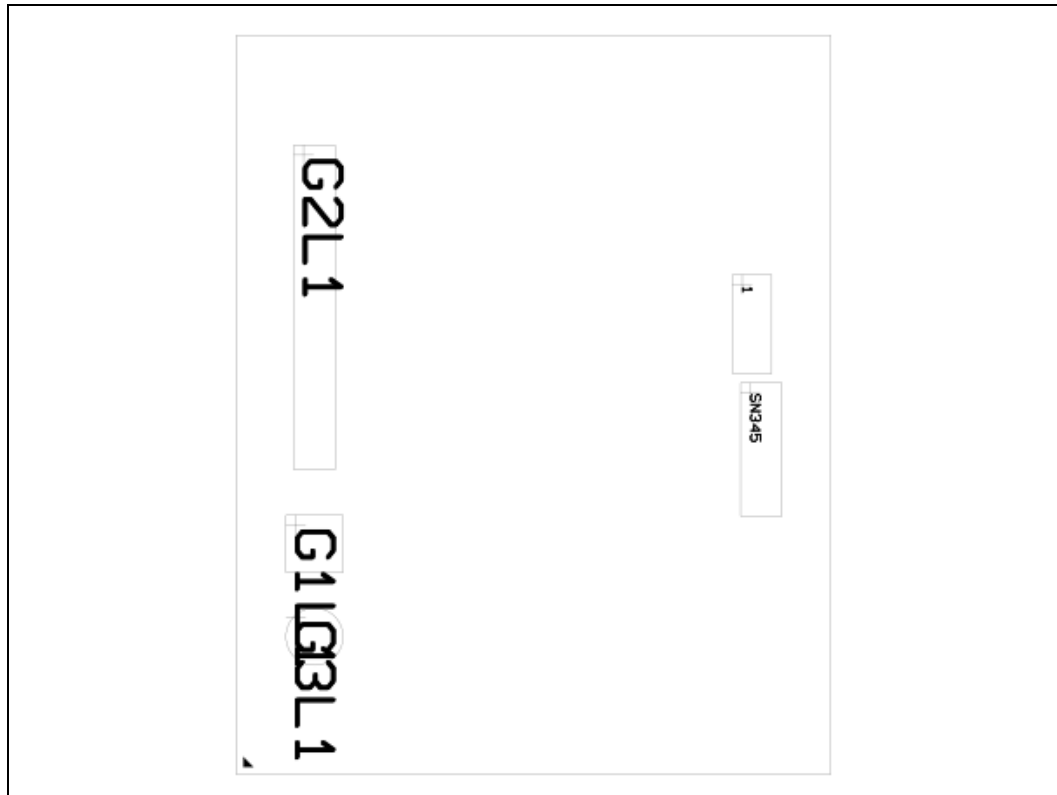
Production (SSPEC):

- SN345
- G1L1: SPARK
- G1L2: TRADEMARK
- G1L3: PROC NUMBER
- G1L4: FPO_ SSPEC

- G1L5: {ex}

Note: “3” is used to extract the unit visual ID (2D ID).

Figure 2-2. HX/HX Plus-Series Chip Package BGA Top-Side Markings



Pin Count: 2114

Package Size (width x height): 30.2 mm x 37.5 mm

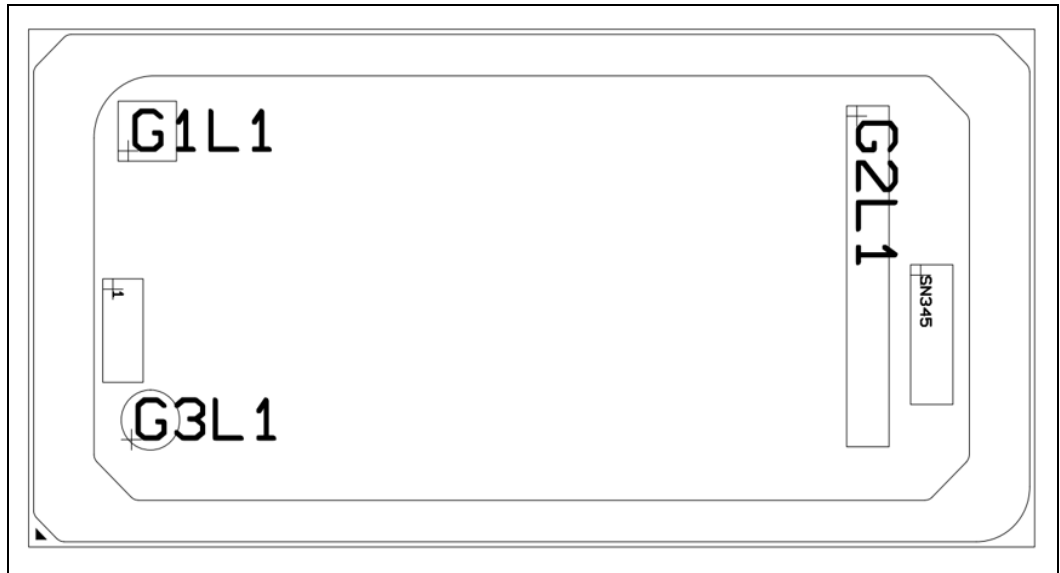
Production (SSPEC):

- SN345
- G1L1: SPARK
- G2L1: FPO_SSPEC
- G3L1: {ex}

Note: “1” is used to extract the unit visual ID (2D ID).

Identification Information

Figure 2-3. H/U-Series Chip Package BGA Top-Side Markings



Pin Count: 2049

Package Size (width x height): 50mm x 25mm

Production (SSPEC):

- SN345
- G1L1: SPARK
- G2L1: FPO_SSPEC
- G3L1: {ex}

Note: "1" is used to extract the unit visual ID (2D ID).

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3 Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed processor stepping. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank box)	This erratum is fixed or does not apply to the listed stepping or specification change does not apply to the listed stepping.

Status	Description
Plan Fix	This erratum may be fixed in a future hardware stepping, firmware, or software update.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	Processor Line					Title
	S/S Plus 8+16	S 6+8	HX/HX Plus	U	H	
ARL001	N/A	N/A	N/A	No Fix	N/A	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
ARL002	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
ARL003	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ARL004	No Fix	No Fix	No Fix	No Fix	No Fix	MSI From VMD-Owned Device May Pass Memory Write
ARL005	No Fix	No Fix	No Fix	No Fix	No Fix	USB 3.2 Device May Not Function as Expected With TC10 Enabled
ARL006	No Fix	No Fix	No Fix	No Fix	No Fix	PCONFIG Error Reporting May be Incorrect
ARL007	No Fix	No Fix	No Fix	No Fix	No Fix	DP Monitor May Not Operate After S4/S5 Resume

Summary Tables of Changes

Erratum ID	Processor Line					Title
	S/S Plus 8+16	S 6+8	HX/HX Plus	U	H	
ARL008	No Fix	No Fix	No Fix	No Fix	No Fix	PCIe Root Port Lane Error Status Register May Not be Cleared
ARL009	No Fix	No Fix	No Fix	No Fix	No Fix	Type-C Display May be Blank Following S3/S4/S5 Resume
ARL010	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
ARL011	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
ARL012	No Fix	No Fix	No Fix	No Fix	No Fix	Processor Trace May Generate PSB Packets Too Infrequently
ARL013	No Fix	No Fix	No Fix	No Fix	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
ARL014	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ARL015	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
ARL016	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event IDQ.MS_UOPS May Undercount
ARL017	No Fix	No Fix	No Fix	N/A	No Fix	Performance Monitoring Event INT_VEC_RETIRE.MUL_256 May Undercount
ARL018	No Fix	No Fix	No Fix	No Fix	No Fix	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
ARL019	No Fix	No Fix	N/A	N/A	N/A	PCIe REFCLK Inactive Prior to PERST#
ARL020	No Fix	No Fix	No Fix	No Fix	No Fix	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
ARL021	No Fix	No Fix	No Fix	No Fix	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
ARL022	No Fix	No Fix	No Fix	No Fix	No Fix	Display Artifacts With YUV420 Format
ARL023	N/A	N/A	N/A	No Fix	No Fix	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
ARL024	N/A	N/A	N/A	No Fix	No Fix	xHCI Out of Order ACK Due to LCRD1

Erratum ID	Processor Line					Title
	S/S Plus 8+16	S 6+8	HX/HX Plus	U	H	
ARL025	N/A	N/A	N/A	No Fix	No Fix	Non Canonical Fault May be Signaled on Access That Wraps Address Space When LAM is Enabled
ARL026	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
ARL027	N/A	N/A	N/A	No Fix	No Fix	SPI0 Dual IO Mode With SPI0 IO2 And SPI0 IO3 Connected to SPI Device
ARL028	No Fix	No Fix	No Fix	No Fix	No Fix	Cache Level Wrongly Reported in Machine Check Banks
ARL029	Fixed	Fixed	Fixed	N/A	Fixed	Incorrect Core TLB Entry May be Retrieved Following VM Exit
ARL030	N/A	N/A	N/A	Fixed	Fixed	Higher Than Expected Power Consumption With VR Slow Slew Rate Enabled
ARL031	N/A	N/A	N/A	N/A	Fixed	Unexpected System Behavior Following S0ix/S4/Warm Reset
ARL032	Fixed	Fixed	N/A	Fixed	N/A	Unexpected Core C-State Auto-Demotion
ARL033	Fixed	Fixed	Fixed	Fixed	N/A	RDTSC Instructions May Return Non-Incremental Value
ARL034	Fixed	Fixed	Fixed	Fixed	Fixed	Processor May Not Enter Package State C3 or Deeper
ARL035	Fixed	Fixed	N/A	N/A	N/A	IA32_HWP_STATUS MSR May be Cleared
ARL036	Fixed	Fixed	Fixed	Fixed	Fixed	Unpredictable System Behavior May Occur When C6 or Deeper Sleep States Are Used
ARL037	Planned Fix	Planned Fix	Planned Fix	N/A	Fixed	A Core May Hang When Entering or Exiting C6 or Deeper Sleep States
ARL038	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ARL039	N/A	N/A	No Fix	No Fix	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
ARL040	No Fix	No Fix	No Fix	No Fix	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
ARL041	N/A	N/A	N/A	N/A	Fixed	Processor May Hang During Core C1E Exit
ARL042	Fixed	Fixed	Fixed	Fixed	N/A	Power State Package C6 Exit May Hang With Bug Check Error VIDEO_TDR_FAILURE (0x116)
ARL043	N/A	N/A	N/A	N/A	Fixed	Unexpected Global Reset During System S0ix/S4

Summary Tables of Changes

Erratum ID	Processor Line					Title
	S/S Plus 8+16	S 6+8	HX/HX Plus	U	H	
ARL044	No Fix	No Fix	No Fix	No Fix	No Fix	xHCI Controller Reset Due to Missing Link Credit From Device
ARL045	No Fix	No Fix	No Fix	No Fix	No Fix	xHCI Controller Hang With Zero-Length Data Packet
ARL046	N/A	N/A	N/A	No Fix	No Fix	I2S Audio Channels Swapped With High Frame Polarity in Device Mode
ARL047	Fixed	Fixed	Fixed	N/A	Fixed	Indirect Branches May Cause Execution of Incorrect Instructions
ARL048	N/A	N/A	N/A	No Fix	No Fix	Non-Responsive USB Port After Disconnecting Full-speed Device
ARL049	N/A	N/A	N/A	N/A	Fixed	System Hang During Warm Reset/Sx Exit When Integrated GFX Has Been Disabled
ARL050	Fixed	Fixed	Fixed	N/A	Fixed	System Hang or System Hang With Internal Timer Machine Check Exception (400h) Following a Core C1 Exit
ARL051	N/A	N/A	Fixed	N/A	N/A	Processor Hang When Reading Core P0 Ratio
ARL052	Fixed	Fixed	Fixed	N/A	N/A	xHCI Controller Latency Tolerance Reporting Values in pCode Version 4502 or Later
ARL053	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event For Memory Bound Stalls May Undercount
ARL054	Fixed	Fixed	Fixed	Fixed	Fixed	REP SCASB or REP CMPSB Instructions May Return Incorrect Results
ARL055	Fixed	Fixed	Fixed	Fixed	Fixed	USB 3.2 Bulk Transfers After Device Initiated Flow Control
ARL056	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT Incorrect CR3-Filtering
ARL057	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect Last Branch From Value in BTS Branch Record During a Task Switch
ARL058	No Fix	No Fix	No Fix	No Fix	No Fix	xHCI Unresponsive Due to Split Transaction Error
ARL059	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event MEMORY_ACTIVITY.STALLS_L2_MISS May Undercount
ARL060	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event MEMORY_STALLS.L2 May Overcount
ARL061	No Fix	No Fix	No Fix	No Fix	No Fix	Timed PEBS Retire Latency Field May be Incorrect

Erratum ID	Processor Line					Title
	S/S Plus 8+16	S 6+8	HX/HX Plus	U	H	
ARL062	No Fix	No Fix	No Fix	No Fix	No Fix	USB DbC or Device Mode Port When Exiting S4, S5, or G3
ARL063	No Fix	No Fix	No Fix	No Fix	No Fix	Certain VMCS Fields May be Incorrect During STM to VMX Transitions
ARL064	No Fix	No Fix	No Fix	No Fix	No Fix	Certain BR_MISP_RETIRED Performance Monitoring Events May Overcount
ARL065	No Fix	No Fix	No Fix	No Fix	No Fix	LBR Event Logging IA32_LBR_x_INFO.PMCx_CNT Field May Undercount
ARL066	N/A	N/A	N/A	No Fix	No Fix	Bandwidth Allocation for USB 2.0 Periodic Devices Behind USB 3.2 Hub
ARL067	No Fix	No Fix	No Fix	No Fix	No Fix	Instruction Timeout VM Exit Will Not Set Guest RFLAGS.RF During #UD
ARL068	No Fix	No Fix	No Fix	N/A	No Fix	PCIe Gen5 Link Exit from L1 Sub-state Low Power State
ARL069	N/A	N/A	N/A	No Fix	No Fix	I3C Interface Minimum Clock Timing Specifications
ARL070	No Fix	No Fix	No Fix	No Fix	No Fix	ICR Read May Not Generate an APIC-Access VM Exit
ARL071	No Fix	No Fix	No Fix	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV_SS or POP_SS Instruction is Not Followed By a Write to SP
ARL072	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ARL073	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ARL074	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect Guest RFLAGS.RF on VM Entry
ARL075	Fixed	Fixed	Fixed	Fixed	Fixed	Execution of IRET in Compatibility Mode May Free Supervisor Shadow Stack Token
ARL076	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect VM Exit Reason When MOV_SS or POP_SS Followed by an x2APIC MSR Access
ARL077	No Fix	No Fix	No Fix	No Fix	No Fix	Overcount of Topdown Bad Speculation Performance Monitoring Events
ARL078	No Fix	No Fix	No Fix	No Fix	No Fix	Undercount of Performance Monitoring Events for Walk Pending
ARL079	N/A	N/A	N/A	No Fix	N/A	Missing #UD Fault for Non-Enumerated AVX-IFMA Instructions

3.3 Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

3.5 Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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4 Errata Details

ARL001	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
Problem	Under complex micro-architectural conditions, single step on branches (IA32_DEBUGCTMSR (Offset 1D9h, bit [1]) and also TF flag in EFLAGS register is set) in guest might be missed when VMM enables notification on VM Exit (IA32_VMX_PROCBASED_CTLS2 MSR, Offset 48Bh, bit [31]) while the dirty access bit is not set for the code page (bit [6] in paging-structure entry).
Implication	When a single step is enabled under the above condition, some single step branches will be missed. Intel has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL002	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
Problem	Intel® VT-d remapping hardware does perform Reserved(0) check on Page Snoop (PGSNP) field in scalable-mode Process Address ID (PASID) table entry when Snoop Control capability is defined as not available in the Extended Capability Register Offset 10h bit 7 (ECAP.SC=0).
Implication	There are no known functional implications due to this erratum. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL003	N/A. Erratum has been removed.
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ARL004	MSI From VMD-Owned Device May Pass Memory Write
Problem	When the storage subsystem is configured to operate in RAID 0 or 1 mode, a Message Signaled Interrupt (MSI) from an Intel® Volume Management Device (Intel® VMD) owned device may interrupt a core before a previous write from the device is completed.
Implication	Due to this erratum, the platform may experience unpredictable system behavior.
Workaround	None identified. The VMD MSI interrupt-handler should initially perform a dummy register read to the MSI initiator device prior to any writes to ensure proper PCIe ordering.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL005	USB 3.2 Device May Not Function as Expected With TC10 Enabled
Problem	When TC10 is enabled, a USB 3.2 device connected to USB Type-C port directly without retimer may not function as expected.
Implication	Due to this erratum, a USB 3.2 device may not function as expected.
Workaround	None identified. It may be possible for the BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL006	PCONFIG Error Reporting May be Incorrect
Problem	If invalid parameters are provided, the PCONFIG instruction should generate a #GP exception. Due to this erratum, the processor may instead set a ZF flag, with EAX reporting failure reasons.
Implication	Due to this erratum, incorrectly configured PCONFIG usage may lead to unexpected error reporting.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL007	DP Monitor May Not Operate After S4/S5 Resume
Problem	When switching a USB Type-C Display Port (DP) monitor connection between Alt Mode and MFD in S4/S5, the monitor may not be enumerated when resuming from S4/S5.
Implication	Due to this erratum, a DP Monitor may not operate when resuming from S4/S5 and may require a hot plug to recover.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL008	PCIe Root Port Lane Error Status Register May Not be Cleared
Problem	Re-enabling a port following a link disable or hot reset the PCIe Lane Error Status register (Offset 0xA38) may not be cleared.
Implication	Due to this erratum, the Lane Error Status register may indicate lane errors on some of the Root Ports. Intel has not observed any functional issues due this erratum.
Workaround	None identified. Software should ignore the lane error status register to mitigate this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL009	Type-C Display May be Blank Following S3/S4/S5 Resume
Problem	When switching between Type-C Display Alt Mode and a Multi-Function Device (MFD) while the system is in S3/S4/S5, the Display may not enumerate.
Implication	When this erratum occurs, the Display may be blank. A device unplug and re-plug may be necessary to recover the display.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL010	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
Problem	A CALL instruction whose target is the next sequential instruction (the same address pushed onto the stack) will not increment the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H, F9H).
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may undercount. Since the CALL is to the next instruction, control flow tracing with the Last Branch Retired (LBR) records should not be affected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL011	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
Problem	On certain types of branch and complex instructions, the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H / 7EH / BFH / C0H / DFH / EBH / FBH / F9H) will overcount by 1. Affected instructions include FAR CALL/JMP, RETF, IRET, VMENTRY/VMEXIT/VMPTLDR, and complex SGX/SMX/CSTATE instructions/flows.
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may overcount.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL012	Processor Trace May Generate PSB Packets Too Infrequently
Problem	A Packet Stream Boundary (PSB) packet should be generated for every PSBFreq number of trace output bytes. Due to this erratum, PSB packets may be generated only after as many as four times that number of output bytes have been generated.
Implication	Due to this erratum, trace decoder software may see fewer PSB packets than expected. This may lead to the trace decoder software needing to search further to find a starting point to decode or, when used in circular mode, being unable to decode the trace due to lacking any PSB packets.
Workaround	None identified. The software can request more frequent PSB packets by programming PSBFreq (bits[27:24]) of IA32_RTIT_CTL MSR (570H) to a value 1/4 of the desired value.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL013	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case, the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL014	N/A. Erratum has been removed.
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ARL015	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
Problem	The performance monitoring events TOPDOWN.BACKEND_BOUND_SLOTS (Event A4h, UMask 02h) and IDQ_BUBBLES.* (Event 9Ch, UMask 01h) may not count when the processor is in the C0.2 power sub-state, which is entered via the TPAUSE or UWAIT instructions. This erratum also impacts the accuracy of MSR_PERF_METRICS fields Frontend Bound, Backend Bound, and Fetch Latency (MSR 329h, Bits [23:16], [31:24] and [55:48]).
Implication	Due to this erratum, these performance monitoring events and the fields in MSR_PERF_METRICS may be inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL016	Performance Monitoring Event IDQ.MS_UOPS May Undercount
Problem	The performance monitoring events IDQ.MS_UOPS, IDQ.MS_SWITCHES, and IDQ.MS_CYCLES_ANY (Event 79h, UMask 30h) may undercount MS_UOPS that come from the Decode Stream Buffer (DSB).
Implication	Due to this erratum, performance monitoring counters may report counts lower than expected.
Workaround	None identified. Performance monitoring event UOPS_RETIRED.MS may be used instead.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL017	Performance Monitoring Event INT_VEC_RETIRE.MUL_256 May Undercount
Problem	The performance monitoring event INT_VEC_RETIRE.MUL_256 (Event E7h, Umask 80h) may not count VPMULLQ instructions.
Implication	Due to this erratum, the performance monitoring event may report lower counts than expected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL018	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
Problem	A VM Exit that occurs while the processor is serving a user interrupt in non-root mode should set the "asynchronous to instruction execution" bit in the Exit Qualification field in the Virtual Machine Control Structure (bit 16). However, if a VM Exit occurs during processing a user interrupt due to an APIC access, the bit will not be set.
Implication	Due to this erratum, the "asynchronous to instruction execution" bit will not be set if an APIC Access VM Exit occurs while the processor is serving a user interrupt. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL019	PCIe REFCLK Inactive Prior to PERST#
Problem	PCIe differential reference clocks may go inactive prior to the assertion of PERST#.
Implication	Due to this erratum, the PCI Express® Card Electromechanical Specification, Revision 5.0, Version 1.0 Power Section 2.2.2 "Management States (S0 to S3/S4 to S0)" requirement is not followed. Intel has not observed any functional implications due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL020	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
Problem	The UC-lock disable feature (MSR_MEMORY_CTRL bit [28] (MSR 33h)) may not cause a fault (#AC(4)) for a page split lock that accesses a page with non-WB memory type if the split lock disable (MSR_MEMORY_CTRL bit [29]) is not set.
Implication	Due to this erratum, system software may not be able to fully prevent bus locks due to locks to non-WB memory unless they use the split-lock disable feature to prevent bus locks due to splits. Intel has not observed this erratum with any commercially available software.
Workaround	None identified. Software using the UC-lock disable feature should also enable the split lock disable feature.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL021	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN will not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL022	Display Artifacts With YUV420 Format
Problem	While in DP2.1 UHBR mode and using the YUV420 format with scaling, displays with a resolution higher than 5K @ 60Hz may show display artifacts.
Implication	Due to this erratum, display artifacts may be seen.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL023	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	The processor may fail to enter C3 or deeper package C-States. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL024	xHCI Out of Order ACK Due to LCRD1
Problem	A delay in the availability of LCRD1 (Link Credit 1) from a USB 3.2 hub, with two or more downstream USB 3.2 bulk endpoint devices engaged in SuperSpeedPlus concurrent transfers, may lead to the connected xHCI controller sending the ACK and Status of a transfer packet out of order.
Implication	Due to this erratum, a USB 3.2 bulk endpoint device may not respond to subsequent transfers. It may be possible for a device driver to recover the USB 3.2 device.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL025	Non Canonical Fault May be Signaled on Access That Wraps Address Space When LAM is Enabled
Problem	When Linear Address Masking (LAM) is enabled, a non-canonical fault may be signaled if there is an access which splits the 64-bit linear address space (and thus touches both linear address FFFF_FFFF_FFFF_FFFFh and 0h).
Implication	Due to this erratum, software may receive an unexpected exception on such accesses. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL026	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
Problem	The processor accesses to TME exclude range may be encrypted but not decrypted if mapped to remap range.
Implication	Due to this erratum, the processor exclude range it will be encrypted but will but not decrypted if mapped to remap range.
Workaround	It may be possible for BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL027	SPI0 Dual IO Mode With SPI0_IO2 And SPI0_IO3 Connected to SPI Device
Problem	On systems with dual IO mode enabled, SPI0_IO2 and SPI0_IO3 may momentarily drive low before these signals are pulled high by internal resistors during boot from the G3 state.
Implication	Due to this erratum, unexpected system behavior may occur on systems when SPI0_IO2 and SPI0_IO3 signals are connected to an SPI device.
Workaround	None identified. To mitigate this erratum, do not connect SPI0_IO2 and SPI0_IO3 to an SPI device in SPI0 dual IO mode enabled systems.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL028	Cache Level Wrongly Reported in Machine Check Banks
Problem	When reporting a machine check in the module level caches (IA32_MC1_STATUS, MSR 405H), a Compound Error Code of type Cache Hierarchy Error will be reported with a Level (LL) Sub-field of 0b10[L2] instead of 0b01[L1].
Implication	Due to this erratum, system software relying on this data, may wrongly categorize the cache level in which the error was reported. The severity of the error will be reported accurately.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL029	Incorrect Core TLB Entry May be Retrieved Following VM Exit
Problem	An incorrect Core TLB entry may be retrieved when the retrieval is not completed prior to VM exit.
Implication	Due to this erratum, hypervisor software may read an invalid value following VM exit, leading to Windows Bug Check HYPERVISOR_ERROR (20001h) or SECURE_KERNEL_ERROR (18Bh).
Workaround	It may be possible for the BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL030	Higher Than Expected Power Consumption With VR Slow Slew Rate Enabled
Problem	On a system with acoustic noise mitigation Voltage Regulator (VR) Slow Slew Rate (SSR) enabled, the latency values may not be correctly calibrated.
Implication	Due to this erratum, the system may experience lower than expected Deepest Runtime Idle Platform State (DRIPS) leading to a higher than expected power consumption.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL031	Unexpected System Behavior Following S0ix/S4/Warm Reset
Problem	Longer than expected processor core power state exit latencies during warm reset or S0ix/S4 flows may delay core wake up.
Implication	Due to this erratum, a system hang with bug check BSOD SYNTHETIC_WATCHDOG_TIMEOUT (1CAh), audio glitches, or other unexpected system behavior may occur.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL032	Unexpected Core C-State Auto-Demotion
Problem	An incorrect P-core telemetry counter value on package C10 exit may lead to an unexpected core C-State Auto-Demotion.
Implication	Due to this erratum, higher than expected package C0 residency may be observed.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL033	RD TSC Instructions May Return Non-Incremental Value
Problem	During an increase in processor frequency, two consecutive RD TSC instructions may return the same value.
Implication	Due to this erratum, software that relies upon the processor monotonically incrementing the time-stamp counter may function incorrectly.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL034	Processor May Not Enter Package State C3 or Deeper
Problem	During PCIe device L0 exit, PCIe Latency Tolerance Reporting (LTR) may not update correctly, resulting in the processor not entering Package State C3 or deeper.
Implication	Due to this erratum, higher than expected power consumption may occur.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL035	IA32_HWP_STATUS MSR May be Cleared
Problem	The fields in the IA32_HWP_STATUS MSR (Offset 777h, bits [5:2, 0]) which indicate to software that it should change a performance state or frequency, may be cleared following package state C10 exit.
Implication	Due to this erratum, software that relies upon the IA_32_HWP_STATUS MSR may not behave as expected.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL036	Unpredictable System Behavior May Occur When C6 or Deeper Sleep States Are Used
Problem	Under complex microarchitectural conditions, a core may encounter incorrect data when other cores in the system are entering Core C6 or deeper sleep states.
Implication	When this erratum occurs, unpredictable system behavior may be observed. Intel has only observed this behavior in a synthetic test environment.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL037	A Core May Hang When Entering or Exiting C6 or Deeper Sleep States
Problem	Under complex microarchitectural conditions involving two or more cores within a module simultaneously entering or exiting Core C6 or deeper sleep states, one or more of those cores may hang without a Machine Check Error being logged.
Implication	Due to this erratum, the system may hang. Intel has only observed this behavior in a synthetic test environment.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL038	N/A. Erratum has been removed.
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ARL039	xHCI USB 2.0 ISOCH Device Missed Service Interval
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets. Note: This issue has only been observed with a USB 3.2 Bulk Stream device.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL040	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL041	Processor May Hang During Core C1E Exit
Problem	On a system with voltage regulator Slow Slew Rate enabled, the core C1E exit latency values may not be correctly calibrated.
Implication	Due to this erratum, the processor may hang.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL042	Power State Package C6 Exit May Hang With Bug Check Error VIDEO_TDR_FAILURE (0x116)
Problem	A Geyserville transition during power state package C6 exit may result in an incorrect iGFX initialization.
Implication	Due to this erratum, the system may hang with a bug check error VIDEO_TDR_FAILURE (0x116).
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL043	Unexpected Global Reset During System S0ix/S4
Problem	When a LAN dongle is connected over Type-C USB, the USB Type-C Sub System may not respond on time to the Power Management Controller (PMC) S0ix/S4 sleep request.
Implication	Due to this erratum, the system may perform an unexpected global reset.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL044	xHCI Controller Reset Due to Missing Link Credit From Device
Problem	The xHCI controller may not send LCRD (Link Credit) to the device after the link U0 state recovery is completed if a USB 3.2 device incorrectly stops sending LCRD.
Implication	When this erratum occurs, subsequence transfers from the device may not be completed and the xHCI host controller driver may initiate a host controller reset.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL045	xHCI Controller Hang With Zero-Length Data Packet
Problem	The xHCI controller may fail to handle a zero-length data packet when doing concurrent traffic with the following devices connected on three separate root ports: • USB 3.2 Gen 2x1 (or 2x2) hub with at least two USB 3.2 bulk devices. • USB 3.2 Gen 2x1 (or 2x2) hub with at least two USB 3.2 bulk devices. • USB isochronous device that sends zero-length data packets.
Implication	Due to this erratum, the xHCI controller may hang. Intel has only observed this behavior with USB audio offload enabled and USB 2.0 audio devices that send zero-length data packets.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL046	I2S Audio Channels Swapped With High Frame Polarity in Device Mode
Problem	When the I2S interface is in device mode, the audio controller may not be correctly configured if the audio codec requires high frame polarity.
Implication	Due to this erratum, the left and right audio channels may swap when frame polarity is set to high.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL047	Indirect Branches May Cause Execution of Incorrect Instructions
Problem	Under complex microarchitectural conditions, an indirect branch may jump to a different location than the location expected and reported, leading to the execution of incorrect instructions, while remaining in the current processor mode.
Implication	When this erratum occurs, the execution of incorrect instructions may lead to unpredictable system behavior.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL048	Non-Responsive USB Port After Disconnecting Full-speed Device
Problem	Disconnecting a USB full-speed device from the USB port while the xHCI controller is in the process of sending the Start of Frame may cause the USB 2.0 functionality to become unresponsive for that specific port.
Implication	Due to this erratum, USB 2.0 devices may not be recognized on the USB port until a host controller reset occurs. Intel has only observed this behavior in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL049	System Hang During Warm Reset/Sx Exit When Integrated GFX Has Been Disabled
Problem	When integrated GFX has been disabled in BIOS, the Power Management Sideband (PMSB) may send an unexpected request to a powered down internal Media Engine during Warm Reset/Sx exit.
Implication	Due to this erratum, the system may hang with a Machine Check Exception MSCOD=PMSB_MESSAGE_CHANNEL_TIMEOUT (0081h), MCACOD=UNKNOWN (0414h).
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL050	System Hang or System Hang With Internal Timer Machine Check Exception (400h) Following a Core C1 Exit
Problem	Under complex microarchitectural conditions, following a Core C1 exit, the execution of instructions on a processor core may be blocked.
Implication	Due to this erratum, the system may hang or hang with an Internal Timer Machine Check Exception (IA32_MCI_STATUS.MCACOD=400h and IA32_MCI_STATUS.MSCOD=E1C4h).
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL051	Processor Hang When Reading Core P0 Ratio
Problem	The processor may use an incorrect Core logical index table instead of Core physical index table when initiating a Core P0 ratio value read.
Implication	Due to this erratum, the processor may hang. Intel has observed this erratum when using BIOS Mailbox command 0x11 functions, such as override voltage offset for a specific core.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL052	xHCI Controller Latency Tolerance Reporting Values in pCode Version 4502 or Later
Problem	For Intel® Core™ Ultra 200HX with pCode versions 4502 or later loaded and for Intel® Core™ Ultra 200S with pCode versions 5071 or later loaded, the xHCI controller Latency Tolerance Reporting (LTR) values may be incorrectly calibrated.
Implication	Due to this erratum, USB 3.2 isochronous IN devices may experience dropped packets. Intel has observed this issue during video playback on an isochronous camera device.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL053	Performance Monitoring Event For Memory Bound Stalls May Undercount
Problem	The Performance Monitoring events, MEM_BOUND_STALLS_LOAD (EventID: 34h) and MEM_BOUND_STALLS_IFETCH (EventID: 35h), and their subevents, will undercount the number of cycles of core initiated requests with latencies that exceed 256 cycles. A CMASK value of 255 may be used to count instances of this erratum.
Implication	Due to this erratum, software monitoring the events for Memory Bound Stalls may undercount.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL054	REP SCASB or REP CMPSB Instructions May Return Incorrect Results
Problem	When software executes Repeat Scan String Byte (REP SCASB) or Repeat Compare String Byte (REP CMPSB) instructions on a core, another core or thread may modify the memory being accessed.
Implication	Due to this erratum, the SCASB or the CMPSB instruction may return incorrect results.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL055	USB 3.2 Bulk Transfers After Device Initiated Flow Control
Problem	When a USB 3.2 device initiates flow control and is connected to the USB Type C* Sub System, the xHCI controller may temporarily pause USB 3.2 bulk transfers until the next micro-frame after the device ends flow control.
Implication	Due to this erratum, USB 3.2 bulk transfers may be temporary paused.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL056	Intel® PT Incorrect CR3-Filtering
Problem	When the Intel® Processor Trace (Intel® PT) CR3-filtering mechanism is enabled using the CR3Filter bit in IA32_RTIT_CTL MSR (MSR 570h, bit 7), CR3 control register bits [63:52] are not compared with the IA32_RTIT_CR3_MATCH MSR (MSR 572h) value.
Implication	Due to this erratum, software that relies upon the IA32_RTIT_CTL MSR (bit 7) may function incorrectly.
Workaround	None identified. Software may mitigate this erratum by copying the CR3 register value into IA32_RTIT_CR3_MATCH MSR.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL057	Incorrect Last Branch From Value in BTS Branch Record During a Task Switch
Problem	When branch tracing is enabled using branch trace store (BTS) during a task switch, the processor reports the linear address of the branch target in the branch record field "Last Branch from" instead of the linear address of the instruction from which branch was taken.
Implication	Due to this erratum, debug tools relying on BTS may misinterpret control flow.
Workaround	None identified. Software should avoid using BTS to determine the accuracy of branch prediction.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL058	xHCI Unresponsive Due to Split Transaction Error
Problem	When multiple USB 2.0 split transaction errors occur, the xHCI host controller may become unresponsive.
Implication	Due to this erratum, USB devices connected to the xHCI controller may not function.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL059	Performance Monitoring Event MEMORY_ACTIVITY.STALLS_L2_MISS May Undercount
Problem	The performance monitoring event MEMORY_ACTIVITY.STALLS_L2_MISS (Event 47h, UMASK 05h) may undercount for cases of streaming partial loads.
Implication	Due to this erratum, performance monitoring counters may undercount values for this event and the Top-down Microarchitecture Analysis (TMA) L2_Bound may be over-estimated for streaming partial loads.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL060	Performance Monitoring Event MEMORY_STALLS.L2 May Overcount
Problem	The performance monitoring event MEMORY_STALLS.L2 (Event 46h, UMASK 02h) may overcount for cases of streaming partial loads.
Implication	Due to this erratum, performance monitoring counters may overcount for this event and the Top-down Microarchitecture Analysis (TMA) L2_Bound may be over-estimated for streaming partial loads.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL061	Timed PEBS Retire Latency Field May be Incorrect
Problem	The retire latency field in the Timed PEBS (Timed Processor Event Based Sampling) record may report lower retire latency values.
Implication	Due to this erratum, software using the retire latency field for performance analysis may not behave as expected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL062	USB DbC or Device Mode Port When Exiting S4, S5, or G3
Problem	If a standalone xHCI controller USB port is configured in DbC mode and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1. The processor exits from S4 or S5, the port may remain in U2. 2. The port is connected to a USB 3.2 Gen 1x1 host controller when exiting from S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance Mode is disabled. 3. The port is connected to a USB 3.2 Gen 2x1 host controller when exiting from S4, S5, or G3, the port may enter an inactive state.
Implication	Due to this erratum, the processor standalone xHCI controller USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL063	Certain VMCS Fields May be Incorrect During STM to VMX Transitions
Problem	When the Intel® Processor Trace (Intel® PT) is enabled by setting VM-Entry control field "Load IA32_RTIT_CTL" (bit 18) and an event is injected during STM (SMM-transfer monitor) to VMX transition (root or non-root), the following VMCS fields may be incorrect: VM-entry interruption-information field (4016h) VM-entry exception error code (4018h) VM-entry instruction length (401Ah)
Implication	Due to this erratum, the processor may enter HLT state or report an incorrect value in the VMCS IDT-vectoring information field (4408h).
Workaround	A mitigation for this erratum is for software (VMM) to verify the VMCS fields on the next VM exit before executing vmresume.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL064	Certain BR_MISP_RETIRED Performance Monitoring Events May Overcount
Problem	The performance monitoring events BR_MISP_RETIRED.COND_TAKEN_FWD_COST and BR_MISP_RETIRED.COND_TAKEN_BWD_COST (Event C5h, UMaskExt 80h) may overcount when a branch misprediction happens right after the processor clears speculative instructions.
Implication	Due to this erratum, when PEBS (Processor Event-Based Sampling) is enabled and triggered on an overcount, then the instruction pointer (EventingIP) and retire latency fields may point to the wrong instruction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL065	LBR Event Logging IA32_LBR_x_INFO.PMCx_CNT Field May Undercount
Problem	Under a complex set of microarchitectural conditions, when LBR (Last Branch Record) Event Logging (EN_LBR_LOG bit 35 in IA32_PERFEVTSELx MSR (186h to 18Fh)) is enabled for performance monitoring counters, some event counts may not be logged to PMCx_CNT fields in IA32_LBR_x_INFO MSR (1200h to 121Fh).
Implication	Due to this erratum, the processor may report incorrect lower values in LBR's record data IA32_LBR_x_INFO.PMCx_CNT.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL066	Bandwidth Allocation for USB 2.0 Periodic Devices Behind USB 3.2 Hub
Problem	The xHCI controller may allocate more bandwidth than can be supported when two or more USB 2.0 periodic devices (Isochronous or Interrupt) are connected behind a USB 3.2 hub.
Implication	Due to this erratum, the xHCI controller may not service the USB 2.0 periodic devices within the required service interval. Intel has only observed missed service intervals when two USB 2.0 Isochronous cameras are connected behind a USB 3.2 Hub and are streaming at 1080p or higher resolution, sometimes resulting in video disruptions on the second camera stream.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL067	Instruction Timeout VM Exit Will Not Set Guest RFLAGS.RF During #UD
Problem	When the VM-Execution Control "Instruction timeout" (bit 31) is set to 1, and a VM exit occurs with basic exit reason 75 (Instruction timeout) during the delivery of an invalid opcode (#UD) exception, the processor will not set Guest RFLAGS.RF (bit 16).
Implication	When the VMM resumes the guest at the same instruction and an instruction breakpoint is set in the guest, it may trigger double instruction breakpoints (#DB).
Workaround	A mitigation for this erratum is for VMMs to set guest RFLAGS.RF before resuming guest execution following an instruction timeout VM exit.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL068	PCIe Gen5 Link Exit from L1 Sub-state Low Power State
Problem	PCIe Gen5 Link may not wake from the Link L1 Low Power sub-State when the processor attempts short back-to-back PCIe config space accesses or when an end Point device asserts CLKREQ.
Implication	Due to this erratum, PCIe Gen5 capable port may hang or the system may hang with Machine Check Error MSCOD= MSCOD=THREE STRIKE (E184H), MCACOD INTERNAL TIMER (0400H).
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL069	I3C Interface Minimum Clock Timing Specifications
Problem	The following clock timing specifications of Serial IO and Integrated Sensor Hub (ISH) I3C interfaces may not meet the minimum timing requirements listed in the MIPI specification version 1.0: • Serial IO and ISH: SCL and SDA fall time when operating in I2C mode for Fast Mode (400 Kbps) and Fast Mode Plus (1 Mbps) speeds. • Serial IO and ISH: SCL rise time when operating in I2C mode for Fast Mode (400 Kbps). • Serial IO: SCL low time when operating in I2C mode for Fast Mode (400 Kbps) and Fast Mode Plus (1 Mbps) speeds.
Implication	There are no known functional implications due to this erratum and Intel has not observed this erratum with any commercially available system.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL070	ICR Read May Not Generate an APIC-Access VM Exit
Problem	When "virtualize APIC accesses" and "IPI virtualization" are both 1, and both "virtual-interrupt delivery" and "APIC-register virtualization" are 0, a memory-mapped read of the Interrupt Command Register (ICR) may return data from the virtual-APIC page (VICR) instead of generating an APIC-access VM exit.
Implication	Due to this erratum, software that relies on an APIC-access VM exit for ICR reads may function incorrectly.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL071	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the stack pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL072	N/A. Erratum has been removed.
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ARL073	N/A. Erratum has been removed.
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ARL074	Incorrect Guest RFLAGS.RF on VM Entry
Problem	When the user-interrupt feature is enabled (CR4.UINTR=1) and a VM exit occurs during user-interrupt delivery due to a fault, the processor may incorrectly set the guest RFLAGS.RF (bit 16) to 1 on VM entry.
Implication	Due to this erratum, software that relies upon the guest RFLAGS.RF may function incorrectly.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL075	Execution of IRET in Compatibility Mode May Free Supervisor Shadow Stack Token
Problem	When the shadow-stack feature of Intel® Control-flow Enforcement Technology (Intel® CET) shadow stack is enabled (SH_STK_EN bit 0 of IA32_U_CET MSR (6A0h) or IA32_S_CET MSR (6A2h)), an IRET (Interrupt Return) instruction that does not change the current privilege level or the shadow stack should not find a supervisor shadow-stack token.
Implication	When this erratum occurs, if an execution in compatibility mode (CS.L=0 within IA-32e mode) finds a busy supervisor shadow-stack token, it will free the token rather than ignore it. This erratum could affect system software that has written a busy shadow-stack token in the middle of a shadow stack (rather than a free token at the bottom). Intel has not observed this erratum with any commercially available software.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL076	Incorrect VM Exit Reason When MOV SS or POP SS Followed by an x2APIC MSR Access
Problem	A MOV SS or POP SS instruction immediately followed by a write to an X2APIC MSR (800H–8FFH) that causes a VM Exit may incorrectly report MOV SS/POP SS is still active in the VM-exit reason (bit[1] of the guest interruptibility-state field in the VMCS).
Implication	When this erratum occurs, software may encounter delayed interrupt delivery until the next instruction executes. Intel has only observed this behavior in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL077	Overcount of Topdown Bad Speculation Performance Monitoring Events
Problem	The Performance Monitoring Events TOPDOWN BAD_SPECULATION.FASTNUKE (Event: 73H, UMask: 02H, UMask2: 00H) and TOPDOWN BAD_SPECULATION.ALL (Event: 73H, UMask: 00H, UMask2: 00H) overcounts the number of issue slots consumed by the backend that were discarded (work lost component) due to Memory Renaming (MRN), Memory Ordering, or Memory Disambiguation machine clears.
Implication	Due to this erratum, software monitoring the events for Bad Speculation due to some types of machine clears will overcount. Additionally, software using Topdown Methodology Analysis (TMA) may observe the counts exceed the total number of slots. Therefore, performance debug software may incorrectly point to bad speculation as cause of performance degradation.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL078	Undercount of Performance Monitoring Events for Walk Pending
Problem	The Performance Monitoring Events DTLB_LOAD_MISSES.WALK_PENDING (Event: 08H, UMask: 10H) and DTLB_STORE_MISSES.WALK_PENDING (Event: 49H, UMask: 10H) may undercount when more than seven page walks are active in a single cycle.
Implication	Due to this erratum, software monitoring the events for Walk Pending may undercount for workloads with a high rate of TLB misses.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

ARL079	Missing #UD Fault for Non-Enumerated AVX-IFMA Instructions
Problem	AVX-IFMA instructions may not generate an #UD fault when the respective AVX_IFMA CPUID feature flag (CPUID.07H.01H:EAX[23]) reports 0.
Implication	Due to this erratum, software that relies on the AVX-IFMA instructions to generate an #UD fault when not enumerated may not work correctly. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes .

5 ***Specification Changes***

None.

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6 ***Specification Clarification***

None.

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7 *Document Change*

None.

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