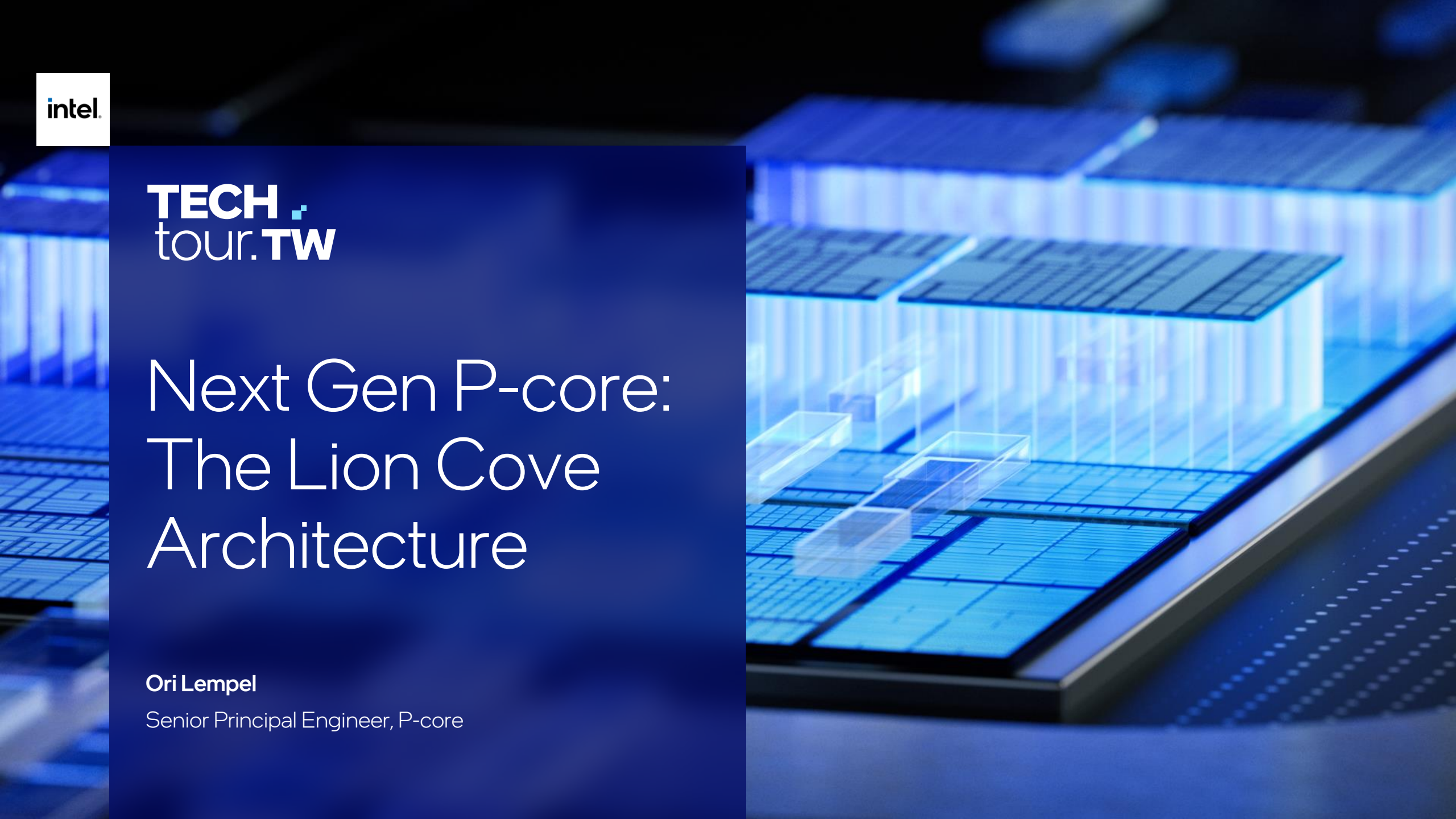

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Next Gen P-core: The Lion Cove Architecture

Ori Lempel

Senior Principal Engineer, P-core

Lion Cove uArch

Goals

Performance & area efficiency

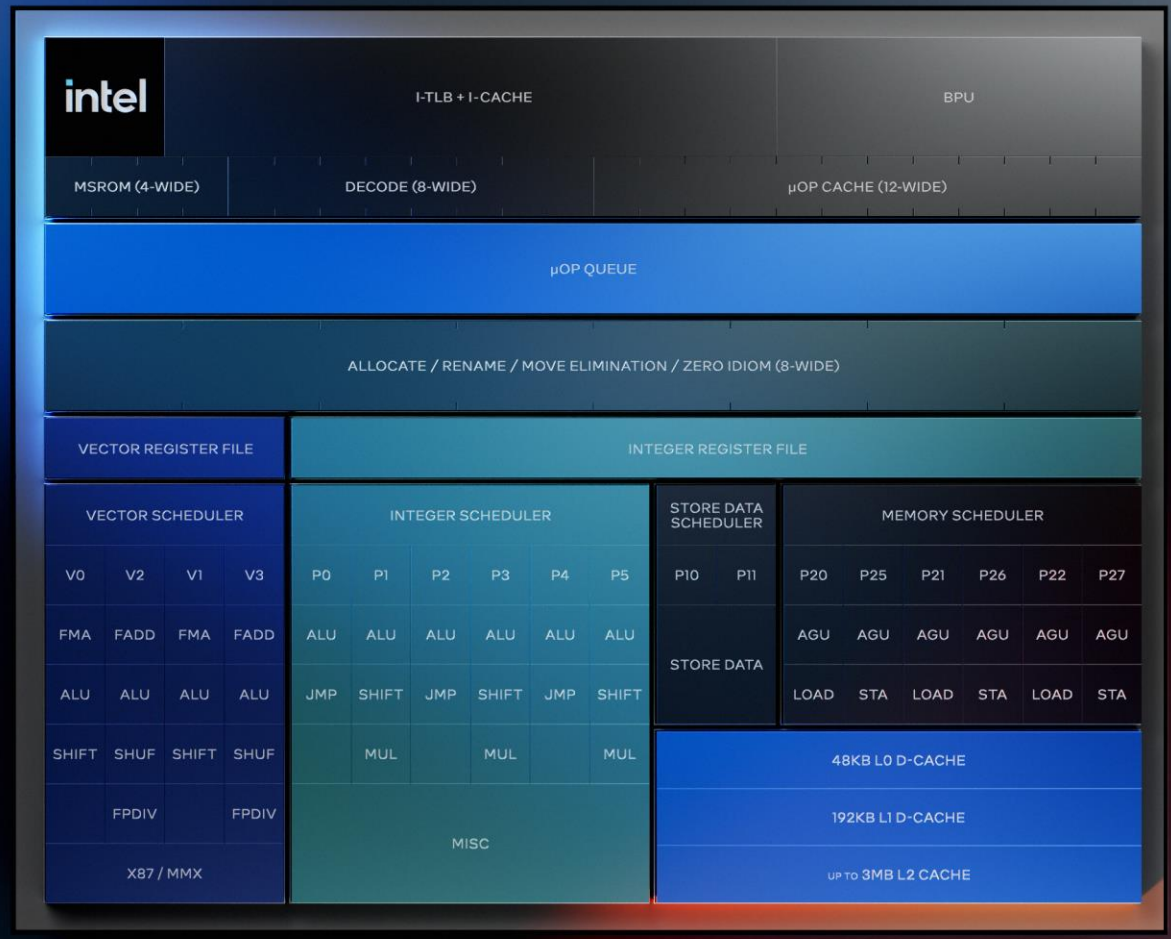
Optimize ST perf/watt and perf/area for client SoCs

Overhaul microarchitecture

Generational IPC improvement and future scalability

Modernize design database

Accelerate innovation going forward



Lion Cove uArch

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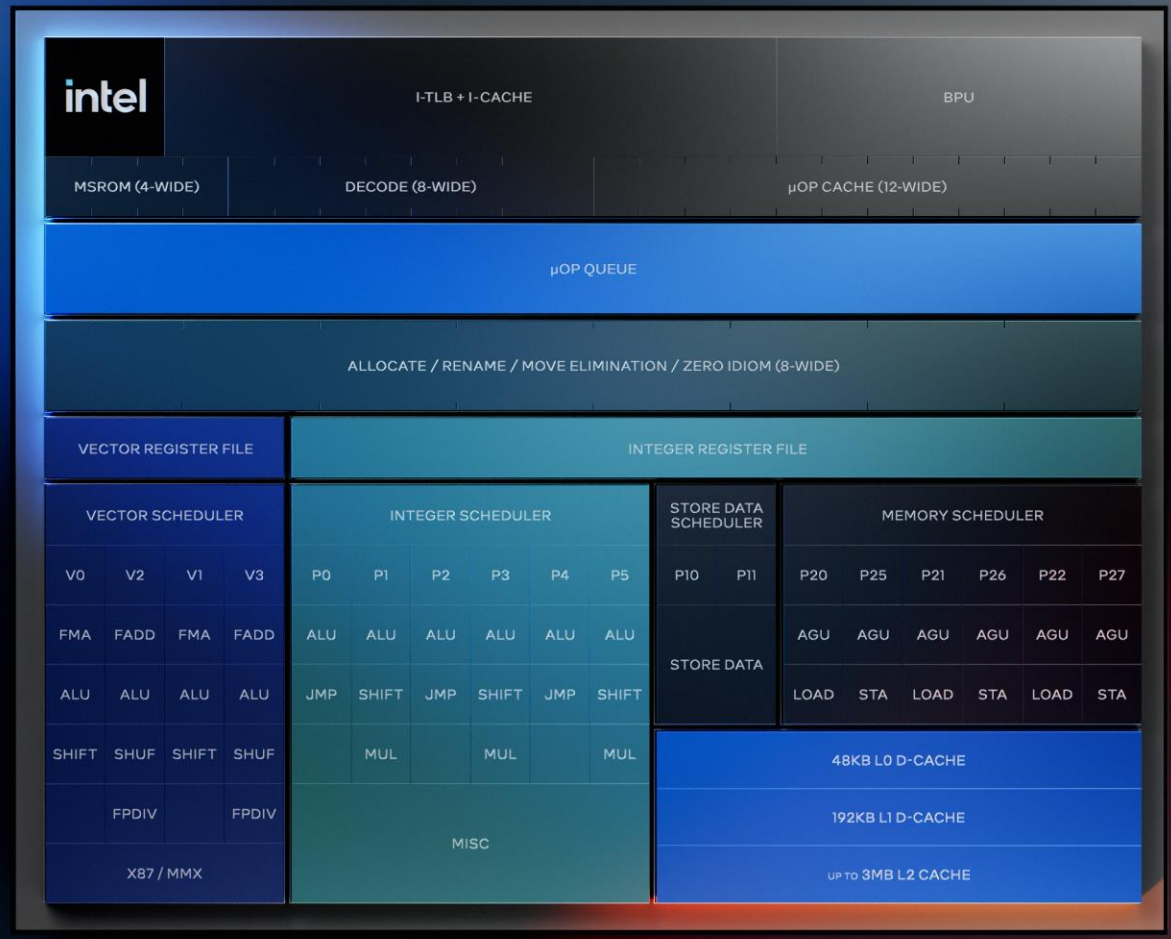
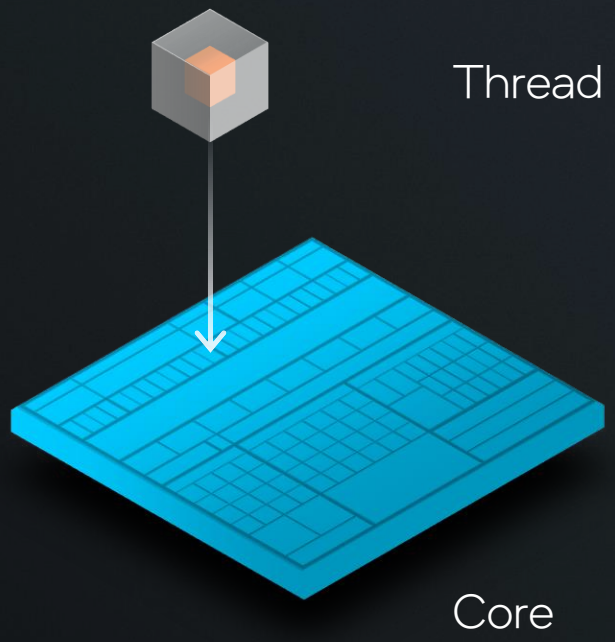


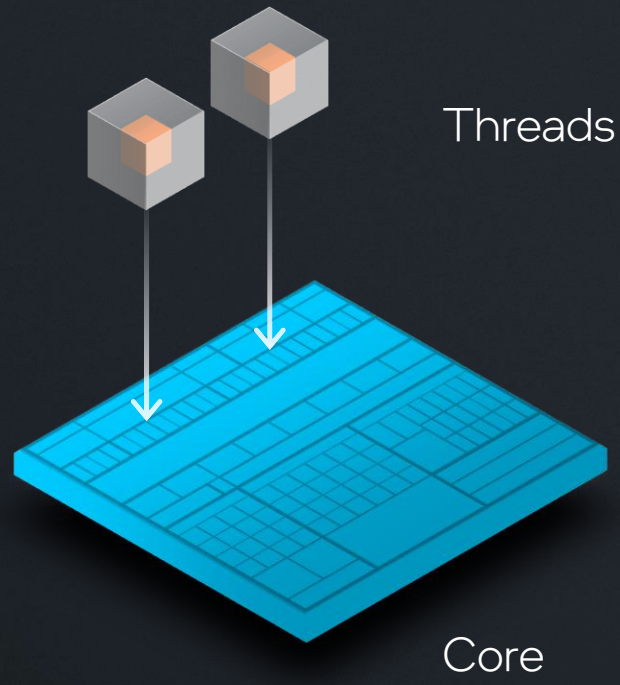
Intel® Hyper-Threading Technology

Revolutionized core computing

Before



After

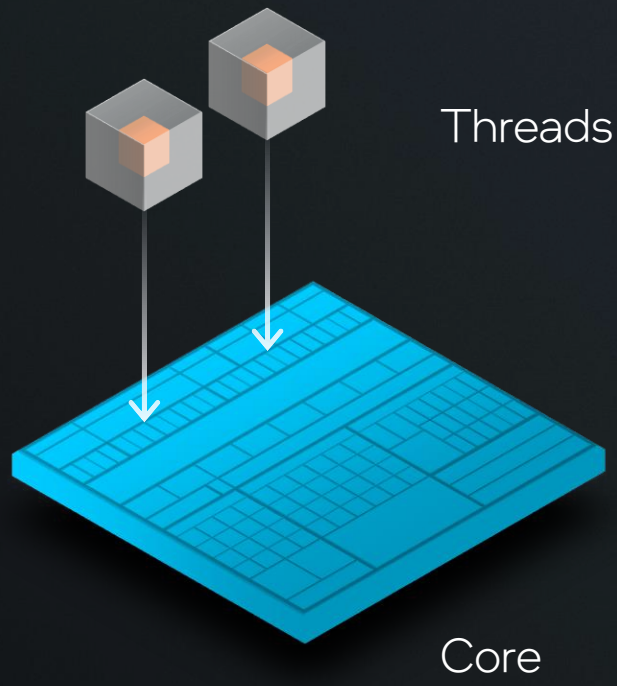


Hyper-Threading Benefits

Improving IPC within the same core area footprint

Hyper-Threading

on latest P-cores

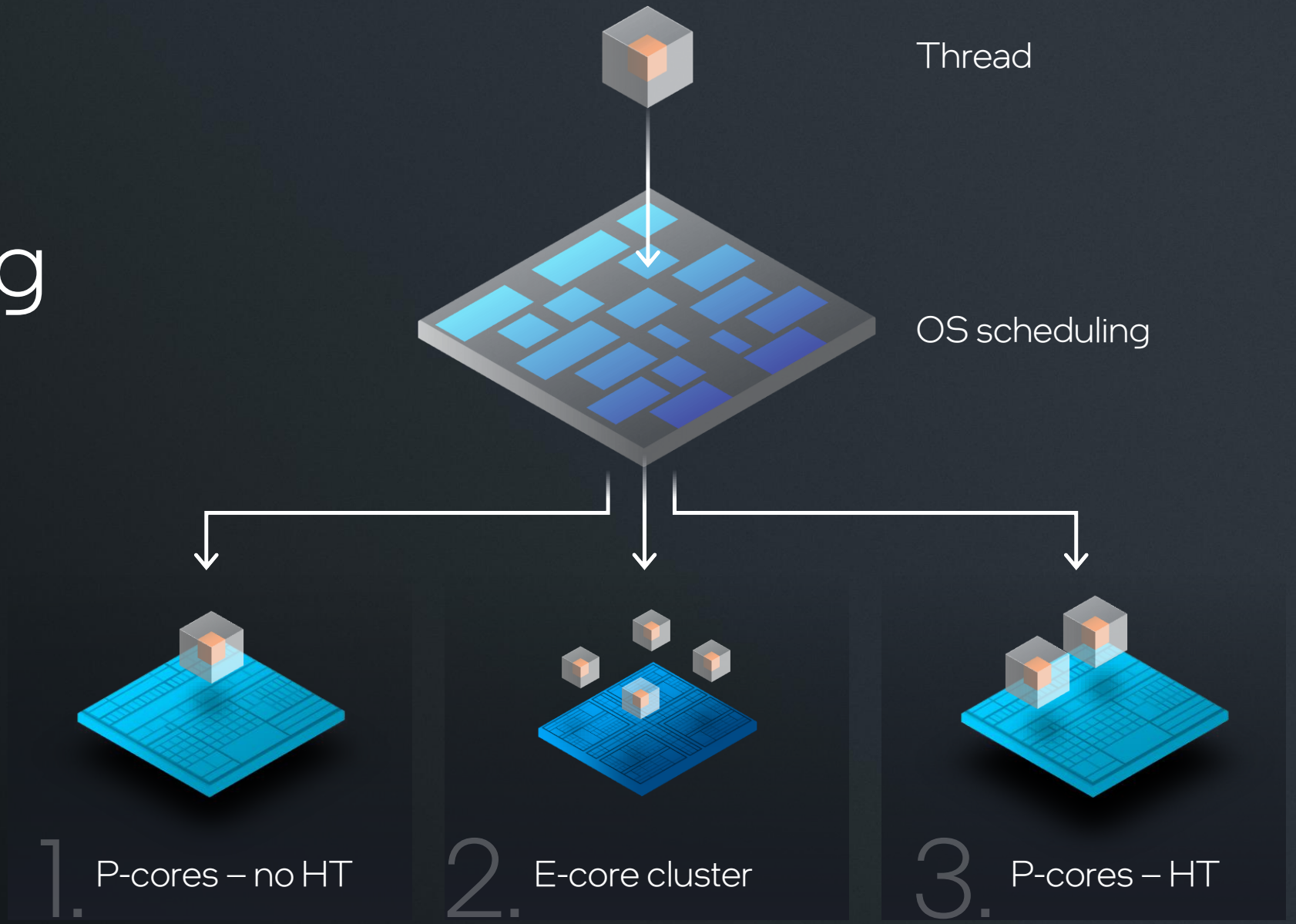


+30%
IPC
(or throughput)

+20%
Cdyn
(power at same V/F)

"Projected architecture representation of best-case benefits of Hyperthreading feature on vs. off on a latest generation P-core

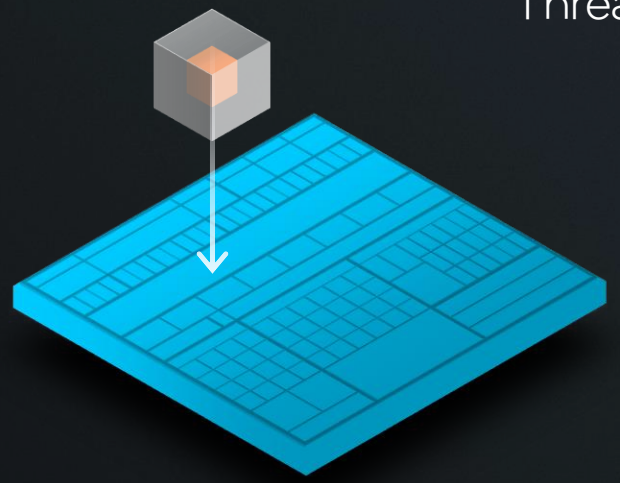
Typical Scheduling on Hybrid Client



Single-Thread Optimized

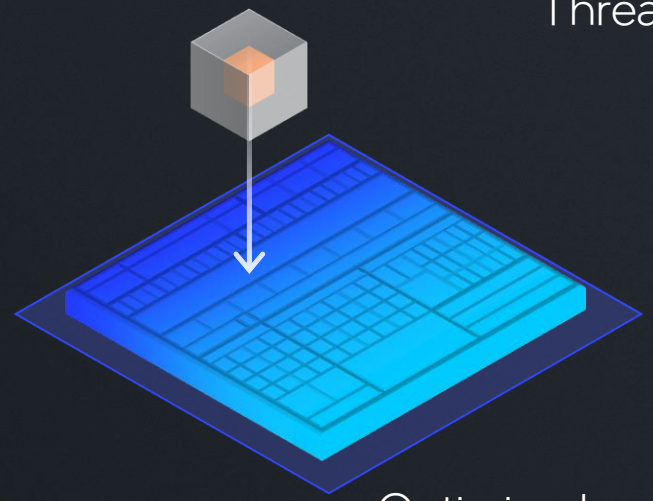
P-core

With Hyper-Threading OFF



P-core

Efficiency optimized



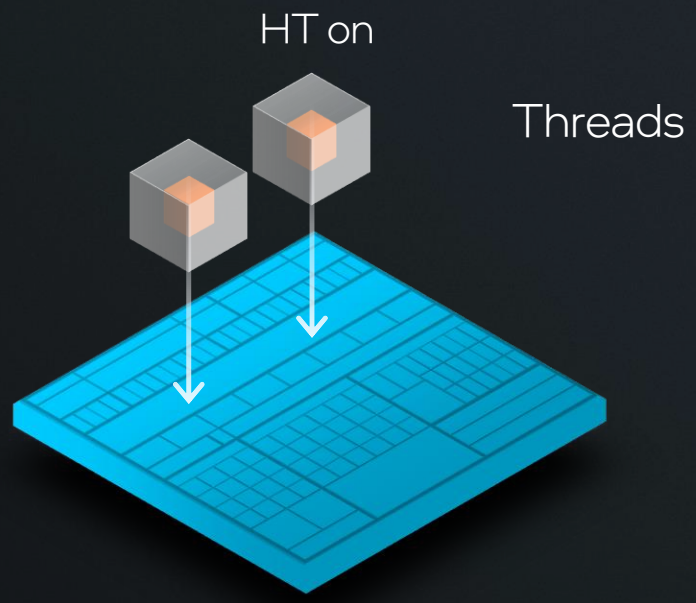
+15%	+10%	+30%
Perf/power	Perf/area	Perf/power/area

*All figures estimated based on hypothetical comparison of HT-capable P-core vs. Optimized P-core

Single-Thread Optimized

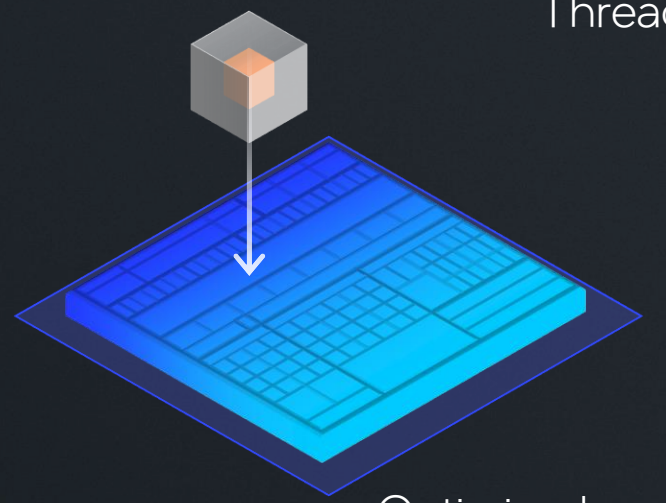
P-core

With Hyper-Threading ON



P-core

Efficiency optimized

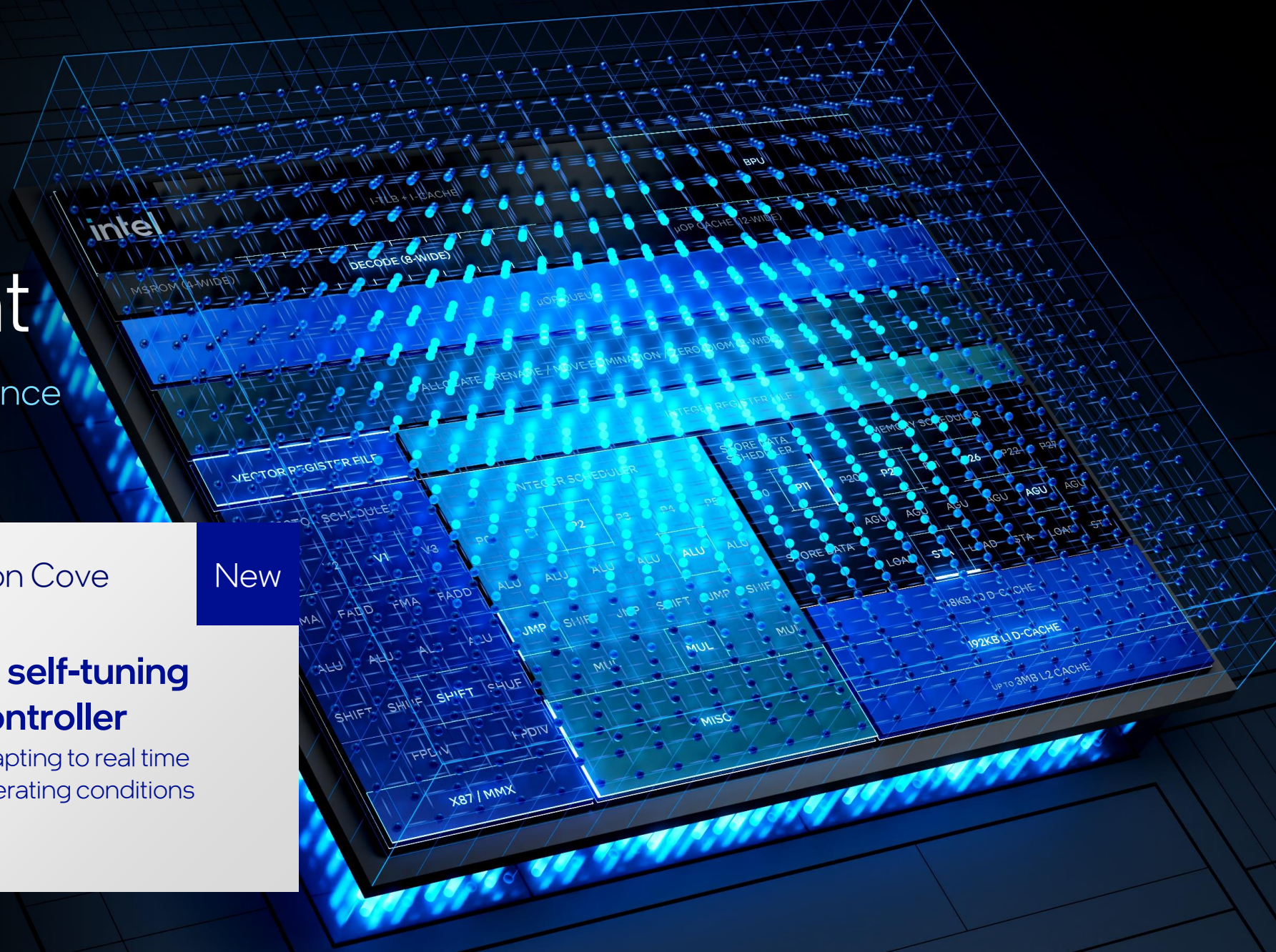


+5%	-15%	+15%
Perf/power	Perf/area	Perf/power/area

All figures estimated based on hypothetical comparison of HT-capable P-core vs. Optimized P-core

Enhanced Power-Management

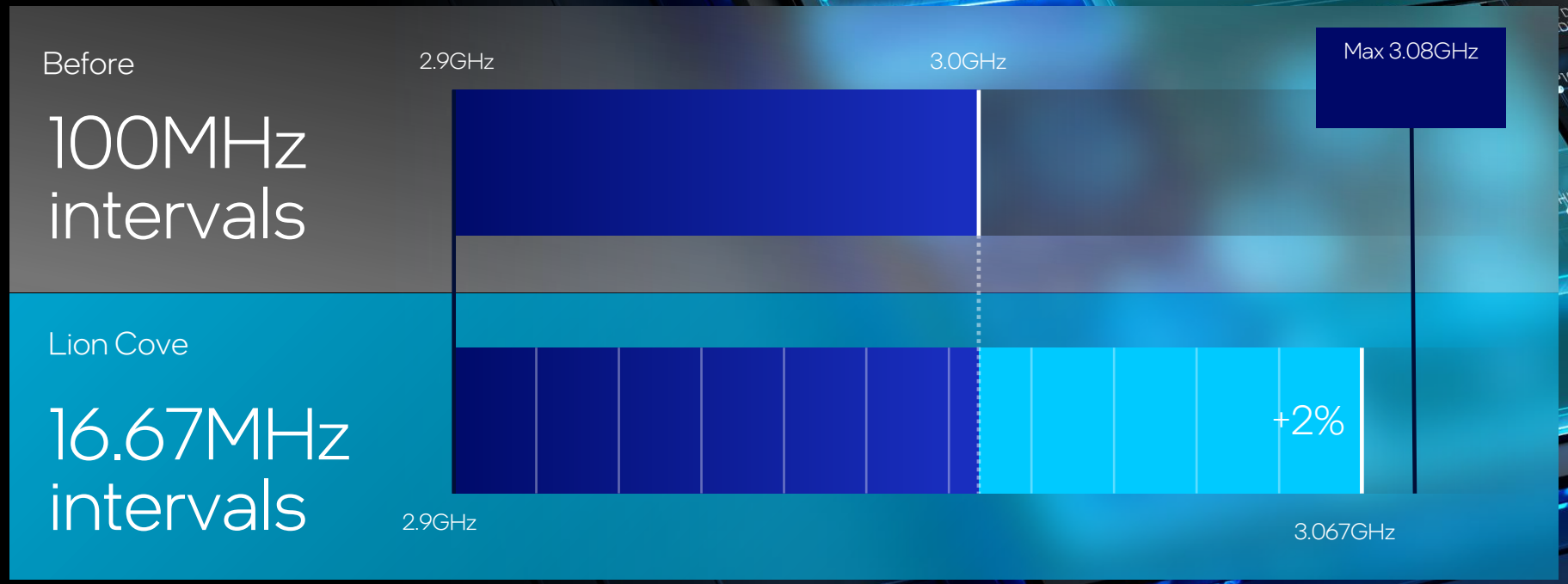
For higher sustained performance



Before	Lion Cove	New
Static preset thermal guard-bands	**AI self-tuning controller** adapting to real time operating conditions	

Finer Clock Granularity

Extract more performance for a given core power budget



Lion Cove uArch

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Performance & area efficiency

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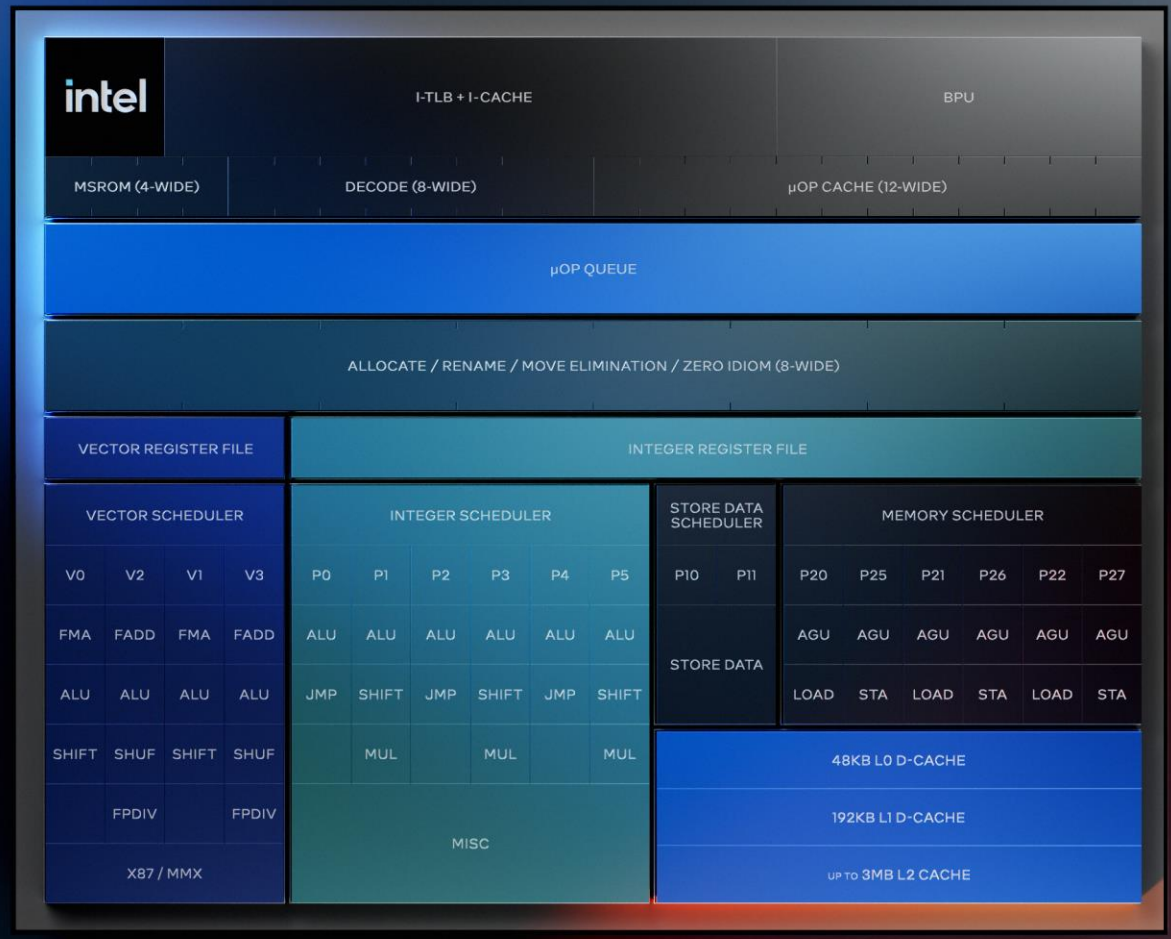


Overhaul Microarchitecture

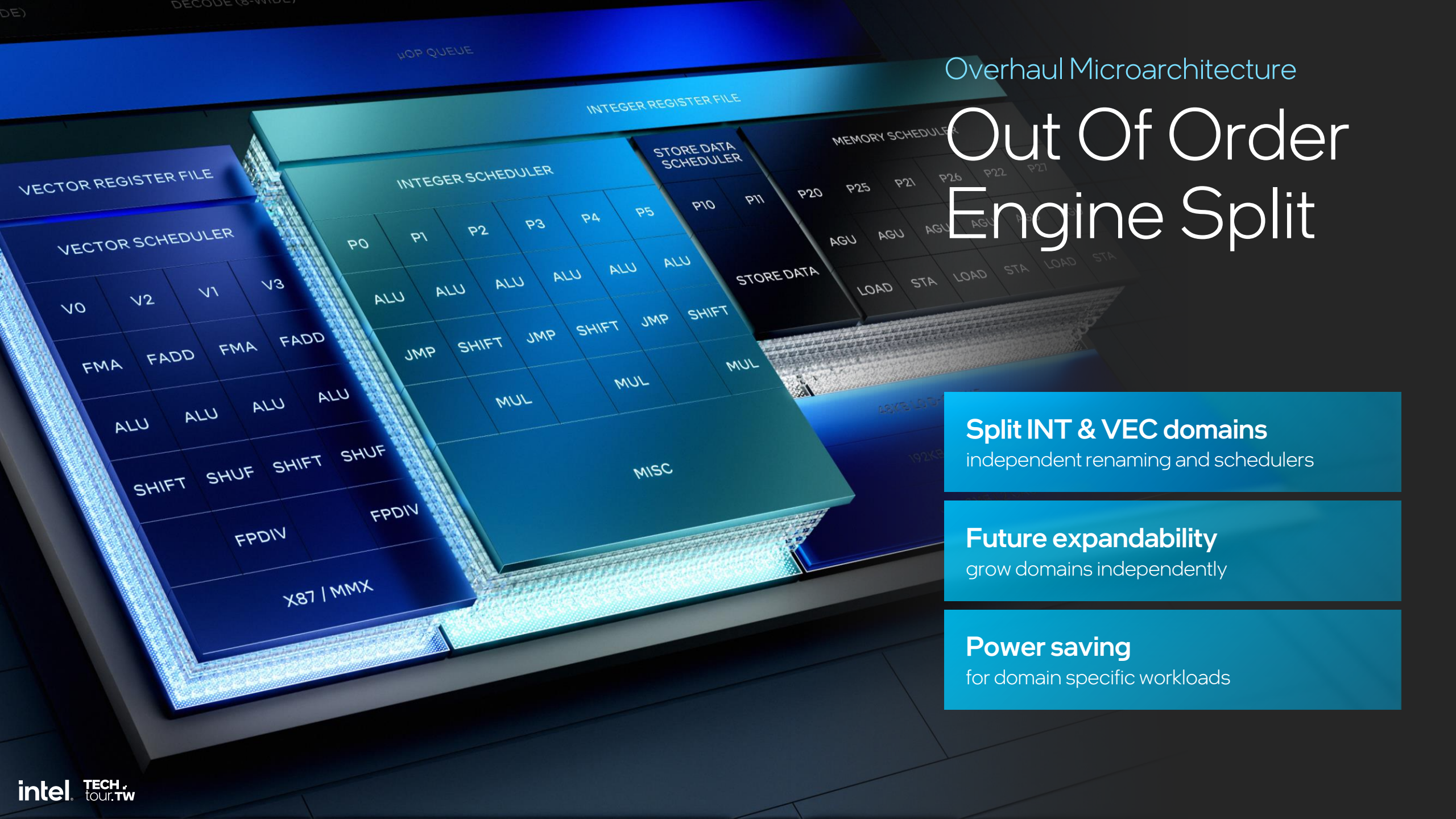
Front-end

Up to 8x
larger prediction block

Wider fetch
and increased decode BW

Uop cache capacity growth
and read BW increase

Uop queue capacity growth



Overhaul Microarchitecture

Out Of Order Engine Split

Split INT & VEC domains
independent renaming and schedulers

Future expandability
grow domains independently

Power saving
for domain specific workloads

Overhaul Microarchitecture

Out Of Order Engine

- 6 ▸ 8 wide alloc/rename
- 8 ▸ 12 wide retirement
- 512 ▸ 576 deep instruction window
- 12 ▸ 18 execution ports

Overhaul Microarchitecture

Integer Execution

- **5 ▸ 6** integer ALU
- **2 ▸ 3** jump units
- **2 ▸ 3** shift units
- **1 ▸ 3** mul 64×64->64

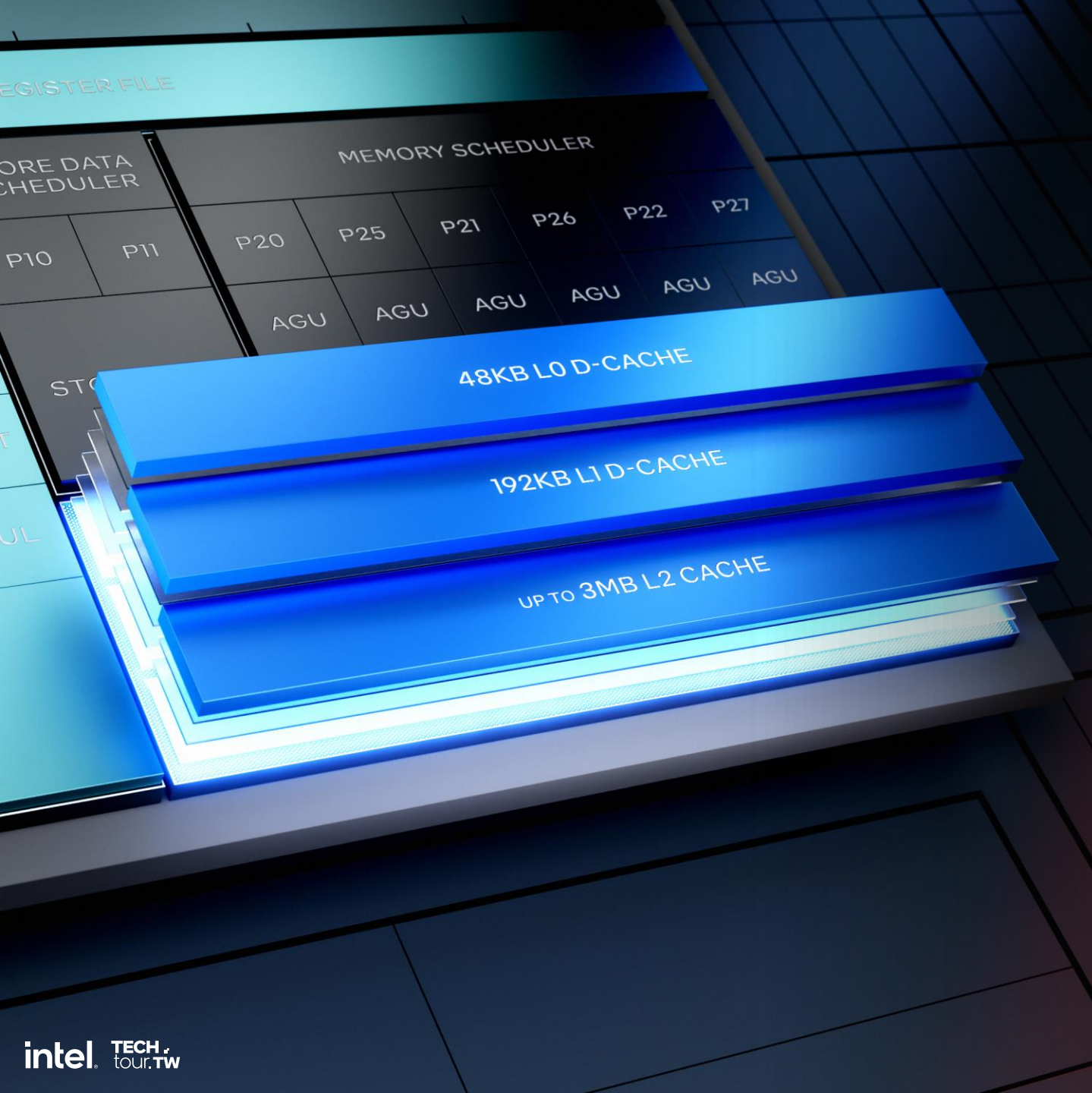
Overhaul Microarchitecture

Vector Execution

3 ▸ 4 SIMD ALUs
(256b)

2 FMAs @ 4 cycle latency
(256b)

1 ▸ 2 FP dividers
with improved latency/ throughput
(256b)



Uarch Infrastructure Overhaul

Memory Subsystem

Redwood Cove (D-side):

Level	Load-To-Use	Read BW	Capacity
L1	5	3x256b / 2x512b	48KB
L2	16	2x64B	2MB

Lion Cove (D-side):

Level	Load-To-Use	Read BW	Capacity
L0	4	3x256b / 2x512b	48KB
L1	9	2x64B	192KB
L2	17	2x64B	2.5MB / 3MB

Uarch Infrastructure Overhaul

Memory Subsystem

96 ▸ **128** pages DTLB

2 ▸ **3** STA AGU

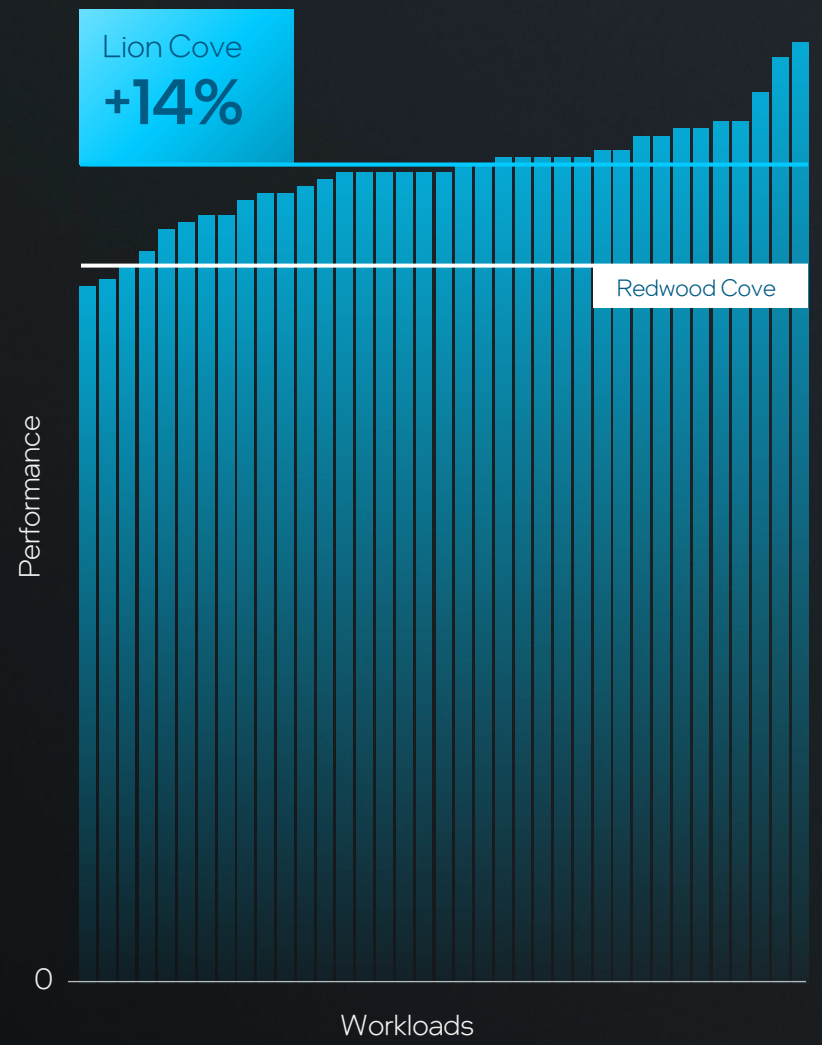
Lion Cove IP Performance Summary

Double-digit IPC over prior generation Redwood Cove and emphasizes PnP at lower TDP

Lion Cove in Lunar Lake

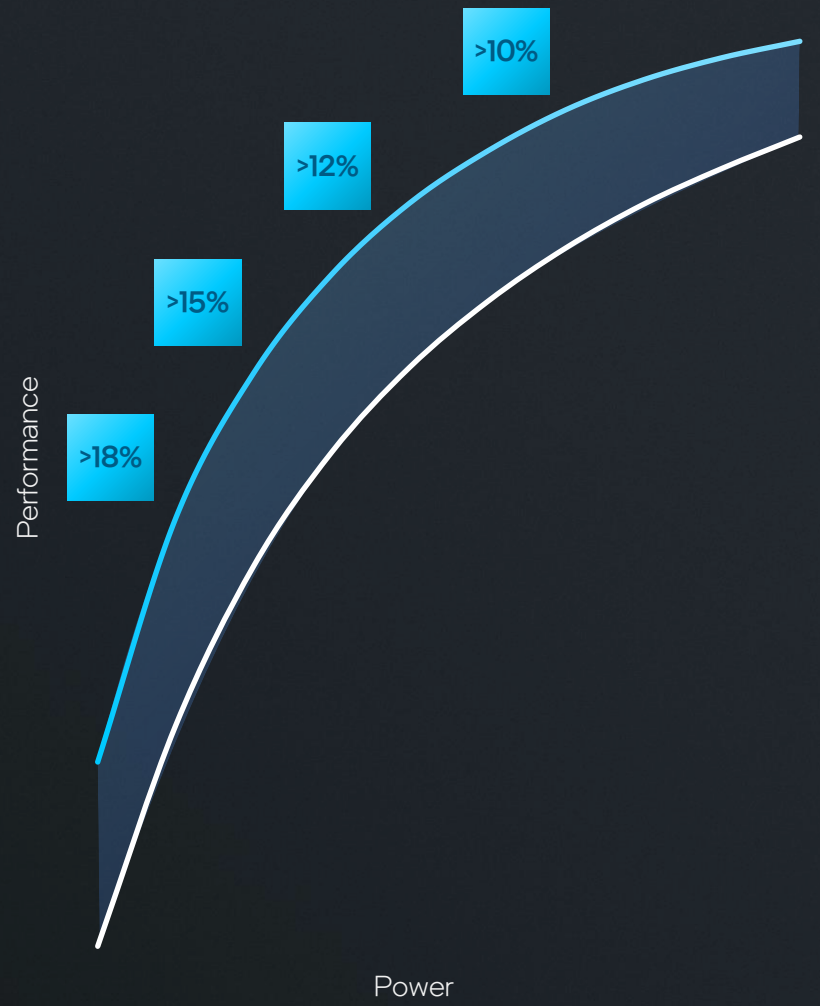
Redwood Cove in Meteor Lake

IPC



Iso frequency benefit estimate across: components of SPECrate2017_int_base and SPECrate2017_fp_base (both estimated) running 1 copy, Cinebench R23 Single Core, Cinebench 2024 Single Core, Geekbench 5.4.5 Single-Core, Geekbench 6.2.1 Single-Core, WebXPRT 4, Speedometer

Performance at power



Results are based on SPECrate2017_int_base (estimated) running n copies. Based on measurement on an Intel internal reference validation platforms at a fixed PL1 power setting.

Lion Cove uArch

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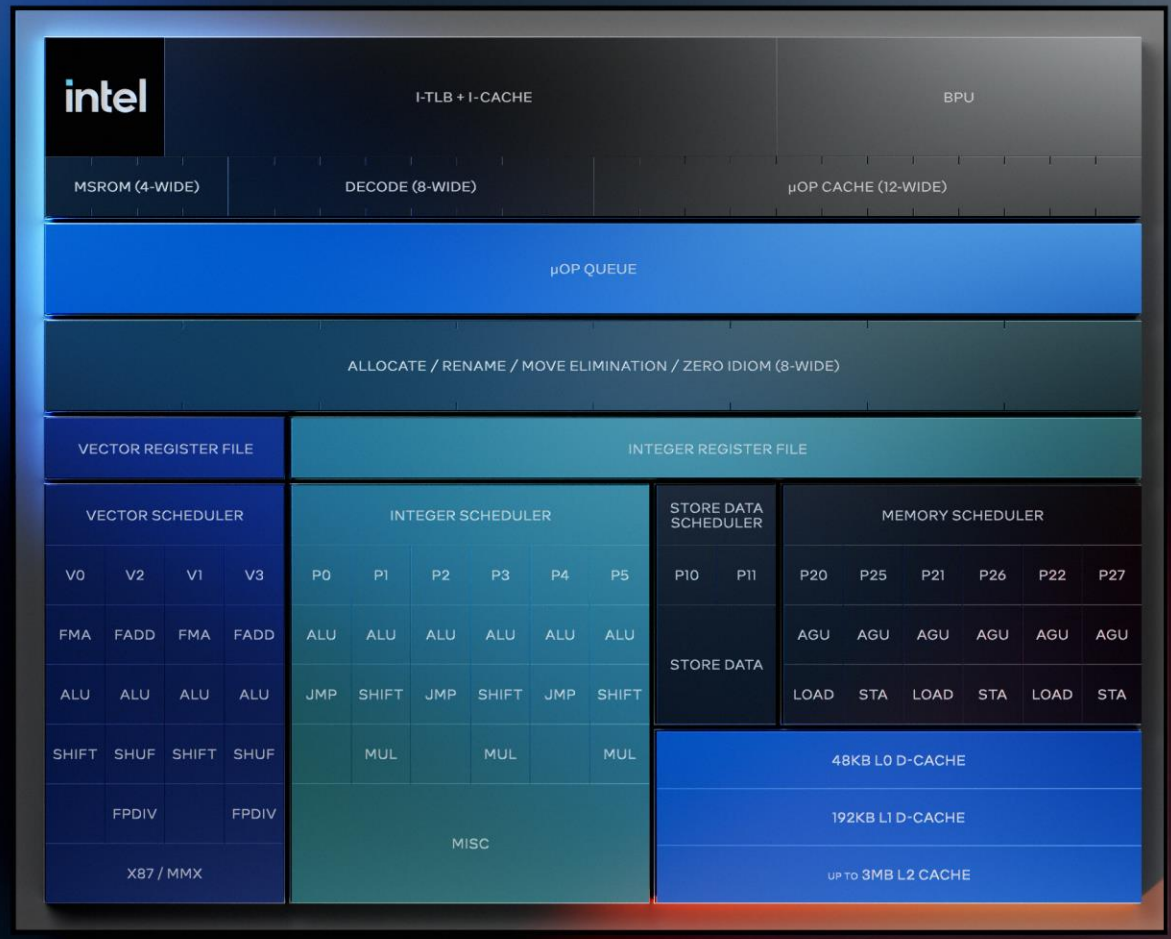
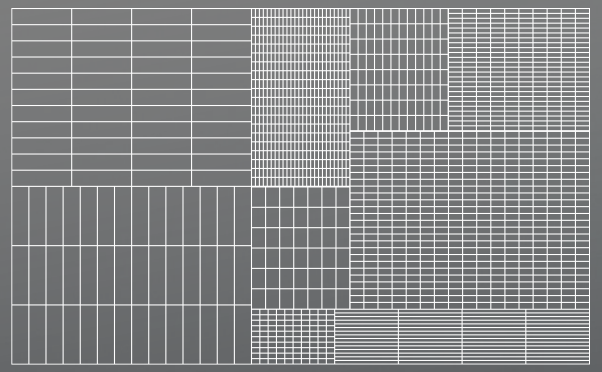
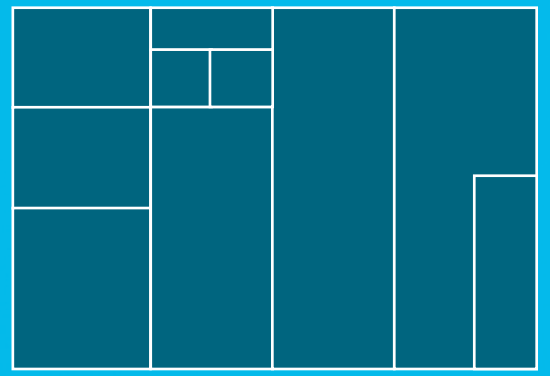


Modernizing P-core Database



Before **Sea of "Fubs"**

- Small partitions - 10s of K cells
- Latch dominated
- Process node specific



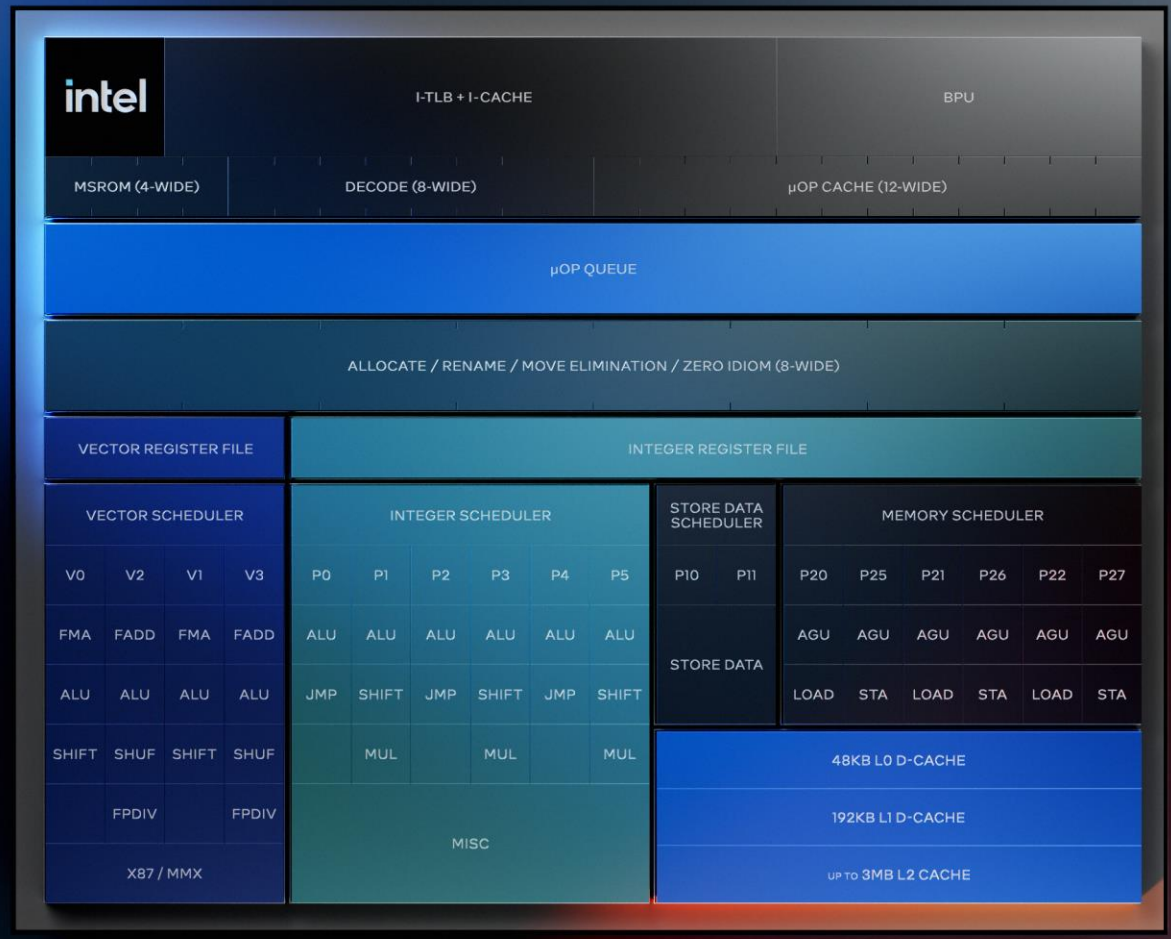
After **Sea of Cells**

- Big partitions - 100s of K cells to 1M cells
- Flop dominated
- 99% process-node-agnostic

Lion Cove

Our most performant yet efficient CPU core architecture

- **Double digit** IPC uplift
- Future **scalability**
- State-of-art **power management**
- **Step function in peak ST** PnP & PPA
- **Modern design TFM**

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Thank You

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APPENDIX

	SLIDE 5: Hyper-Threading Benefits
Hyper-Threading scaling characterized as adding 30% IPC (or throughput) for 20% Cdyn (or power at the same V/F	Projected architecture representation of best-case benefits of Hyperthreading feature on vs. off on latest generation P-core microarchitecture.
	SLIDES 7-8: Single-Thread Optimized
Removing Hyper-Threading we get comparable single thread IPC for 15% lower Cdyn and 10% smaller area which translates into 15% better performance per power and 30% better performance per-power per-area vs. a single thread running on a Hyper-Threading-capable core	All figures estimated based on hypothetical comparison of an HT-capable P-core vs. an Efficiency optimized P-core.
	SLIDE 19: Lion Cove IP Performance Summary
Lion Cove core delivers 14% better IPC vs. Redwood Cove core	Ilso frequency benefit estimate across: components of SPECrate2017_int_base and SPECrate2017_fp_base (both estimated) running 1 copy, Cinebench R23 Single Core, Cinebench 2024 Single Core, Geekbench 5.4.5 Single-Core, Geekbench 6.2.1 Single-Core, WebXPRT 4, Speedometer
Lion Cove Performance at different power levels vs. Redwood Cove	Results are based on SPECrate2017_int_base (estimated) running n copies. Based on measurement on an Intel internal reference validation platforms at a fixed PL1 power setting.


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