Product Change Notification

108482 - 01

Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

Americas Contact: asmo.pcn@intel.com

Asia Pacific Contact: apacgccb@intel.com

Europe Email: eccb@intel.com

Japan Email: jccb.ijkk@intel.com

Product Change Notification

Change Notification #: 108482 - 01

Change Title: Intel® Core™2 Duo Processor E8500, E8400 and Dual-Core Intel® Xeon® Processor E3110, PCN 108482-01, Product Design, Core Stepping Conversion, Reason for Revision: Updated Products Affected / Intel Ordering Codes Tables

Date of Publication: Jun 02, 2008

Key Characteristics of the Change:

Product Design

Forecasted Key Milestones:

Date of Samples Availability:	May 19 -30, 2008
Date of Qualification Data Availability:	August 11, 2008
Date Customer Must be Ready to Receive Post-Conversion Material:	August 20, 2008
Date of First Availability of Post-Conversion Material:	June 27, 2008

The date of "First Availability of Post-Conversion Material" is the projected date that a customer may expect to receive the Post-Conversion Materials. This date is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the Post-Converted Materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.

Description of Change to the Customer:

Reason for Revision: Updated “Products Affected / Intel Ordering Codes” tables

The Intel® Core™2 Duo Processor E8500, E8400 and Dual-Core Intel® Xeon® Processor E3110 will undergo the following changes for the C-0 to E-0 stepping conversion:

- New SSpec and MM numbers for the converting products
- CPUID will change from 0x10676 to 0x1067A
- Power Status Indicator (PSI) is supported
- PECI implementation change
- New instructions added – XSAVE/XRSTOR
  - New ISA extension for save/restoring context of x87, SSE, and future processor state
- New feature added - ACNT2
  - Improved mechanism for determining processor utilization. To be used for more efficient P-state determination.
- Package change to Halide free package

Customer Impact of Change and Recommended Action:

- No BIOS or board changes required for ACNT2 feature. The operating system (if it supports this feature) will check the feature flag and enable this feature.
- No Bios changes required for XSAVE/XRSTOR. Refer to *Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 3A: System Programming Guide* and *Intel® Advanced Vector Extensions Programming Reference* for details.
- Power state Indicator (PSI) will require new circuits on the board to support the feature. Please refer to the Platform Design guide document for chipset that support the PSI feature.

Qualification required for the new features and instructions supported on these processors. Please refer to the appropriate documents for more details.

Minimal re-qualification and/or validation is expected for features already supported on C-0 stepping. Intel® Core™2 Duo Processor E8500, E8400 and Dual-Core Intel® Xeon® Processor E3110 will require a BIOS update. Once customers implement the BIOS update, they will be able to accept both C-0 and E-0 stepping material. Customers should be ready to receive a combination of both C-0 stepping material and E-0 stepping material by the "Date Customer Must be Ready to Receive Post-Conversion Material" above. For customers implementing their own BIOS, it is necessary to incorporate the latest BIOS to support the E-0 stepping. Please contact your local Intel representative for further technical questions.

Products Affected / Intel Ordering Codes:

Intel® Core™2 Duo Processors

Processor#, Frequency	Pre Conversion Product Code	Pre Conver-sion S-Spec	Pre Conversion MM#	Pre Conver-sion Stepping	Post Conversion Qualification Samples QDF#	Post Conversion Qual Samples MM#	Post Conversion Product Code	Post Conversion S-Spec	Post Conversion MM#	Post Conversion Stepping
E8400, 3 GHz	EU80570PJ0806M	SLAPL	893557	C-0	QHEZ	898147	AT80570PJ0806M	SLB9J	898841	E-0
E8500, 3.16 GHz	EU80570PJ0876M	SLAPK	893556	C-0	QHEY	898145	AT80570PJ0876M	SLB9K	898838	E-0

Dual-Core Intel® Xeon® Processor

Processor#, Frequency	Pre Conversion Product Code	Pre Conver-sion S-Spec	Pre Conversion MM#	Pre Conver-sion Stepping	Post Conversion Qualification Samples QDF#	Post Conversion Qual Samples MM#	Post Conversion Product Code	Post Conversion S-Spec	Post Conversion MM#	Post Conversion Stepping
E3110, 3 GHz	EU80570KJ0806M	SLAPM	893558	C-0	QHFA	898141	AT80570KJ0806M	SLB9C	898848	E-0

Reference Documents / Attachments:

Document:	Location #:

PCN Revision History:

Date of Revision:	Revision Number:	Reason:
May 22 , 2008	00	Originally Published PCN
Jun 2, 2008	01	Updated Products Table