



Product Change Notification

103349 - 00

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Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geography location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

Americas Contact: Your local account representative

Asia Pacific Contact: Your local account representative

Europe Email: eccb@intel.com

Japan Email: jccb.ijkk@intel.com

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Product Change Notification

Change Notification #: 103349 - 00
Change Title: D/120JCT-LS, PCN 103349-00, FYI, Releases new board assemblies that incorporates 3.3 volt version of QLSLAC, changes micro-controller, changes the front end protection fuses and changes to improve response time when performing a Memory Read.
Date of Publication: June 10, 2003

Type of Change Notification:
FYI - (For Your Information)

Key Characteristics of the Change:
Product Design

Forecasted Key Milestones:

Date of First Availability of Post-Conversion Material:	Jul 18, 2003
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The date of "First Availability of Post-Conversion Material" is the projected date that a customer may expect to receive the Post-Conversion Materials. This date is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the Post-Converted Materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.

Description of Change to the Customer:

Incorporates a 3.3 volt version of QLSLAC in place of 5 volt version and changes the micro-controller to provide timing required for the 3.3 volt QLSLAC. Change of the front end protection fuses on the Daughter board from 1¼ Amp to ½ Amp. Changes to PCI EEPROM to improve the response time associated with memory reads by configuring the PCI interface chip to issue retries within 3 PCI clocks.

Customer Impact of Change and Recommended Action:

This change is a design enhancement and has no impact on units in the field.

This change has been thoroughly evaluated to ensure that it does not have any negative functional implications to our customer.

Customers should modify their databases in order to place orders against the new order codes. See details below.

Products Affected / Intel Ordering Codes:

Board Products Table

Affected Pre-Change Product Code	Pre-Change MM#	Post Change Product Code	Post-Change MM#
D120JCTLSU	850172	D120JCTLSU	854889
D120JCTLSUCN	850174	D120JCTLSUCN	854915
D120JCTLSUIN	850175	D120JCTLSUIN	854916
D120JCTLSUJP	850173	D120JCTLSUJP	854914

Reference Documents / Attachments:

Document:

Location #:

PCN Revision History:

Date of Revision:

June 10, 2003

Revision Number:

00

Reason:

Originally Published PCN