



Product Change Notification

108114 - 00

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Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

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Product Change Notification

Change Notification #: 108114 - 00
Change Title: Intel® 5100 Memory Controller Hub Chipset, PCN 108114-00, Product Design, A-0 to B-0 stepping conversion
Date of Publication: December 11, 2007

Key Characteristics of the Change:

Product Design

Forecasted Key Milestones:

Date of Samples Availability:	Dec 11, 2007
Date of Qualification Data Availability:	Feb 22, 2008
Date Customer Must be Ready to Receive Post-Conversion Material:	May 16, 2008
Date of First Availability of Post-Conversion Material:	Feb 29, 2008

The date of "First Availability of Post-Conversion Material" is the projected date that a customer may expect to receive the Post-Conversion Materials. This date is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the Post-Converted Materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.

Description of Change to the Customer:

The MCH component of the Intel® 5100 chipset is converting from the A-0 stepping to the B-0 stepping. Please plan to validate the B-0 stepping of the Intel® 5100 chipset.

For technical details of the Intel® 5100 chipset, please refer to the latest Spec Update available on IBL (Intel Business Link), EDS (Electrical Design Specification) and PDG (Platform Design Guide) or go to the following link: <http://www.intel.com/products/chipsets/5100/>

Customer Impact of Change and Recommended Action:

The B-0 stepping of the Intel® 5100 chipset will be backward compatible for customers launching on the A-0 stepping, who do not plan to implement any of the new B-0 features. The B-0 will require the use of BIOS MRC 1.0 or later. Please see the Intel® 5100 chipset Spec Update.

New S-Spec and MM numbers are provided below for the 5100 Memory Controller Hub Chipset production units.

Products Affected / Intel Ordering Codes:

Pre Conversion Product Code	Pre Conversion MM#	Pre Conversion Stepping	Post Conversion Qualification Samples QDF#	Post Conversion Qualification Samples MM#	Post Conversion Product Code	Post Conversion S-Spec	Post Conversion MM#	Post Conversion Stepping
QG5100MCH	891936	A-0	Q 009	891559	QG5100MCH	S LARL	894163	B-0

Reference Documents / Attachments:

Document:

Location #:

PCN Revision History:

Date of Revision:

December 11, 2007

Revision Number:

00

Reason:

Originally Published PCN