Product Change Notification

107917 - 04

Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

Americas Contact: asmo.pcn@intel.com

Asia Pacific Contact: apacgccb@intel.com

Europe Email: eccb@intel.com

Japan Email: jccb.ijkk@intel.com

Product Change Notification

Change Notification #: 107917 - 04

Change Title: Intel® G31/P31 Express Chipset, PCN 107917-04, Product Design, A2 to B0 stepping change, Reason for Revision: Changes in Ballout

Date of Publication: January 11, 2008

Key Characteristics of the Change:

Product Design

Forecasted Key Milestones:

Date of Samples Availability:	Sep 28, 2007
Date of Qualification Data Availability:	Dec 21, 2007
Date Customer Must be Ready to Receive Post-Conversion Material:	Jan 04, 2008
Date of First Availability of Post-Conversion Material:	Dec 21, 2007

The date of "First Availability of Post-Conversion Material" is the projected date that a customer may expect to receive the Post-Conversion Materials. This date is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the Post-Converted Materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.

Description of Change to the Customer:

Reason for Revision: Changes in Ballout (See details below)

The Intel® G31 & P31 Express chipset will undergo the following changes for the A2 to B0 stepping change
- G31 and P31 REVID will change from 02h to 10h
- New QDF, S-spec and MM numbers for qualification and production units for the converting products.
- 220nF cap added to package to improve DDR2 power delivery
  - No functional impact with CAP stuffed on; customers will need to run quick regression tests at the highest (POR) FSB - DDR frequencies
  - Updated samples in limited quantity available October 26, 2007 with the same S spec and Material Master numbers listed in the product table below

Reason for Revision: Changes in Ballout details
- There are several ballout changes from the G31/P31 A2 step to B0 step. On the B0 package, the signals in the chart below are not connected from the solder ball to the die. These signals are connected internally on the B0 die. Note: If the existing board design is to use both A2 and B0 step silicon it is required to connect DDR_SRCOMP1, DDR_SRCOMP0, DDR_SMRCOMPVOL, and DDR_SMRCOMPVOH as outlined in the Intel® G31/P31 Express Chipset Platform Design

Guide. A2 and earlier silicon requires these signals be connected however B0 silicon does not. B0 silicon will operate properly with or without the signals connected on the board.

Ball name and location	G31/P31 B0 package	G31/P31 A2 package
RSVD (reserved) Ball # BB2	NC- No Connection Ball unconnected(open)	Ball connected to Die bump
DDR_SRCOMP1 Ball # AN3	NC- No Connection Ball unconnected(open)	Ball connected to Die bump
DDR_SRCOMP0 Ball # AN2	NC- No Connection Ball unconnected(open)	Ball connected to Die bump
DDR_SMRCOMPVOL Ball # AM8	NC- No Connection Ball unconnected(open)	Ball connected to Die bump
DDR_SMRCOMPVOH Ball # AM10	NC- No Connection Ball unconnected(open)	Ball connected to Die bump
RSVD (reserved) Ball # AA39	NC- No Connection Ball unconnected(open)	Ball connected to Die bump

Customer Impact of Change and Recommended Action:

As there are no logic changes between the A2 and B0 stepping, minimal validation effort for this conversion is expected

- The Intel® G31 & P31 Express Chipset will not require a BIOS update
- Customers will be able to accept both A2 stepping material and B0 stepping material
  - Ballout changes will not affect existing boards designed to operate with A2 step silicon. New designs only using B0 silicon can remove connections for DDR_SRCOMP1, DDR_SRCOMP0, DDR_SMRCOMPVOL and DDR_SMRCOMPVOH as these signals are connected internally on the die and do not need external connections.
- Intel anticipates no additional impact to customer platforms designed to Intel guidelines
- Customers must be ready to receive a combination of both A2 stepping material and B0 stepping material by January 4, 2008

Products Affected / Intel Ordering Codes:

Pre Conversion Product Code	Pre Conversion S-Spec	Pre Conversion MM#	Post Conversion Qualification Samples QDF#	Post Conversion Qualification Samples MM#	Post Conversion Product Code	Post Conversion S-Spec	Post Conversion MM#
LE82P31	S LAHX	892044	QR90	892989	LE82P31	SLASK	895744
LE82G31	S LAJ3	892056	QR89	892987	LE82G31	SLASJ	895740

Reference Documents / Attachments:

Document:	Location :
PCN 108110-00	http://content.intel.pcnalert.com/dm/d.aspx/1447A1FA-D0CE-4E84-9B46-84AFC5D1D851/PCN108110-00.pdf
CDI DOC ID: 355862 (Intel® G31/P31 Express Chipset Platform Design Guide)	http://www.intel.com/cd/edesign/library/asmo-na/eng/355862.htm

PCN Revision History:

Date of Revision:	Revision Number:	Reason:

September 20, 2007	00	Originally Published PCN
October 10, 2007	01	Add reference to P31 for change to REVID, add additional description verbiage, and change date for post conversion MM numbers availability
November 2, 2007	02	Addendum for addition of Post Conversion Product Information
November 20, 2007	03	Correction to REVID
January 11, 2008	04	Changes in Ballout between A2 and B0 stepping.