# Product Change Notification

**Change Notification #:** 117689 - 00

**Change Title:** Intel® Stratix® 10 10 Devices, PCN 117689-00, Documentation, Datasheet, User Guides, and Reference Documents Updates

**Date of Publication:** July 15, 2020

## Key Characteristics of the Change:

Documentation

## Forecasted Key Milestones:

**Table 3**

| Milestone | Availability |
|---|---|
| **Availability of Intel Stratix 10 Device datasheet update** | Now |
| **Availability of Intel Stratix 10 Device Design Guidelines update** | Now |
| **Availability of Intel Stratix 10 Pin Connection Guidelines update** | Now |
| **Availability of Intel Stratix 10 Configuration User Guide update** | Now |
| **Availability of Intel Stratix 10 HPS Technical Reference Manual update** | Now |
| **Availability of Intel Stratix 10 SoC FPGA Boot User Guide** | Now |

## Description of Change to the Customer:

This is the same change described in ADV2021 issued on July 10, 2020.

Intel® is notifying customers of important updates to Intel Stratix® 10 Device Datasheet, User Guides, and other reference documents.

Refer to Table 1 for the list of major updates and Table 2 for further details.

**Table 1**

| Updates | Reference for further details |
|---|---|
| Clarification of nCONFIG Operation | Table 2; S# 1 |
| Removal of SDMMC Configuration Scheme in Intel Stratix 10 Devices | Table 2; S# 2 |
| Removal of estimated configuration time specification in Intel Stratix 10 Device Datasheet | Table 2; S# 3 |
| Correction of typo error in Intel Stratix 10 Device Datasheet | Table 2; S# 4 |
| Updated bit stream sizes for selected Intel Stratix 10 Devices | Table 2; S# 5 |
| Updated Intel Stratix 10 GX 10M Device specifications | Table 2; S# 6 |

**Table 2**

| S# | Update Details | Updated Resource Links |
|---|---|---|
| 1. | **Clarification of nCONFIG Operation:**<br><br>To ensure error recovery under all circumstances, Intel recommends that you design your system to support power cycling the device if needed. In almost all use cases, asserting nCONFIG will provide adequate error recovery, however, a power cycle may be required in rare instances. A power cycle completely re-initializes the device, samples MSEL, reads the fuses and runs the SDM BootROM code.<br>Device power up and power down sequences must be followed during the power cycle. | • Intel Stratix 10 Device Design Guidelines<br>• Intel Stratix 10 Pin Connection Guidelines<br>• Intel Stratix 10 Configuration User Guide<br>• Intel Stratix 10 HPS Technical Reference Manual |
| 2. | **Removal of SDMMC Configuration Scheme in Intel Stratix 10 Devices:**<br><br>Intel is removing support for the SD/MMC configuration scheme for Intel Stratix 10 devices. SD/MMC is currently not enabled in the Intel Quartus Prime software for customer use. | • Intel Stratix 10 Device Datasheet<br>• Intel Stratix 10 Device Design Guidelines<br>• Intel Stratix 10 Pin Connection Guidelines<br>• Intel Stratix 10 Configuration User Guide<br>• Intel Stratix 10 HPS Technical Reference Manual<br>• Intel Stratix 10 SoC FPGA Boot User Guide |
| 3. | **Estimated configuration time guidance:**<br><br>Maximum configuration time estimation in Table 104 and Table 105 in Intel Stratix 10 Device Datasheet has been removed.<br><br>For guidance on estimated configuration time, refer to section 2.6 of the Intel Stratix 10 Configuration User Guide. | • Intel Stratix 10 Device Datasheet<br>• Intel Stratix 10 Configuration User Guide |
| 4. | **Correction of typo error in Intel Stratix 10 Device Datasheet:**<br><br>Footnote (17) related to HPS_PORSEL in Intel Stratix 10 Device Datasheet has been removed. | • Intel Stratix 10 Device Datasheet |

<table>
<tr><th>S#</th><th>Update Details</th><th>Updated Resource Links</th></tr>
<tr><td>5.</td><td>Updated bit stream sizes for selected Intel Stratix 10 Devices:<br><br>Following are the bitstream size updates made in Table 103 in the Intel Stratix 10 Device Datasheet.
<table>
<tr><th rowspan="2">Product Line</th><th colspan="2">Compressed Configuration Bitstream Sizes (Mbits)</th></tr>
<tr><th>Change From</th><th>Change To</th></tr>
<tr><td>GX400, SX400</td><td>127</td><td>79</td></tr>
<tr><td>GX1650, GX2100, SX1650, SX2100</td><td>379</td><td>577</td></tr>
</table></td><td>• Intel Stratix 10 Device Datasheet</td></tr>
<tr><td>6.</td><td>Updated Intel Stratix 10 GX 10M Device specifications<br><br>Intel Stratix 10 GX 10M Device specifications have been added to the Intel Stratix 10 Device Datasheet.</td><td>• Intel Stratix 10 Device Datasheet</td></tr>
</table>

## Customer Impact of Change and Recommended Action:

Customers are requested to review the changes and determine the impact on their designs. Refer to the revision history of the updated documents for a complete list and history of updates.

For questions or support, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

## Products Affected / Intel Ordering Codes:

All Intel Stratix 10 Devices.

**The list of affected part numbers (OPNs) can be downloaded in Excel form:**
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2021-opn-list.xlsx

## PCN Revision History:

| Date of Revision: | Revision Number: | Reason: |
|---|---|---|
| July 15, 2020 | 00 | Originally Published PCN |

# Product Change Notification
# 117689 - 00

**INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

**Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.**

**Americas Contact:** asmo.pcn@intel.com
**Asia Pacific/PRC Contact:** apacgccb@intel.com
**Europe Email:** eccb@intel.com
**Japan Email:** jccb.ijkk@intel.com