Product Change Notification

108361 - 01

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Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

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Product Change Notification

Change Notification #:	**108361 - 01**
Change Title:	**Intel (R) CE5060 and CE5063 Tuners, PCN 108361-01, Manufacturing Site, Qualification of Additional Test and Assembly Site, Reason for Revision: Updated Drawing**
Date of Publication:	**April 25, 2008**

Key Characteristics of the Change:

Manufacturing Site

Forecasted Key Milestones:

Date of Qualification Data Availability:	Jun 30, 2008
Date Customer Must be Ready to Receive Post-Conversion Material:	Jun 10, 2008

Reason for Revision: Updated Drawing

Description of Change to the Customer:

In order to ensure continuous supply, Intel and their supplier have qualified an additional assembly and test location in Malaysia for the CE5060 and CE5063 Tuners. During the transition, customers may see products from either test location. Assembly will be transitioned in June.

There is a change to the assembly process; the packages from the new location will be sawn as opposed to punched.

There will be a minor change to part characteristics described in the data sheet, as the package outline drawing (POD) will change to reflect the 0.1mm maximum package thickness increase and edge profile.

Both changes conform to JEDEC MO-220. The new and old diagrams are attached as Appendices A and B.

Product assembled and tested at the new site will be of equal or better quality than the current product.

Customer Impact of Change and Recommended Action:

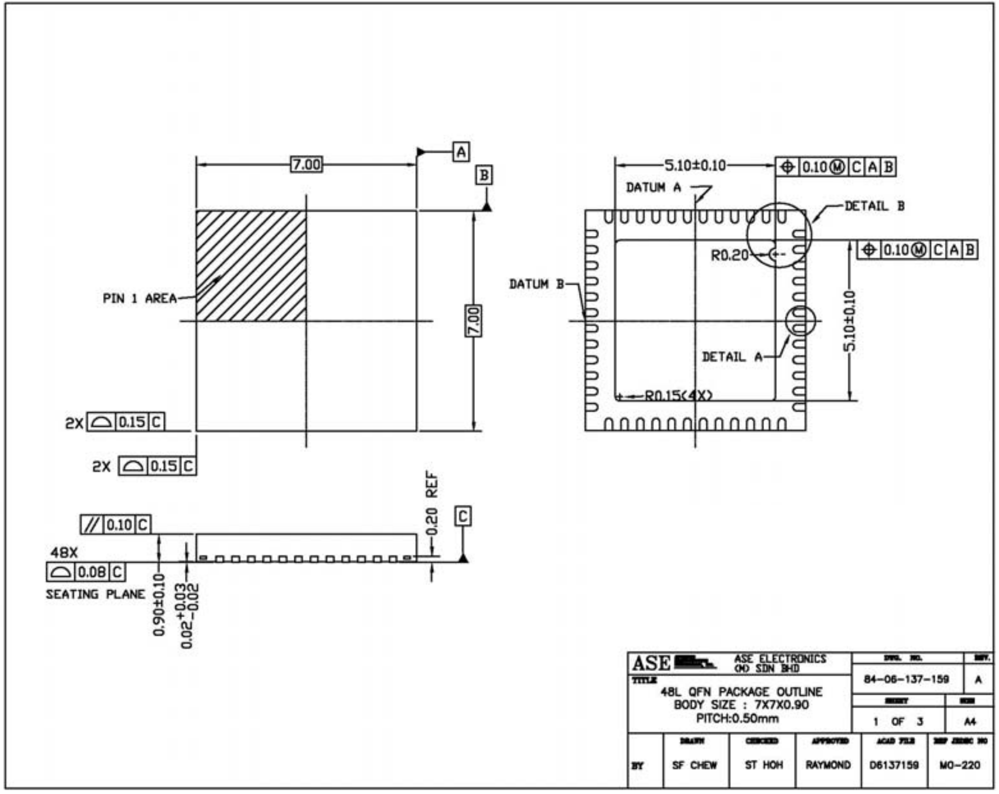
Intel anticipates no impact to customers, as there are no changes to function or reliability of the product. Changes to the form or fit are minor.

Products Affected / Intel Ordering Codes:

Affected Product Code	Affected S-Spec	Affected MM#
WGCE5060		882546
WGCE5060	S L9FQ	882547
WGCE5063	S L9FS	882550
WGCE5063		882555

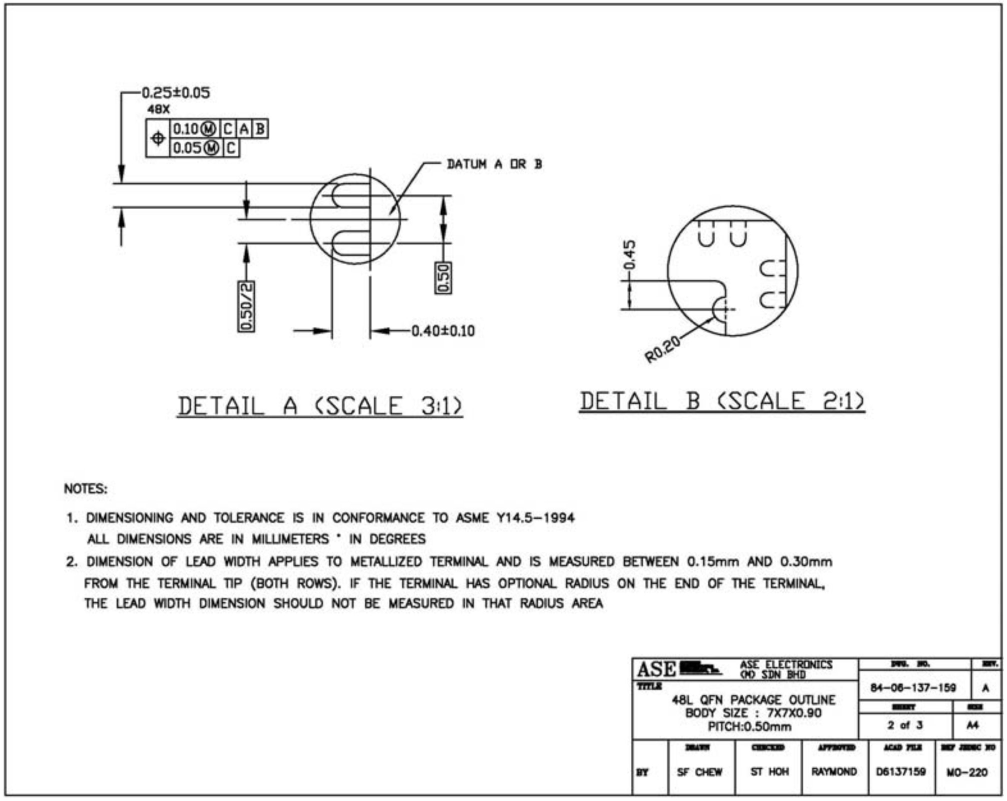
Reference Documents / Attachments:

Appendix A - ASE 48LD QFN 7X7 PACKAGE OUTLINE DRAWING (NEW):



ASE ELECTRONICS (M) SDN BHD
TITLE 48L QFN PACKAGE OUTLINE
BODY SIZE : 7X7X0.90
PITCH:0.50mm
DWG. NO. 84-06-137-159
REV. A
SHEET 1 OF 3
SIZE A4
BY
DRAWN SF CHEW
CHECKED ST HOH
APPROVED RAYMOND
ACAD FILE D6137159
REF JEDEC NO MO-220

(Appendix A continued):

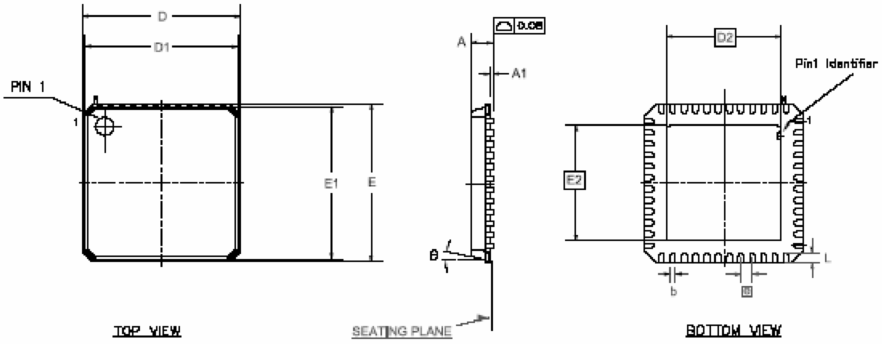


NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

ASE ELECTRONICS (M) SDN BHD
TITLE 48L QFN PACKAGE OUTLINE
BODY SIZE : 7X7X0.90
PITCH:0.50mm
DWG. NO. 84-06-137-159
REV. A
SHEET 2 of 3
SIZE A4
BY
DRAWN SF CHEW
CHECKED ST HOH
APPROVED RAYMOND
ACAD FILE D6137159
REF JEDEC NO MO-220

Appendix B – PACKAGE OUTLINE FOR 48 LEAD QFN (7 X 7 X 0.85MM)



	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.800	0.850	0.900
A1	0.005	0.025	0.045
b	0.180	0.230	0.300
D	6.900	7.000	7.100
D1	6.650	6.750	6.850
D2	5.10 BSC		
E	6.900	7.000	7.100
E1	6.650	6.750	6.850
E2	5.10 BSC		
N	48		
Nd	12		
Ne	12		
e	0.50 BSC		
L	0.300	0.400	0.500
θ	10°	11°	12°

Conforms to JEDEC MO-220

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS IN X & Y DIRECTION RESPECTIVELY.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. LEAD COUNT IS 48
5. PACKAGE WARPAGE MAX 0.08mm.
6. NOT TO SCALE.

PCN Revision History:

Date of Revision:	**Revision Number:**	**Reason:**
March 28, 2008	00	Originally Published PCN
April 25, 2008	01	Updated Drawing