



# Product Change Notification

## 106506 - 00

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Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

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# Product Change Notification

**Change Notification #:** 106506 - 00  
**Change Title:** Intel® 3100 Chipset, PCN 106506-00, Product Design, A-0 to A-1 Stepping Change  
**Date of Publication:** August 29, 2006

## Key Characteristics of the Change:

Product Design

## Forecasted Key Milestones:

<b>Date of Samples Availability:</b>	Sep 01, 2006
<b>Date of Qualification Data Availability:</b>	Sep 29, 2006
<b>Date Customer Must be Ready to Receive Post-Conversion Material:</b>	Nov 28, 2006
<b>Date of First Availability of Post-Conversion Material:</b>	Oct 07, 2006

*The date of "First Availability of Post-Conversion Material" is the projected date that a customer may expect to receive the Post-Conversion Materials. This date is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the Post-Converted Materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.*

## Description of Change to the Customer:

In order to correct three errata items associated with the Intel® (3100) chipset, Intel will be implementing a conversion from A-0 stepping to A-1 stepping. The three items that have been corrected are identified below. See the Intel® 3100 Chipset Specification Update for additional information.

### 1. Arbiter/EDMA Hang issue:

The Intel 3100 Chipset will lock-up when simultaneous downstream transactions are destined to the same PCI Express port PEA link.

### 2. 2Gb Refresh Violation.

The Intel 3100 Chipset violates the auto refresh cycle time (Trfc) specification for 2Gb technology DDR2-400 memory devices. The Intel 3100 Chipset currently has a refresh cycle time of 27 clocks (135 ns); However, a minimum of 39 clocks (195 ns) is necessary for 2Gb technology DDR2-400 memory devices.

### 3. Split Lock Hang issue.

A hang condition occurs when the processor issues split-locked request (R-R-W-W) to any PCI express device on Port B, combined with heavy traffic on both Port A and Port B.

**A new version of BIOS is required for the A-1 stepping of (3100).**

## Customer Impact of Change and Recommended Action:

Intel (R) 3100 Chipset A-1 is backwards compatible with the Intel (R) 3100 Chipset A-0.

Minimal validation effort is required for conversion due to no logic changes between A-0 and A-1 steppings of the Intel (R) 3100 Chipset.

Intel (R) 3100 Chipset A-1 stepping will require a BIOS Update.

Once customers implement the BIOS update, they will be able to accept both A-0 Step material and A-1 Step material

For customers implementing their own BIOS, it is necessary to incorporate the latest Micro-Code Update (MCU).

Customers should place order for A1 stepping with the new order codes provided in the Affected products table.

## Products Affected / Intel Ordering Codes:

### Component Product Table

Pre-Conversion Product Code	Pre-Conversion Spec/ROM	Pre-Conversion MM#	Post-Conversion Product Code	Post-Conversion Spec/ROM	Post-Conversion MM#
LE3100MICH	S L8YC	876677	LE3100MICH	S L9P0	883904
LE828007MICH	Q 176	871181	LE3100MICH	Q 773	885503

## Reference Documents / Attachments:

**Document:**

**Location #:**

## PCN Revision History:

**Date of Revision:**

August 29, 2006

**Revision Number:**

00

**Reason:**

Originally Published PCN