Product Change Notification

107909- 01

Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

Americas Contact: asmo.pcn@intel.com

Asia Pacific Contact: apacgccb@intel.com

Europe Email: eccb@intel.com

Japan Email: jccb.ijkk@intel.com

Product Change Notification

Change Notification #: 107909– 01

Change Title: Revised Boxed Dual-Core Intel® Xeon® 5100 Series (Woodcrest), PCN 107909-01, Product Design, B2 to G0 Stepping Change, Pushing out RTR and removing 2 GHz & 2.66 GHz from conversion

Date of Publication: October 18, 2007

Key Characteristics of the Change:

Product Design

Forecasted Key Milestones:

	Boxed Dual-Core Intel® Xeon® 5100 Series (Woodcrest)
Date Customer Must be Ready to Receive Post-Conversion Material:	November 21, 2007
Date of First Availability of Post-Conversion Material:	October 10, 2007

Description of Change to the Customer:

Reason for Revision: Pushing Ready to Received Date from October 10th to November 21st 2007. Also removing the 2 GHz and 2.66 GHz from the PCN and conversion; they may convert at a later date.

From the Original PCN:
The Boxed Dual-Core Intel® Xeon® processors 5100 Series Processors (Woodcrest) will convert from B-2 to G-0. Woodcrest will undergo the following change as it converts to G-0:

•Increased Energy Efficiency
- Certain SKUs will receive some amount of C1E power reduction on G-step
- SKUs already at the lowest bus to core frequency ratio or lowest voltage operating point cannot drop to the lower power state required for Extended HALT

- Enhanced Virtualization Technology
  - APIC Task Priority Register (TPR) Virtualization
  - NMI-window exiting
  - Advanced VM-exit information for INS & OUTS
- Woodcrest CPUID will change from 06F6 to 06FB
- New SSPEC and MM numbers for the converting products

Customer Impact of Change and Recommended Action:

Intel is finalizing a technical solution to allow mixed stepping configurations of B-step and G-step Woodcrest on Bensley platforms. This solution requires appropriate microcode updates to be loaded; current microcode updates for Woodcrest B-2 stepping will need to be replaced. Solution requires BIOS change; BIOS will detect mixed stepping configuration and set a bit in a Model Specific Register (MSR).

Customers creating their own BIOS should adhere to the guidelines provided in the "Dual-Core Intel(R) Xeon(R) Processor 5100 Series [Woodcrest] Mixed Steppings Support Guide, May 2007" that can be found on IBL

- IBL Path: IBL Home > Information Desk > Processors > Server/Workstation > Dual Core Intel® Xeon® Processor 5100 Series > Technical

Once customers implement the BIOS update, they will be able to support same stepping and mixed stepping configurations. Customers should be ready to receive a combination of both B-2 stepping material and G-0 stepping material by the "Date Customer Must be Ready to Receive Post-Conversion Material" above.

Products Affected / Intel Ordering Codes:

Boxed Dual-Core Intel® Xeon® 5100 Series (Woodcrest)

Processor#	Frequency	Pre Conversion			Post Conversion		
		Product Code	S-Spec	MM#	Product Code	S-Spec	MM#
5160	3.00G 4M 1333	BX805565160A	SLABS	890794	BX805565160A	SLAG9	892194
5160	3.00G 4M 1333	BX805565160P	SLABS	890795	BX805565160P	SLAG9	892200
5140	2.33G 4M 1333	BX805565140A	SLABN	890800	BX805565140A	SLAGB	892167
5140	2.33G 4M 1333	BX805565140P	SLABN	890801	BX805565140P	SLAGB	892169
5110	1.60G 4M 1066	BX805565110A	SLABR	890806	BX805565110A	SLAGE	892147
5110	1.60G 4M 1066	BX805565110P	SLABR	890807	BX805565110P	SLAGE	892149

Reference Documents / Attachments:

Document: **Location #:**

PCN Revision History:

Date of Revision:	Revision Number:	Reason:
September 10, 2007	00	Originally Published PCN
October 15, 2007	00	Pushing out RTR and removing the 2GHz and 2.66 GHz from PCN and conversion.