Product Change Notification

106324 - 00

Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

Americas Contact: asmo.pcn@intel.com

Asia Pacific Contact: apacgccb@intel.com

Europe Email: eccb@intel.com

Japan Email: jccb.ijkk@intel.com

Product Change Notification

Change Notification #:	**106324 - 00**
Change Title:	**Dual-Core Intel® Xeon® processor LV 2 GHz and 1.66 GHz (Sossaman), PCN 106324-00, Product Design, C-0 stepping to D-0 stepping change**
Date of Publication:	**June 2, 2006**

Key Characteristics of the Change:

Product Design

Forecasted Key Milestones:

Date of Samples Availability:	July 21st – Aug 4th, 2006
Date of Qualification Data Availability:	Sep 29, 2006
Date Customer Must be Ready to Receive Post-Conversion Material:	Oct 13, 2006
Date of First Availability of Post-Conversion Material:	Sep 15, 2006

The date of "First Availability of Post-Conversion Material" is the projected date that a customer may expect to receive the Post-Conversion Materials. This date is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the Post-Converted Materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.

Description of Change to the Customer:

Dual-Core Intel® Xeon® processor LV 2 GHz & 1.66 GHz will undergo the following changes for the C-0 to D-0 core processor stepping change:

- D-0 Stepping will require a BIOS update
- No platform thermal changes expected
- CPUID will change from 06E8h to 06ECh
- New QDF#, S-Spec, and MM numbers will be provided for D-0 Step Qualification Samples & Production units.
- C-0 is pin compatible with D-0

Please refer to the Dual-Core Intel® Xeon® Processor LV Electrical, Mechanical, and Thermal Specifications - NDA (EMTS), for the latest specification information.

Customer Impact of Change and Recommended Action:

As there are no logic changes between C-0 Stepping and D-0 Stepping, minimal validation effort for this conversion is expected. Dual-Core Intel® Xeon® processor LV D-0 stepping will require a BIOS Update. Once customers implement the BIOS update, they will be able to accept both C-0 Stepping material and D-0 Stepping material. Customers should be ready to receive a combination of both D-0 stepping material and C-0 stepping material by October 13th, 2006 (See "Date Customer Must be Ready to Receive Post-Conversion Material" above.) For customers implementing their own BIOS, it is necessary to incorporate the latest Micro-Code Update (MCU) to support D-0 stepping.

Products Affected / Intel Ordering Codes:

Dual-Core Intel® Xeon® processor LV 2 GHz and 1.66 GHz

Product Code	Frequency	Pre-Conversion Production Units		Post-Conversion Qualification Samples		Post-Conversion Production Units	
		S-Spec	MM #	QDF #	MM #	S-Spec	MM #
LF80539KF0282M	1.66GHz	S L98Q	879414	QNVY	879999	SL9HP	883109
LF80539KF0412M	2 GHz	S L8WT	876095	QNVI	880035	SL9HN	883108

Reference Documents / Attachments:

Document: **Location #:**

PCN Revision History:

Date of Revision:	Revision Number:	Reason:
June 2, 2006	00	Originally Published PCN