



# Product Change Notification

## 104048 - 00

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Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geography location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

Americas Contact: [asmo.pcn@intel.com](mailto:asmo.pcn@intel.com)

Asia Pacific Contact: [apacgccb@intel.com](mailto:apacgccb@intel.com)

Europe Email: [eccb@intel.com](mailto:eccb@intel.com)

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# Product Change Notification

**Change Notification #:** 104048 - 00  
**Change Title:** FLWB1400, FLWB1500, FLWB1501,  
FLWB1510 Framer, PCN 104048-00, FFF, C0  
to C1 Stepping Conversion  
**Date of Publication:** April 21, 2004

**Type of Change Notification:**  
FFF - (Form-Fit-Function)

**Key Characteristics of the Change:**  
Product Design

## Forecasted Key Milestones:

<b>Date of Samples Availability:</b>	May 28, 2004
<b>Date of Qualification Data Availability:</b>	Jul 23, 2004
<b>Date Customer Must be Ready to Receive Post-Conversion Material:</b>	Oct 18, 2004
<b>Date of First Availability of Post-Conversion Material:</b>	May 28, 2004

*The date of "First Availability of Post-Conversion Material" is the projected date that a customer may expect to receive the Post-Conversion Materials. This date is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the Post-Converted Materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.*

## Description of Change to the Customer:

- 1) In the JTAG circuitry of rev C0, the TDO output is updated on the rising edge of TCK instead of the falling edge as required by IEEE 1149.1 standard. As a result, the TDO output is  $\frac{1}{2}$  TCK cycle too early. This is fixed in rev C1 silicon to comply with the JTAG standard.
- 2) INTB and TEAB\_BERRB cell disable values do not match the output logic level when cell is disabled as per IEEE1149.1-2001 B.8.14.4 rule k) part 2) and therefore cannot be described using syntactically correct BSDL description. This is fixed in rev C1 silicon to comply with the JTAG standard.
- 3) The JTAG ID is changed from 0011 in C0 to 0100 in C1 as a result of the stepping.

## Customer Impact of Change and Recommended Action:

The C1 revision is pin, register, and form-factor compatible with C0 except as described above. The new devices will be marked FLWB1xxx.C1.

Customers currently using the C0 revision should prepare to receive and qualify revision C1 on their systems per the key milestones listed above. Samples will be available per the key milestones listed above. C0 material will be available to ship after the conversion date but will not be available after inventory is depleted.

## Products Affected / Intel Ordering Codes:

### Component Product Table

Pre-Conversion Product Code	Pre-Conversion Spec/ROM	Pre-Conversion MM#	Post-Conversion Product Code	Post-Conversion Spec/ROM	Post-Conversion MM#
FLWB1400.C0	Q E000	857096	FLWB1400.C1		862140
FLWB1500.C0	Q E000	857097	FLWB1500.C1		862141
FLWB1501.C0	Q E000	857098	FLWB1501.C1		862142
FLWB1510.C0	Q E000	857099	FLWB1400.C1		862143

## Reference Documents / Attachments:

Document:

Location #:

## PCN Revision History:

Date of Revision:

April 21, 2004

Revision Number:

00

Reason:

Originally Published PCN