Product Change Notification

Change Notification #:	**116724 - 02**
Change Title:	**Readiness Plan: EU RoHS Exemption 15, PCN 116724-02, Product Material, Order Code, Scope Change, Reason for Revision: Updated tables 1 and 2, and added table 3, which contains a list of issued PDNs on the phase out of parts with leaded 1st level interconnect (bumps)**
Date of Publication:	**January 15, 2021**

Key Characteristics of the Change:

Product Material, Order Code

Forecasted Key Milestones:

Date Customer Must be Ready to Receive Post-Conversion Material:	January 18, 2019

Description of Change to the Customer:

This revision is the same one communicated as a follow up to ADV1828, issued on January 15, 2021.

Reason for Revision:

1. Updated Table 1 with "Not Converting" product families.
2. Updated Table 2 Package Form information and added the Package Outline Drawing (POD) download/search tool link. Updated the Qualification status row.
3. Added Table 3 for list of issued product discontinuance (PDNs) on the phase out of parts with leaded 1st level interconnect (bumps).

Intel® is notifying customers of the readiness plan addressing the EU Restriction of Hazardous Substances (RoHS) Directive Exemption 15 scope change.

Exemption 15 scope for electronic products originally covered:

> Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit flip chip packages

Upon revision, the scope of Exemption 15a will only cover:

> Lead in solders to complete a viable electrical connection between the semiconductor die and carrier within integrated circuit flip chip packages where at least one of the following criteria applies:
> - a semiconductor technology node of 90 nm or larger;
> - a single die of 300 mm^2 or larger in any semiconductor technology node;
> - stacked die packages with die of 300 mm^2 or larger, or silicon interposers of 300 mm^2 or larger.

Changes will affect Field Programmable Grid Array (FPGA) Flip Chip products that currently use leaded solder bumps on the 1st level interconnect.

- Selected products will be converted to the leadfree SnAg1.8 solder bumps, replacing the 63/37 Sn-Pb bumps.
- There will also be a selected set of products that will not transition to leadfree solder bumps and were discontinued.

See Table 1 for the conversion plan and Table 2 for important information about the converted products.

Table 1: Leadfree Solder Bumps Conversion Plan

Conversion Timeline	**Converting in 2019** ***Immediately impacted with latest Ex15 scope change***	**Converting in 2020** ***Applicable Ex15a extension to year 2021***	**Not Converting (see note 2)**
Product Family	• Arria® II GX • Arria® V (small die) • Stratix® III (small die) • Stratix® IV (small die)	• Arria® II GZ • Arria® V (large die) • Stratix® III (large die) • Stratix® IV (large die) • Stratix® V	• Stratix® II & Stratix® II GX • Arria® GX • HardCopy II, HardCopy III, HardCopy IV, HardCopy Si Pro
Samples and Production Timeline	In production	Converted samples can be ordered now	Not Applicable

Note:

1. Small die is < $300mm^2$; Large die is $\geq 300mm^2$
2. Refer to Table 3 discontinuance notice list. PDN2041 issued for Stratix II, Stratix II GX, and Arria GX

Table 2: Important Information About the Converted Products

Ordering Code	New Ordering Part Numbers (OPNs) with the "G" suffix will be assigned to converted products. Existing OPNs with leaded solder bumps were retired and Product Discontinuation Notices (PDN) were issued to customers. See Table 3 for PDN list.
Quality and Reliability Qualification Status	Package reliability qualification testing has been successfully completed for all product families that are converting.
Assembly Site	The assembly sites are the same: ASE Taiwan and Amkor Korea.
Bill of Materials	The 63/37 Sn-Pb leaded bumps will be replaced with leadfree SnAg1.8 bumps. The leadfree solder bumps necessitated changes to other materials within the BOM (Bill of Materials) to meet manufacturability and package reliability requirements.

Package Form and Fit	There will be modifications to the package form and fit for Stratix III & Arria II GX (lidless package). Certain packages on other converted families may also have updated tolerances though no actual modification to the packages. Please update your Package Outline Drawings (POD) by looking up the part number and downloading "RoHS6 G Suffix" POD version from this search tool: https://www.intel.com/content/www/us/en/programmable/support/literature/lit-index/lit-pkg/package-search.html?type=search
Function and Electrical Specification	The change does not impact the function and electrical specifications of the affected products.

Table 3: Product Discontinuance Notification (PDNs) issued to OPNs with leaded 1st level interconnect (bumps).

PDN#	Scope	PDN Link
PDN2041	All Arria GX, Stratix II, Stratix II GX	https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/pdn2041.pdf
PDN2018	Selected Arria GX part numbers	https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/pdn2018.pdf
PDN2009	Part numbers with leaded solder balls as 2nd level interconnect and eutectic Tin-Lead bumps for 1st level interconnect for: Arria II, Arria V, Stratix III, Stratix IV, Stratix V.	https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/pdn2009.pdf
PDN2007	Part numbers ("N") with leaded 1st level interconnect (bumps) for: Arria II GZ, Arria V (FPGA & SoC), Stratix III, Stratix IV, Stratix V.	https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/pdn2007.pdf
PDN1926	Part numbers ("N") with leaded 1st level interconnect (bumps) for Arria II, Arria V (<365 KLEs), Stratix III (≤70 KLEs), Stratix IV (≤110 KLEs).	https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/pdn1926.pdf

Reason for Change:

This change is in preparation for the RoHS Directive Exemption 15 scope change. This change also aligns with Intel's long-standing commitment to preserving the environment, health, and safety.

Customer Impact of Change and Recommended Action:

It is recommended for customers to switch to the fully lead-free converted products (with the "G" suffix). Please see the link provided in the "Products Affected" section where the new OPNs of the converted parts are listed.

For more information, please contact your Sales representative or submit a Service Request at the My Intel support page.

Products Affected / Intel Ordering Codes:

The link below contains the list of affected OPNs with the corresponding conversion status and new OPN (where applicable).

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv1828-opn-list.xlsx

PCN Revision History:

Date of Revision:	Revision Number:	Reason:
January 18, 2019	00	Originally Published PCN
April 16, 2020	01	Updates to products conversion status and tables 1 and 2. Removed and corrected Exemption status of some products
January 15, 2021	02	Updated tables 1 and 2, and added table 3, which contains a list of issued PDNs on the phase out of parts with leaded 1st level interconnect (bumps)

Product Change Notification 116724 - 02

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

Americas Contact: asmo.pcn@intel.com
Asia Pacific/PRC Contact: apacgccb@intel.com
Europe Email: eccb@intel.com
Japan Email: jccb.ijkk@intel.com

Copyright © Intel Corporation 2021. Other names and brands may be claimed as the property of others.

3D XPoint, ACEX, Altera, APEX, AnyWAN, Arria, Avalon, Axxia, BlueMoon, BunnyPeople, Celeron, Centrino, Cilk, CONVERGATE, Cyclone, Docea, eASIC, easicopy, Enpirion, Flexpipe, Hyperflex, Intel, the Intel logo, Intel Adaptix, Intel Agilex, Intel Atom, Intel CoFluent, Intel Core, Intel. Experience What's Inside, the Intel. Experience What's Inside logo, Intel Falcon, Intel Inside, the Intel Inside logo, Intel Nervana, Intel Optane, Intel RealSense, Intel Shooting Star, Intel Sirius, Intel SpeedStep, Intel Unite, Intel vPro, Intel Xeon Phi, Iris, Itanium, MAX, Movidius, Myriad, neon, Nios, OpenVINO, the OpenVINO logo, Pentium, Puma, Quark, Quartus, SICOFI, Simics, SMARTi, SoftSilicon, Sound Mark, StarPro, Stratix, the Stratix logo, Stay With It, the Engineering Stay With It logo, StreamSight, Tarari, The Journey Inside, Thunderbolt, the Thunderbolt logo, Transcede, Ultrabook, VTune, Xeon, X-GOLD, XMM, X-PMU and XPOSYS are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries.

Microsoft, Windows, and the Windows logo are trademarks, or registered trademarks of Microsoft Corporation in the United States and/or other countries. Java is a registered trademark of Oracle and/or its affiliates. Bluetooth is a trademark owned by its proprietor and used by Intel Corporation under license. Intel Corporation uses the Palm OS* Ready mark under license from Palm, Inc. OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission by Khronos.
Learn how to use Intel Trademarks and Brands correctly at http://www.intel.com/intel/legal/tmusage2.htm.