



# Product Change Notification

## 107487 - 00

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Should you have any issues with the timeline or content of this change, please contact the Intel Representative(s) for your geographic location listed below. No response from customers will be deemed as acceptance of the change and the change will be implemented pursuant to the key milestones set forth in this attached PCN.

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# Product Change Notification

**Change Notification #:** 107487 - 00  
**Change Title:** Intel NetStructure (R) MPCBL0001 Single Board Computer, PCN 107487-00, Product Design, Removal of Ground Isolation Washer  
**Date of Publication:** April 24, 2007

## Key Characteristics of the Change:

Product Design

## Forecasted Key Milestones:

<b>Date Customer Must be Ready to Receive Post-Conversion Material:</b>	Apr 27, 2007
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## Description of Change to the Customer:

In a few cases the MPCBL0001 does not meet the IEC 60950 standard requirements of 1.3mm spacing required between TNV2 (>60VDC) and SELV (<60VDC). For Customers using installations with a >±60VDC voltage range, there is a potential for exposure to currents exceeding required limits.

As a workaround the washer which isolates chassis ground from logic ground is being removed. This change to the default grounding configuration of the board combines chassis and logic ground together. This is an acceptable PICMG grounding configuration.

## Customer Impact of Change and Recommended Action:

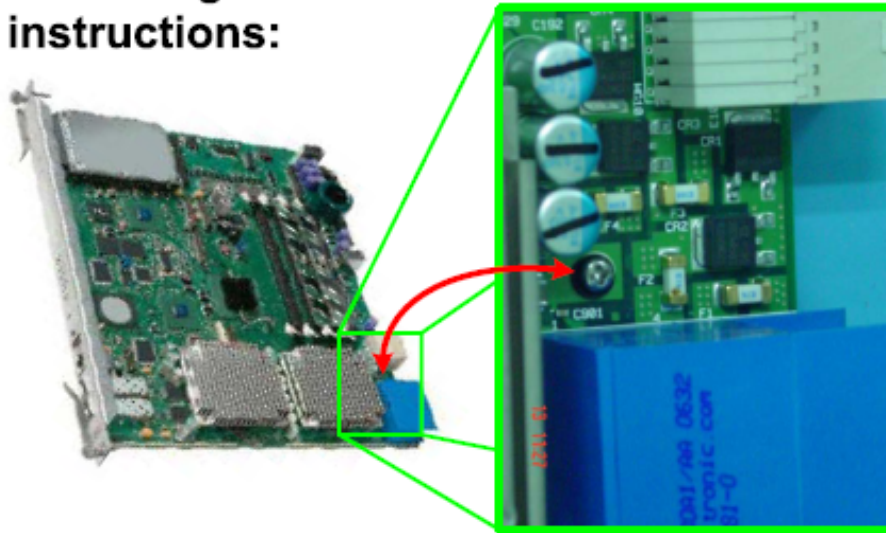
Field Exposure:

1. Intel has confirmed that this matter is not an issue for customers using a -48VDC installation because the voltage range (-42V to -56V) will never exceed the nominal -60VDC threshold. The IEC60950 requirement does not apply to voltages below ±60V to ground.
2. If the chassis and logic ground are isolated, and the supply voltage to the board is >±60VDC, there is a potential for exposure to currents exceeding required limits.

To remove the potential exposure, Intel has made the decision to modify the default grounding configuration of these products.

Customers who operate this equipment in -48VDC power systems which do not exceed  $\pm 60$ VDC may choose to modify the board to an isolated grounding configuration. Intel has included detailed rework instructions with this document that give you step by step rework instructions to return the grounding configuration to isolate chassis and logic ground. Please read and follow these instructions carefully.

## Ground configuration instructions:



*Figure 1: Location of Isolation Screw/washer*

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### Contents of plastic bag:

Qty 1 Phillips head 6mm screw (M2.5)  
Qty 1 Flat Nylon Washer (M2.5)

### Equipment needed:

#1 Phillips head torque screwdriver

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Ground configuration instructions:

1. Take steps to confirm appropriate grounding of board and service person prior to removing board from ESD bag.
2. Using a #1 Phillips head screw driver, remove and dispose of screw from board located beside the large blue power connector P10, as shown in figure 1.
3. Remove screw and washer from plastic bag and install plastic washer onto the screw.
4. Replace the screw removed in step 2 with the combined screw and washer using a #1 Phillips head torque screwdriver. Torque to 4 in-lbs.

Customers who determine the supply voltage exceeds  $\pm 60$ VDC in their target environment should not modify the default grounding configuration of these boards.

Intel values our longstanding collaborations and appreciates your continued business. Should you have any questions or concerns, please contact your Intel representative for assistance.

## Products Affected / Intel Ordering Codes:

Board Products Table

Pre Change Product Code	Pre Change MM#	Pre Change TA	Pre Change PBA	Post Change MM#	Post Change TA	Post Change PBA
MPCBL0001N04	855964	C13354-021	C44585-407	855964	C13354-022	C44585-407
MPCBL0001F04	855965	C55360-022	A97017-407	855965	C55360-023	A97017-407
MPCBL0001F04Q	875601	D17324-005	D16300-104	875601	D17324-006	D16300-104
MPCBL0001N04Q	875602	D18530-005	D18536-104	875602	D18530-006	D18536-104

## PCN Revision History:

**Date of Revision:**

April 24, 2007

**Revision Number:**

00

**Reason:**

Originally Published PCN