Solution Brief

Open RAN Enablement Package
Intel FPGAs

Accelerate Open RAN 4T4R O-RU Deployments with Intel Agilex® 7 SoC FPGA and Open RAN O-RU Enablement Package

Based on an Intel Agilex 7 SoC FPGA with a single F-Tile package optimized for cost- and power-sensitive radio applications, this enablement package provides a fully validated Open Radio Access Network (O-RAN)-compliant low-PHY and digital front-end (DFE) datapath solution, enabling customers to develop their differentiated four-transmitter four-receiver (4T4R) multicarrier O-RAN Radio Unit (O-RU) up to 280 MHz of radio frequency (RF) bandwidth targeting both commercial and private 5G deployments.

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Introduction

Fixed and mobile wireless connectivity and the number of connected devices continue to experience exponential growth. This, in turn, drives the demand for a flexible radio access network (RAN) architecture. O-RAN aims to enable an open, competitive, and interoperable multi-vendor ecosystem that leads to innovation, reduced cost, improved performance, and agility. To support the O-RAN concept, the O-RAN Alliance[1], a worldwide community of mobile network operators, vendors, and research and academic institutions working in telecommunications, was formed to define the architecture and specifications for O-RAN. A related entity is the 3rd Generation Partnership Project (3GPP)[2], an umbrella term for organizations developing standardized mobile telecommunications protocols.

O-RAN disaggregates traditional RAN components in the form of a proprietary baseband unit (BBU) and remote radio head (RRH) into three parts with open interfaces – a centralized unit (O-CU), a distributed unit (O-DU), and a radio unit (O-RU). This is depicted in Figure 1.

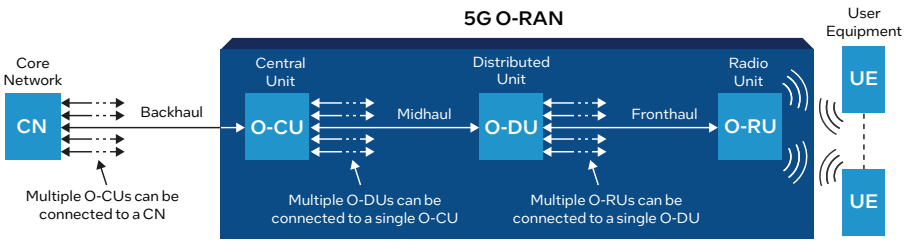

Figure 1. High-level visualization of a 5G NR O-RAN architecture

At its simplest level, the O-CU performs non-real-time higher L2 and L3 processing; the O-DU performs real-time L2 and part of the higher L1 – or high PHY layer – processing; and the O-RU handles the digital front-end functions, including lower L1 – or low PHY layer – processing as well as the conversion between the analog RF and digital domain. Furthermore, the fronthaul interface linking the O-RU and the O-DU, typically through Ethernet, is the most bandwidth-intensive and time-sensitive portion of the mobile network.

O-RUs are the most common and numerous elements in the network. Each O-RU services an area called a cell, the size of which depends on the application, such as a small business, a larger establishment, a small village, or a larger area in a city. Cells may be classed as femtocells, picocells, microcells, and macrocells based on their power output and the area they can cover. Femtocells, picocells, and microcells may be collectively called "small cells". Femtocells have the lowest power output and shortest range, with 100 to 200 milliwatts covering up to ~10 meters. In contrast, macrocells have the highest power output, delivering the largest range, with tens of watts covering tens of kilometers.

Macrocells will account for approximately 90% of 5G New Radio (NR) O-RU deployments worldwide in 2023[5]. It's widespread to see 4T4R configurations, which can be used to implement 4x4 multiple-input and multiple-output (MIMO) to improve spectral efficiency and boost capacity. Such configurations are considered by many to be the "Swiss Army Knife" of O-RU implementations.

The Intel® Open RAN O-RU Enablement Package is a complete 4T4R end-to-end solution for developing small cell and microcell radio. It is built around a 5G NR O-RU workload that includes an O-RAN or enhanced Common Public Radio Interface (eCPRI) 25GE interface with the Intel Precision Timing Protocol (Intel PTP) Servo running over the Linux* OS, a flexible low-PHY implementation, along with digital up-conversion (DUC) or digital down-conversion (DDC) functionality realized using an Intel Agilex® 7 SoC FPGA with a single 16-transceiver F-Tile referred as R24D package. The Open RAN O-RU Enablement Package has a comprehensive development tool suite, user guides, training, and hardware validation platforms.

The typical digital section of the O-RU consists of a fronthaul interface, eCPRI transport, O-RAN processing, lower layer 1 PHY, and a DFE. Intel provides these elements as intellectual property (IP) functions. Some of these functions are supplied as hard IP functions implemented in silicon. Others are provided as soft IP functions, which may be presented either as algorithms captured in a programming language to be compiled into machine code and run on a processor or as algorithms captured in a hardware description language (HDL) to be synthesized into a configuration file and implemented in an FPGA's programmable fabric.

Even when provided with access to all the hard and soft IP functions required to implement an O-RU, doing so is a complex plug-and-play exercise, not least that there are numerous ways to configure and connect these elements. Developing a system-level architecture for a complete and functional foundational O-RU can take years of effort in both design and validation. This is what Intel has done, including analyzing and tuning buses, data rates, and throughputs. Instead of simply stitching a bunch of IP functions together, the Intel Open RAN O-RU Enablement Package is a pre-validated solution that accelerates customers in developing unique 4T4R O-RU solutions.

O-RAN C/U/S/M Planes

As was noted above, the fronthaul interface linking the O-RU and the O-DU is the most bandwidth-intensive and time-sensitive portion of the mobile network. In the case of a packet-based network of this type, establishing and measuring the level of simultaneity or the temporal ordering of events requires those events to be timestamped. In turn, these timestamps must be associated with a common timescale.

Legacy networks using Common Public Radio Interface (CPRI) for the fronthaul rely on synchronous, point-to-point connections between the BBU and RRH. In contrast, the rest of the network interfaces are based on Ethernet. By comparison, O-RAN can leverage converged Ethernet for the entire RAN. This not only improves scalability by allowing multipoint-to-multipoint connectivity between nodes, including the fronthaul, but it also enables a common system synchronization scheme based on industry-standard protocols, including Synchronous Ethernet (SyncE), to transfer frequency information and Precision Time Protocol (PTP), as per the IEEE 1588 standard, to transfer phase and time information. O-RAN includes a synchronization plane (S-plane), which embraces industry standards and protocols to satisfy system timing and synchronization requirements. In addition, the O-RAN specification consists of the control plane (C-plane) to provide real-time control information, the user plane (U-plane) to handle real-time user data, and the management plane (M-plane) to support non-real-time system management and configuration data.

A high-level view of the C/U/S/M-plane packet processing performed by the Intel Open RAN O-RU Enablement Package implemented using an Intel Agilex 7 SoC FPGA is illustrated in Figure 2.

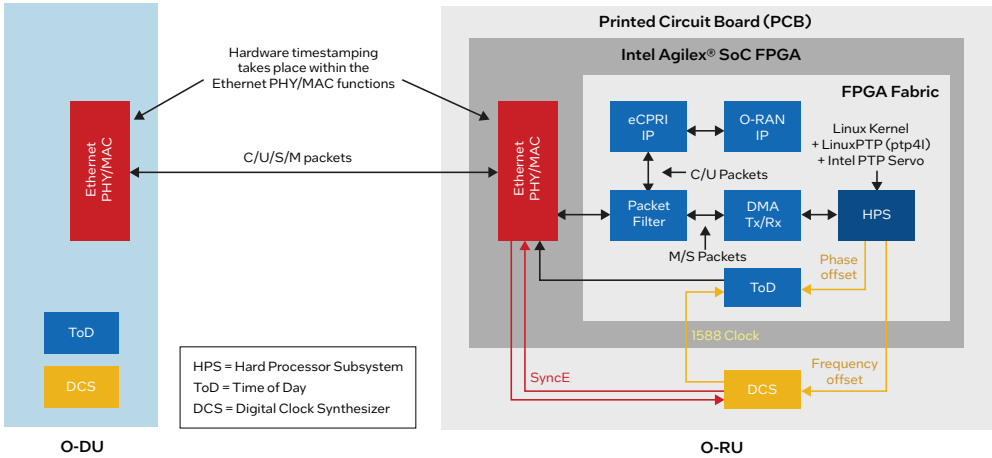

Figure 2. High-level visualization of O-RU C/U/S/M packet processing in an Intel Agilex FPGA.

The O-DU receives O-RAN traffic from the Intel Agilex 7 SoC FPGA's Ethernet PHY/MAC. A packet filter sends C/U-plane packets to the eCPRI and O-RAN IP functions, while M/S-plane packets are conveyed to the hard processor system (HPS).

C-Plane

The C-plane handles real-time scheduling, mixed numerology and Physical Random Access Channel (PRACH) configurations, and precoding weight transmission between the O-DU and the O-RU. This excludes any in-band and quadrature sample data, part of the user plane. Section Type 3 is supported mainly for PRACH configurations in the Intel Open RAN O-RU Enablement Package.

U-Plane

The U-plane oversees the quadrature sample data transferred between the O-DU and the O-RU. The datapath utilizes a buffer structure in the Intel Open RAN O-RU Enablement Package to compensate for frame delay variations (FDV) associated with the input data packets. This buffer is four orthogonal frequency division multiplexing (OFDM) symbols long to absorb fronthaul and O-DU scheduling delay variations. A maximum distance of 10 km is assumed between the O-DU and the O-RU. The Intel O-RAN IP core supports window monitoring for different sub-carrier spacing (SCS) and block floating-point compression for fronthaul bandwidth efficiency.

M-Plane

The M-plane handles non-real-time management operations and register configurations between the O-DU and the O-RU. The M-plane is not part of the enablement package as this is application-specific software created by the end user.

S-Plane

The S-plane is responsible for time and frequency synchronization distributed between the O-DU and the O-RU. O-RAN specifications impose strict time, phase, and frequency requirements to implement high-performance time division duplex (TDD), massive multiple-input multiple-output (mMIMO), and multicarrier systems. O-RAN defines a network profile based on frequency, phase, and time synchronization parameters to achieve these requirements, requiring a set of features and options for network components, including switches and endpoints. O-RAN proposes four synchronization configuration topologies to address different deployment requirements to support O-RU synchronization. The Intel Open RAN O-RU Enablement Package and optional Intel PTP Servo support all four O-RAN synchronization topologies and meet the stringent conformance requirements stated by the synchronization profile. A full description of S-plane and O-RAN synchronization topologies is outside the scope of this document. For more information, please refer to the O-RAN WG4 CUS-plane specifications.[4]

The Intel Open RAN O-RU Enablement Package

A high-level view of the Intel Open RAN O-RU Enablement Package is shown in Figure 3. While the design was validated on a HiTek eSOM7 Development Board, it can be implemented on other Intel Agilex FPGA-based development platforms. In addition to an Intel Agilex 7 SoC FPGA, the other main elements of the O-RU are DDR4 memory and a board-mounted digital clock synthesizer (DCS) or D-PLL device, where DCS devices suitable for O-RAN applications are available from multiple suppliers. The Intel Open RAN O-RU Enablement Package is:

- A complete U/C/S datapath that drastically reduces development cost, verification time, and RnD effort.
- Delivered with DSP Builder sources to allow for quick customer customization.
- A fully validated ORAN/LowPHY/DFE workload.
- Integrates LinuxOS framework leveraging the Intel PTP servo.

Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are used to interface between the DFE, which is implemented in the Intel Agilex 7 SoC FPGA and the RF front end (RFFE), which is implemented on a separate card. The example in Figure 3 employs a 4T4R carrier card to supply ADC/DAC functionality, although 8T8R carrier cards are also available, 8T8R implementations can be implemented with multiple instances of the Intel Open RAN O-RU Enablement Packages. In this example, the DFE has been optionally implemented in the Intel Agilex 7 SoC FPGA. Still, this functionality could be moved out of the FPGA and onto a suitable carrier card. The transceiver-agnostic JESD interfaces employed in this example provide customers with the ability to leverage off-the-shelf third-party converter solutions from traditional analog companies, thereby offering more options to optimize system design and high-power amplifier (HPA) efficiency, leading to reduced system cost and power consumption. Intel has performance integration and interoperability with the most popular converters in the market, with both 4T4R and 8T8R. Please get in touch with your sales representative to inquire about your specific converter needs.

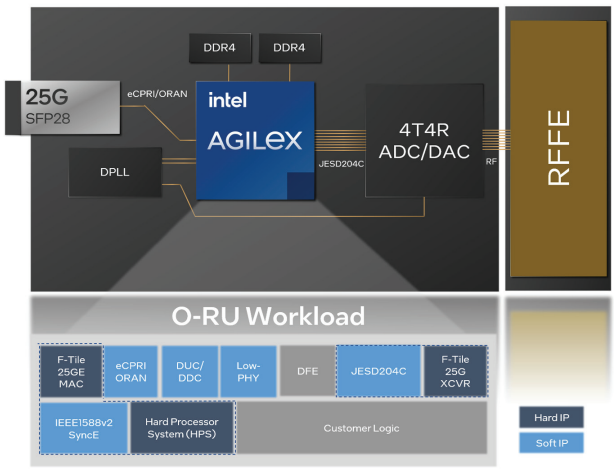

Figure 3. High-level view of the Intel Open RAN O-RU Enablement Package.

The Intel Agilex 7 FPGA family includes FPGAs and SoC FPGAs. Both support hard interfaces in their fabric for external DDR4 memory and have a Secure Device Manager (SDM). SoC FPGAs also have a HPS.

A chiplet, also known as a "tile", is a small integrated circuit die containing a well-defined subset of functionality. In addition to the main FPGA die, Intel Agilex 7 devices can have between two to six transceiver (XCVR) tiles. These XCVR tiles are connected to the main FPGA die using Intel's Embedded Multi-die Interconnect Bridge (EMIB) technology, an elegant and cost-effective approach to the in-package high-density interconnect of heterogeneous chips. The result is that the chip and chiplets combine as a single large die.

Intel Agilex 7 SoC FPGAs support multiple types of XCVR tiles, including E-Tiles, F-Tiles, P-Tiles, and R-Tiles. Different Intel Agilex FPGA family members provide different combinations of these tiles. In addition to various general-purpose input/output (GPIO) and high-speed SerDes interfaces, F-Tiles can support up to 400 Gbps Ethernet. F-Tiles also support PTP hardware timestamping.

The Intel Open RAN O-RU Enablement Package is based on an Intel Agilex 7 SoC FPGA with a 16-channel XCVR F-Tile integrated into an R24D package. This O-RU implementation features multiple Intel hard IP functions – in the form of the HPS and the F-Tile XCVR and Ethernet MAC/PCS – and soft IPs functions – in the form of software code running on the HPS and RTL code functions – implemented in the programmable fabric. Clocking is provided externally by the DCS. A high-level view of the Intel Agilex SoC FPGA portion of the Intel Open RAN O-RU Enablement Package is depicted in Figure 4.

The Intel Open RAN O-RU Enablement Package supports a 4T4R antenna configuration with two component carriers (2CCs) aggregated per antenna. Each component carrier has a 100 MHz bandwidth 5G NR at 30 kHz SCS, resulting in an occupied bandwidth (oBW) of 200 MHz and an instantaneous bandwidth (iBW) of 280 MHz.

Four versions of the R24D packaged device are available—scaling from ~600k logic elements (LEs) (AGF006) up to ~1.4M LEs (AGF014) and are pin-compatible with 2 F-tile packages (R24C), giving customers significant flexibility in package selection. In addition to implementing the soft IP functions provided by Intel, customers can use the programmable fabric to implement their own "secret sauce" IP functions and logic, once again allowing them to differentiate their solution from competitive offerings. A summary of the various elements comprising the Intel Open RAN O-RU Enablement Package is presented in Table 1.

For the DFE portion of the design, the example provided by the Intel Open RAN O-RU Enablement Package includes optional DUC and DDC soft IP functions. The channel filter coefficients are run-time configurable for downlink (DL) and uplink (UL) transmissions to enable users to meet different specifications. The crest factor reduction (CFR) and digital pre-distortion (DPD) functions are not directly integrated into the Intel Open RAN O-RU Enablement Package, allowing users to select versions that best meet their unique requirements. Intel has developed both CFR and DPD solutions, and we are happy to discuss them with interested customers. Furthermore, as noted above, DFE functionality can be easily bypassed or removed from the FPGA's soft logic and implemented along with the ADC/DAC functionality in silicon from third-party vendors. PRACH processing is done per eAxC in the O-RU Enablement Package supporting all short format PRACH.

In addition to the Linux kernel, application programming interfaces (APIs), software drivers, and O-RAN M-plane functions, the HPS also runs a PTP stack and the software radio application itself. Customers can use the radio application provided as part of the Intel Open RAN O-RU Enablement Package as a foundation upon which they can add their own "secret sauce" to differentiate their solution from competitive offerings.

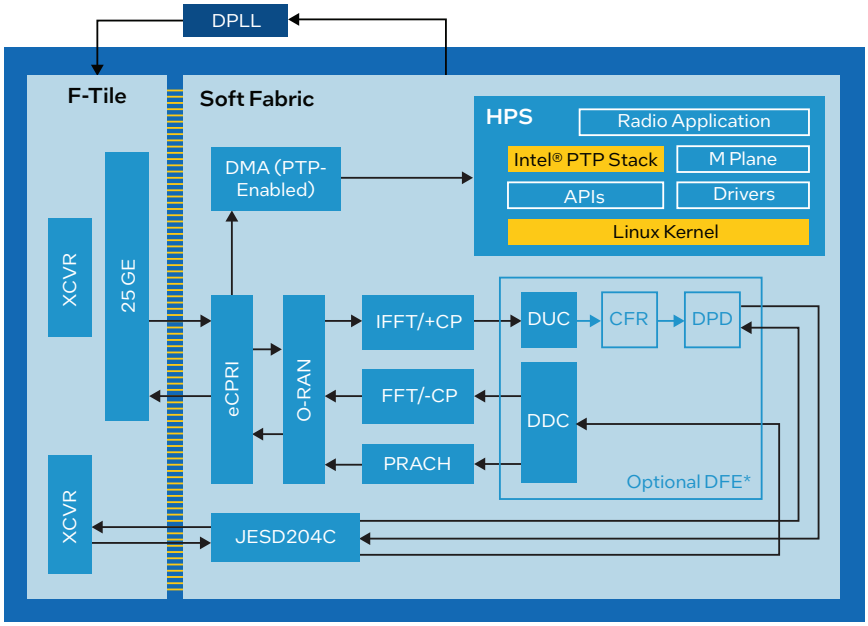

Figure 4. A high-level view of the Intel Agilex SoC FPGA portion of the Intel Open RAN O-RU Enablement Package.

The PTP stack provided by default in the Intel Open RAN O-RU Enablement Package is ptp4l, included natively with the Linux kernel, which supports basic point-to-point timing and synchronization operations.

The International Telecommunication Union (ITU)[3] is a specialized agency of the United Nations responsible for information and communication technologies. O-RAN specifications are linked to several ITU recommendations and IEEE specifications. The methodology of delivering the appropriate timing to the RU is based substantially on the G.826x and G.827x families of ITU recommendations. The integrated IEEE 1588v2 and SyncE solution provided by default in the Intel Open RAN O-RU Enablement Package takes the guesswork out of system timing and synchronization, supporting G.8275.1 and G.8275.2 profiles and all four O-RAN low-level split (LLS) synchronization topologies.

As previously noted, the default open-source PTP servo included with ptp4l may be inadequate for some more advanced O-RU implementations that require partial timing support (PTS) to cope with packet delay variation (PDV). To address these cases, Intel has developed a proprietary PTP servo called the Intel PTP Servo, which is fully compliant with O-RAN. WG4.CUS.0 technical specifications can be optionally offered with the Intel Open RAN O-RU Enablement Package.

In the case of PTS network architectures, for example, the Intel PTP Servo achieves a maximum absolute time error (|TE|) of 1 µs, as compared to the default ptp4l proportional-integral (PI) servo solution, which can achieve only 138 µs. For a network operator, this equates to the ability to use an existing legacy network between the DU and the RU, thereby avoiding the costs associated with investing in a new full-timing support (FTS) network.

Category	Deliverables
Intel Hard IP	HPS
	25G Ethernet MAC/PHY with PTP timestamping
Intel O-RU Foundation Soft IP	eCPRI
	O-RAN
	JESD204C
	Linux with 1588 PTP4L and Intel PTP servo (optional)
Intel DSP Builder O-RU Library	Fast Fourier transform (FFT) / inverse FFT (iFFT)
	PRACH
	DUC/DDC
Development Tools	Intel Quartus® Prime Design Software
	DSP Builder for Intel FPGAs
Support	Wireless Specialist FAE
	Customer Experience Group
Documentation	O-RU Workload Product Verification Testing and User Guide
Training	Online videos and tutorials

Table 1. Summary of the elements comprising the Intel Open RAN O-RU Enablement Package.

Real World Results

Intel FlexRAN™ is a virtual RAN (vRAN) reference architecture for virtualized cloud-enabled RANs. The O-RU workload depicted in Figure 3 has been fully validated with the FlexRAN O-DU and the Keysight Open RAN Studio* O-DU emulator. The Intel IP libraries comply with Open RAN and 3GPP standards, facilitating interoperability with O-RAN-compliant network components. Some key points worth noting are as follows:

- The O-RU Enablement Package includes an end-to-end RTL simulation performed using the Cadence Xcelium Logic Simulator* and Questa*-Intel® FPGA Edition software with a loop-back at the DFE output.
- A MATLAB*-based graphical user interface (GUI) has been developed for all register configurations and debugging purposes. As shown in Figure 5, different capture points have been added to the GUI to dump the data for each symbol ID, slot ID, subframe ID, and eAxC ID along the transmit and receive chain. This screenshot captures a symbol-long data from the received low PHY processing output, showing the received constellations and reporting error vector magnitude (EVM). The screenshot also shows the provisioning for an injection buffer at the receive side, which is used for PRACH testing and validation.
- The Intel O-RU Enablement Package has been validated in hardware by sending O-RAN traffic from Keysight Open RAN Studio* over a 25 GbE to the O-RU. The O-RU receives the O-RAN traffic, performs the low PHY processing, channel filtering, and digital up-conversion, and loops the data back to the UL direction. After DDC and low-PHY processing, the UL data is fed to the O-RAN IP function and returned to the ORAN Studio. Figure 6 shows the received data results using a Keysight vector signal analyzer. The overall RMS EVM is reported as 0.79 % in the VSA.
- PRACH test vectors are generated using the MATLAB 5G toolbox, stored in a pattern buffer in the FPGA, and passed through the PRACH IP. The preamble ID is verified in the VSA.
- Time synchronizing the O-DU with the O-RU.
- A Grand Master (GM) sends PTP to the O-RU and the O-DU.
- The O-RU workload closes timing on the slowest speed grade, enabling lower power and cost.

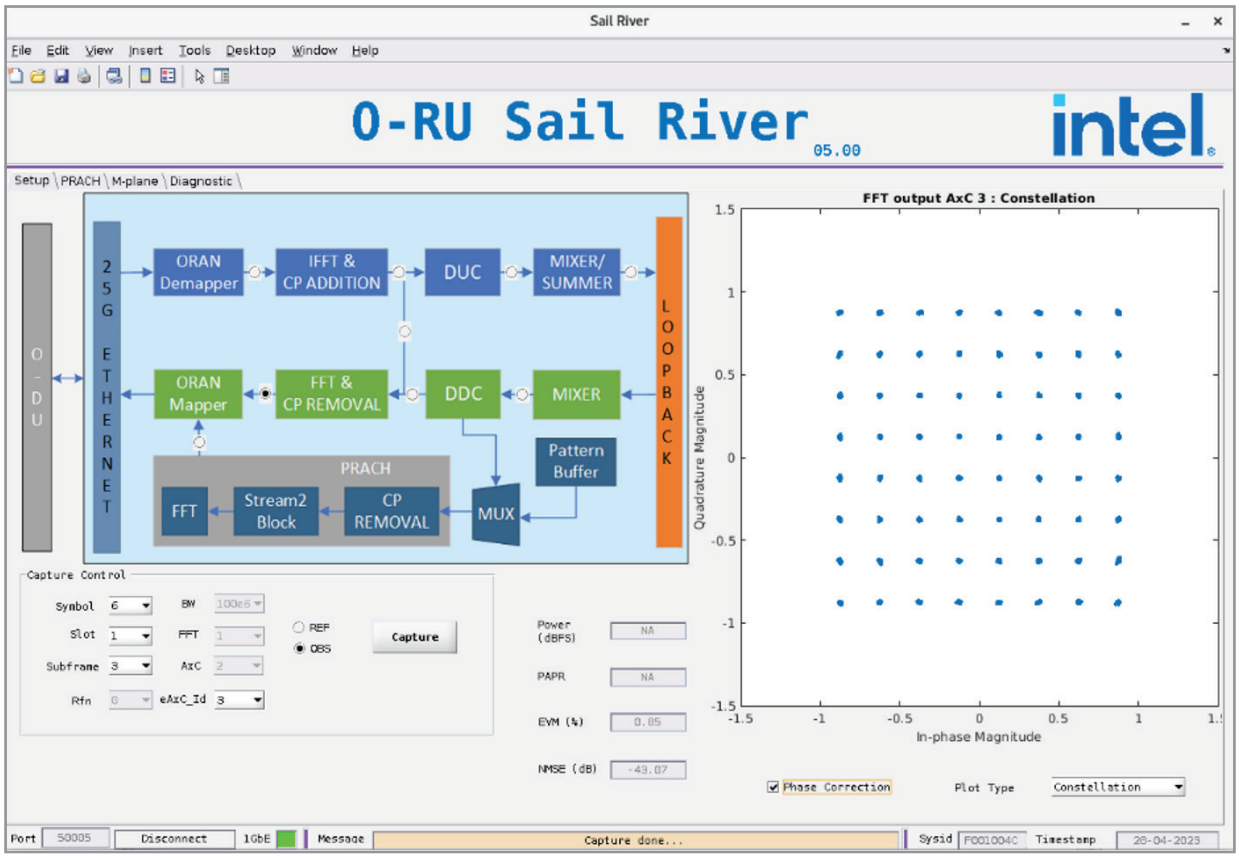

Figure 5. The MATLAB GUI used to define register values and control debugging.

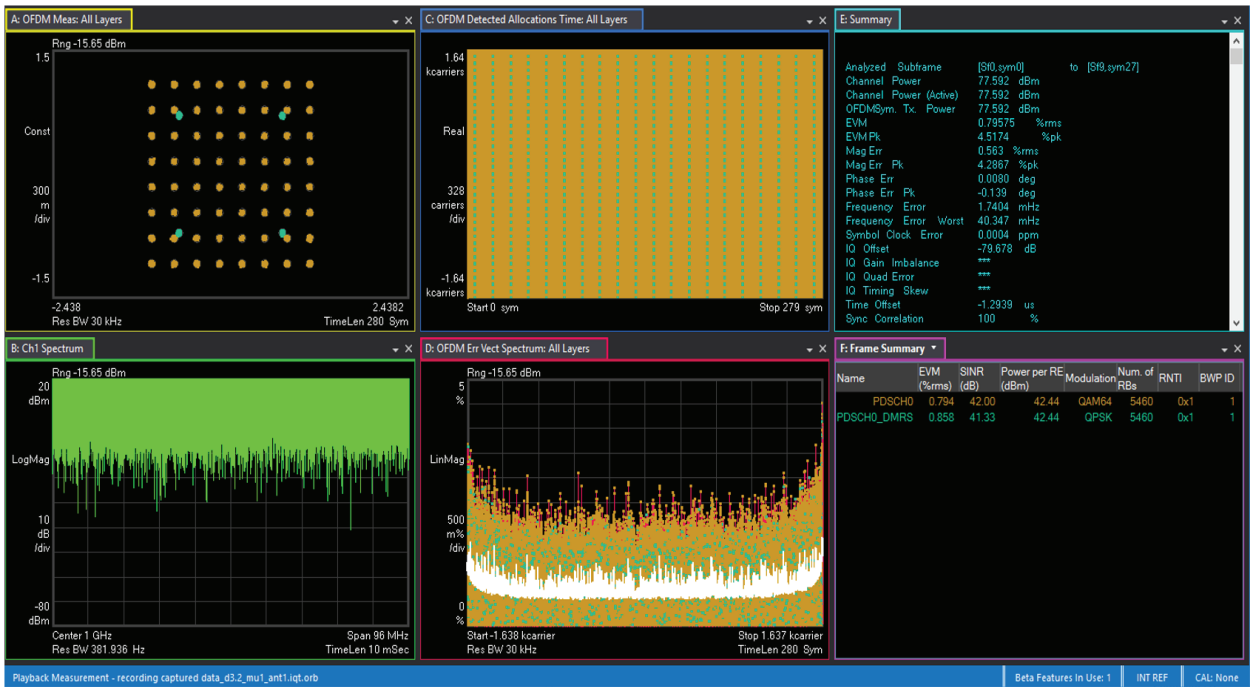

Figure 6. The received data results in Keysight Vector Signal Analyzer.

Conclusion

The Intel Open RAN O-RU Enablement Package, which adheres to O-RAN and 3GPP standards, provides a functional proof-of-concept O-RU implementation that illustrates how users can develop their own differentiated 4T4R O-RU microcell and low-power solutions. It leverages proven and integrated soft and hard IP functions to provide a scalable solution that reduces CAPEX, research and development costs, and time to market. It is also adaptable to customers' specific requirements.

The O-RU workload provides a baseline CAT-A radio implementation supporting two component carriers for 4T4R, xDD(TDD or FDD), and 2x100MHz of oBW, enabling system designers to focus on product differentiation and accelerating time to market. This cost-optimized solution implements a complete 4T4R 200 MHz oBW O-RU in an Intel Agilex SoC FPGA AGF008 using a single 16-transceiver F-Tile with less than 70% logic utilization. The workload closes timing with the lowest speed grade, enabling lower power and cost.

In summary, the Intel Open RAN O-RU Enablement Package provides a comprehensive solution consisting of all the necessary IP functions and tools, coupled with an extensive knowledge base and supported by a baseline design example to jumpstart your own O-RU development projects.

For more details, visit the Intel Open RAN O-RU Enablement Package web page and contact your local Intel sales representative for evaluation.

References

1 https://www.o-ran.org/

2 https://www.3gpp.org/

3 https://www.itu.int/

4 https://www.o-ran.org/specifications

5 Dell'Oro Group. "MOBILE RAN Quarterly Report." Vol. 24, No. 1, 1Q23, M1A Market Summary & Vendor Information, 17 May 2023.

Additional Resources

- Contact Us
- O-RU enablement package web page
- mMIMO Whitebox Platform and Workload
- Intel PTP Servo for IEEE PTP 1588 Time Synchronization Applications
- Build More Cost-Effective and More Efficient 5G Radios with Intel Agilex FPGAs
- Implementing Advanced Networking Solutions with F-Tiles in Intel Agilex 7 FPGAs

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