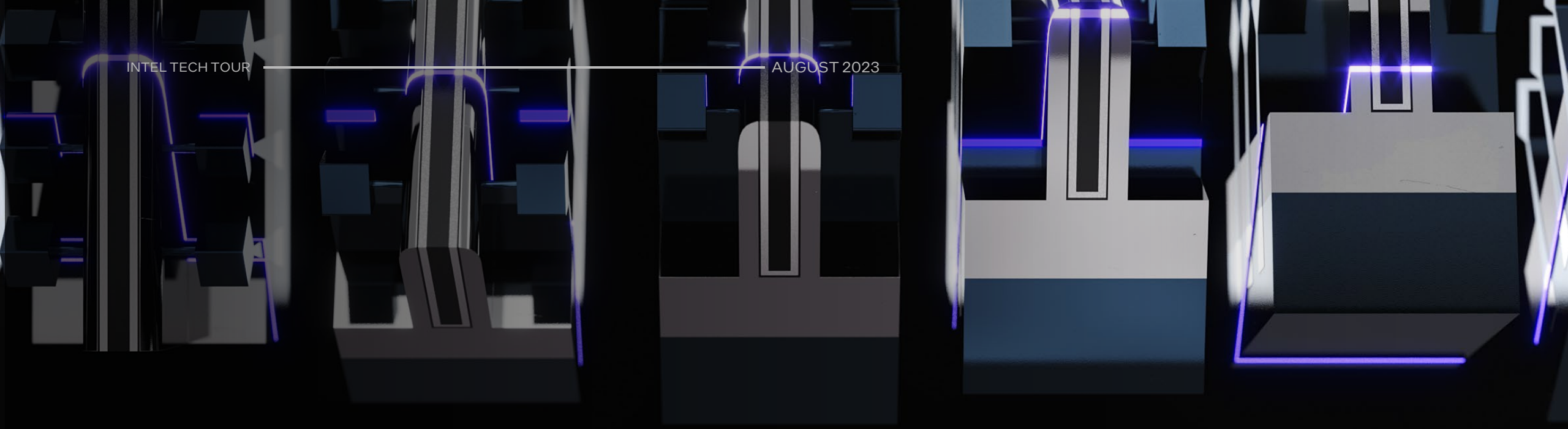


INTEL 4

Bill Grimm
Vice President, Logic Technology Development

Advancing Moore's Law
5 NODES IN 4 YEARS



Introducing

Intel 4

Logic process technology

2x
area scaling
for High Perf Logic library vs Intel 7

EUV
lithography for process simplification

>20%
power efficiency vs Intel 7

8VTs
for CPU optimization

High-density MIM
for Power Delivery



*Based on internal estimates.
Learn more at www.intel.com/PerformanceIndex.
Results may vary.

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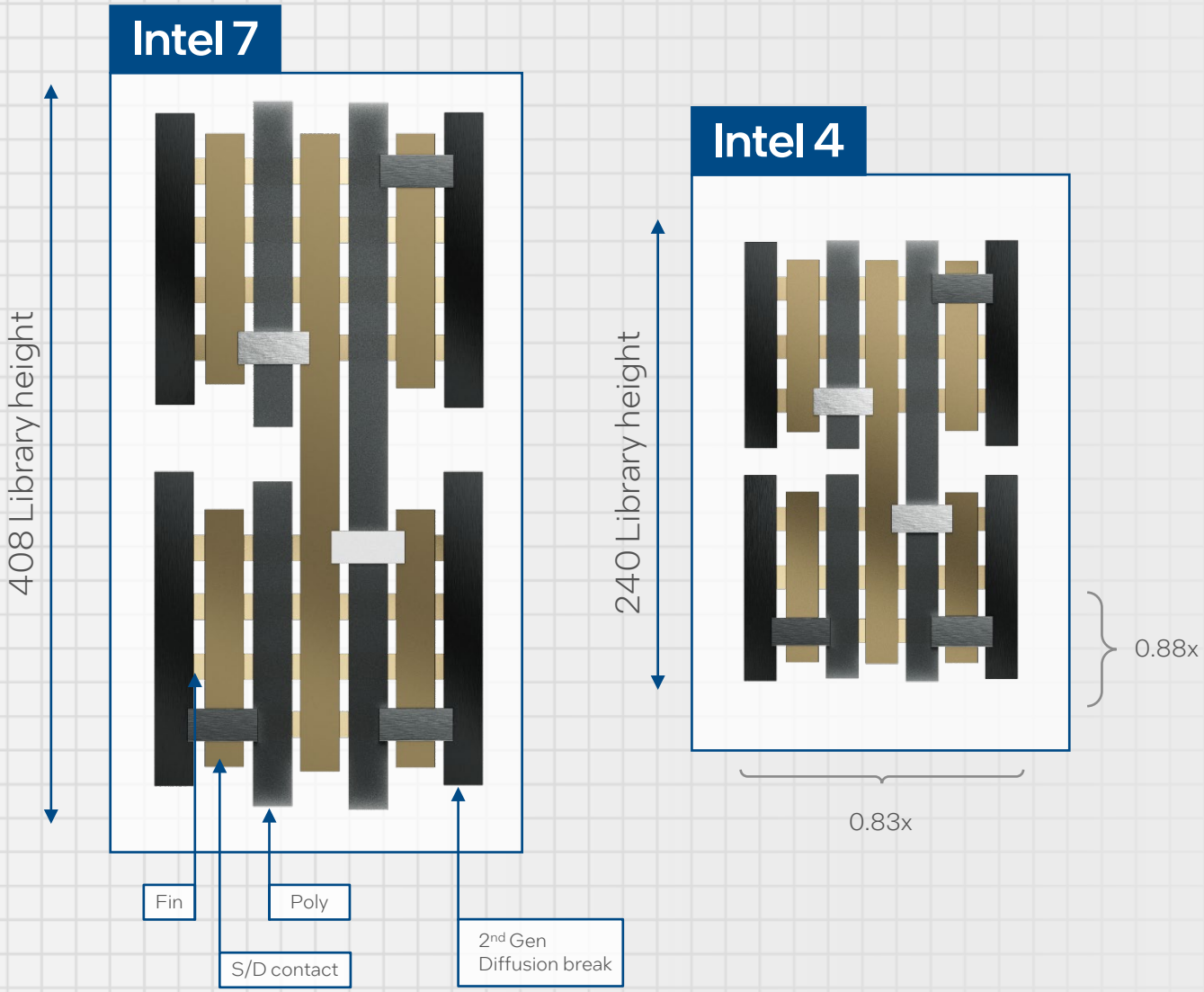
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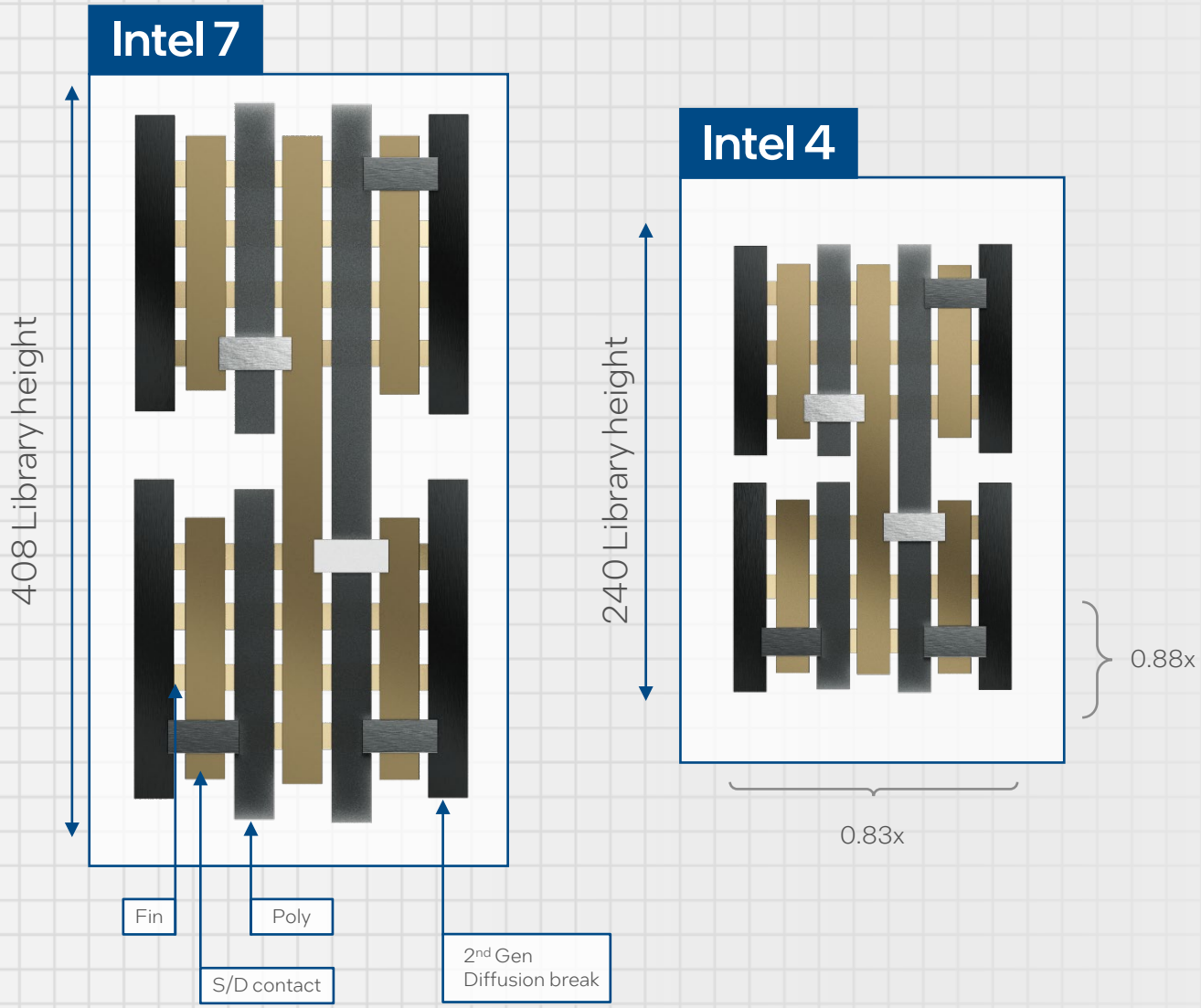
2x

High-Performance Library Scaling

High-Performance Library area scales by ~2x from Intel 7 to Intel 4

	Intel 7	Intel 4	Scaling
Contacted Gate Pitch (nm)	54/60	50	0.83x
Fin Pitch (nm)	34	30	0.88x
M0 Pitch (nm)	40	30	0.75x
HP Library Height (nm)	408	240	0.59x

*2022 IEEE VLSI Symposium



2x

High-Performance Library Scaling

4 Fin → 3Fin
Tighter Gate ETE Spacing
Fin Pitch Scaling of 0.88x
2nd Generation
- Dummy Gate Removal
- Contact on Active Gate

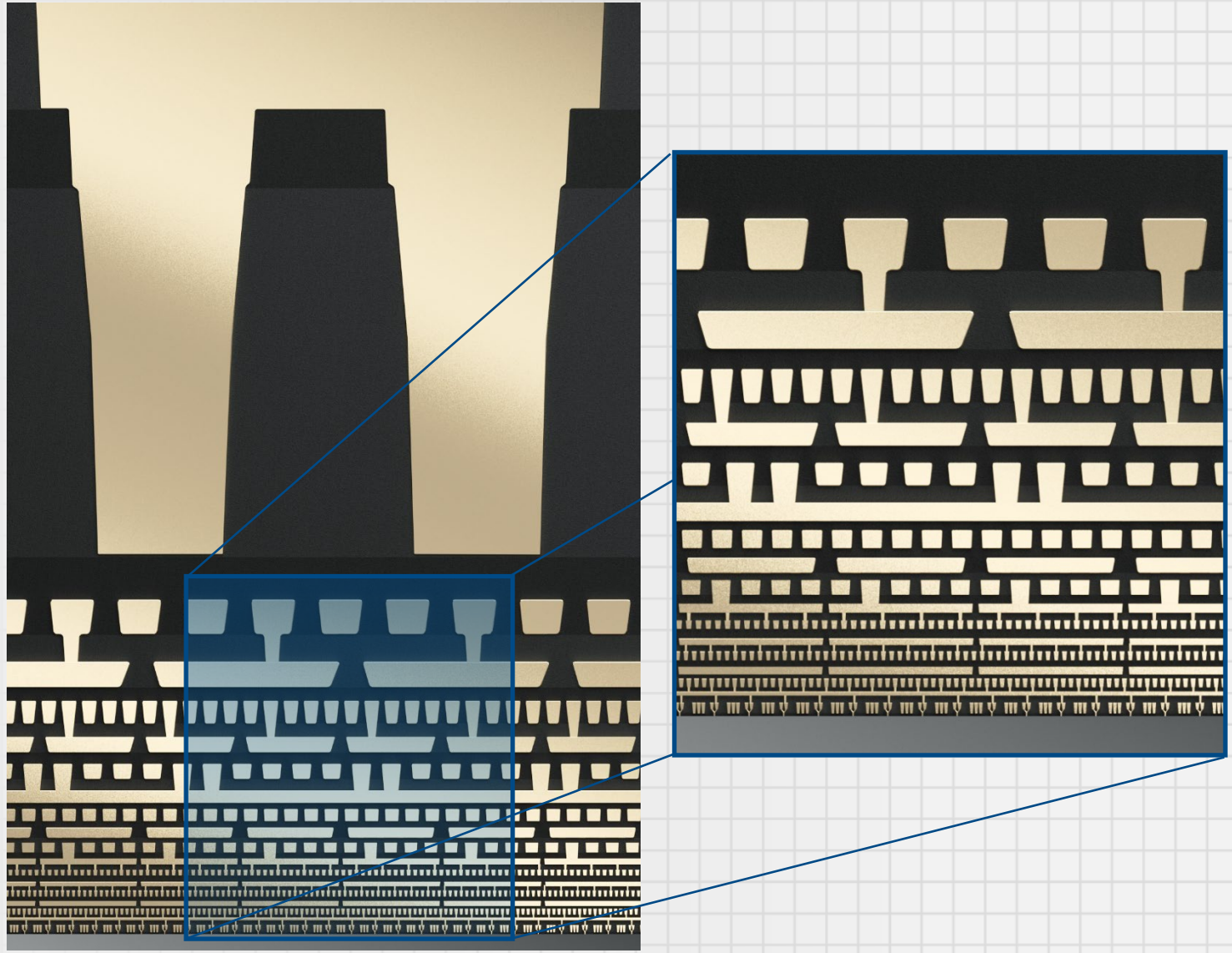
Contacted Gate Pitch Scaling of 0.83x

*2022 IEEE VLSI Symposium

Interconnects

18 Metal layer stack optimized for high-performance computing applications

- Metal 0 (30nm pitch with SAQP)
- 5 Enhanced Cu + 13 Cu interconnect layers
- EUV used extensively across multiple layers

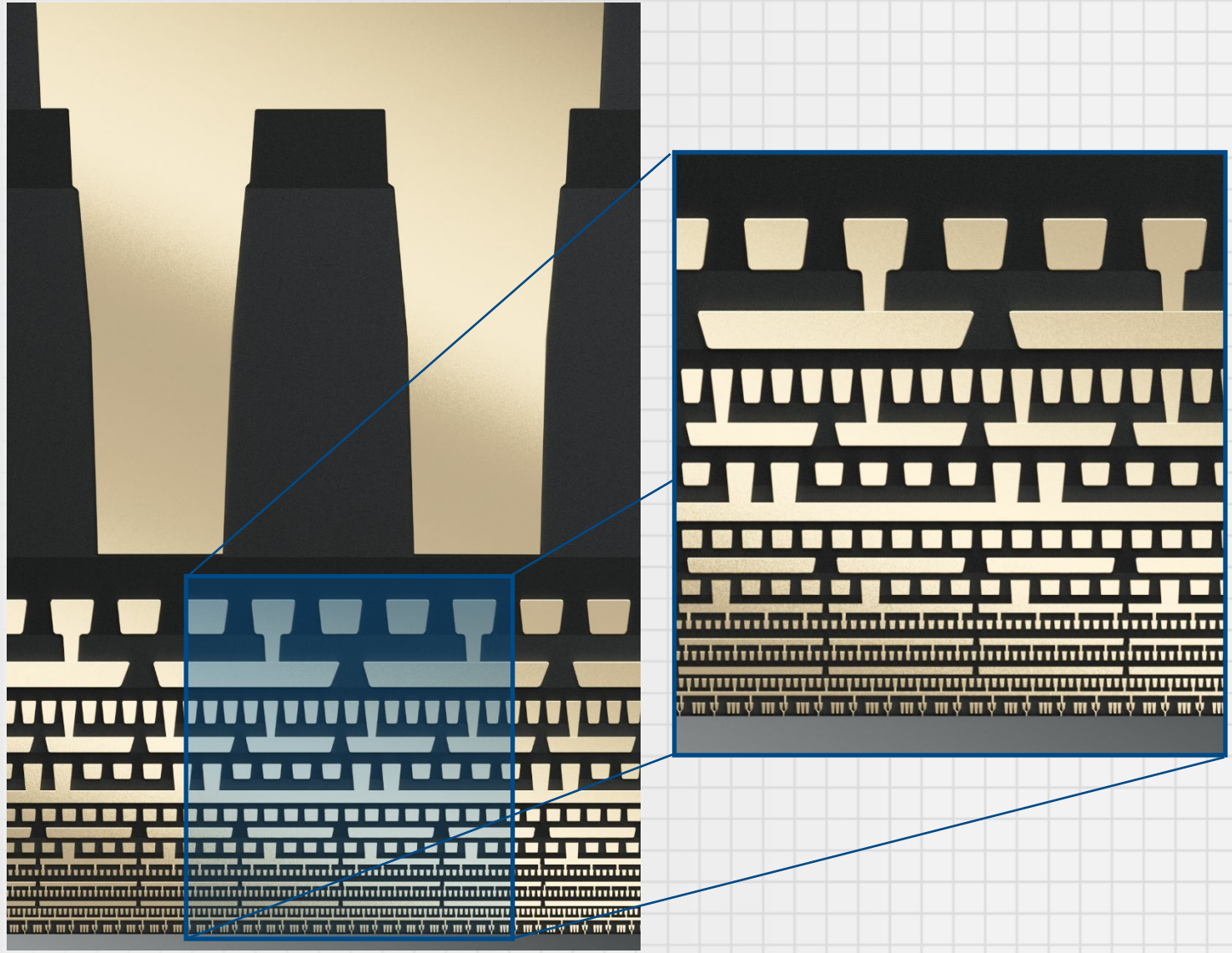


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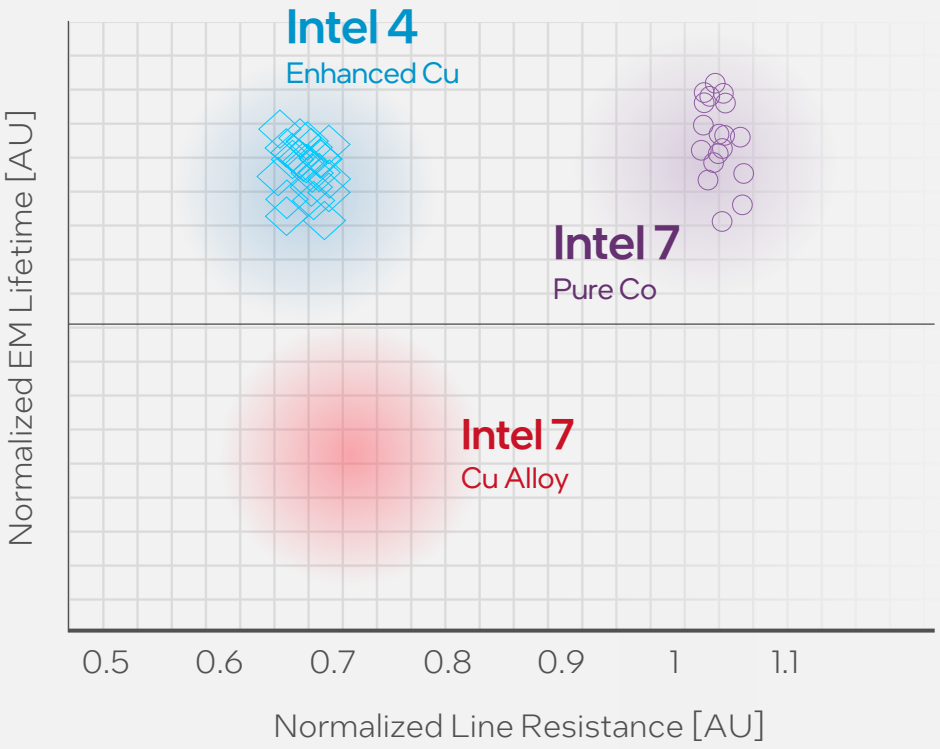
- Metal 0 (30nm pitch with SAQP)
- 5 Enhanced Cu + 13 Cu interconnect layers
- EUV used extensively across multiple layers



*2022 IEEE VLSI Symposium

Electromigration vs RC Optimization

Interconnect stack is optimized for RC while providing healthy EM reliability



Intel 7
Ta barrier with
Co lines



Intel 7
TaN with
Cu Alloy



Intel 4
Ta/Co with
pure Cu

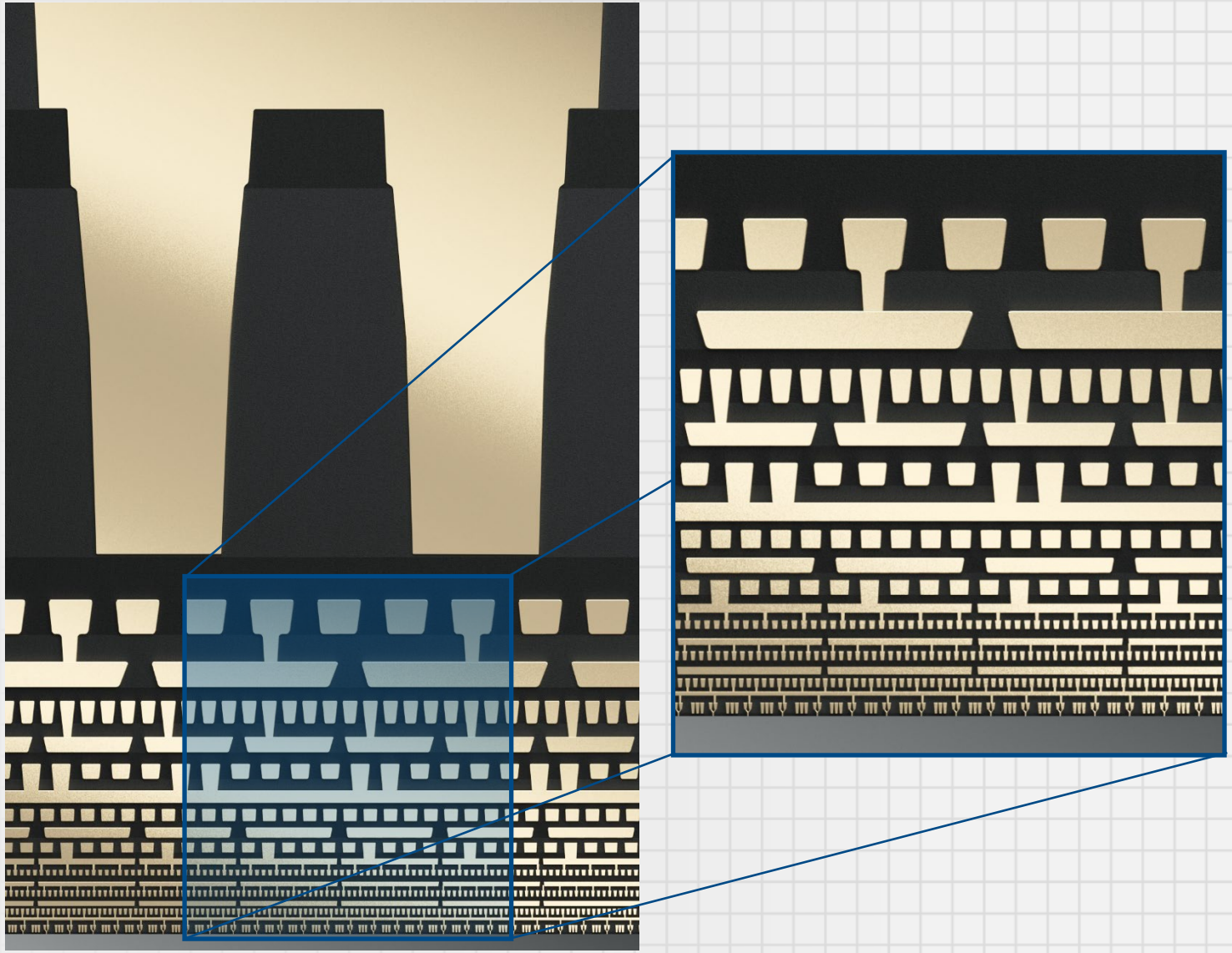


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Process Simplification with EUV

EUV lithography enables significant process flow simplification while supporting scaling

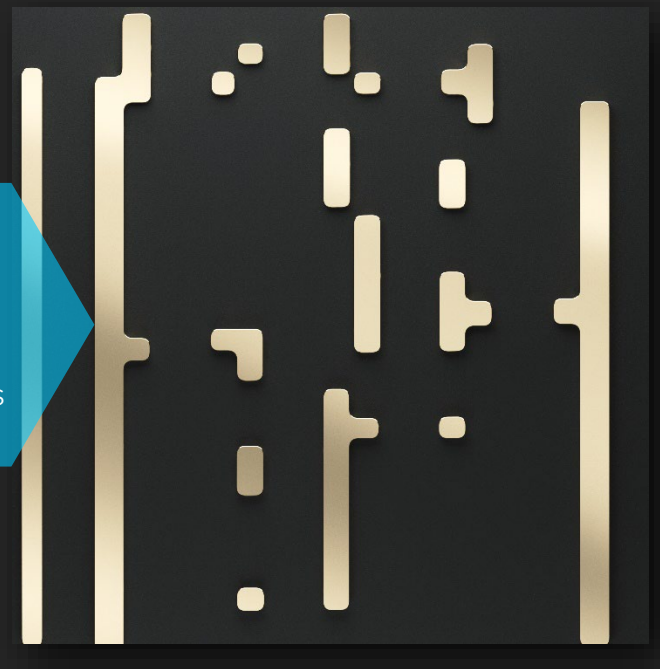
*Based on internal estimates.

1 Grating + 4 collection layers



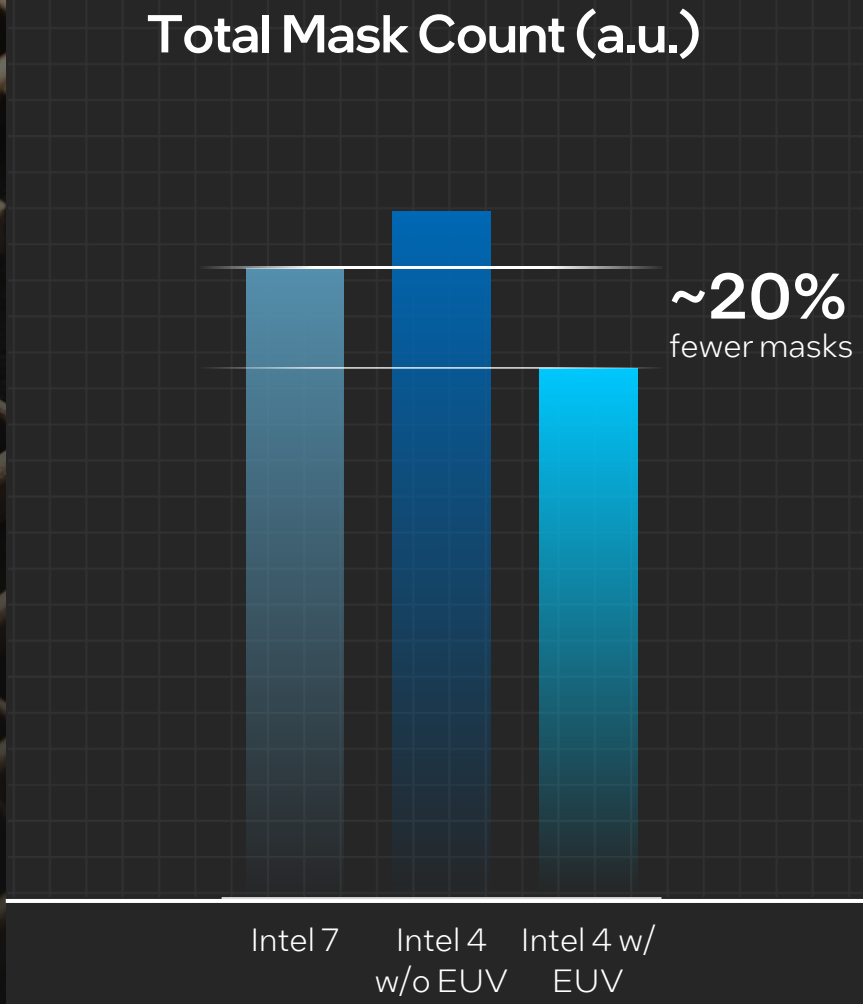
3-5x
reduction in process steps

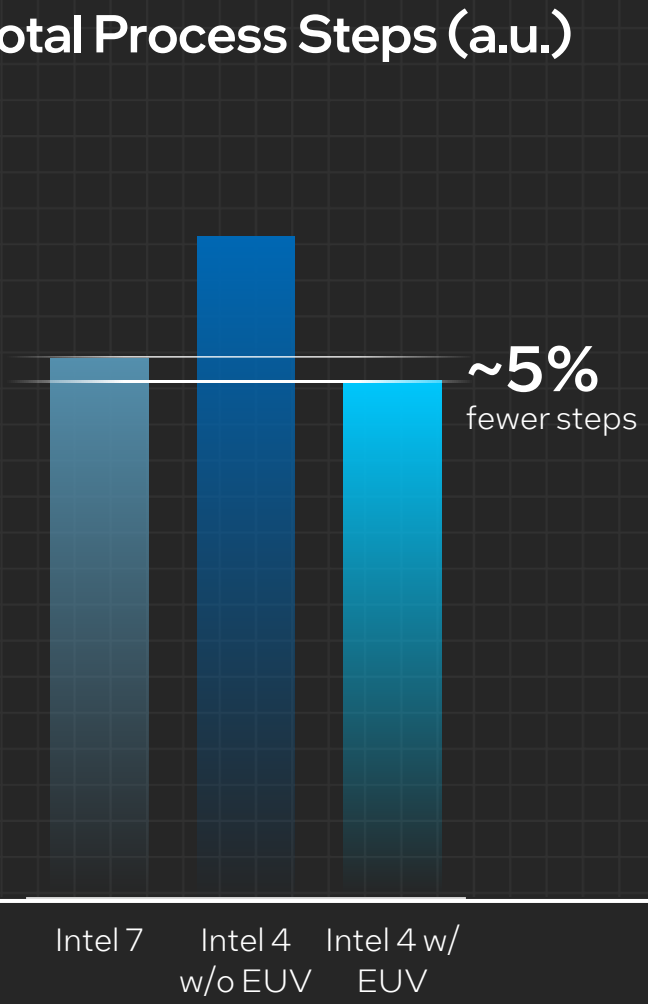
Single EUV layer



Lower Total Step Count in Intel 4 with EUV

Extensive use of EUV lithography enables total mask and total step count reduction in Intel 4

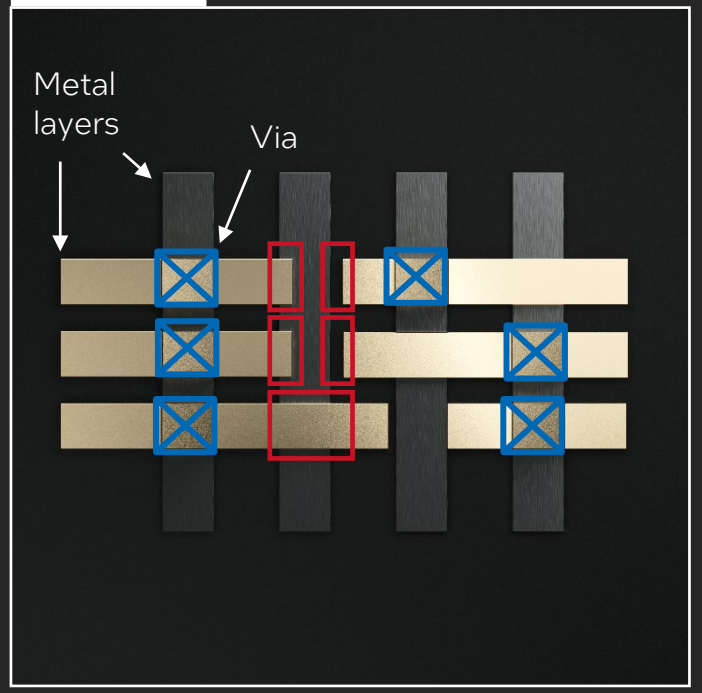




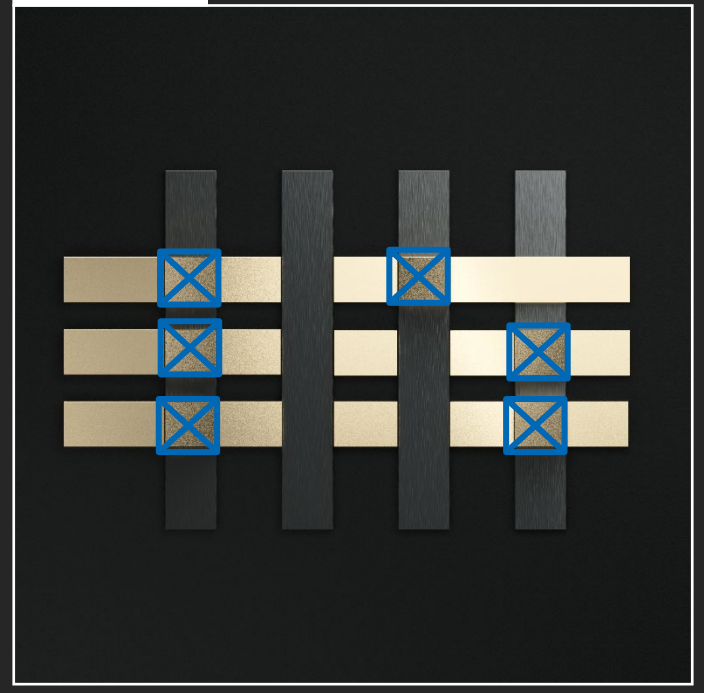
Gridded Interconnect Architecture

Gridded interconnect design rules benefit process predictability design optimization

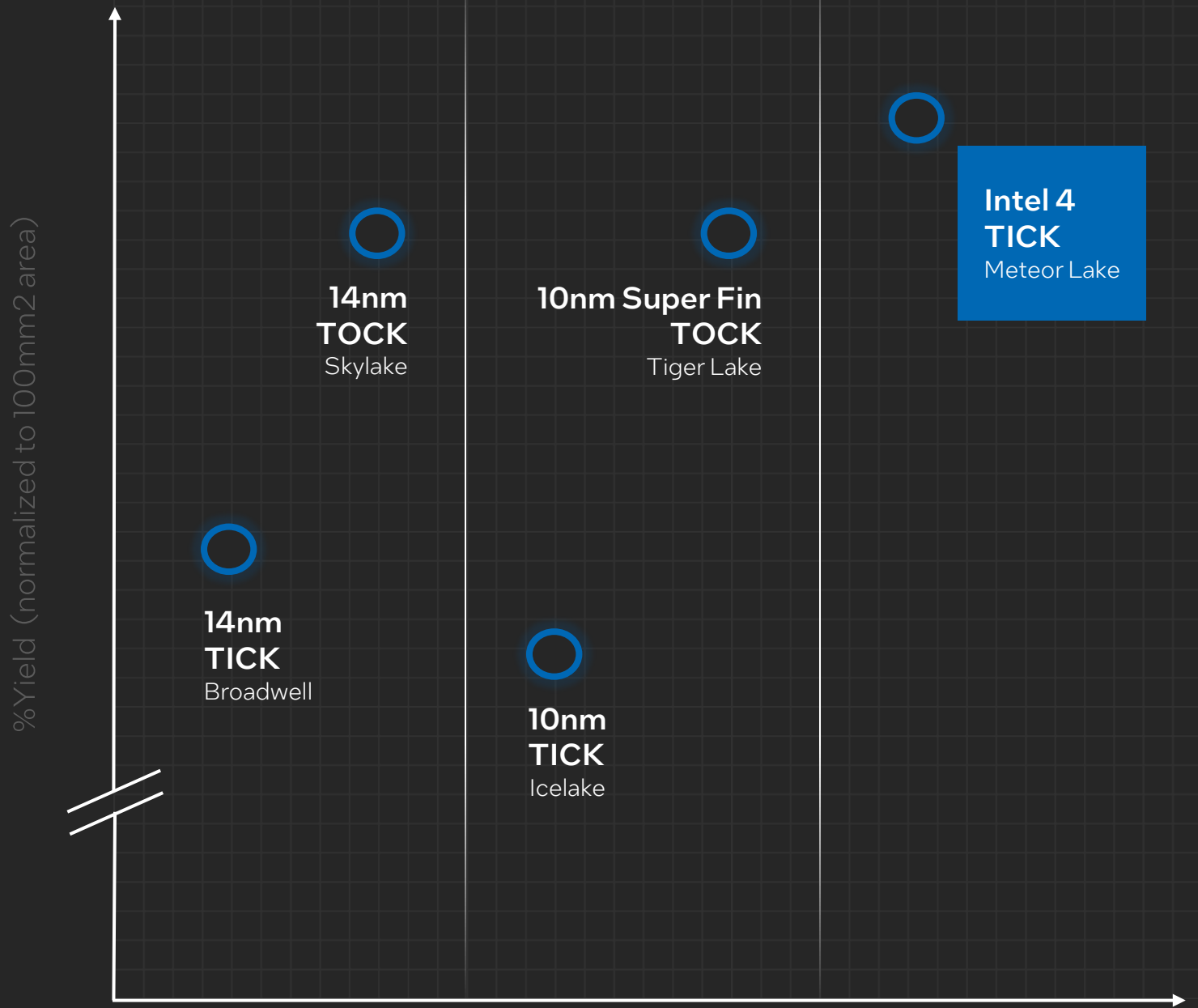
Intel 7



Intel 4



Client Yield during Launch Quarter



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Logic process technology

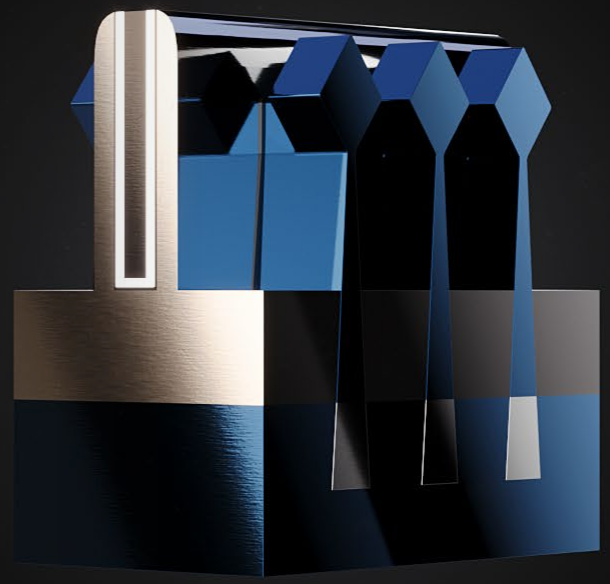
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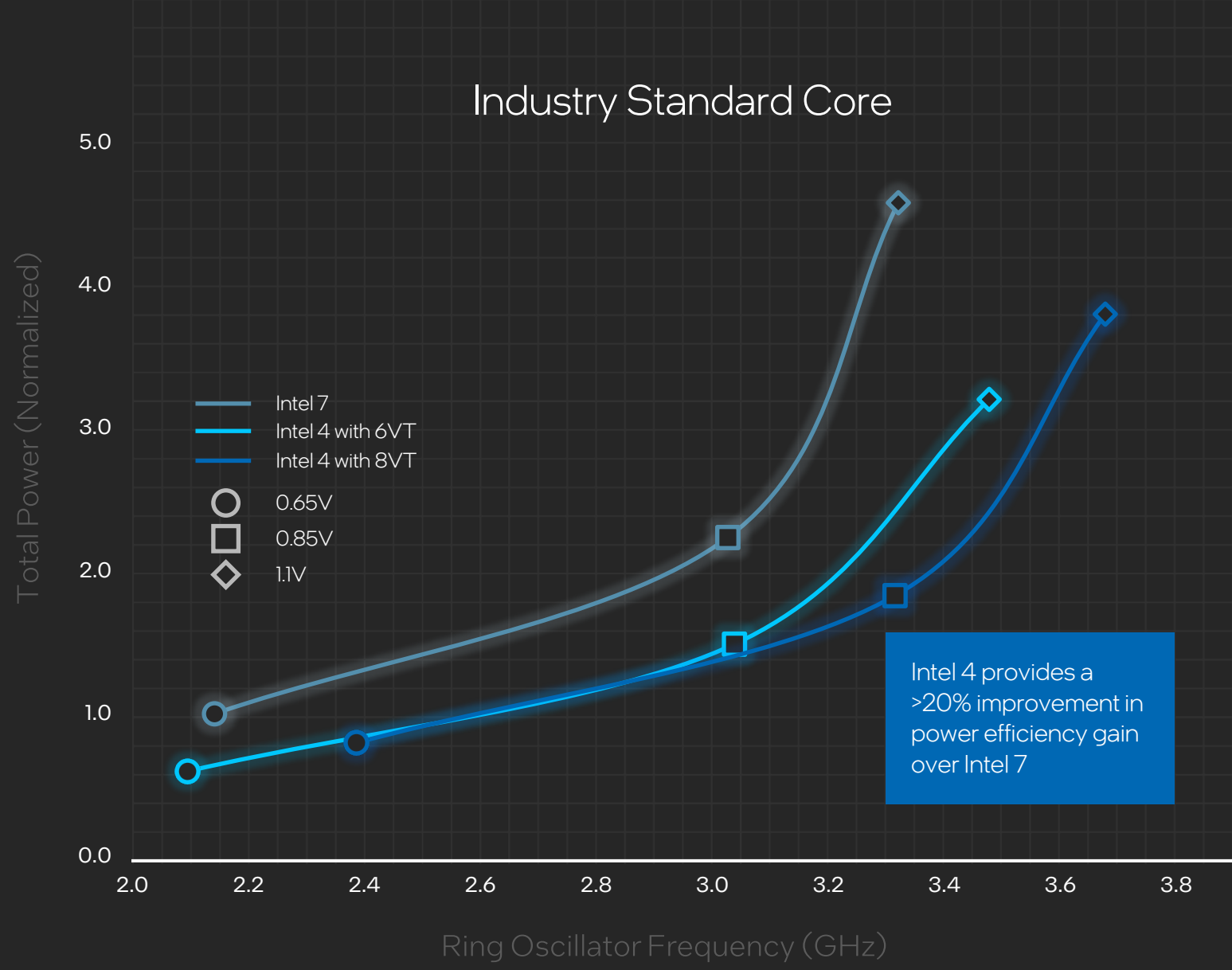
High-density MIM
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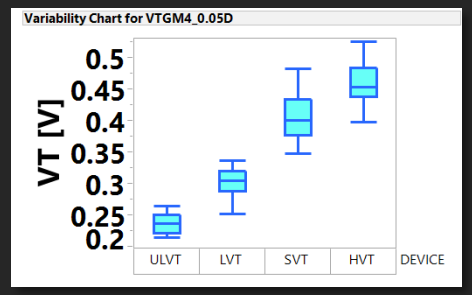
Power Performance Area

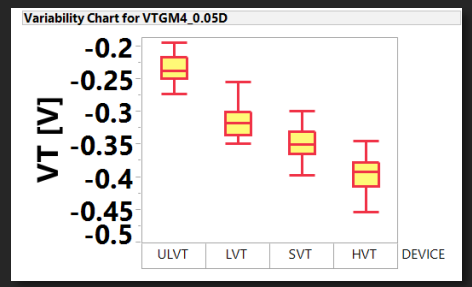
Intel 4 is optimized for HPC applications to support both low voltage (<0.65V) and high voltage (>1.1V) operation



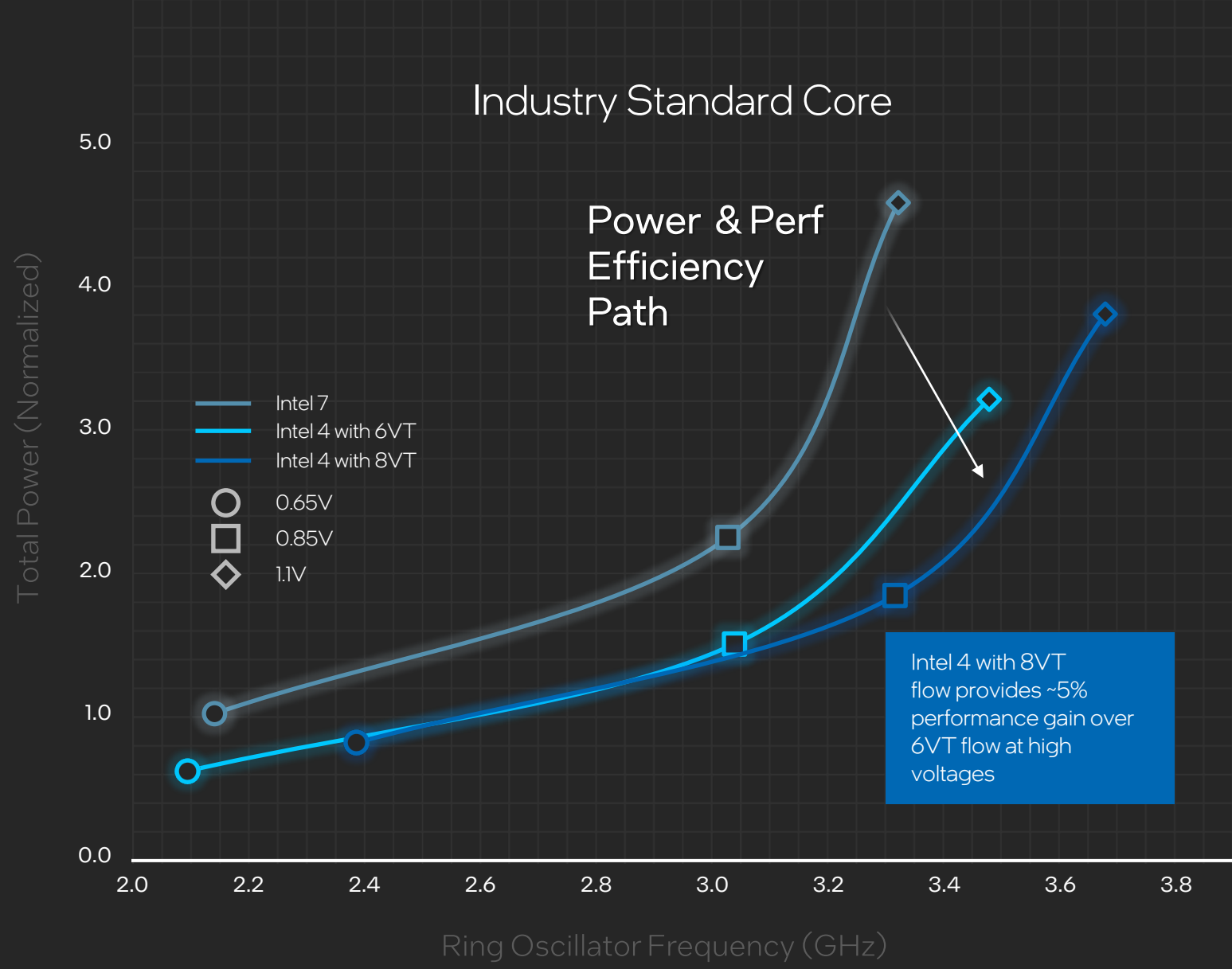
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Power Performance Area





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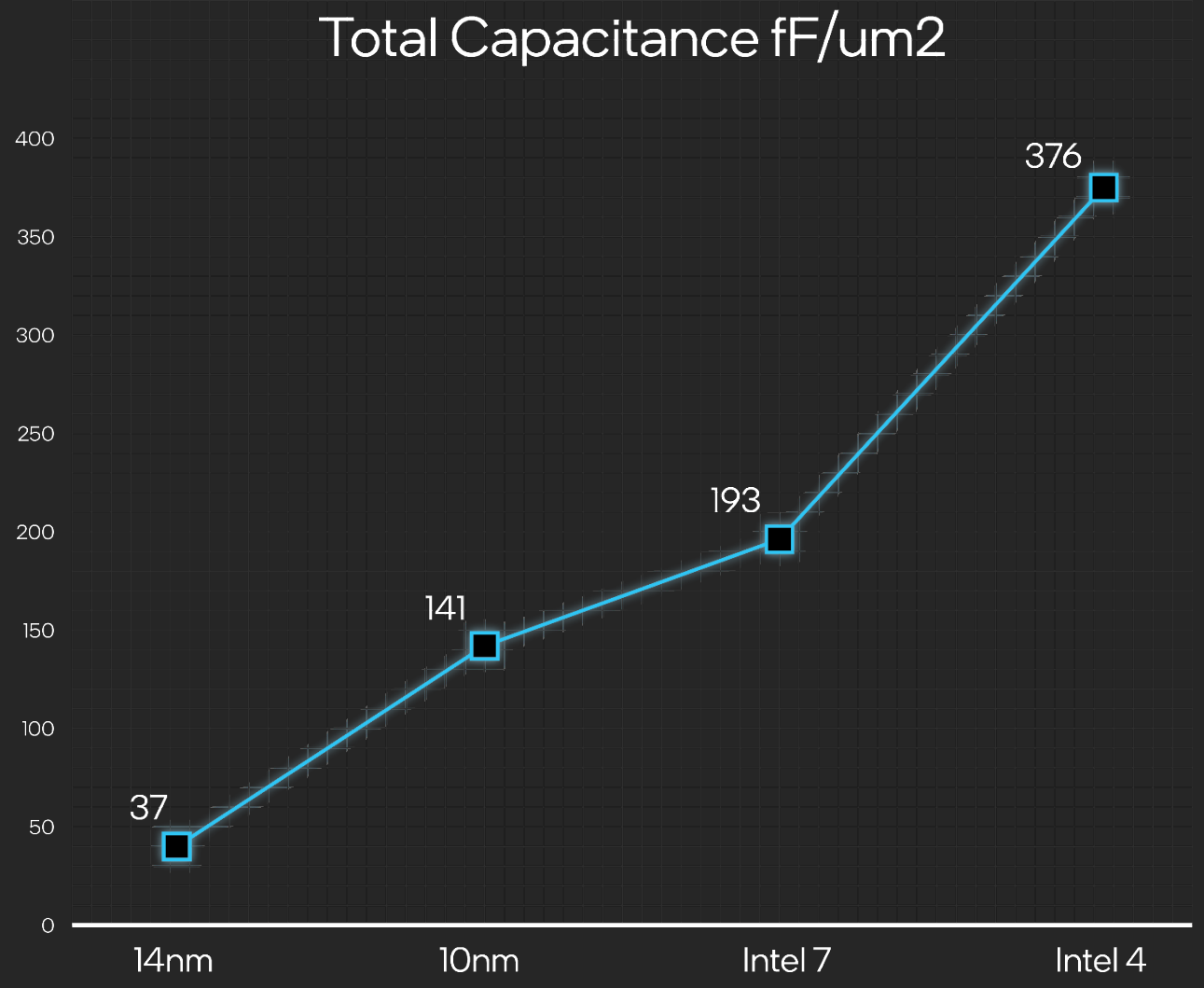
High-density MIM
for Power Delivery



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MIM Capacitor for Superior Power Delivery



Intel 4 offers ~2x increase in MIM cap density over Intel 7

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THANK YOU

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