Intel Atom® x7000 Processor Series, Intel® Processor N Series, Intel® Core™ i3-N305 Processor, & Intel® Core™ 3 Processor N355 for Edge Applications

Datasheet Addendum

February 2026

Revision 1.7

Document Number: 767454-1.7

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Revision History

Revision Number	Description	Revision Date
1.7	Added: • Added LFM value to the following tables: — Table 3 — Table 4 — Table 5 — Table 6	February 2026
1.6	Added: • Added x7000FE processor series information • Added Table 5 • Added Section 1.6 • Added Chapter 19.0 • Added Chapter 20.0 Updated: • Updated Intel® Core™ i3-N305 Processor throughout the document. • Updated Chapter 1.0 • Updated Table 1 • Updated Table 6 • Updated Table 8 • Updated Table 9 • Updated Table 10 • Updated Table 11 • Updated Figure 7 by adding title • Updated Table 21 • Updated Table 23 • Updated Table 24 • Updated Table 25 • Updated Table 26 • Updated Chapter 14.0 by adding "Note: C8, C10, & S0ix states are not supported on the • Intel Atom® x7000FE processor series." • Updated Section 16.1 by adding x7000FE processor series • Updated Section 21.1 by adding "Note: These registers are only applicable for the Intel Atom® x7000 processor series". • Updated Section 21.2 by adding "Note: These registers are only applicable for the Intel Atom® x7000 processor series". • Updated Section 21.3 by adding "Note: These registers are only applicable for the Intel Atom® x7000 processor series".	August 2025
1.5	Added: • Features and specifications for Intel® Core™ 3 Processor N355. Updated • Intel Atom® x7000 Processor Series, Intel® Processor N Series, Intel® Core™ i3-N305 Processor, & Intel® Core™ 3 Processor N355 for Edge Applications throughout the document. • All instances of "Network and Edge" to "Edge Applications". • Chapter 1.0, "Introduction". — Updated Table 2. — Updated Table 5. • Chapter 11.0, "Electrical Specifications". — Updated Table 24. — Updated Table 25. — Updated Table 26.	March 2025

Revision Number	Description	Revision Date
1.4	Added: • Chapter 2.0, "Thermal Management". — Added Section 2.1.1 "Opportunistic Throttling Management". • Chapter 6.0, "Flexible High Speed Input/Output (I/O)". — Added Note to Section 6.2. • Chapter 7.0, "Gigabit Ethernet Controller and Time-Sensitive Networking". — Added Note to Section 7.1. • Chapter 21.0, "Registers" — Added Note. Updated: • Intel Atom® x7000 Processor Series, Intel® Processor N Series, & Intel® Core™ i3 N305 Processor throughout the document. • Chapter 4.0, "Display" — Updated Section 4.1.2. • Chapter 5.0, "Graphics" — Updated Section 5.1.1. • Chapter 11.0, "Electrical Specifications". — Updated Table 24 and Table 25. • Chapter 13.0, "Image Processing Unit". • Chapter 18.0, "Memory". — Updated Table 30.	October 2024
1.3	Added: • x7000RE & x7000C information throughout the document. • Chapter 15.0, "Power Delivery". • Chapter 16.0, "Communication & Industrial Use Condition Compliance". • Chapter 17.0, "Enhanced Serial Peripheral Interface (eSPI)". • Chapter 18.0, "Memory". Updated: • Intel Atom® Processors x7000 Series, Intel® Processor N Series, & Intel® Core™ i3-N305 Processor throughout the document. • Chapter 1.0, "Introduction". — Added Figure 2. — Updated Table 3. — Updated Table 4. • Chapter 2.0, "Thermal Management". — Added "The Processor Die and PCH power management features are disabled." — Added Table 9 and Table 11. — Updated the title for Table 8 and Table 10. • Chapter 3.0, "In-Band Error Correction Code". — Updated "IBECC errors can be reported by the IOP as an MCE (Machine Check Error)." • Chapter 4.0, "Display". — Updated Note for Section 4.1. — Updated Resolution Supported "SKUs 1, 3-11". • Chapter 5.0, "Graphics". — Updated Note for Section 5.1. • Chapter 8.0, "USB-C* Sub System (TCSS)". — Added "Intel Atom® x7000C processors do not support DPoC, DisplayPort, or HDMI". — Added Table 20. • Chapter 11.0, "Electrical Specifications". — Updated Table 24.	February 2024

Revision Number	Description	Revision Date
1.2	Updated: • GBE controller naming throughout the document. • NEX and Network & Edge naming throughout the document. • Table 1. • Table 24. • Table 25. • Table 26. Added: • Chapter 2.0, "Thermal Management". — Added new Section 2.1. • Chapter 3.0, "In-Band Error Correction Code". — Added additional bullets for Section 3.3. • Chapter 5.0, "Graphics". — Add Note for Section 5.1. • Chapter 13.0, "Image Processing Unit". — Added Note before Section 13.1. • Chapter 7.0, "Gigabit Ethernet Controller and Time-Sensitive Networking". — Added new Notes for Section 7.2.1 and Section 7.2.2. Removed: • Chapter 1.0, "Introduction". — Note 1 for Table 3.	October 2023
1.0	• Initial release.	February 2023

Contents

Figures

Tables

1.0 Introduction

This Datasheet Addendum is a supplementary document that covers Edge Applications specific features and complements for the following:

- Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet, Volume 1 of 2 (RDC #759603)
- Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet - Volume 2 of 2 (RDC #759604)

Intel Atom® x7000 Processor Series, Intel® Processor N Series, Intel® Core™ i3-N305 Processor, & Intel® Core™ 3 Processor N355 for Edge Applications are 64-bit, multi-core processors built on Intel 7 process technology and are offered in a 1-package Platform that includes the Processor Die and Platform Controller Hub (PCH) die on the same Multi-Chip Package (MCP).

This document serves as a supplementary documentation, ensure all required specifications from the following are met prior to using this document, unless mentioned otherwise:

- Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet, Volume 1 of 2 (RDC #759603)
- Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet - Volume 2 of 2 (RDC #759604)

1.1 Terminology

Table 1. Terminology

Term	Description
4k	Ultra High Definition (UHD)
AES	Advanced Encryption Standard
AGC	Adaptive Gain Control
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
AVC	Advanced Video CODEC
ARP	Address Resolution Protocol
ART	Always Running Timer
BAR	Base Address Register
BGA	Ball Grid Array
BIOS	Basic Input Output System
BIST	Built-in Self-Tests
BIU	Bus Interface Unit
CMCI	Corrected Machine-Check Interrupt
CMOS	Complementary Metal Oxide Semiconductor. A manufacturing process used to produce electronics circuits, but in reference to RTC is used interchangeably as the RTC's RAM (i.e., clearing CMOS meaning to clear RTC RAM).
COE	Checksum Offload Engine
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSE	Converged Security Engine
CtC	Check the Checker
cTDP	Assured Power (previously known as configurable TDP)
DCI	Debug Connect Interface
DMA	Direct Memory Access
DP*	Display Port*
e2e	End-to-End
ECC	Error Correction Code
eDP*	embedded Display Port*
EIPV	error IP is valid
FEC	Fetch Execution Cluster (Instruction Cache/Fetch)
FIA	Flex IO Adapter
FSP	Firmware Support Package
FuSa	Functional Safety
FLR	Function Level Reset
GbE	Gigabit Ethernet
GPU	Graphics Processing Unit
HW	Hardware
I2C	Inter Integrated Circuit

Table 1. Terminology

Term	Description
IBECC	In-band ECC
ICMP	Internet Control Message Protocol
IEEE	Institute of Electrical and Electronics Engineers
IEH	Integrated Error Handler
IERR	Internal Error
Intel® TCC	Intel® Time Coordinated Computing
IOMCA	I/O machine check bank
IOSF-SB	Intel On-chip System Fabric - Sideband
IP	Internet Proctocol
IPU	Image Processing Unit
IRQ	Interrupt Request (usually wire)
ITSS	Interrupt and Timer Sub-System
JTAG	Joint Test Action Group
LLC	Last Level Cache
LVT	Local Vector Table
MAC	Media Access Control
MCA	Machine Check Architecture
MCE	Machine Check Exception
MCERR	Machine Check Error
MDIO	Management Data Input/Output
MCi	Machine Check Interrupt
MCIP	Machine Check Interrupt Pending
MEC	Memory Execution Cluster (Data Cache/Fetch/Store)
MSI	Message Signalled Interrupt
MSR	Model-Specific Register
NMI	Non Maskable Interrupt
OS	Operating System
P2SB	Primary to Sideband Bridge
PCH	Platform Controller Hub
PCI*	Peripheral Component Interconnect*
PCS	Physical Coding Sublayer
PMC	Power Management Controller - dedicated microprocessor running power management firmware
PMIP	Power Management IP
PPM	Parts Per Million. Used to provide crystal accuracy or as a frequency variation indicator
PS	Power State (exp: PS0,PS1, etc.)
PSF	Primary Sideband Fabric
PTR	Processor Transaction Router
RAM	Random Access Memory
RDC	Resource & Documentation Centre (Intel)

Table 1. Terminology

Term	Description
RDMSR	Read MSR
RIPV	restart IP is valid
SERR#	System Error
SGMII	Serial Gigabit Media Independent Interface
SKU	Stock Keeping Unit
STA	Station Management
SW	Software
TBI	Ten Bit Interfaces
TC	Traffic Class
TCC	Thermal Control Circuit
TCP	Transmission Control Protocol
TDP	Processor Base Power (a.k.a Thermal Design Power)
TSN	Time-Sensitive Networking
TSO	TCP Segmentation Offload
UART	Universal Asynchronous Receiver Transmitter
UCR	Uncorrected Recoverabl
UDP	User Datagram Protocol
USB	Universal Serial Bus
VR	Voltage Regulator
WRMSR	Write MSR

1.2 Reference Documents

Table 2. Reference Documents

Document	Document No./Location
Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet - Volume 1 of 2	759603
Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet - Volume 2 of 2	759604

1.3 Processor Block Diagram

Figure 1. Processor Die Block Diagram

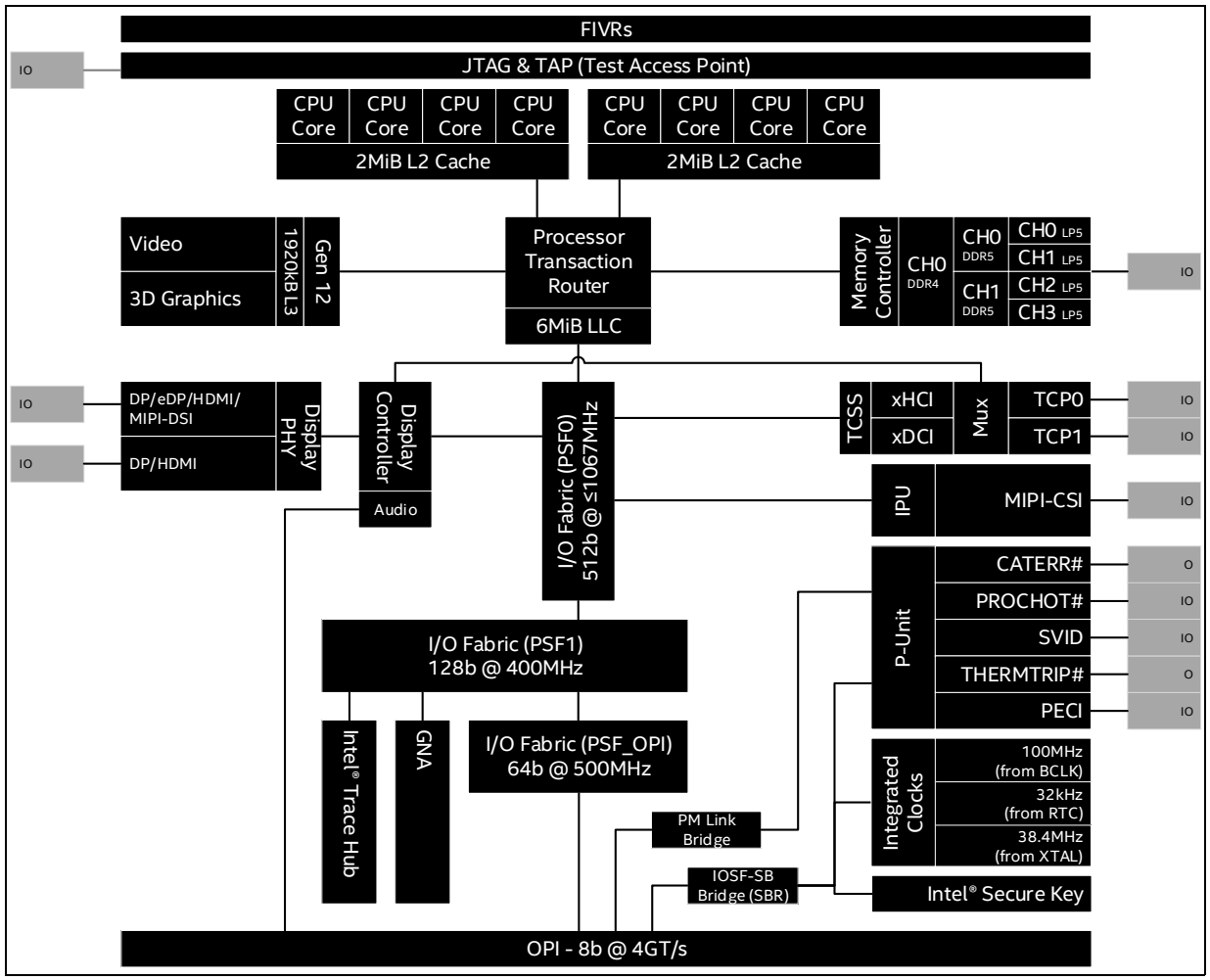


Figure 2. Processor Die Block Diagram (x7000C)

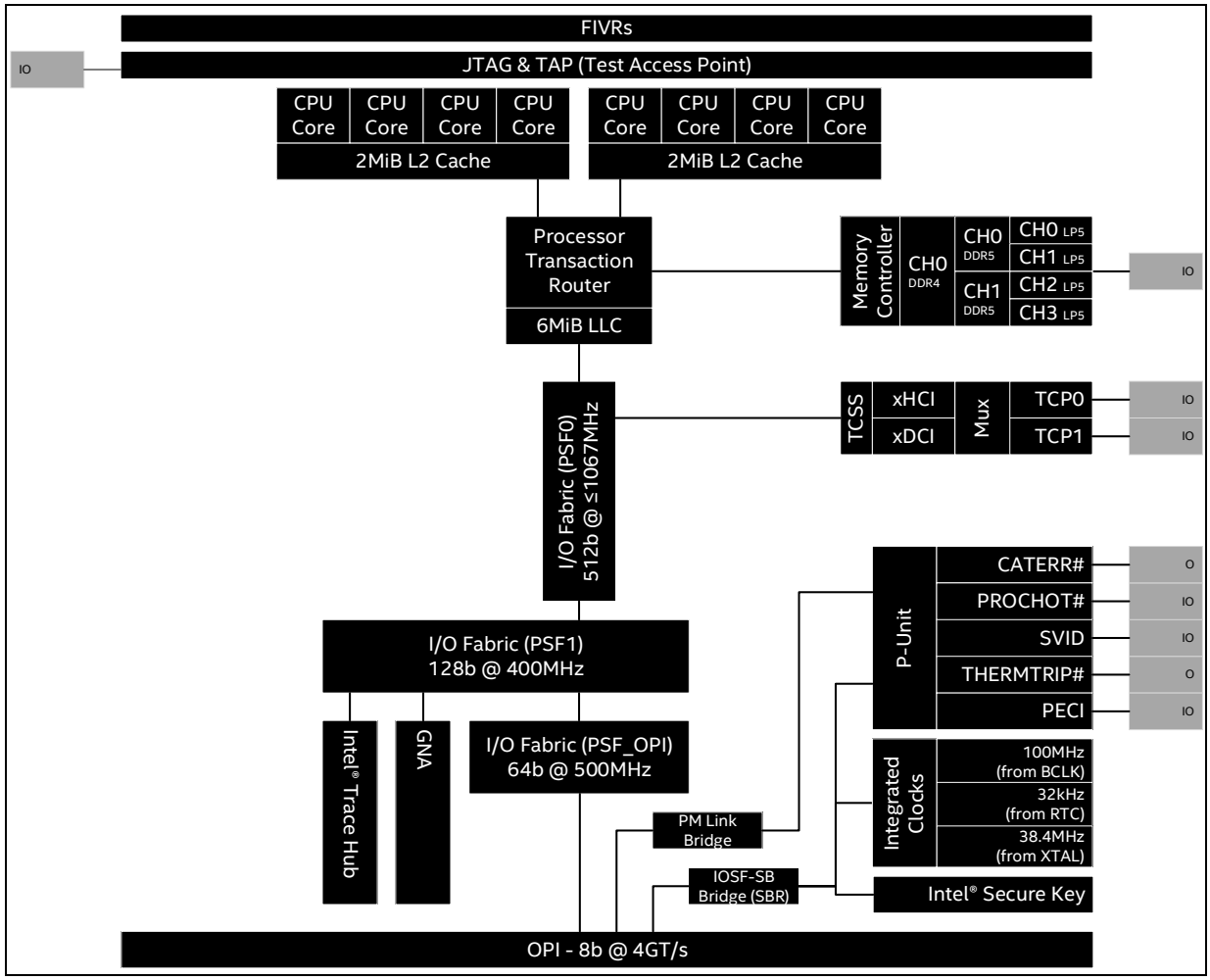


Figure 3. PCH Block Diagram

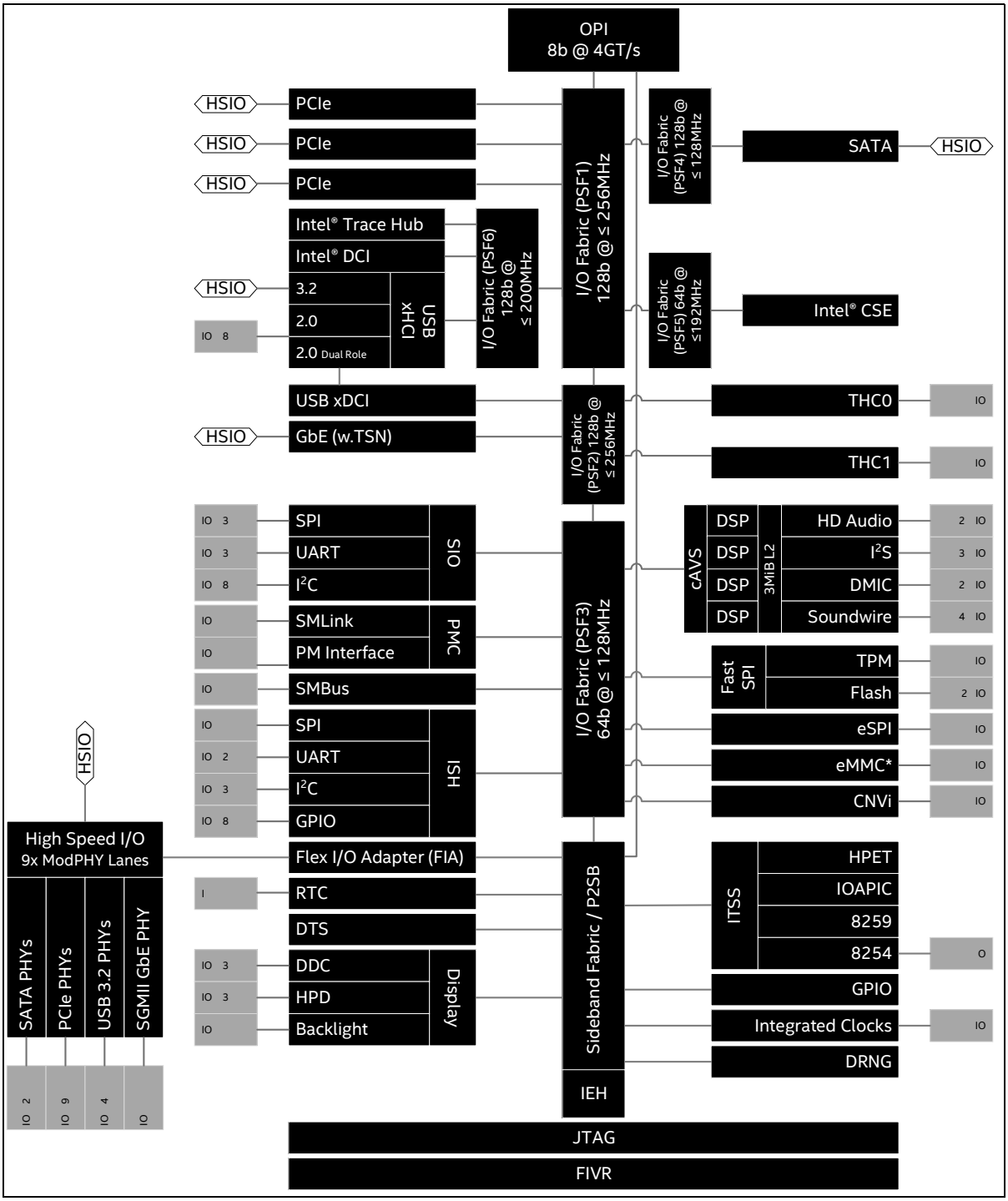
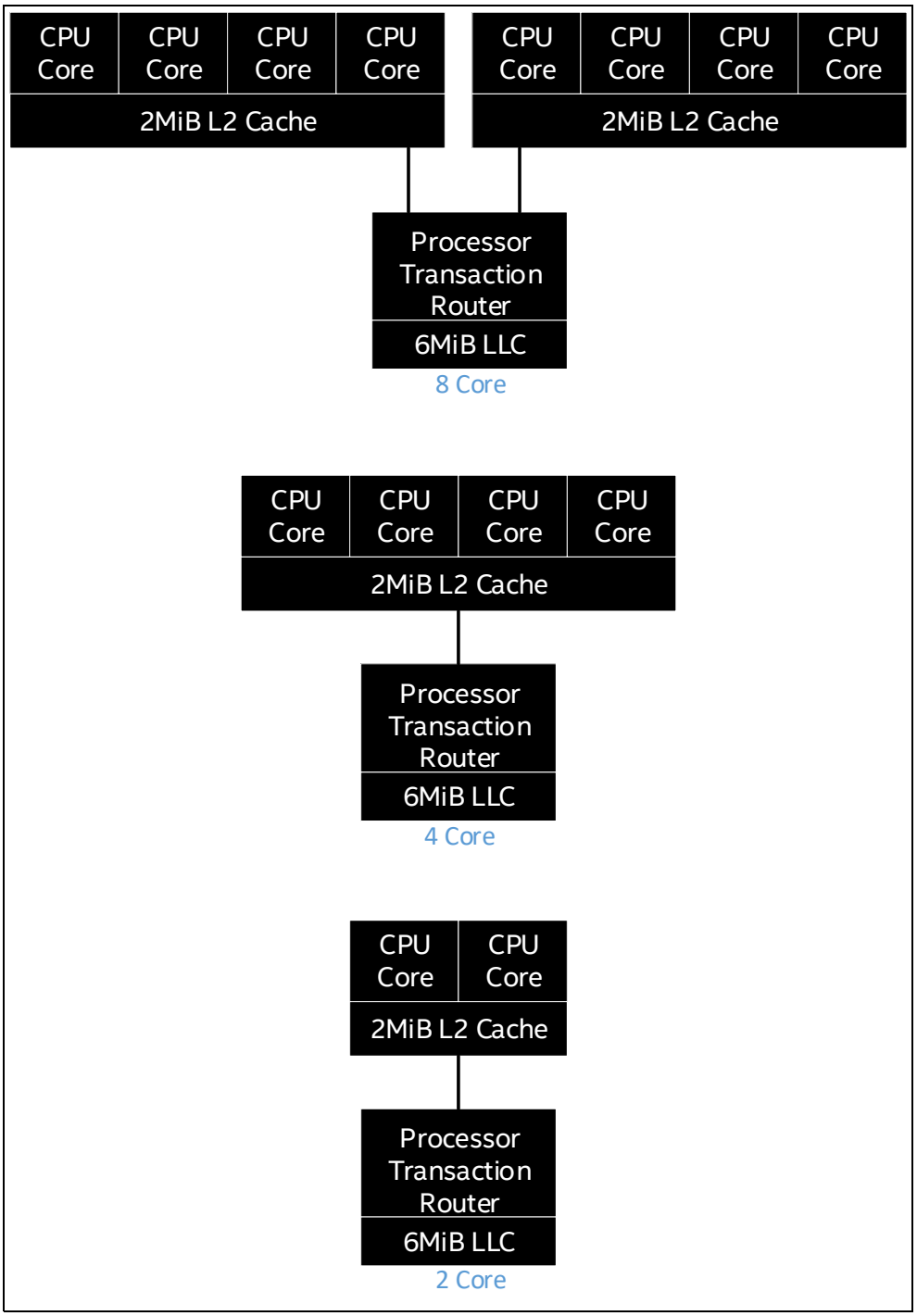


Figure 4. CPU Core Counts



1.4 Supported SKUs

Table 3. Supported SKU Map (N series and x7000E)

Processor	SKU 1	SKU 2	SKU 3	SKU 4		SKU 5	SKU 6	SKU 7
Brand	Intel® Processor N50	Intel® Processor N97	Intel® Processor N200	Intel® Core™ i3-N305		Intel Atom® x7211E	Intel Atom® x7425E	Intel Atom® x7213E
Use Condition	PC Client		See Table 1 in Datasheet Volume 1 for further information	PC Client		Embedded		
TDP(W)	6	12		15	cTDP=9[2]	6	12	10
Core Count	2	4		8		2	4	2
CPU HFM	1.0GHz	2.0GHz		1.8GHz	1.0GHz[2]	1.0GHz	1.5GHz	1.7GHz
1C Turbo	3.4GHz	3.6GHz		See Table 1 in Datasheet Volume 1 for further information		3.2GHz	3.4GHz	3.2GHz
MC Turbo	3.4GHz	2.9GHz				2.9GHz	2.7GHz	2.9GHz
EU Count	16	24				16	24	16
GFx HFM	600MHz	850MHz				600MHz	800MHz	800MHz
Turbo	750MHz	1.2GHz				1.0GHz	1.0GHz	1.0GHz
Intel® TCC	No	No	No	No		Yes	Yes	Yes
GbE MAC	No	No	No	No		Yes	Yes	Yes
CNVi	Yes	Yes	Yes	Yes		Yes	Yes	No
IPU	Yes	Yes	Yes	Yes		Yes	Yes	No
LFM	400MHz	400MHz	400MHz	400MHz		400MHz	400MHz	400MHz

Note:

1. Assured Power (cTDP) and Low-Power Mode (LPM) are not supported by Intel Dynamic Tuning Technology (DTT) driver for these SKUs in Edge Applications.
2. This information serves as a Specification Clarification to Table 1 of Datasheet Volume 1 and is not an Edge Applications specific feature.

Table 4. Supported SKU Map (x7000RE and x7000C)

Processor	SKU 8	SKU 9	SKU 10	SKU 11	SKU 12	SKU 13	SKU 14
Brand	Intel Atom® x7211RE	Intel Atom® x7213RE	Intel Atom® x7433RE	Intel Atom® x7835RE	Intel Atom® x7203C	Intel Atom® x7405C	Intel Atom® x7809C
Use Condition	Embedded, Communication & Industrial				Embedded & Communication		
TDP(W)	6	9	9	12	9	12	25
Core Count	2	2	4	8	2	4	8
CPU HFM	1.0GHz	2.0GHz	1.5GHz	1.3GHz	2.0GHz	2.2GHz	2.4GHz
1C Turbo[2]	3.2GHz	3.4GHz	3.4GHz	3.6GHz	3.2GHz	3.4GHz	3.6GHz
MC Turbo[2]	2.9GHz	2.9GHz	2.7GHz	3.0GHz	2.9GHz	2.7GHz	3.0GHz
EU Count	16	16	32	32	N/A	N/A	N/A
GFx HFM	400MHz	600MHz	600MHz	800MHz	N/A	N/A	N/A
GFx Turbo[2]	1.0GHz	1.0GHz	1.0GHz	1.2GHz	N/A	N/A	N/A
Intel® TCC	Yes	Yes	Yes	Yes	Yes	Yes	Yes
GbE MAC	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CNVi	No	No	No	No	No	No	No
IPU	Yes	No	Yes	Yes	No	No	No
LFM	400MHz	400MHz	400MHz	400MHz	400MHz	400MHz	400MHz

Note:

1. Assured Power (cTDP) and Low-Power Mode (LPM) are not supported by Intel Dynamic Tuning Technology (DTT) driver for these SKUs in Edge Applications.
2. Turbo must be disabled for Communications or Industrial use conditions.

Table 5. Supported SKU Map (x7000FE)

Processor	SKU 18	SKU 19
Brand	x7433FE	x7835FE
Use Condition	Embedded, Communication & Industrial	
TDP(W)	9	12
Core Count	4	8
CPU HFM	1.5 GHz	1.3 GHz
1C Turbo[2]	3.4 GHz	3.6 GHz
MC Turbo[2]	2.7 GHz	3.0 GHz
EU Count	32	
GFx HFM	600 MHz	800 MHz
GFx Turbo[2]	1.0 GHz	1.2 GHz
Intel® TCC	Yes	Yes
GbE MAC	Yes	Yes
CNVi	No[3]	No[3]

IPU	Yes	Yes
LFM	400MHz	400MHz

Note:
1. Assured Power (cTDP) and Low-Power Mode (LPM) are not supported by Intel Dynamic Tuning Technology (DTT) driver for these SKUs in Edge Applications.
2. Turbo must be disabled for Communications or Industrial use conditions.
3. CNVi is not supported for Edge Applications.

Table 6. Supported SKU Map (N Series)

Processor	SKU 15	SKU 16	SKU 17	
Brand	Intel® Processor N150	Intel® Processor N250	Intel® Core™ 3 N355	
Use Condition	See Table 1 in the Datasheet Volume 1 for further information	See Table 1 in the Datasheet Volume 1 for further information	PC Client	
TDP(W)			15	cTDP=9
Core Count			8	
CPU HFM			1.9GHz	1.0GHz[2]
1C Turbo			See Table 1 in the Datasheet Volume 1 for further information	
MC Turbo				
EU Count				
GFx HFM				
GFx Turbo				
Intel® TCC	No	No	No	
GbE MAC	No	No	No	
CNVi	No[1]	No[1]	No[1]	
IPU	Yes	Yes	Yes	
LFM	400MHz	400MHz	400MHz	

Note:
1. Assured Power (cTDP) and Low-Power Mode (LPM) are not supported by Intel Dynamic Tuning Technology (DTT) driver for these SKUs in Edge Applications.
2. This information serves as a Specification Clarification to Table 1 of the Datasheet Volume 1 and is not an Edge Applications specific feature.
3. CNVi is not supported for Edge Applications.

1.5 Operating Systems Support

Table 7. Operating Systems Support

Windows* 10	Windows* 11	Android	Linux
Yes[1,2]	Yes	Yes[1,2]	Yes

Note:

1. Not supported on Intel Atom® x7000C processors.

2. Not supported on Intel® Processors N150 & N250 and Intel® Core™ 3 Processor N355.

1.6 Power Management Support

This section applies only to Intel Atom® x7000FE processors. For other processors, refer to Section 1.4 of the Datasheet Volume 1 (RDC #759603).

1.6.1 Processor Core Power Management

- Full support of ACPI C-states as implemented by the following processor C-states:

— C0, C1, C1E, C6

Note: C8 & C10 states are not supported.

- Enhanced Intel SpeedStep® Technology
- Intel® Speed Shift Technology

1.6.2 System Power Management

- S0, S3, S4, S5

Note: S0ix states are not supported.

§ §

2.0 Thermal Management

Note: For any capability not mentioned in this section, refer to Chapter 12 of the Datasheet Volume 1 of 2 (RDC# 759603).

2.1 Processor Thermal Management

Note: This section serves as a Specification Clarification to the corresponding section of Datasheet Volume 1 and is not an Edge Applications specific feature. A Specification Clarification describes a specification in greater detail or further highlight a specification impact to a complex design situation.

Processor Base Power (a.k.a TDP) is the average power dissipation (at Tj=100 °C) that is validated during manufacturing for the base configuration when executing a near worst case commercially available workload as specified by Intel for the SKU segment. The workload specified for this platform is CPU-intensive with minimal GPU activity.

The average power dissipation of some processors may be caused to exceed the specified TDP value when:

- A concurrently CPU-intensive and GPU-intensive workload is executed.
- The platform design is different from the base configuration. For example, when an HDMI display is used instead of an eDP display.
- The Processor Die and PCH power management features are disabled.

In such cases where the TDP value is exceeded, the processor will opportunistically throttle the CPU and/or GPU frequency to ensure the processor stays within configured power and thermal limits.

2.1.1 Opportunistic Throttling Management

In platforms where the base configuration and/or workload results in opportunistic throttling, it may be possible to reduce the throttling by increasing the Power Limit 1 (PL1) value above TDP.

Note: PL1 must not be set higher than thermal solution cooling limits.

Note: PL1 must be increased only to the value where CPU and/or GPU stops opportunistically throttling below their High-Frequency Mode (HFM) frequencies.

Caution: Increasing PL1 above TDP + 8W is not supported and may result in the processor's inability to meet Intel's reliability goals.

2.2 Processor Line Thermal and Power Specifications

The following notes apply to Package Turbo Specification below.

Note	Definition
1	Can be modified at runtime by MSR writes, with MMIO and with PECI commands.
2	'Turbo Time Parameter' is a mathematical parameter (units of seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds. Refer to Platform Power Control under Thermal Management in the Datasheet Volume 1 of 2 (RDC #759603) for further information.
3	The shown limit is a time averaged-power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.
4	The Processor will be controlled to a specified power limit. If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.
5	This is a hardware default setting and not a behavioral characteristic of the part.
6	For controllable turbo workloads, the PL2 limit may be exceeded for up to 10ms.
7	Hardware default of PL1 Tau=1s, By including the benefits available from power and thermal management features the recommended is to use PL1 Tau=28s.
8	PL1 Tau max recommendation value is the default value in the BIOS/BKC and this value is been tested

Table 8. Intel Atom® x7000E Processor Series, Intel® Processor N Series, Intel® Core™ i3-N305 Processor, & Intel® Core™ 3 Processor N355 for Edge Applications

Processor IA Cores, Graphics, Configuration and Processor Base Power (a.k.a TDP)	Parameter	Minimum	Tau MSR Max Value	Recommended Value	Units	Notes
4 Core 12W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	12	W	
	Power Limit 2 (PL2)	N/A	N/A	25	W	
2 Core 10W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	10	W	
	Power Limit 2 (PL2)	N/A	N/A	25	W	
2 Core 6W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	6	W	
	Power Limit 2 (PL2)	N/A	N/A	25	W	

Notes:

- No Specifications for Min/Max PL1/PL2 values.
- PL2 - Processor opportunistic higher Average Power – Reactive, Limited Duration controlled by Tau_PL1 setting.
- PL1 Tau - PL1 average power is controlled via PID algorithm with this Tau, the larger the Tau, the longer the PL2 duration.
- System cooling solution and designs found to not being able to support the Performance TauPL1, adjust the TauPL1 to cooling capability.

Table 9. Package Turbo Specification: Intel Atom® x7000RE, x7000C, &7000FE Processor Series

Processor IA Cores, Graphics, Configuration and Processor Base Power (a.k.a TDP)	Parameter	Minimum	Tau MSR Max Value	Recommended Value	Units	Notes
8 Core 25W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	25	W	
	Power Limit 2 (PL2)	N/A	N/A	35	W	
8 Core 12W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	12	W	
	Power Limit 2 (PL2)	N/A	N/A	35	W	
4 Core 12W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	12	W	
	Power Limit 2 (PL2)	N/A	N/A	25	W	
4 Core 9W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	9	W	
	Power Limit 2 (PL2)	N/A	N/A	25	W	
2 Core 9W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	9	W	
	Power Limit 2 (PL2)	N/A	N/A	25	W	
2 Core 6W	Power Limit 1 Time (PL1 Tau)	0.1	448	28	S	1,2,3,4,5,6,7,8
	Power Limit 1 (PL1)	N/A	N/A	6	W	
	Power Limit 2 (PL2)	N/A	N/A	25	W	

Notes:

- No Specifications for Min/Max PL1/PL2 values.
- PL2 - Processor opportunistic higher Average Power – Reactive, Limited Duration controlled by Tau_PL1 setting.
- PL1 Tau - PL1 average power is controlled via PID algorithm with this Tau, the larger the Tau, the longer the PL2 duration.
- System cooling solution and designs found to not being able to support the Performance TauPL1, adjust the TauPL1 to cooling capability.

Table 10. Intel Atom® x7000E Processor Series, Intel® Processor N Series, Intel® Core™ i3-N305 Processor, & Intel® Core™ 3 Processor N355 for Edge Applications

Segment	Symbol	Package Turbo Parameter	Temperature Range		Processor Base Power (a.k.a TDP) Specification Temperature Range		Units	Notes
			Minimum	Maximum	Minimum	Maximum		
BGA	T_j	Junction Temperature Limit	0	105	35	105	°C	1,2
Intel Atom® SKUs	DTR	N/A	T_{BOOT} -70	T_{BOOT} +70	N/A	N/A	°C	3

Notes:
1. The processor supports commercial ambient temperature range, and memory devices should operate in the same condition.
2. For other junction temperature specification, refer to the note mentioned under *Thermal Management* in the *Datasheet Volume 1 of 2 (RDC #759603)*.
3. For a single operational cycle, the processor executes at full data sheet performance across the full Dynamic Temperature Range (DTR) without requiring a cold reset (S0 to S5 to S0 state transition). DTR is the range of Tj starting from boot (T_{BOOT}) and transitioning Cold-to-Hot (T_{BOOT} + DTR) and/or Hot-to-Cold (T_{BOOT} - DTR). A Tj outside of the DTR range requires a re-boot but is not enforced by the hardware.

Table 11. Processor Temperature Specifications: Intel Atom® x7000RE, x7000C, & x7000FE Processor Series for Edge Applications

Segment	Symbol	Package Turbo Parameter	Temperature Range		Processor Base Power (a.k.a TDP) Specification Temperature Range		Units	Notes
			Min	Max	Min	Max		
BGA	T_j	Junction Temperature Limit	-40 (x7000RE & x7000FE) 0 (x7000C)	105	35	105	°C	1,2
Communication Use Condition	DTR	N/A	T_{BOOT} -70	T_{BOOT} +70	N/A	N/A	°C	3

Segment	Symbol	Package Turbo Parameter	Temperature Range		Processor Base Power (a.k.a TDP) Specification Temperature Range		Units	Notes
			Min	Max	Min	Max		
Embedded Use Condition	DTR	N/A	T_{BOOT} -90 (x7000RE, x7000FE)	T_{BOOT} +90	N/A	N/A	°C	3,5
			T_{BOOT} -70 (x7000C)	T_{BOOT} +70				3,4
Industrial Use Condition	DTR	N/A	T_{BOOT} -110 (x7000RE, x7000FE)	T_{BOOT} +110	N/A	N/A	°C	3,5

Notes:

1. x7000RE & x7000FE processors support extended ambient temperature range, and memory devices should operate in the same condition. x7000C processors support commercial ambient temperature range, and memory devices should operate in the same condition.
2. For other junction temperature specification, refer to the note mentioned under *Thermal Management* in the *Datasheet Volume 1 of 2 (RDC #759603)*.
3. For a single operational cycle, the processor executes at full data sheet performance across the full Dynamic Temperature Range (DTR) without requiring a cold reset (S0 to S5 to S0 state transition). DTR is the range of Tj starting from boot (T_{BOOT}) and transitioning Cold-to-Hot (T_{BOOT} + DTR) and/or Hot-to-Cold (T_{BOOT} - DTR). A Tj outside of the DTR range requires a re-boot but is not enforced by the hardware.
4. Applicable to x7000C processors only.
5. Applicable to x7000RE & x7000FE processors only.

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3.0 In-Band Error Correction Code

3.1 In-Band Error Correction Code Introduction

The In-Band Error Correction Code (IBECC) module improves accuracy and reliability by providing error check and correct protection to all or specific regions of the physical memory space. The IBECC can be enabled for memory technologies that do not support the out-of-band ECC, where the cost of adding an additional device to each channel for ECC data storage is prohibitive.

Note: IBECC support is OS agnostic and only requires BIOS configuration to be active.

3.2 IBECC Transaction

3.2.1 Functionality Overview

The IBECC recognizes whether a region should be protected, based on the incoming request address. The IBECC will allow up to eight different address regions to be protected. An ECC space will also be reserved to store the ECC values for all protected regions and the minimum size for each region is 32MB. All the regions and the corresponding ECC space will have to be configured through BIOS.

The IBECC protects data at a cache line granularity (64 Bytes), with a 16-bit SECDED code. An ECC data cache line will contain the ECC value of 32 data (non-ECC) cache lines. So, the IBECC will add a memory overhead of 1/32, if the entire memory is protected by ECC. However for simplicity, when the IBECC is enabled, 1/32 of total DRAM size must be reserved for ECC storage regardless of the size and number of the protected regions. BIOS must ensure that a sufficient overflow region is allocated to account for this overhead, and that the space is removed from usable DRAM address space. The IBECC can be enabled for DDR4, DDR5 and LPDDR5 technologies. Nevertheless, all populated memory channels need to be of the same size.

The IBECC converts a read/write transaction (cache line access) to a protected region of memory into two separate memory requests (read/write), one to the actual data cache line and another to the cache line containing the ECC value. Based on the incoming read/write address the IBECC determines the address of the ECC data corresponding to that cache line.

3.2.2 Protected Read

For protected reads, the IBECC:.

- Tracks when both reads have completed.
- Uses its ECC unit to detect and correct for any errors.
- Forwards the post-correction data to the requesting agent.

3.2.3 Protected Full Writes

For protected full writes, the IBECC needs to ensure that it:

- Generates the ECC value for the write, using the ECC generation logic with the appropriate byte enables set.

3.2.4 Protected Partial Writes

For protected partial writes, the IBECC needs to:

- Issue a protected, read transaction for the underfill.
- Do the merge with the original write data.
- Issue a protected, full write.

Note: In this case, for protected partial writes, the IBECC will have to issue 2 read and two write requests in total.

3.3 Error Reporting and Logging

The IBECC needs to identify ECC errors and report them. For the reported error, the IBECC needs to keep the following fields:

- CMI Address.
- Syndrome.
- Type of error valid bits - correctable and uncorrectable.

The IBECC will report all correctable and uncorrectable errors by sending PCIE_ERR message on IOSF-SB to IOP.

Note: IBECC errors can be reported by the IOP as an MCE (Machine Check Error).

Logging - there is only one event logged. The IBECC shall always keep the worst first error. This means that:

- A correctable error is logged if no error was reported before.
- The first uncorrectable error may override previous correctable errors.
- Later uncorrectable errors do not override the first uncorrectable error.
- Any correctable errors that happen when the CERRSTS bit is set, only the CERR_OVERFLOW bit is set.
- Any uncorrectable errors that happen when MERRSTS bit is set, only the MERR_OVERFLOW bit is set.
- If real-time error reporting is required, for applications such as IBECC testing, then the platform software will need to clear each error after it is logged.

The ECC_ERROR_LOG contents are valid only when either the MERRSTS or CERRSTS bits are set.

An uncorrectable error on underfill read is not logged, but the WDB entry is poisoned so it is rewritten to memory as uncorrectable error.

Note: Refer to the Table 3-3, *Datasheet Volume 2 of 2 (RDC #759604)* for IBECC registers definition and details.

Note: Since the IBECC module operates on the CMI data bus connecting the Processor Transaction Router and the Memory Controller, rather than on a per memory channel basis, it is not possible to correlate the error syndrome to the external data signal that is in error.

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4.0 Display

4.1 Display Features

Note:

1. For any capability not mentioned in this section, refer to Chapter 23 (Display) of Datasheet Volume 1 of 2 (RDC# 759603).
2. Intel Atom® x7000C processors do not have any display capabilities.

4.1.1 General Capabilities

- Supports:
  - Up to 3x4K60 SDR[1]
  - Pipelock[2]: 2 outputs synchronization

Note:

1. 3x4K60 is available on SKU 2, refer to Table 3 for further SKU details.
2. Pipelock is the mechanism to synchronize multiple display outputs and the processor supports two monitor synchronization. It is not possible to implement Pipelock using one DDI display output and one TCSS display output.

4.1.2 Embedded Display Port Maximum Resolution

Standard	Resolution Supported
eDP*	All SKUs (except SKU 2): 1920x1080 @ 60Hz SKU 2: 4096x2160 @ 60Hz
Notes: 1. Maximum resolution is based on the implementation of 4 lanes at HBR3 link data rate. 2. bpp - bit per pixel. 3. Resolution support is subject to memory BW availability. 4. High resolution are supported, validation is dependent on panel market availability.	

Table 12. Display Matrix

Maximum of 3 Simultaneous Displays						
	1 Display Only		2 Displays		3 Displays	
	1 Internal	1 External	1 Internal + 1 External	2 External	1 Internal + 2 External	3 External
Internal #1[1]	eDP 1.4b: 1920x1080 @ 60Hz MIPI-DSI: 1920x1080 @ 60Hz **Only SKU 2:** eDP 1.4b: 4096x2304 @ 60Hz MIPI-DSI: 1920x1080 @ 60Hz	N/A	eDP 1.4b: 1920x1080 @ 60Hz MIPI-DSI: 1920x1080 @ 60Hz **Only SKU 2:** eDP 1.4b: 4096x2304 @ 60Hz MIPI-DSI: 1920x1080 @ 60Hz	N/A	eDP 1.4b: 1920x1080 @ 60Hz MIPI-DSI: 1920x1080 @ 60Hz **Only SKU 2:** eDP 1.4b: 4096x2304 @ 60Hz MIPI-DSI: 1920x1080 @ 60Hz	N/A
External #1	N/A	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz
External #2	N/A	N/A	N/A	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz	DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz
External #3	N/A	N/A	N/A	N/A	N/A	DP 1.4a: 1920x1080 @ 60Hz HDMI 2.0b: 1920x1080 @ 60Hz **Only SKU 2:** DP 1.4a: 4096x2304 @ 60hz HDMI 2.0b: 4Kx2K @ 60Hz

Notes:
1. 4K60 and 3x 4K60 external display only supported on SKU 2.
2. Simultaneous displays are configuration dependent
3. Dual eDP/MIPI or eDP+ MIPI configurations are not supported.

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5.0 Graphics

5.1 Graphics SR-IOV

Note:

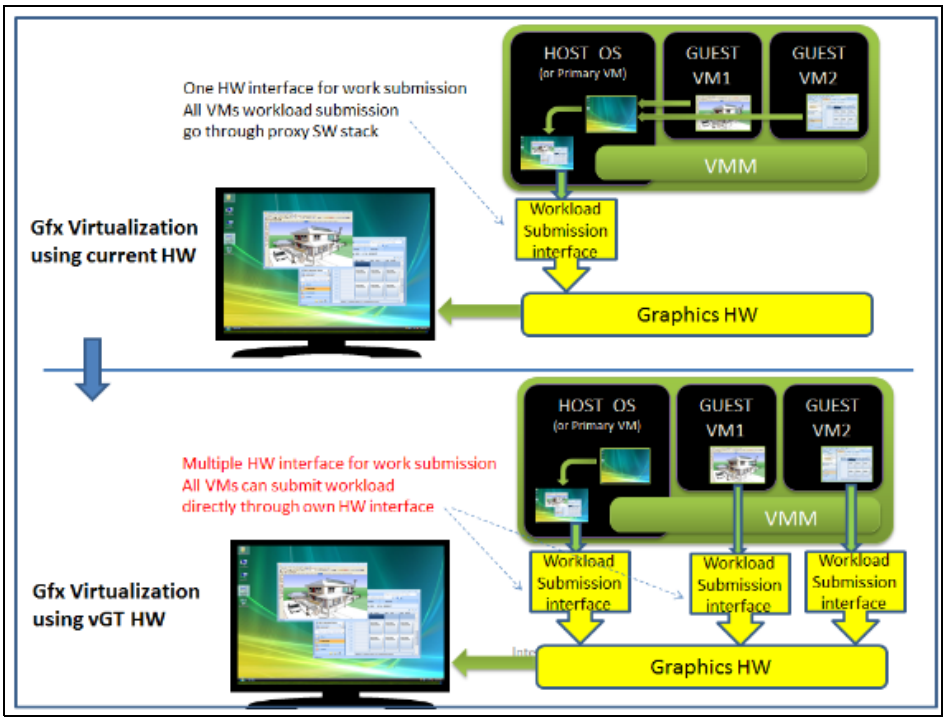
1. For any capability not mentioned in this section, refer to Chapter 22 (Graphics) of Datasheet Volume 1 (RDC# 759603).
2. Intel Atom® x7000C processors do not have any graphics capabilities.

5.1.1 Introduction

Graphics SR-IOV (Single Root Input/Output Virtualization) allows multiple Virtual Machines (VMs) to have access to the processor's GPU (Graphics Processing Unit) Execution Units (EUs) and hardware accelerated video decoders & encoders with better performance and a lower processing overhead compared to previous methods of graphics virtualization.

Rather than sharing hardware access to the GPU between VMs, Graphics SR-IOV allows each VM to have its own direct hardware access. Figure 5 illustrates the differences between Graphics SR-IOV and an example earlier graphics virtualization method.

Figure 5. Differences Between Graphics SR-IOV & Earlier Graphics Visualization Method

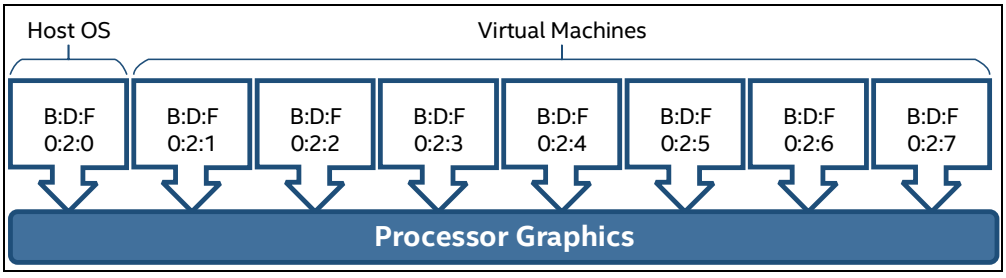


5.2 Processor Capabilities

The processor implements a number of capabilities to support Graphics SR-IOV (Single Root Input/Output Virtualization).

- Up-to seven Virtual Functions (VFs) in PCI configuration space: Bus 0, Device 2, Functions 1:7. Each Virtual Machine (VM) is assigned its own VF

Figure 6. Virtual Functions in PCI Configuration Space



- Resources to submit the graphics workload:
  o Memory (aperture) allowing each VM to submit workload and associated data surfaces;
  o A graphics translation table (GTT) to manage aperture pages;
  o MMIO configuration registers exposed to each VM

- A signalling mechanism to invoke the hardware to execute the workload
- A signalling mechanism for the hardware to convey relevant information by sending interrupts
- A mechanism to display the output produced by the execution of the workload.

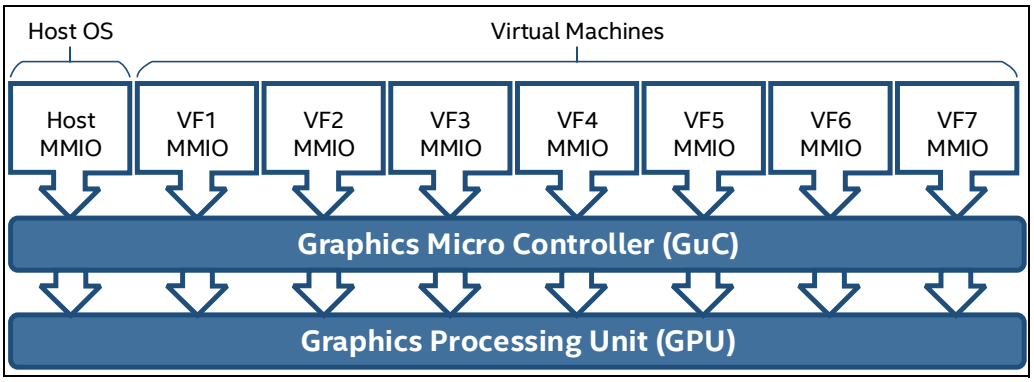
5.3 Graphics Microcontroller (GuC)

The Graphics Micro Controller (GuC) is an embedded micro-controller in the graphics sub-system that is designed to perform graphics workload scheduling on the various Graphics Processing Unit (GPU) Execution Units (EUs). In this scheduling model, software submits work through one of the 256 graphics doorbells, and this triggers the GuC to perform the scheduling operation on the appropriate EU.

Scheduling operations include determining which workload to run next, submitting a workload to a command streamer, pre-empting existing workloads running on an engine, monitoring progress, and notifying host SW when work is done.

The graphics driver in the Host OS and the Virtual Machines communicate with the GuC to offload some operations, such as the scheduling described above.

Figure 7. Virtual Functions and the Graphics Micro Controller (GuC)



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6.0 Flexible High Speed Input/Output (I/O)

6.1 Flexible High Speed Input/Output (HSIO) Introduction

Flexible Input/Output (I/O) is a technology that allows some of the PCH High Speed I/O (HSIO) lanes to be configured for connection to a PCIe* Controller, an eXtensible Host Controller Interface (xHCI) USB 3.2 Controller, an Advanced Host Controller Interface (AHCI) SATA Controller or Gigabit Ethernet (GbE) Controller. Flexible I/O enables customers to optimize the allocation of the PCH HSIO interfaces to better meet the I/O needs of their system.

Note: For any capability not mentioned in this section, refer to Section 1.10 of Datasheet Volume 1 (RDC# 759603).

6.2 Flexible HSIO Lane Multiplexing

Figure 8. Flexible HSIO Lane Multiplexing in the PCH

<table>
<tr><th>Flex HSIO Lane</th><th colspan="5">HSIO Type and Lane</th></tr>
<tr><td>0</td><td>PCIe 1 #1</td><td rowspan="4">X4</td><td rowspan="2">X2</td><td>X1</td><td>USB 3.2 #1</td></tr>
<tr><td>1</td><td>PCIe 1 #2</td><td>X1</td><td>USB 3.2 #2</td></tr>
<tr><td>2</td><td>PCIe 1 #3</td><td rowspan="2">X2</td><td>X1</td><td>USB 3.2 #3</td></tr>
<tr><td>3</td><td>PCIe 1 #4</td><td>X1</td><td>USB 3.2 #4</td></tr>
<tr><td>6</td><td colspan="3">PCIe 2 #7</td><td>X1</td><td>GbE Controller</td></tr>
<tr><td>8</td><td>PCIe 3 #9</td><td rowspan="4">X4</td><td rowspan="2">X2</td><td>X1</td><td rowspan="2"></td></tr>
<tr><td>9</td><td>PCIe 3 #10</td><td>X1</td></tr>
<tr><td>10</td><td>PCIe 3 #11</td><td rowspan="2">X2</td><td>X1</td><td>SATA #0</td></tr>
<tr><td>11</td><td>PCIe 3 #12</td><td>X1</td><td>SATA #1</td></tr>
</table>

The 9 Flexible HSIO Lanes [11:8,6,3:0] supports the following configurations:

- Up to 9 PCIe* Lanes
- A maximum of 5 PCIe* Root Ports (or devices) can be enabled.
- PCIe* Lanes 1-4 (PCIe* Controller #1), 7 (PCIe* Controller #2), and 9-12 (PCIe* Controller #3) must be individually configured.
- Up to 1 Gigabit Ethernet (GbE) SGMII port.

Note: The SGMII interface and GbE controller are only supported on the Intel Atom® x7000 processor series.

Note: Universal Flash Storage (UFS) is not supported for Edge Applications.

6.2.1 Flexible I/O Lane Selection

HSIO lane configuration and type is statically selected by soft straps.

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7.0 Gigabit Ethernet Controller and Time-Sensitive Networking

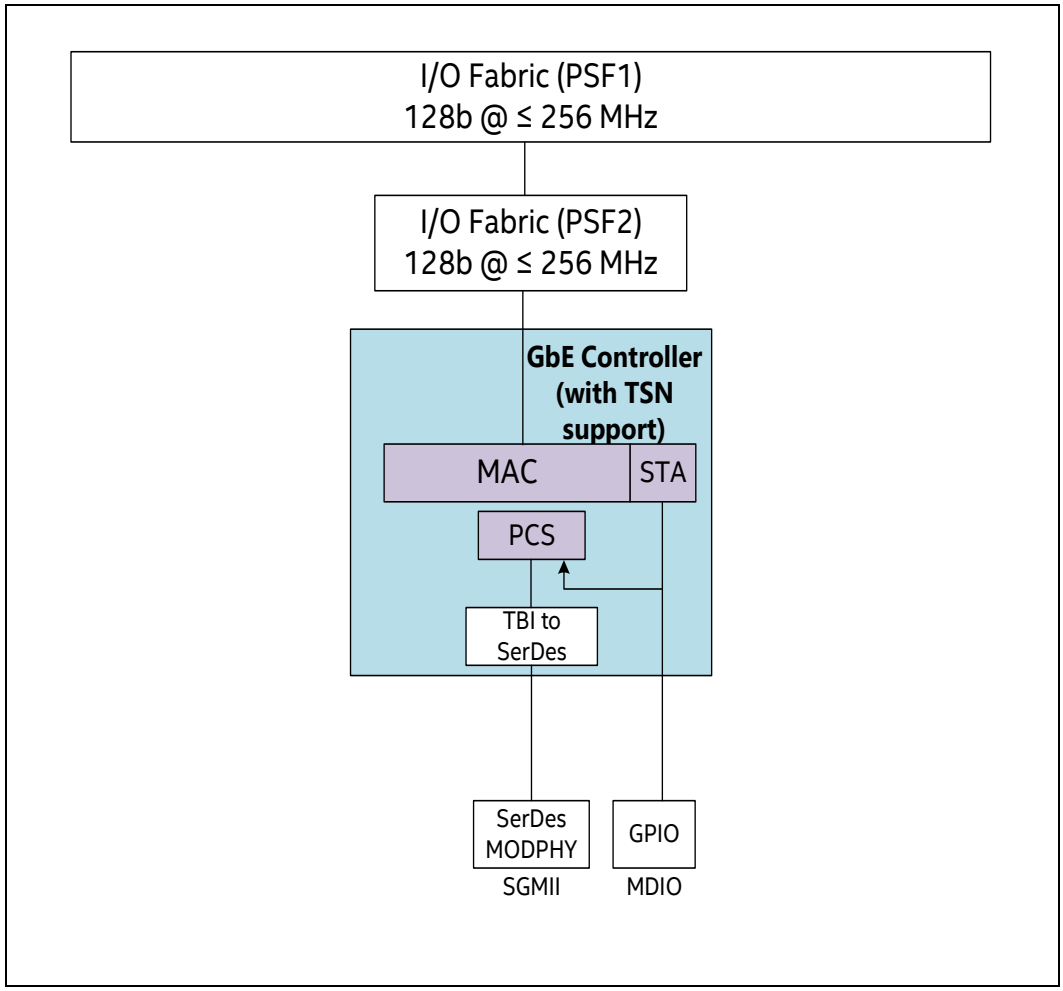
7.1 Overview

This section describes the behavior of the one integrated Gigabit Ethernet (GbE) controller with Time-Sensitive Networking (TSN) support that reside in PCH. The GbE controller can operate at multiple speeds, 10/100/1000 & 2500 Mbps Serial Gigabit Media-Independent Interface (SGMII) and in either full duplex or half duplex mode. The integrated GbE Media Access Controller (MAC) has a unique 48-bit MAC Address. This MAC Address is located in a BIOS Sub-Region and is assigned by the customer using the Capsule Update method which runs in an OS.

Note: The GbE controller is only supported on the Intel Atom® x7000 processor series.

Figure 9 shows the GbE Controller Placement in the PCH.

Figure 9. GbE Controller Placement



The GbE controller is accessed by the IA Processor cores through system software via PCH IO Fabric (PSF2 and PSF1) and supports a SGMII interface.

The MAC has an IEEE Std 802.3 Station Management (STA) Entity that is accessible to software via the Memory Mapped IO (MMIO) registers to control the associated MDIO interface. See IEEE Std 802.3, Clause 22 and Clause 45 for MMIO registers. The Physical Coding Sublayer (PCS) module provides the sublayer circuitry between the GMII of the MAC and the Ten Bit Interface (TBI) of the SGMII Serializer/Deserializer (SerDes) circuitry. See IEEE Std 802.3 Clause 35 for GMII and Clause 36 for TBI.

7.2 Features Description

The GbE controller features listed in this section.

7.2.1 Ethernet Features Description

The GbE controller instances supports the following Ethernet features:

- 10Mbps/100Mbps/1Gbps/2.5Gbps SGMII mode through SerDes interface.

Note: Auto-negotiation between 10Mbps/100Mbps/1Gbps and 2.5Gbps is not supported natively by the controller.

Note: The maximum line rate for 2.5Gbps is expected to be less than 2.0Gbps for standard (1518 bytes) Ethernet frames and less than 2.3Gbps for Jumbo (9018 byte) Ethernet frames.

- MDIO (station management) interface.
- Software soft reset is used for PHY initialization. Hardware PHY reset is not supported.
- 4 TX queues and 6 RX queues with separate DMA channels and interrupts. Each TX/RX queue is 4kB for storing at least two normal packets with total of 40kB memory (TX+RX). Each queue size is programmable with TX queue size not to exceed 16kB and RX queue size not to exceed 24kB.

Note: The MTL Receive FIFO Size (RXFIFOSIZE) bits [4:0] in register MAC_HW_FEATURE1 (MMIO offset 120h) advertises 32kB as the allowable RX FIFO size, while the implemented size is 24kB. If software allocation of RX queues exceeds this amount, then data attempted to be queued greater than 24kB will be lost. Software should not allocate an aggregate size of more than 24kB for MTL RX queues.

- Supports normal (1518/1522 bytes) and jumbo (9018 bytes) packets:
  - On the receiving side, supports both cut-through and store and forward modes.
  - On the transmitting side, supports only store and forward mode.

Note: Jumbo packet support can be dependent on PHY compatibility and, if jumbo packet platform support is required, Intel recommends confirming support with the PHY vendor

- Support for TCP/IP Offloading:
  - Checksum Offload Engine (COE) that does Checksum insertion (on TX path) and detection (on RX path) for TCP/UDP/ICMP segments encapsulated in IPv4/ IPv6 datagrams.
  - TCP Segmentation Offload (TSO) Engine where large TCP packets are split into multiple small packets to save application bus cycles. 4 TX DMA Channels with separate 1kB memory (256 bytes per channel).
- Double VLAN support:
  - Insertion, replacement, or deletion of up to four VLAN tags on TX path
  - Packet filtering (layer-2) and stripping based on any one of four VLAN tags on RX path
- MAC Management Counters (MMC) for gathering statistics on the received and transmitted packets. Interrupts are generated for various events.
  - On TX: Jabber Timeout, No Carrier or Loss of Carrier, Late Collision, Packet Underflow, Excessive Deferral and Excessive Collision
  - On RX: CRC error, Runt packet (shorter than 64 bytes), Alignment error (in 10/100Mbps only), Length error (non-Type packet only), Out of Range (non-Type packet only, longer than 1518 bytes), GMII_RXER Input error
- Low power management
  - IEEE Std 802.3az-2010 Energy Efficient Ethernet (EEE) with automatic entry/exit when link is Idle – Low Power Idle mode. Both link TX/RX clocks can be clock gated.
- RX Filtering
  - 64 Address (SA/DA) based layer-2 perfect and Hash table filtering
  - 4 VLAN tag layer-2 filters
  - Two Layer-3 and Layer-4 frame filters

- Functional Level Reset (FLR)
- FSM protection
  - 1–3 bits errors in the data and address
- Timeout on certain interfaces
  - Control and Status Register (CSR) Interfaces, MDIO Interfaces, AXI Primary Interfaces, and AXI Secondary

Note: The Split Headers (SPH) function is not supported by the processor. Platform firmware & software shall not set any DMA_CH[0:7]_CONTROL.SPH register field to 0x1.

- Wake on LAN (WoL) is not supported natively by the controller.

7.2.2 TSN Features Description

TSN is a set of IEEE standards that are intended to ensure quality transmission of the time sensitive data over Ethernet networks. TSN standards are governed by an IEEE Std 802.1 task group driven by, in part, Avnu Alliance which is a consortium of organizations involved and invested in deterministic Ethernet Technology.

Table 13. TSN IEEE Standards

IEEE Standard	Description
IEEE Std 1588™-2008 v2	Precision Clock Synchronization Protocol for Networked Measurement and Control Systems
IEEE Std 802.1AS	A specific profile of IEEE Std 1588-2008. IEEE Std 802.1AS specifies the generalized Precision Time Protocol (gPTP). It provides a Layer 2 time synchronizing service
IEEE Std 802.1Qav 2009	Forwarding and Queueing Enhancements for Time-Sensitive Streams, which specifies the Credit Based Shaper
IEEE Std 802.1Qbu 2016	Frame Preemption. It allows a Bridge Port to suspend the transmission of non time critical frames while one or more time critical frames are transmitted
IEEE Std 802.3br 2015	Interspersed Express Traffic (IET)
IEEE Std 802.1Qbv 2015	Enhancements for Scheduled Traffic. It specifies time aware queue draining to schedule the transmission of frames relative to a known time scale

In addition to IEEE Standards above, the GbE controller instances supports the following TSN features.

- Time Based Scheduling (TBS)
  - Time deterministic transmission of the packet according to per packet transmit time specified by users.
- IEEE Std 1588™-2002/2008 timestamp support for PTP packets
  - 80-bit internal system timer that runs at 200MHz for high-precision one-step time stamping
  - 64-bit ART timer that runs at 19.2MHz with Time Synchronization support for local and system timer correlation
  - The ART timer and system timer values are captured with precision less than 5ns for timing correlation
- GPIO Auxiliary Timestamp Trigger input (IEEE Std 802.1AS)
- GPIO based Pulse Per Second output with programmable pulse width
- Each Control List of 1K entries for all Tx queues. 32x128(x8) memory for Control List to support IEEE Std 802.1Qbv

- Provision to route traffic on low latency on low fabric channel with traffic class-based routing. Two virtual channels and traffic classes (TC) are supported. All express traffic is mapped to Virtual Channel-1 (VC1) and best effort is mapped to Virtual Channel-0 (VC0). Each queue is independently mapped to any of the supported VC/TC.

Note: Concurrent usage of the 802.1Qav and 802.1Qbv features is not supported.

7.3 GbE Time-Stamping Logic

The Precision Time Protocol (PTP) over Ethernet is described in the IEEE Std 1588-2002 and 2008 versions. The subsystem provides the following features:

- IEEE Std 1588-2002 and 2008 formats
- Provides an option to take time snapshots of all packets or only PTP type packets
- Provides an option to take time snapshots of only event messages
- Provides an option to take the time snapshot based on the clock type: ordinary; boundary; end-to-end transparent; peer-to-peer transparent
- Provides an option to select the node to be a primary clock or secondary clock for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in the packets sent directly over Ethernet and sends the status
- Provides an option to measure sub-second time in digital or binary format
- Two time stamp sources, as follows:
  a. External timestamp
  b. Internal timestamp which is selected by software

7.4 GbE Cross-Timestamp Logic

Additional logic is included in the GbE design to provide time synchronization between the 64-bit timer Always Running Timer (ART) and the 80-bit system timer in the GbE controller.

When system software sets the cross-timestamp enable bit in the GbE ART MDIO register, it captures simultaneous snapshots of the values of the GbE system timer and the ART. System software can then read the captured time values to establish a relationship between ART and GbE system timer; When the GbE system timer value is X, the ART value is Y.

7.5 External Interfaces

The selection for the GbE controller is Serial Gigabit Media-Independent Interface (SGMII).

The PCH does not use any of the Precision Time Protocol (PTP) capture capabilities that may exist in the external PHY component. All the PTP events and timestamps are triggered in the MAC portion of the subsystem.

7.5.1 Serial Gigabit Media-Independent Interface (SGMII)

Serial Gigabit Media-Independent Interface (SGMII) is a de-facto industry standards for achieving Ethernet LAN speeds of 10Mbps, 100Mbps, 1Gbps and 2.5Gbps. It consists of two sets of Current-Mode Logic (CML) differential signal using one of the multiplexed PCH ModPHY lanes. The design embeds the SGMII transmit clock in the transmit data and expects the SGMII receive clock to be embedded in the receive data. This eliminates four of the standard GMII interface pins. For the controller's IEEE Std 802.3 Physical Sublayer configuration and management, it also provides two

CMOS Management Data Input/Output (MDIO) interface signals. SGMII provides a reduced-pin implementation of GMII (IEEE Std 802.3, Clause 35) which would require 25 single-ended signals plus the two MDIO interface signals.

7.5.2 Management Data Input/Output (MDIO)

The External PHY can be accessed and configured through Management Data Input/Output (MDIO) from the GbE controller by SW/HW/BIOS. The IEEE Std 802.3 defines MDIO Management interface which serves to access the Management registers of IEEE Std 802.3 complaint devices. This is a two-line interface including MDC (clock) and MDIO (bidirectional data).

Note: The interface supports MDIO operation as defined in IEEE Std 802.3 Clause 45 except at a signal voltage of 1.8V, not 1.2V.

7.6 Signal Description

7.6.1 SGMII Signals

Table 14. SGMII GbE LAN Signals

Pin	Signal Name[1]	Type (Voltage Domain)	Direction	Description
CG11	PCIE7_TXP / **GBE_SGMII_TXP**	CML differential signal (1.05V)	Output	Transmit P&N of the serial differential output
CG12	PCIE7_TXN / **GBE_SGMII_TXN**			
CK5	PCIE7_RXP / **GBE_SGMII_RXP**	CML differential signal (1.05V)	Input	Receive P&N of the serial differential input
CK6	PCIE7_RXN / **GBE_SGMII_RXN**			

Note:
1. Refer to Section 6.0 for a description of how these signals are routed by the ModPHY lanes.

7.6.2 MDIO Signals

Table 15. MDIO Signals

Pin	Signal Name	GPIO Type (Voltage Domain)[1]	Direction	Description
DA24	GPP_F17 / **GBE_MDC** / THC1_SPI2_RST#	CMOS (1.8V)	Output	Management Data Clock This clock signal is driven by the GbE controller to clock the serial MDIO data. The clock period is programmable.
DB28	GPP_F18 / **GBE_MDIO** / THC1_SPI2_INT#	Open Drain (1.8V)	Input/Output	Management Data Input Output This signal is driven by either the GbE controller or the external PHY/Switch component during the MDIO transaction.

Note:
1. The signals should be configured to 1.8V using the multiplexed GPIO's Individual Voltage Select soft strap.

7.6.3 Miscellaneous Signals

Table 16. Miscellaneous Signals

Pin	Signal Name	GPIO Type (Voltage Domain)	Direction	Description
CV59	GPP_S1 / SNDW0_DATA / **GBE_INT** / I2S1_SFRM	CMOS (1.8V)	Input	Interrupt This input signal is driven by the external SGMII PHY device.
CV56	GPP_S0 / SNDW0_CLK / **GBE_AUXTS** / I2S1_SCLK	CMOS (1.8V)	Input	Auxiliary Time Stamp Trigger This edge-sensitive input signal triggers the storing of the time stamp into a 4x64 deep FIFO on its rising edge. Note: This signal may also be called External Time Stamp Trigger (EXTTS) in other platform documentation.
CW56	GPP_S3 / SNDW1_DATA / DMIC_DATA_0 / **GBE_PPS** / I2S1_RXD	CMOS (1.8V)	Output	Pulse-Per-Second This output signal is generated as a pulse by the LAN controller each time its system timer indicates a new “seconds” value.

7.7 GbE Interrupts and Message Signaled Interrupt

The GbE subsystem has the following 13 interrupts. These interrupts are routed through the Message Signaled Interrupt (MSI). The MSI has separate Vector Number. The GbE interrupts and MSI Vector Number are tabulated in Table 17.

Table 17. GbE interrupts and Message Signaled Interrupt (MSI) Vector Number

No	Interrupt Name	Direction	Description	MSI Vector No
1	Queue_TX0_IRQ	O	Per channel Transmit signal to host system	5'b00001
2	Queue_TX1_IRQ	O		5'b00011
3	Queue_TX2_IRQ	O		5'b00101
4	Queue_TX3_IRQ	O		5'b00111
5	Queue_RX0_IRQ	O	Per channel Receive signal to host system	5'b00000
6	Queue_RX1_IRQ	O		5'b00010
7	Queue_RX2_IRQ	O		5'b00100
8	Queue_RX3_IRQ	O		5'b00110
9	Queue_RX4_IRQ	O		5'b01000
10	Queue_RX5_IRQ	O		5'b01010
11	Low Power Idle (LPI) Interrupt	O	LPI RX exit interrupt output. This signal is high when the MAC receiver exits the LPI state. This is used for EEE and CSR clocks can be gated.	5'b11100
12	MAC_IRQ	O	Interrupt signal to the host system – generated by the MAC	5'b11101
13	PCS Interrupt	O	Interrupt signal to the host system – generated by the PCS	5'b11110

7.8 Supported System Configurations

Table 18 lists all the supported configurations, operating mode, and link partners for the GbE controller. Selecting the desired PHY and system configuration is determined at power on through the use of soft strap and register configuration.

Table 18. Supported System Configurations

Connection	Speed	Electrical Interface	Third Party PHYs[1]
10BASE-T 100BASE-TX 1000BASE-T	10 Mb/s 100 Mb/s 1 Gb/s	SGMII	Marvell* 88E1512 MaxLinear* GPY115 TI* DP83867
10BASE-T 100BASE-TX 1000BASE-T 2.5GBASE-T	10 Mb/s 100 Mb/s 1 Gb/s 2.5 Gb/s	SGMII	Marvell* 88E2110 MaxLinear* GPY211 MaxLinear* GPY215

Note:
1. Intel strongly recommends that only the PHYs listed be used in platform designs. Firmware and software incompatibilities may occur between other GbE PHYs and Intel's BKC due to per-vendor or per-model PHY-specific programming requirements.

7.9 Registers

Refer to Chapter 21.0 for a description of the registers associated with this section.

7.10 References

Specification	Location
IEEE Std 802.3-2015 Standard for Ethernet	https://standards.ieee.org/standard/802_3-2015.html
IEEE Std 802.1 AS-2011 Standard for Timing and Synchronization for Time-Sensitive Applications	https://standards.ieee.org/standard/802_1AS-2011.html
IEEE Std 1588 2008 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems	https://standards.ieee.org/standard/1588-2008.html
IEEE Std 802.1Qav 2009 Standard for Forwarding and Queuing Enhancements for Time-Sensitive Streams	https://standards.ieee.org/standard/802_1Qav-2009.html
IEEE Std 802.1Qbu 2016 Standard for Frame Preemption	https://standards.ieee.org/standard/802_1Qbu-2016.html
IEEE Std 802.3br 2016 Standard for Specification and Management Parameters for Interspersing Express Traffic	https://standards.ieee.org/standard/802_3br-2016.html
IEEE Std 802.1Qbv 2015 Standard for Enhancements for Scheduled Traffic	https://standards.ieee.org/standard/802_1Qbv-2015.html
IEEE Std 802.3az 2010 Standard for Media Access Control Parameters, Physical Layers, and Management Parameters for Energy-Efficient Ethernet	https://standards.ieee.org/standard/802_3az-2010.html

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8.0 USB-C* Sub System (TCSS)

USB-C* is a cable and connector specification defined by USB-IF. The USB-C sub-system supports USB3, DPoC (DisplayPort over Type-C) protocols. The USB-C sub-system can also be configured as native DisplayPort or HDMI interfaces. USB-C solution brand requires USB2, USB3 (10 Gbps), USB3/DP implemented at the connector.

8.1 General Capabilities

Note: For any capability not mentioned in this section, refer to Section 17.1 of Datasheet Volume 1 of 2 (RDC# 759603).

- USB Type-A is supported on the processor side
- USB Type-Micro AB is supported on the processor side.
- Intel Atom® x7000C processors do not support DPoC, DisplayPort, or HDMI

Table 19. USB-C* Port Configuration

	Port	Supported Features
Group A	TCP 0	USB 3.2[3] DisplayPort[1] HDMI[2]
	TCP 1	

Notes:
1. Supported on Type-C or Native connector.
2. Supported only on Native connector.
3. USB 3.2 supported link rates:
   - USB 3.2 Gen 1x1 (5 Gbps)
   - USB 3.2 Gen 2x1 (10 Gbps)
4. USB 2 interface supported over Type-C connector, sourced from PCH.
5. USB Type-A & Type Micro AB connectors are supported.
6. Display interface can be connected directly to a DP/HDMI/Type-C port.

Table 20. USB-C* Lanes Configuration

Lane 1	Lane 2	Comments
USB3	No Connect	Any combination of • USB3.2 Gen 1x1 (5 Gbps) • USB3.2 Gen 2x1 (10 Gbps)[1]
No Connect	USB3	

Lane 1	Lane 2	Comments
USB3	DPx2	Any of HBR2/HBR1/RBR for DP and USB3.2 (5 Gbps)
DPx2	USB3	Any of HBR3/HBR2/HBR1/RBR for DP and USB3.2 (10 Gbps) [1]
USB3		Both lanes at the same DP rate - no support for 2x DPx2 USB-C connector
Note: 1. Not supported for Communication & Industrial Use Conditions		

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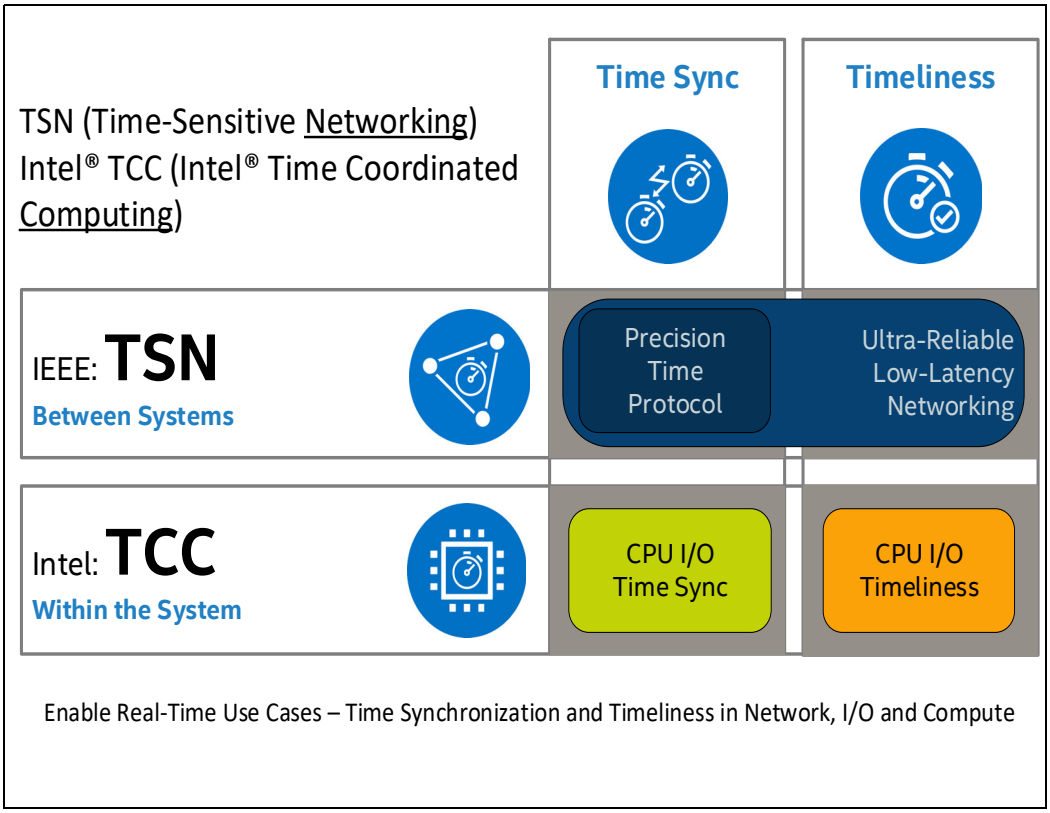
9.0 Intel® Time Coordinated Computing

9.1 Introduction

Intel® Time Coordinated Computing (Intel® TCC) is ushering in a new era of coordination of computation scheduling to reduce jitter and improve performance of time-sensitive applications. Intel® TCC is not an IP block but a set of capabilities available across multiple IP blocks of the processor. Intel® TCC enhances performance along two vectors: Time Synchronization and Timeliness. Timeliness is traditionally referred to as "Real-Time" systems that are focused on the optimization. Time Synchronization provides a hardware mechanism to precisely determine how various IP specific clocks are related. Real-Time provides a hardware mechanism to minimize the latency of data packets from one IP block to another IP block. This section describes the key features and requirements that compose Intel® TCC, split into the respective performance vectors. For each feature, the motivation, description, software interface (if any), hardware dependencies (if any) and formal requirements are listed.

Figure 10. Intel® TCC Features within System and TSN between Systems



9.2 Intel® Time Coordinated Computing Features

Intel® TCC helps real-time applications meet performance metrics, such as worst-case execution time (WCET). In addition, it keeps all software and hardware time-synchronized. Intel® TCC performance is measured by the temporal determinism afforded to the critical tasks. The following section outlines the platform capabilities that enable temporal determinism.

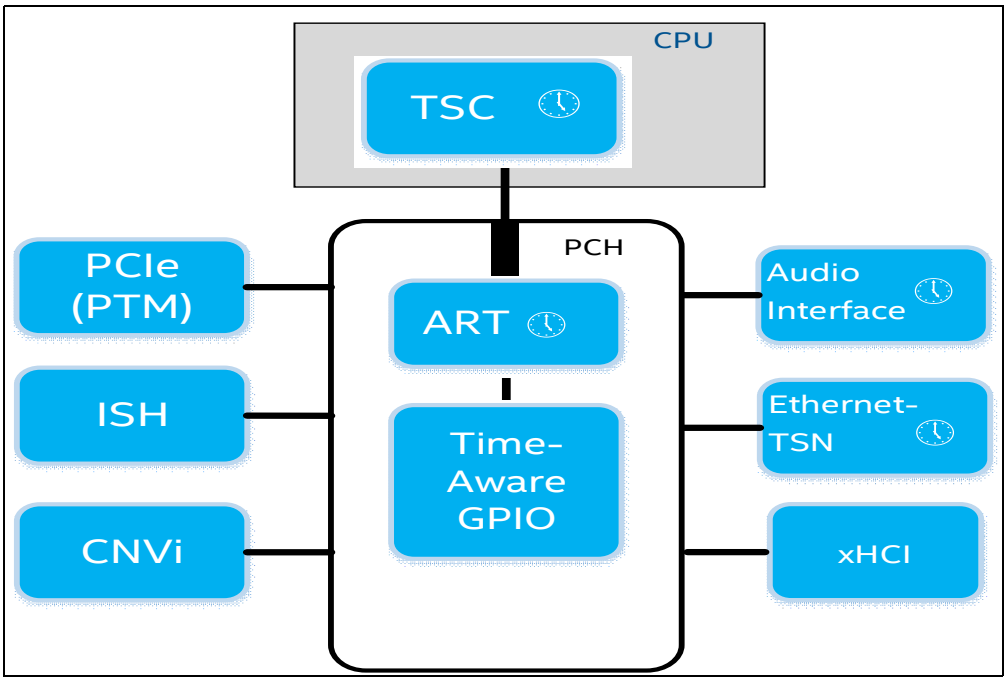
9.2.1 Time-Synchronization Support Features

The processor provides a common timekeeping framework, based on the Always Running Timer (ART) defined in Intel® 64 and IA-32 Architectures Software Developer's Manual. ART runs at the core crystal clock frequency. The ART clock is at 38.4MHz. This makes it possible for software to calculate the precise time relationship between numerous subsystems, including the CPU's timestamp counter (TSC), the network device, Time-Aware GPIOs, and other various IPs. This processor support makes deep sub-microsecond time-correlation / synchronization possible, which is a requirement of coordinated computing, sensing, and actuation.

Processor Time-Synchronization Support provides the following:

- Global time reference based on Always Running Timer (ART)
- IEEE Std 802.1AS, the TSN standard for time synchronization across wired Ethernet network
- Global time synchronization for the following local time bases with respect to ART:
  - Ethernet Time-Sensitive Networking (TSN)
  - High Definition Audio
  - PCI Express Root-ports Precision Time Measurement (PCIe* PTM)
  - Integrated Sensor Hub (ISH)
  - Time-Aware GPIO
  - Intel® Integrated Connectivity (CNVi)
  - xHCI Controllers

Figure 11. Platform Time-Synchronization Support



9.2.1.1 CPU Time Stamp Counter to I/O Time-Synchronization Support

The CPU Time Stamp Counter (TSC) Root in the Power Management Controller (PMC) is the global referenced time in the Time Synchronization architecture. The software can access the CPU TSC through the Read Time Stamp Counter (RDTSC) assembly instruction. RDTSC is based on the ART counter, which is the root of time in the system. The CPU TSC is derived from ART. ART is discoverable in the CPUID leaf 15H, and the ART relationship to all other clock domains is maintained in software.

The relation between the network device timestamp clock and ART (also TSC) is determined using cross-timestamp hardware. Using TSN the ART clock is extended outside of the platform. The relation between Audio hardware clock and ART (also TSC) is determined using crosstimestamp hardware. The Time-Aware GPIO interface logic is driven by ART. Edge events (one shot and pulse train) can be sampled or driven with respect to the ART clock.

9.2.1.2 Off-Chip Time-Synchronization Support via PCIe* PTM

Besides supporting known hardware, ART also extends to PCIe peripherals using Precision Time Measurement (PTM). PTM provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

9.2.1.3 IEEE Std 802.1AS Network Time-Synchronization Support

The IEEE Std 802.1AS TSN standard extends time synchronization across multiple platforms for time-sensitive applications such as audio and video when these platforms are Ethernet connected. The integrated Ethernet MAC supports the IEEE Std 802.1AS generalized Precision Time Protocol (gPTP) event messages for network path delay measurement between two time-aware systems.

Time Synchronization utilizes the standard IEEE Std 802.1AS capability as the base feature to enable cross-platform time synchronization. At the high level, the IEEE Std 802.1AS implements the following:

- Select the best clock source on the network using the algorithm specified in IEEE Standard 802.1AS.
- Determine the propagation delay through the network.
- Calculate the offset between the selected clock source and the local clock The IEEE Std 802.1AS timer runs on its Local Time base. It supports a 38.4MHz crystal oscillator clock determined by a pin-strap based on platform configurations where it does not require any PLL to be running. The crystal oscillator continues running when Std IEEE Std 802.1AS time synchronization is enabled such that a valid time stamp is always available when gPTP event messages are transmitted or received.

9.2.1.4 Audio Cross-Timestamp

For Time Synchronization, the audio software stack handles the scheduled audio cross-timestamp such that an audio stream plays in-sync with multiple audio/video components in a network distributed system. Using audio hardware-assisted time synchronization, software can determine the relation between the best clock source and the local audio clock by determining the appropriate start time across the network on the network using the algorithm specified in IEEE Standard 802.1AS. Any error is corrected using audio sample rate conversion by performing linear regression approximation to calculate variance. Software may utilize other information available to achieve the best audio cross-timestamp accuracy. Before the scheduled start of the stream is carried out, software is expected to trigger a time synchronization request such that offset tracking between the Local Time base and the ART is intact and does not roll over.

9.2.1.5 Time-Aware GPIO

The PCH has two Time-Aware GPIO (TGPIO) controllers. Each controller can be independently configured to generate or capture timestamped events. TGPIO events are timestamped using the Always Running Timer (ART) clock.

Refer to Section 27.1.7 (Datasheet Volume 1 of 2 RDC# 759603) for detailed information on TGPIO.

9.2.2 Real-Time Features for I/O

The processor provides hardware mechanisms to improve the worst-case, which aims to put an upper bound on the latency for data coming into the system. The following features are required to provide a bounded latency for incoming transactions.

9.2.2.1 Upstream Virtual Channels

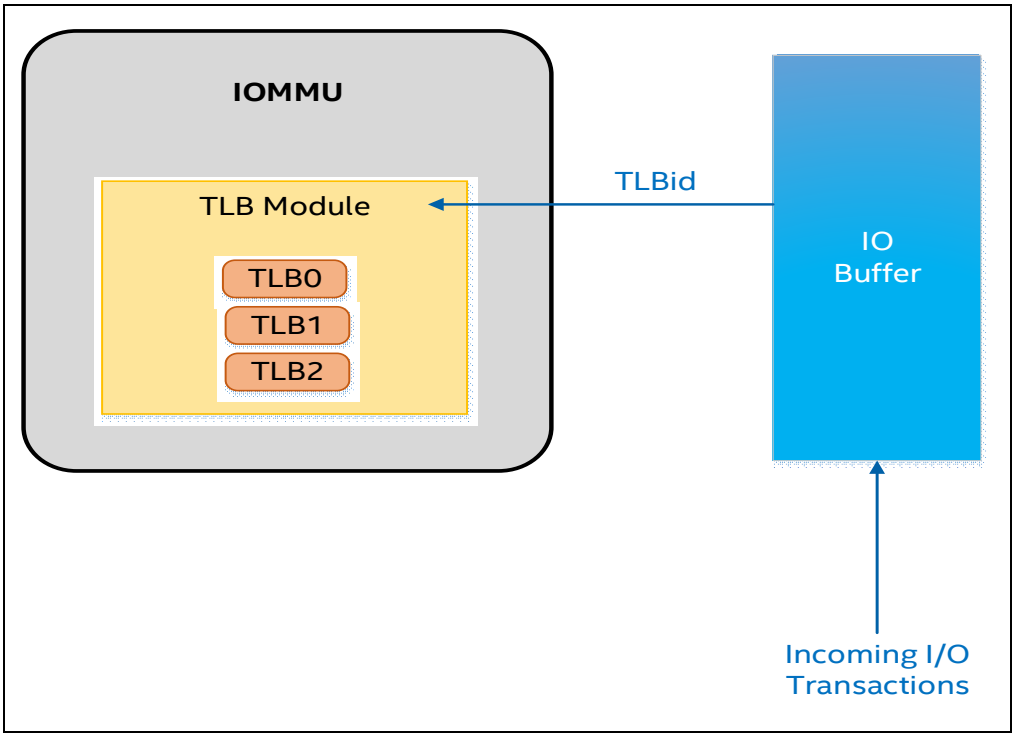
The processor provides support for upstream virtual channels through the processor fabric. I/O devices are expected to make use of the PCIe base specification definition around quality of service mechanisms for data movement, specifically those related to Traffic Class. Upstream transactions that are differentiated by Traffic Class have the ability to be mapped to a separate virtual channel in an attempt to provide a low latency path to the coherent domain. Only 1 virtual channel is supported on the PCH.

9.2.2.2 Dedicated IOTLB

The processor provides support for a dedicated I/O Translation Lookaside Buffer (IOTLB) to cache critical address translations for real-time I/O traffic. When workload consolidation is implemented with virtualization, the I/O transactions of real-time workloads running in a virtual machine are

subject to increased jitter as a result of a page walk by the I/O Memory Management Unit (IOMMU). To avoid additional page walk latency on all I/O transactions, an IOTLB is implemented in the IOMMU to cache the guest physical address to host physical address translation. There are no Quality of Service (QoS) mechanisms available on this cache, and therefore translations for time-critical addresses are subject to eviction as a result of concurrent best effort traffic.

Figure 12. IOTLB Usage



By providing a dedicated IOTLB for time-critical transactions, it is possible to minimize the additional latency and jitter previously introduced by the IOMMU. The processor specifies a TLBid based on the PCIe traffic class used, avoiding contention on the cache resources from concurrent best effort traffic.

9.2.3 Real-Time Features for Processor

The processor provides mechanisms to promote the reduction of execution jitter, leading to a more deterministic computing environment.

9.2.3.1 Multiple Outstanding MMIO

The processor provides support for tracking multiple downstream non-posted transactions simultaneously targeting the Memory Mapped I/O subsystem.

9.2.3.2 Alignment Check Exception on Split Lock

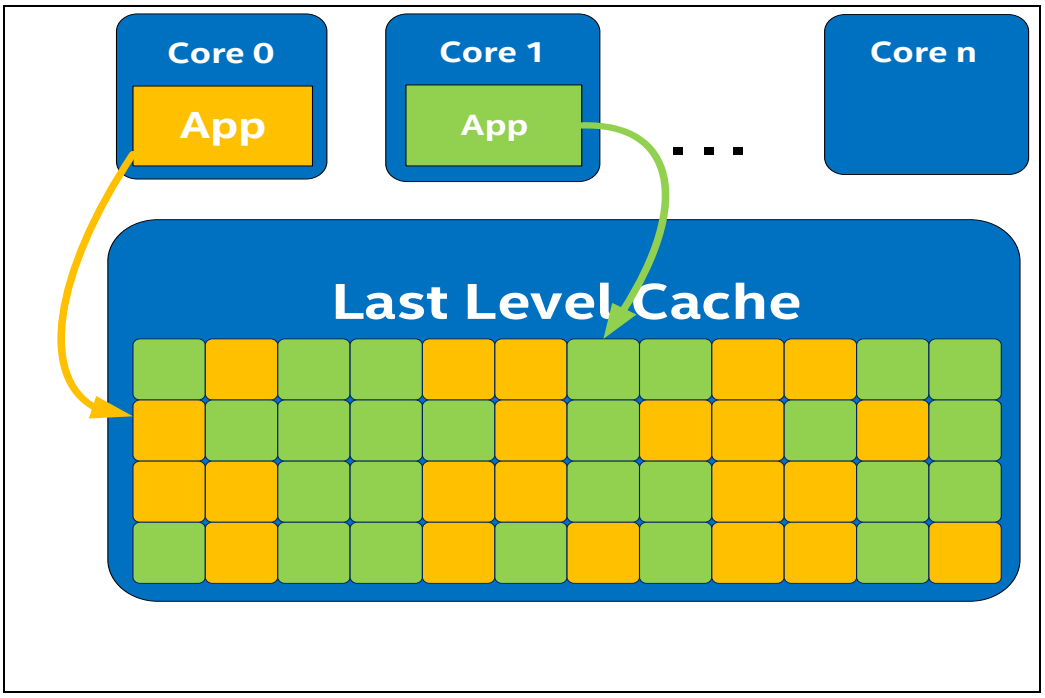
The processor provides support to generate an Alignment Check Exception (#AC) when an application attempts to issue a split lock. When the LOCK prefix is used on an unaligned operand, there is the potential for the operand to span multiple cache lines. In the case where an atomic operation is necessary across two cache lines, a bus lock is executed. A bus lock stops all cores

and I/Os from initiating transactions, resulting in an increase in latency. This increased latency can be significant, and many real-time applications cannot tolerate the jitter that a split lock introduces.

9.2.3.3 L2 and L3 Cache QoS

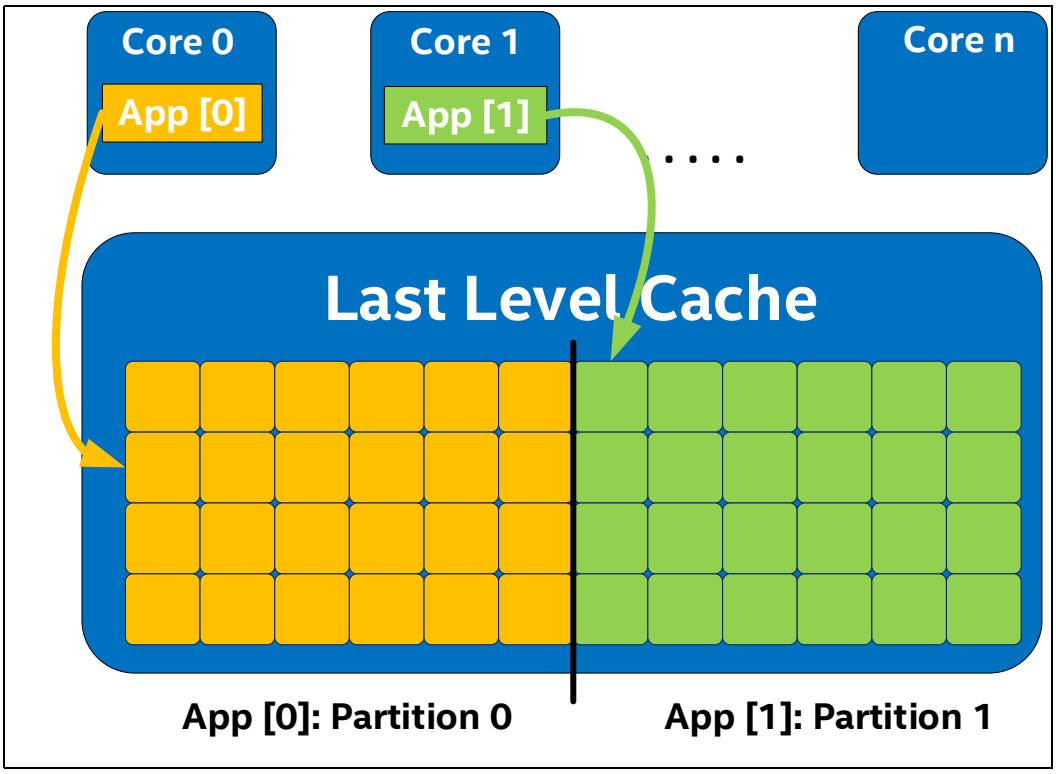
The processor provides support for Cache Allocation Technology (CAT), a Quality of Service (QoS) feature under the Intel® Resource Director Technology (Intel® RDT) portfolio. A model specific, non-architectural version of L3 CAT is supported. Support for this feature will not be enumerated via CPUID leafs as indicated in the Intel Software Developers Manual. CAT helps address shared cache resource contention by providing software control of where data is allocated into the Level 2 (L2) cache and L3 cache, enabling isolation and prioritization of key applications. Without CAT, cache resources are shared between applications.

Figure 13. LLC without Cache QoS



With CAT, cache resources can be partitioned. This partitioning leads to improved performance determinism.

Figure 14. LLC with Cache QoS



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10.0 Processor and PCH Device IDs

10.1 Processor Device IDs

Table 21. Host Device ID (DID0)

Platform	Device ID
0+8 (SKUs 11 & 14)	4675h
0+8 (SKUs 19)	4646h
0+4 (SKUs 18)	4652h
0+4 (SKUs 10 & 13)	4674h
0+4 (SKU 2)	4678h
0+4 (SKU 6)	4679h
0+2 (SKU 1)	4614h
0+2 (SKU 9)	4632h
0+2 (SKUs 8 & 12)	4673h
0+2 (SKU 7)	4677h
0+2 (SKU 5)	467Ch

Table 22. Processor Graphics Device ID (DID2)

Platform	Processor Step	GT SKU	Device ID
0+8, 0+4	N0	32EU	46D0h
0+4	N0	24EU	46D1h
0+2	N0	16EU	46D2h

10.2 PCH Device and Revision IDs

Table 23. PCH Device and Revision IDs

PCH Dev ID	Device Function - Device Description
5481 (SKUs 1,2) 5489 (SKUs 5 -7) 548A (SKUs 8-14) 548C (SKUs 18,19)	**D31: F0** - Enhanced Serial Peripheral Interface (eSPI) Controller
54AC (SKUs 5-14, 18, 19)	**D30:F4** - GbE Controller

Note: For any device not mentioned in this section, refer to Section 2 of Datasheet Volume 1 of 2 (RDC# 759603).

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11.0 Electrical Specifications

11.1 DC Power Rail Specifications

Table 24. VCCCORE Supply DC Voltage and Current Specifications

Symbol	Parameter	SKU	Min	Typical	Max[2]	Unit
Operating voltage	Active voltage Range for VCCCORE	All SKUs	0	-	1.6	V
IccMAX_CORE	Max. Current for Processor VCCCORE Rail	SKUs 2,6, 13	-	-	37	A
		SKUs 1,5, 7-9, 12	-	-	27	A
		SKU 10, 18	-	-	32	A
		SKUs 11, 14, 19	-	-	53	A
IccTDC_CORE (When iRMS enable)	Thermal Design Current (TDC) for Processor VCCCORE Rail	SKUs 11, 14, 19	-	-	22	A
		SKUs 1,2, 5-10, 12, 13, 18	-	-	12	A
IccTDC_CORE (When iRMS disable/ iPL2)	Max. Current for Processor VCCCORE Rail during a PL2 event	SKUs 11, 14, 19	-	-	34	A
		SKUs 1,5,7-9,12	-	-	20	A
		SKUs 2,6, 10, 13, 18	-	-	26	A
TOB_CORE	VCCCORE Tolerance	PS0,PS1	-	±20	-	mV
		PS2,PS3	-	±20	-	mV
Ripple	Ripple Tolerance	PS0	-35	-	+50	mV
		PS1	-35	-	+50	mV
		PS2	-35	-	+50	mV
		PS3	-35	-	+50	mV
di/dt	IccMax Slew rate for transient measurement	SKUs 2 & 6	-	348	-	A/µs
		SKUs 11, 14, 19	-	499	-	A/µs
		SKUs 1,5, 7-9, 12	-	171	-	A/µs
		SKU 10, 18	-	243	-	A/µs
		SKU 13	-	281	-	A/µs
di	IccMAX transient (75% of IccMAX)	SKUs 2 & 6	-	27.75	-	A
		SKUs 11, 14, 19	-	39.75	-	A
		SKUs 1,5, 7-9, 12	-	20.25	-	A
		SKU 10, 18	-	24	-	A
		SKU 13	-	27.75	-	A
dt[5]	Duration for di step	SKUs 2,6, 11,14, 19	-	79.7	-	ns
		SKUs 1,5, 7-9, 12	-	118.2	-	ns
		SKUs 10, 13, 18	-	98.7	-	ns

Symbol	Parameter	SKU	Min	Typical	Max[2]	Unit
DC_LL	DC Loadline	SKUs 11, 14, 19	-	-	4.7	mΩ
		SKUs 1, 2, 5-10, 12-13, 18	-	-	5.0	mΩ
AC_LL	AC Loadline	SKUs 11, 14, 19	-	-	4.7	mΩ
		SKUs 1, 2, 5-10, 12-13, 18	-	-	5.0	mΩ
T_OVS_MAX	Max Overshoot time	All SKUs	-	-	500	µs
V_OVS_MAX	Max Overshoot	All SKUs	-	-	10	%

Notes:

1. Refer to Datasheet, Volume 1 of 2 (RDC #759603) for SKUs 3-4 & 15-17 specifications.
2. A line item does not need to be characterized for SKU2 and SKU6.
3. Refer to DC Specifications notes in Datasheet, Volume 1 of 2 (RDC #759603).
4. Refer to Section 1.4 for supported SKU Map definition.
5. Simulated at processor motherboard pads. This parameter is not tested.

Table 25. VCCGT Supply DC Voltage and Current Specifications

Symbol	Parameter	SKU	Min	Typical	Max[2]	Unit
Operating voltage	Active voltage Range for VccGT	All SKUs	0	-	1.5	V
IccMAX_GT	Max. Current for Processor Graphics Rail	SKUs 2, 6, 10-11, 18 - 19	-	-	29	A
		SKUs 1, 5, 7-9	-	-	23	A
IccTDC_GT	Thermal Design Current (TDC) for Processor Graphics Rail	SKUs 2, 6, 10-11, 18 - 19	-	-	20	A
		SKUs 1, 5, 7-9	-	-	16	A
TOB_GT	VccGT Tolerance	PS0,PS1	-	±20	-	mV
		PS2,PS3	-	±20	-	mV
Ripple	Ripple Tolerance	PS0	-35	-	+50	mV
		PS1	-35	-	+50	mV
		PS2	-35	-	+50	mV
		PS3	-35	-	+50	mV
di/dt	IccMax Slew rate for transient measurement	All SKUs	-	365	-	A/µs
di	IccMAX transient (70% of IccMAX)	SKUs 2, 6, 10-11, 18 - 19	-	20.3	-	A
		SKUs 1, 5, 7-9	-	16.1	-	A
dt[5]	Duration for di step	SKUs 2, 6, 10-11, 18 - 19	-	55.6	-	ns
		SKUs 1, 5, 7-9	-	44.1	-	ns
DC_LL	DC Loadline	All SKUs	-	-	6.5	mΩ
AC_LL	AC Loadline	All SKUs	-	-	6.5	mΩ

Table 25. VCCGT Supply DC Voltage and Current Specifications

Symbol	Parameter	SKU	Min	Typical	Max[2]	Unit
T_OVS_MAX	Max Overshoot time	All SKUs	-	-	10	µs
V_OVS_MAX	Max Overshoot	All SKUs	-	-	70	%

Notes:

1. Refer to Datasheet, Volume 1 of 2 (RDC #759603) for SKUs 3-4 & 15-17 specifications.
2. A line item does not need to be characterized for SKU2 and SKU6.
3. Refer to DC Specifications notes in Datasheet, Volume 1 of 2 (RDC #759603).
4. The VCCGT power rail may be connected to VSS on platforms that support only Intel Atom® x7000C processors.
5. Refer to Section 1.4 for supported SKU Map definition.
6. Simulated at processor motherboard pads. This parameter is not tested.

Table 26. VCCIN_AUX Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typical	Max	Unit
VCCINAUX	Voltage Range	-	1.8	-	V
IccMAX	Maximum VccIN_AUX Icc	-	-	27	A
IccTDC	Thermal Design Current (TDC)	-	-	12	A
TOB_VCCIN_AUX	VCCIN_AUX Tolerance	-10	-	+5	%
di/dt	IccMax Slew rate for transient measurement	-	156	-	A/µs
di	IccMAX transient (70% of IccMAX)	-	19.11	-	A
dt	Duration for di step	-	122.5	-	ns
VOS	Maximum Overshoot Voltage TDP/virus mode	-	-	1.89	V
TVOS	Maximum Overshoot time TDP/virus mode	-	-	5	µs
DC_LL	DC Loadline	-	-	2.0	mΩ

Notes:

1. Refer to the Datasheet, Volume 1 of 2 (RDC #759603) for SKUs 3-4 & 15-17 specifications.
2. Refer to DC Specifications notes in Datasheet, Volume 1 of 2 (RDC #759603).

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12.0 Universal Serial Bus (USB)

This section serves as a Specification Clarification to the corresponding Section18.0 of Datasheet Volume 1 of 2 (RDC #759603) and is not an Edge Applications specific feature. A Specification Clarification describes a specification in greater detail or further highlight a specification impact to a complex design situation.

12.1 USB Dual Role Support - eXtensible Device Controller Interface (xDCI) Controller

The USB subsystem incorporates a xDCI USB 3.0 device controller (5Gb/s) that supports all 32 endpoints (in both USB3 and USB2 modes) for maximum configurability.

The USB subsystem also supports Dual Role Capability. The xHCI is paired with a standalone eXtensible Device Controller Interface (xDCI) to provide dual role functionality. The USB subsystem incorporates a xDCI USB 3.2 device controller.

Note: Usage of this controller is only supported via the PCH USB 2.0 ports. Usage of this controller via the PCH USB 3.2 ports is not supported.

The dual role capability splits the support for SuperSpeed USB 5 Gbps on the CPU xDCI controller, and High-Speed (HS) on the PCH xDCI controller. These device controllers are instantiated as a separate PCI function. The USB implementation is compliant to the Device specification and supports host/device only through the integrated USB Type-C* connector.

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13.0 Image Processing Unit

This section serves as a Specification Clarification to the corresponding Section 9.0 of Datasheet Volume 1 of 2 (RDC #759603) and is not an Edge Applications specific feature. A Specification Clarification describes a specification in greater detail or further highlight a specification impact to a complex design situation.

Note: For any capability not mentioned in this section, refer to Chapter 9 (Image Processing Unit) of Datasheet Volume 1 of 2 (RDC# 759603)

Intel Atom® x7000C processors do not have any IPU capabilities.

13.1 CSI-2 Lane Configuration

Table 27. CSI-2 Lane Configuration

Port Data/Clock	Config. Option 1	Config. Option 2	Config. Option 3	Config. Option 4
Port A Clock	NA	x2	x2	NA
Port A Lane 0 **Note:** multiplexed with Port B Lane 3 for x4 configuration.	x4			x4
Port A Lane 1 **Note:** multiplexed with Port B Lane 2 for x4 configuration.				
Port B Clock		x2	x2	
Port B Lane 0				
Port B Lane 1				
Port C Clock	x4	x2	x4	x2
Port C Lane 0				
Port C Lane 1				
Port D Lane 0 **Note:** multiplexed with Port C Lane 3 for x4 configuration.		x2		x2
Port D Lane 1 **Note:** multiplexed with Port C Lane 2 for x4 configuration.				
Port D Clock	NA		NA	

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14.0 Power Management

Note: For any capability not mentioned in this section, refer to Chapter 10 (Power Management) of Datasheet Volume 1 of 2 (RDC# 759603).

Note: C8, C10, & S0ix states are not supported on the Intel Atom® x7000FE processor series.

14.1 Functional Description

14.1.1 Power Management Sub-State

NOTES

1. Other board capabilities such as power control for RTD3 cold may be implicitly required to satisfy requirements.
2. For external bypass voltage selection, VNN_CTRL can be used to select the external bypass.
3. The integrated GbE controller must be disabled if the platform is required to enable S0ix states.

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15.0 Power Delivery

15.1 Power and Ground Signals

This section describes the power rails.

Table 28. Power Rail Description

Name	Description
VCCGT	Processor Graphics power rail ***Note:*** VCCGT may be connected to VSS on platforms that support only Intel Atom® x7000C processors.

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16.0 Communication & Industrial Use Condition Compliance

16.1 Introduction

In Communication & Industrial use conditions (10 years @ 100% Active), the following design recommendations must be in place for the entire duration of the product's operating lifetime to meet Intel's goals

Note:

1. This chapter only applies to Intel Atom® x7000RE, x7000C, x7000FE processors.
2. For the eMMC & TCSS interfaces, two design recommendation options are listed. Only one out of two of these options should be implemented
   - Reduced Activity Factor
   - Reduced Frequency
3. Activity Factor (AF) is defined as the percentage of time that the interface signals are switching while the processor is active (in an S0 state) across the entire use condition duration.

16.1.1 Power Delivery: VCCANA Mode

The VCCANA power rail must be implemented in FIVR Mode. Implementing VCCANA in MBVR (Motherboard Voltage Regulator) Mode is not allowed.

16.1.2 Intel® Turbo Boost Technology 2.0

The CPU & GPU Intel® Turbo Boost Technology 2.0 features should be disabled by the system BIOS, so the maximum frequency is limited to the HFM value.

16.1.3 embedded Multi Media Card (eMMC*)

Note: These design recommendations apply to the following interface signals unless otherwise stated below: EMMC_CMD, EMMC_DATA[7:0], EMMC_RCLK & EMMC_CLK

Transition Direction	Use Condition	Reduced Activity Factor(AF)	Reduced Activity Factor Mitigation	Reduced Frequency	Reduced Frequency Mitigation
TX (Transmit) RX (Receive)	Communication Industrial	≤ 25% [1,2,3]	The AF can be reduced by using software to put the eMMC controller into a D3 device state when not in use.	≤ 50MHz	The interface frequency can be reduced by using the system BIOS. The configured registers bits are described in Section 16.1.3.1

NOTES:
1. For HS200 and HS400 modes.
2. An activity factor of 100% will result in a failure rate of up-to twice that of Intel's goals at 10 years of operation.
3. With an activity factor of 100%, the failure rate will remain within Intel's goals at up-to 7 years of operation.

16.1.3.1 Reduced Frequency Mitigation

1. Enable interface capabilities bypass
   - Cap_byps.Enable_Cap_Bypass = 5Ah
2. Disable HS400 mode
   - Cap_byps_reg1.hs400_support = 0b
3. Disable HS200 mode
   - Cap_byps_reg1.sdr104_support = 0b

The locations for the registers listed above are described below.

1. Capabilities Bypass (Cap_byps)—Offset 810h
   - Type: MEM (Memory Mapped)
   - BAR – Base Address Register
     i.BAR: [B:0, D:26, F:0] + 10h
     ii.BAR_HIGH: [B:0, D:26, F:0] + 14h
2. Cap_byps_reg1
   - Type: MEM (Memory Mapped)
   - BAR – Base Address Register

16.1.4 USB-C* Sub System (TCSS)

Note: These design recommendations apply to the following interface signals unless otherwise stated below: TCP[1:0]_TX_P[1:0], TCP[1:0]_TX_N[1:0], TCP[1:0]_TXRX_P[1:0], TCP[1:0]_TXRX_N[1:0], TCP[1:0]_AUX_P & TCP[1:0]_AUX_N

Transition Direction	Use Condition	Reduced Activity Factor(AF)	Reduced Activity Factor Mitigation	Reduced Frequency	Reduced Frequency Mitigation
TX (Transmit) RX (Receive)	Communication Industrial	N/A	N/A: Reduced Frequency Mitigation must be used	5 GT/s	The frequency can be changed with soft straps.

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17.0 Enhanced Serial Peripheral Interface (eSPI)

This section serves as a Specification Clarification to the corresponding section of the Datasheet Volume 1 (RDC# 759603) and is not an Edge Applications specific feature. A Specification Clarification describes a specification in greater detail or further highlight a specification impact to a complex design situation.

Note: For any capability not mentioned in this section, refer to Chapter 36 (Enhanced Serial Peripheral Interface (eSPI)) of Datasheet Volume 1 (RDC# 759603).

17.1 Multiple Target Device Support

The eSPI controller supports up to two target devices. This section describes specifications that are specific to implementing more than one target device.

17.1.1 Second Target Device Presence

The controller does not perform discovery to confirm the presence of the target connection. If a second device is enabled by soft strap, it must be physically present on the platform. If the second device is enabled by soft strap but is not physically present, the platform will fail to boot.

17.1.2 Peripheral Channel (Channel 0)

- **Tunnel all Host to eSPI Target (EC/SIO) Debug Device Accesses:**
  These are the accesses that used to go over the LPC bus. These include various programmable and fixed I/O ranges as well as programmable Memory ranges. The programmable ranges and their enables reside in the PCI Configuration space.

Note: These accesses can only be routed to one CS# signal at a time. The CS# is selected using the eSPI CS1 IO Routing Enables (ESPI_CS1IORE) register.

Note: Only CS0# has four Generic I/O Ranges assigned to it, which are configured using the ESPI_LGIR[4:1] registers. CS1# has one Generic I/O Range assigned, which is configured using the ESPI_CS1GIR1. An eSPI device requiring >1 Generic I/O range must be connected to CS0#.

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18.0 Memory

Note: For any capability not mentioned in this section, refer to Chapter 16 (Memory) of Datasheet volume 1 (RDC# 759603).

18.1 Supported Memory Modules and Devices

Table 29. Supported DDR4 Non-ECC SoDIMM Module Configurations

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
E	32 GB	16 Gb	2048M x 8	16	2	17/10	16	8K

Table 30. Supported LPDDR5 x32 DRAMs Configurations

Maximum System Capacity[4]	PKG Type	(Die bits per Ch x PKG bits)[2]	Die Density	PKG Density	Rank Per PKGs
32 GB	ODP	16 x 32	16 Gb	16 GB	2

Notes:
1. x32 BGA devices are 315 balls
2. DDP = Dual Die Package, QDP = Quad Die Package, ODP = Octal Die Package
3. Each LPDDR5 channel includes two sub-channels
4. Maximum system capacity refers to a system with all 4 sub-channels populated.
5. Supports 8 bank mode (8B) LPDDR5 only.

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19.0 Machine Check Architecture (MCA)

MCA is a mechanism for detecting and reporting hardware (machine) errors in processor. A special I/O machine check bank, designated as IOMCA, is also configured to report I/O-based errors through the MCA mechanism. Software can configure the processor to handle Machine Check Exceptions (MCEs).

The processor supports preserving the machine state across the assertion of a Platform Reset. Only upon the assertion (the signal transition from low to high) of the PROCPWRGD input signal (indicating POWERGOOD, power-on) is the MCA state reinitialized. The BIOS can save the MCA state following the assertion of Platform Reset, which allows the BIOS and OS to perform enhanced error recovery before restarting. Consider, for example, a subsystem that produces uncorrected errors. The BIOS or OS may run additional diagnostics on the subsystem and possibly reconfigure the system to avoid the problematic hardware before restarting.

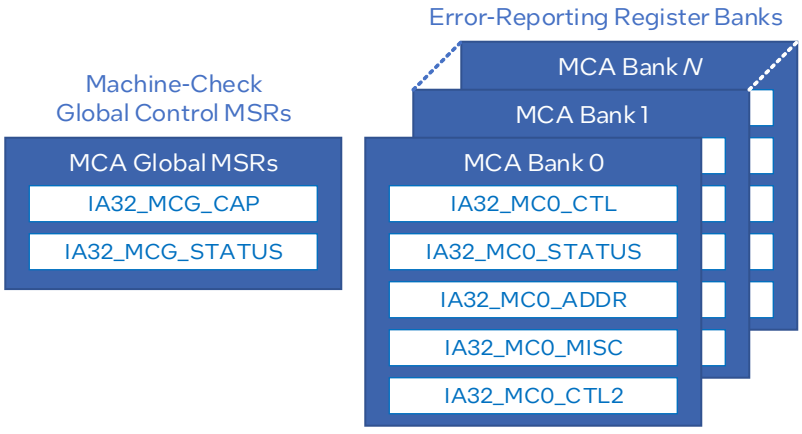
MCA state information is accessible via Model-Specific Register (MSR) accesses using Read MSR (RDMSR) and Write MSR (WRMSR) instructions. RDMSR and WRMSR are described in Volume 2, Chapter 4, of the Intel® 64 and IA-32 Architectures Software Developer's Manual (#671200). MCA is described in Volume 3, Chapter 17, of the same manual.

- Volume 3, Chapter 17 of the Intel® 64 and IA-32 Architectures Software Developer's Manual describes the correct procedures to read and write MCA registers. Not following these procedures will cause a general protection exception to occur.

Intel® Architecture defines two classifications of Machine-Check MSRs (see the following figure):

- Machine-Check Global Control MSRs
- Error-Reporting Register Banks

Figure 15. Structure of Machine-Check MSRs



19.1 Machine-Check Global Control MSRs

The following Machine-Check Global Control MSRs are implemented by the processor:

- IA32_MCG_CAP Register (address 0x179) - This register indicates the MCA capability of the processor. The value of this register is read-only and cannot be modified by any means. It is recommended that OS/BIOS should first check bits [7:0] of IA32_MCG_CAP MSR to identify the total number of Machine-Check Exception (MCE) error-reporting banks supported by a given processor SKU.
- IA32_MCG_STATUS Register (address 0x17A) - This register describes the current processor state after a machine check exception occurs including if an MCE is already in progress (MCIP), if the instruction pointer (IP) associated with the error IP is valid (EIPV) and if the restart IP is valid (RIPV).
- The processor does not implement the IA32_MCG_CTL and IA32_MCG_EXT_CTL Machine-Check Global Control MSRs.

19.2 Error-Reporting Register Banks

Each Error-Reporting Register Bank may contain up to five MSRs (where MCi refers to a specific bank of registers):

- IA32_MCi_CTL
- IA32_MCi_STATUS
- IA32_MCi_ADDR
- IA32_MCi_MISC
- IA32_MCi_CTL2

A brief description of each register type follows. Refer to Volume 3, Chapter 15 of the Intel® 64 and IA-32 Architectures Software Developer's Manual for a more comprehensive description.

- **IA32_MCi_CTL MSR** - This register controls the signaling of machine check exceptions for each machine check bank. Each of the Enable bits represent a specific error event. Each bank implements its own bit definitions. Software sets an Enable bit to enable the signaling of a machine check exception upon the occurrence of the associated error. When the Enable bit is cleared, the associated error is still logged but a machine check exception is not signaled. IA32_MCi_CTL is the only MSR in the bank that is cleared on warm reset.
- **IA32_MCi_STATUS MSR** - This register contains information related to a machine check error for the machine check bank. The information is set by the hardware. Software is responsible for clearing this register by writing all 0's. If software attempts to set any bits in this MSR, a general protection exception occurs.

Note: Asynchronous MCA error injection is not supported.

- **IA32_MCi_ADDR MSR** - This register contains the address of the instruction or data that triggered the MCE. The address contained in the IA32_MCi_ADDR MSR is an offset into a segment, linear, or system address (also known as physical address). The processor supports up to 42 bits of address (bits 41:0) so the upper bits (bits 63:42) are reserved. When the IA32_MCi_ADDR MSR is implemented, it can be cleared by explicitly writing all zeros. If software attempts to set any bits in this MSR, a general protection exception occurs.

Note: Software must check the ADDRV flag (Bit 58) in the corresponding IA32_MCi_STATUS MSR prior to accessing IA32_MCi_ADDR MSR. If the ADDRV flag in the associated IA32_MCi_STATUS MSR is not set, the IA32_MCi_ADDR MSR is either not implemented or does not contain a valid address.

- **IA32_MCi_MISC MSR** - This register contains bank-specific additional information describing the machine-check error if the MISCV flag in the IA32_MCi_STATUS register is set. For Uncorrected Recoverable (UCR) errors (when Corrupt Data Containment is enabled), the address mode as specified in bits 8:6 will always be reported as a system address (physical address). When the IA32_MCi_MISC MSR is implemented, it can be cleared by explicitly writing all zeros. If software attempts to set any bits in this MSR, a general protection exception occurs.

Note: Software must check the MISCV (Bit 59) flag in the corresponding IA32_MCi_STATUS MSR prior to accessing IA32_MCi_MISC MSR. If the MISCV flag in the associated IA32_MCi_STATUS MSR is not set, the IA32_MCi_MISC MSR is either not implemented or does not contain valid data.

- IA32_MCi_CTL2 MSR - This register provides the programming interface for corrected machine check error signaling capability (see Corrected Machine-Check Interrupt (CMCI) on page 12) that is indicated by IA32_MCG_CAP[10] = 1. For the processor, IA32_MCG_CAP[10] = 1 and therefore the IA32_MCi_CTL2 MSR exists for all the applicable banks. However, signaling interface for corrected errors may not be supported in all banks. The value of this register is also retained after a warm reset.

The following table specifies various attributes of the MSRs for Error-Reporting Register Banks.

Table 31. Attributes of MSRs for Error-Reporting Register Banks

MSR	Implemented Always/Optional	Cleared by Warm Reset
IA32_MCi_CTL	Always	Yes
IA32_MCi_STATUS	Always	No
IA32_MCi_ADDR	Optional[1]	No
IA32_MCi_MISC	Optional[1]	No
IA32_MCi_CTL2	Optional[1]	No

1. If any of the optionally implemented MSRs are not implemented in a machine check bank, reads, and writes to that register address causes a general protection exception.

See Chapter 19.4 “Processor MCA Error-Reporting Register Banks and MSR Addresses” on page 93 for a list of the Error-Reporting Register Banks supported by the processor.

19.3 Corrected Machine-Check Interrupt (CMCI)

Corrected Machine-Check Interrupt (CMCI) is an architectural enhancement to the MCA. It provides capabilities beyond those of threshold-based error reporting. With threshold-based error reporting, software is limited to use periodic polling to query the status of hardware-corrected Machine-Check errors.

CMCI provides a signaling mechanism to deliver a local interrupt that is based on threshold values that software can program in bits [14:0] of the Machine-Check Bank IA32_MCi_CTL2 MSRs.

CMCI is disabled by default. The MCP_CMCI_P bit of the IA32_MCG_CAP Global Machine Check register, when set, indicates that the processor has the CMCI capability. Bit 30 of each IA32_MCi_CTL2 register must be checked to determine whether the particular Machine-Check Bank has the CMCI-signaling capability.

Corrected Machine-Check Errors detected in the non-core portion of the processor generate a CMCI to all cores of the processor.

The processor's APIC Local Vector Table (LVT) has an IA32_X2APIC_LVT_CMCI (address 0x82F) register that specifies Interrupt Delivery Mode (refer to Table 32 for further information) and Vector to be taken when an overflow condition of corrected machine check error count reaching a threshold value occurs in a machine check bank supporting CMCI.

Table 32. Interrupt Delivery Mode (IA32_X2APIC_LVT_CMCI.DELIVERY_MODE)

DELIVERY_MODE Value	DELIVERY_MODE Definition
000b (default)	Fixed
001b	Reserved
010b	SMI
011b	Reserved
100b	NMI
101b -111b	Reserved

19.4 Processor MCA Error-Reporting Register Banks and MSR Addresses

The following table lists the MCA error-reporting register banks supported by the processor and the corresponding MSR addresses.

Table 33. Processor MCA Error-Reporting Register Banks and MSR Addresses

MCA Error-Reporting Register Bank		MSR Address				
Machine Bank Number	Processor Module[1]	IA32_MCi_CTL	IA32_MCi_STATUS	IA32_MCi_ADDR	IA32_MCi_MISC	IA32_MCi_CTL2
0	BIU[2]	0x400	0x401	0x402	0x403	0x280
1	L2 Cache[2]	0x404	0x405	0x406	0x407	0x281
2	L1 Instruction Cache (FEC)[3]	0x408	0x409	0x40A	0x40B	0x282
3	L1 Data Cache (MEC)[3]	0x40C	0x40D	0x40E	0x40F	0x283
4	Memory Encryption Engine (MEE)[4]	0x410	0x411	0x412	0x413	0x284
5	Unused[5]					
6	IOMCA	0x418	0x419	Unused	0x41B	0x286
7	P-Unit	0x41C	0x41D	0x41E	0x41F	0x287
8	Power Management IP (PMIP)[6]	0x420	0x421	0x422	0x423	0x288
9	PTR/Last Level Cache (LLC) - 3MB	0x424	0x425	0x426	0x427	0x289
10	PTR/Last Level Cache (LLC) - 3MB	0x428	0x429	0x42A	0x42B	0x28A

1. Key:
   - BIU - Bus Interface Unit
   - MEC - Memory Execution Cluster (Data Cache/Fetch/Store)
   - FEC - Fetch Execution Cluster (Instruction Cache/Fetch)
   - PMIP - Power Management IP
   - PTR - Processor Transaction Router
2. The Bus Interface Unit (BIU) MCA bank (Bank 0) and L2 MCA bank (Bank 1) are shared by all cores in the same module.
3. The Fetch Execution Cluster (FEC) MCA bank (Bank 2) and Memory Execution Cluster (MEC) MCA bank (Bank 3) are implemented for each individual core.
4. The MEE is used to configure & secure memory used for the processor microcode patch.
5. MSRs in unused banks are read as 0 and writes to these registers are dropped.
6. PMIP is a processor die controller that works in parallel with & in collaboration with the P-Unit. It manages the energy efficiency & power limits of the processor.

Note: The Machine Bank Numbers supported may vary based on processor SKU. It is recommended that OS/BIOS should first check bits [7:0] of IA32_MCG_CAP MSR (address 0x179) to identify the total

number of error-reporting banks supported by a given processor SKU. Refer to the Intel® 64 and IA-32 Architectures Software Developer's Manual for further details about error-reporting register banks.

The Bus Interface Unit (BIU) MCA bank (Bank 0) and L2 Cache MCA bank (Bank 1) are shared by all cores in the same module. The L1 Data Cache MCA bank (Bank 2) and L1 Instruction Cache MCA bank (Bank 3) are implemented for each individual core. The rest of the MCA banks are shared by all the cores in the processor.

Note: Only 8 core processors have two modules.

MCE are always broadcast to all cores. CMCI is contained to the domain at which the error occurs. For example:

- CMCI due to a corrected error in the L2 would be sent to all cores in the same module, but not to other CPU core modules.
- CMCI due to a parity error in the Instruction cache would only go to the core containing that Instruction cache.

19.5 IOMCA

IOMCA introduces an error reporting bank (Bank 6) within the Processor Transaction Router (PTR) to log errors detected by the PTR itself.

- In-band ECC (IBECC)
- Graphics Processing Unit (GPU)
- Image Processing Unit (IPU)
- Processor Transaction Router (PTR)
- Display Controller
- PSF[0:1,OPI]
- Platform Controller Hub (PCH)

Note: The Integrated Error Handler (IEH) must be configured to be in Enabled Mode, for PCH errors to be logged. Refer to Chapter 20.3.2 for further information.

The IOMCA bank follows the MCA architecture as defined in Volume 3, Chapter 17 of the Intel® 64 and IA-32 Architectures Software Developer's Manual (#671200).

The IOMCA registers are shown in the following table.

Table 34. IOMCA Error-Reporting Bank Registers

Register	Address	Description
IA32_MC6_CTL	0x418	MCA enables
IA32_MC6_STATUS	0x419	Standard MCi_STATUS register
IA32_MC6_MISC	0x41B	Error logging for I/O Fabric errors
IA32_MC6_CTL2	0x286	Corrected machine check error signaling control

Because there is no physical address information associated with I/O errors, the IA32_MC6_ADDR register is not included in the IOMCA bank and the ADDRV bit in the IA32_MC6_STATUS register is always 0.

Table 35. IA32_MC6_CTL

Bits	Name	Description
0	IOSF_FatalMcaEn	Enable MCA signaling for PSF fatal errors
1	IOSF_NonFatalMcaEn	Enable MCA signaling for PSF non-fatal errors
2	IOSF_CorrMcaEn	Enable MCA signaling for PSF correctable errors
3	MC_FatalMcaEn	Enable MCA signaling for Memory Controller fatal errors
4	MC_NonFatalMcaEn	Enable MCA signaling for Memory Controller non-fatal errors
5	MC_CorrMcaEn	Enable MCA signaling for Memory Controller correctable errors

Table 36. IA32_MC6_STATUS

Range	Name	Description	Notes
15:0	MCACOD	Machine Check Error Code	0x008F: Memory Controller (including IBECC) 0x0E0B: All other controllers
16	MSCOD	Model Specific Error Code: Fatal error reported	Broadcasted as MCE
17	MSCOD	Model Specific Error Code: Non-fatal error reported	Broadcasted as MCE
18	MSCOD	Model Specific Error Code: Corrected error reported	Broadcasted as CMCI
23:19	MSCOD	Undefined	
31:24	MSCOD	Model Specific Error Code: Error source	0x00: Memory Controller (including IBECC) 0x01: GPU & Display Controller 0x02: IPU 0x03: OPI 0x05-0x08: PTR 0x10: PTR (IOP) 0x11: Display Controller 0x12: PSF0 0x13: PSF1 0x14: PSF_OPI 0x1F: PCH[1]
37:32	OTHER	Other Info	Always 0
52:38	ERR_CNT	Corrected Error Count	
54:53	THRS_ERR_ST	Threshold-based error status[2]	
55	AR	Recover Action Required[3]	
56	S	Signaling an uncorrected recoverable error[3]	Set to 1 if an Uncorrected Recoverable (UCR) – Nonfatal error occurs
57	PCC	Processor context corrupt	Set to 1 if an Uncorrected – Fatal error occurs
58	ADDRV	IA32_MC6_ADDR register valid	Always 0
59	MISCV	IA32_MC6_MISC register valid	Set to 0 when error source has no PCI Bus/ Device/Function number
60	EN	Error reporting enabled	Set if corresponding IA32_MC6_CTL bit was set

Table 36. IA32_MC6_STATUS

Range	Name	Description	Notes
61	UC	Uncorrectable error	Set to 1 if an uncorrected error occurs
62	OVR	Error overflow	Set to 1 if an error occurs where a valid error is already logged
63	VAL	IA32_MC6_STATUS register valid	Set to 1 when valid error occurs

1. The Integrated Error Handler (IEH) must be configured to be in Enabled Mode, for PCH errors to be logged. Refer to Section 20.3.2 for further information.
2. Part of OTHER range when IA32_MCG_CAP[11] is not set.
3. Reserved when IA32_MCG_CAP[11] or IA32_MCG_CAP[24] are not set.

Table 37. IA32_MC6_MISC Definition for Memory Controller Errors

Range	Name	Description
23:0	Reserved	Always 0
31:24	Memory Controller Source ID	Source ID of the PCIE_ERR message
63:32	Reserved	Always 0

Table 38. IA32_MC6_MISC for All Other Controllers

Range	Name	Description
15:0	Reserved	Always 0
18:16	Function_Log	PCIe function number of IOMCA error source
23:19	Device_Log	PCIe device number of IOMCA error source
31:24	Bus_Log	PCIe bus number of IOMCA error source
63:32	Reserved	Always 0

Table 39. IA32_MC6_CTL2 Definition

Range	Name	Description
14:0	CORR_ERR_CNT	Corrected error count threshold
29:15	Reserved	Always 0
30	CMCI_EN	CMCI enable
63:31	Reserved	Always 0

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20.0 Intel® Silicon Integrity Technology

This section provides an overview of supported Functional Safety (FuSa) features.

For additional details on FuSa features, do check with your Intel representative on the availability of FuSa documentation packages.

Note: This chapter only applies to Intel Atom® x7000FE processors.

20.1 Overview

Intel® Silicon Integrity Technology comprises a set of processor hardware and firmware capabilities plumbed into select Intel processors that works in conjunction with the system BIOS to support FuSa solutions in multiple application domains such as industrial, fixed robotics, automotive, avionics and autonomous mobile robots. Table 40 provides a high-level description of the main feature categories.

Table 40. Integrity-Related Macro Feature Categories

Integrity-Related Macro Feature Categories
Core diagnostic and in-field test (Array/Logic Built-in Self-Tests (BIST), Core Lockstep)
Fabric Integrity (End-to-End (e2e) parity across fabrics)
Core, uncore, memory, array protection (ECC parity, CRC)
Off-line tests and flows (BIST, power-on set tests, Check-the-checker)
Error reporting and logging (aligned with Intel's Machine Check Architecture (MCA) Recovery)
Clock, voltage, power integrity (integrity monitors)

Intel® Silicon Integrity Technology can assist in contributing to:

- Decreasing the residual failure rate of dangerous undetected faults
- Efficiently detecting transient (soft errors) and permanent faults
- Augmenting the integrity of on-chip shared and infrastructural resources, thus increasing the control of common cause failures
- Offering an efficient error reporting and logging infrastructure
- Enabling on-demand in-field diagnostic against latent fault accumulation
- Enhancing the on-chip anomaly detection capability for general silicon health diagnostics

Intel® Silicon Integrity Technology features support two main categories, based on the execution phase (offline or runtime) during which the diagnostics are active.

- Offline diagnostic tests include features such as memory BIST and CtC (Check the Checker) executed during a dedicated on-demand offline diagnostic flow and further classified by:

— Pre-BIOS diagnostics: run on-demand before the bootloader is executed and involves firmware of different IPs.

— BIOS diagnostics: run on-demand and implemented mainly via Firmware Support Package (FSP) or the bootloader.

- Runtime features include those that are always active (such as dual core lockstep, ECC/Parity, E2E Parity) and those that are periodically executed (periodic Mem BIST). Some of these require configuration by the BIOS or bootloader.

20.2 Signal Description

The following signals are relevant to Functional Safety.

Table 41. Signal Description

Signal Description	Type	Description
PROCHOT#	I/O	**Processor Hot:** The PROCHOT# signal can be configured to the following modes: • Input Only: PROCHOT# is asserted by an external device, such as a Voltage Regulator (VR), to activate the Thermal Control Circuit (TCC). • Output Only: PROCHOT# is asserted by the processor when the TCC is active. • Bi-Directional: Both external device & processor can assert PROCHOT#.
CATERR#	O	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: • Legacy MCERRs: CATERR# is asserted for 160ns. • Legacy IERRs: CATERR# remains asserted until a warm or cold reset.
GPP_F22 / VNN_CTRL / **IEH_CORR_ERR0#** GPP_F23 / V1P05_CTRL / **IEH_NONFATAL_ERR1#** GPP_H3 / SX_EXIT_HOLDOFF# / **IEH_FATAL_ERR2#**	O	**Error (active low):** These signals indicate to the external circuitry the severity of a detected error: • IEH_CORR_ERR0#: Correctable Error • IEH_NONFATAL_ERR1#: Non-Fatal Error • IEH_FATAL_ERR2#: Fatal Error (system reset likely required to recover) While PLTRST# is asserted, these signals are not valid and should be ignored by the platform board circuitry.
THERMTRIP#	O	**Thermal Trip**: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. If THERMTRIP# goes active, the processor is indicating an overheat condition, and the PCH immediately transitions to an S5 state, driving SLP_S3#, SLP_S4#, SLP_S5# low, and setting the GEN_PMCON_2.PTS bit. ***Note:*** THERMTRIP# is also used to indicate FIVR faults at power-on.
FUSA_DIAGTEST_EN (Ball CJ39[1])	I	**FuSa Diagnostic Test Enable:** This signal is driven by an external device to configure FuSa diagnostic testing: • 0: Disable FuSa diagnostic testing • 1: Enable FuSa diagnostic testing
FUSA_DIAGTEST_MODE (Ball CW25[2])	I	**FuSa Diagnostic Test Mode:** This signal is driven by an external device to configure the FuSa diagnostic testing mode • 0: Enable BIOS diagnostic testing mode • 1: Enable pre-BIOS diagnostic testing mode

1. The GPP_D1 / ISH_GP1 / BK1 / SBK1 signal functions are not available for use in Intel Atom® x7000FE processors.
2. The GPP_F6 / CNV_PA_BLANKING signal functions are not available for use in Intel Atom® x7000FE processors.

20.3 Functional Description

20.3.1 PROCHOT#

Refer to Section 12.1.3.3 of the Datasheet Volume 1 (RDC#759603) for further information.

Note: It is recommended to have PROCHOT# signal set as Output Only or Bi-Directional by default for FuSa applications, so that the processor can be monitored by the system integrator to activate any temperature control mechanisms.

20.3.2 IEH_CORR_ERR0#, IEH_NONFATAL_ERR1#, IEH_FATAL_ERR2#

The Integrated Error Handler (IEH) is part of the Primary to Sideband Bridge (P2SB) device and maps all PCH detectable uncorrected errors, including legacy errors, to an error output dependent on the configured IEH mode.

The IEH defaults to 'BIOS Mode' after reset. During boot, the BIOS must configure the IEH to operate in either 'Bypass Mode' or 'Enabled Mode'.

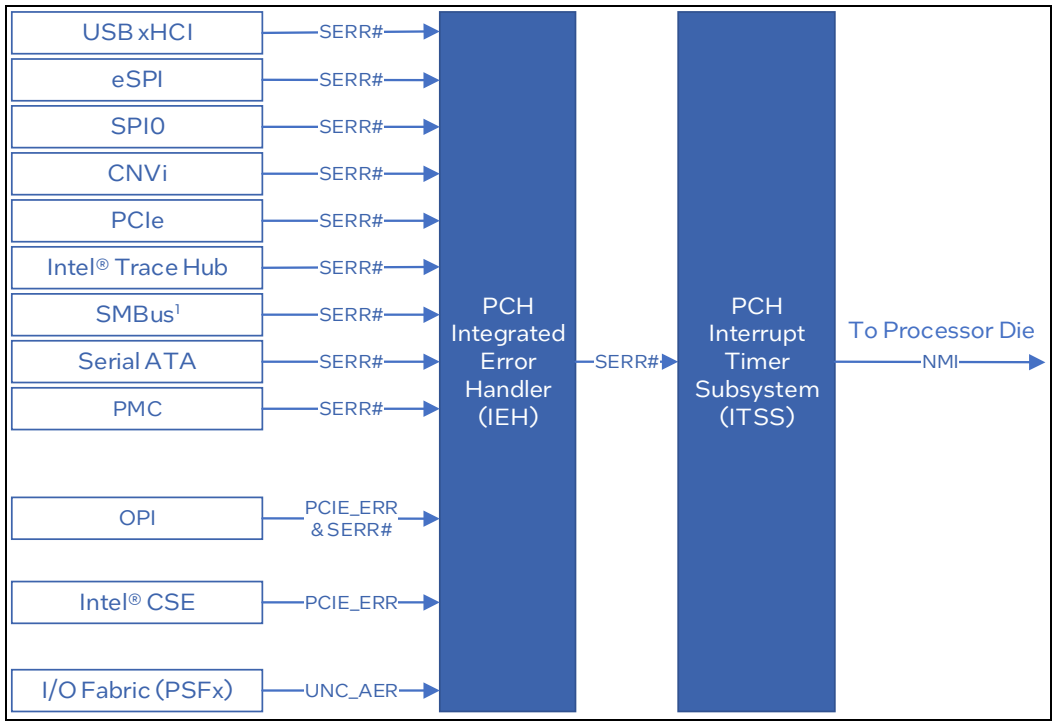
20.3.2.1 Bypass Mode

The IEH maps all PCH detectable uncorrected errors, including legacy errors, to a System Error (SERR#) that is routed to the Interrupt and Timer Sub-System (ITSS). Upon receipt of the SERR#, the ITSS initiates a Non Maskable Interrupt (NMI) to the processor die over the IOSF-SB bus.

Note: The IEH_CORR_ERR0#, IEH_NONFATAL_ERR1#, IEH_FATAL_ERR2# signals are inactive in Bypass Mode.

Note: Bypass Mode is supported by all processors specified within this document.

Figure 16. IEH Bypass Mode



Note: The SMBus controller can also generate a SERR# in response to a SERR# message received over the On Package Interface (OPI) from the processor die.

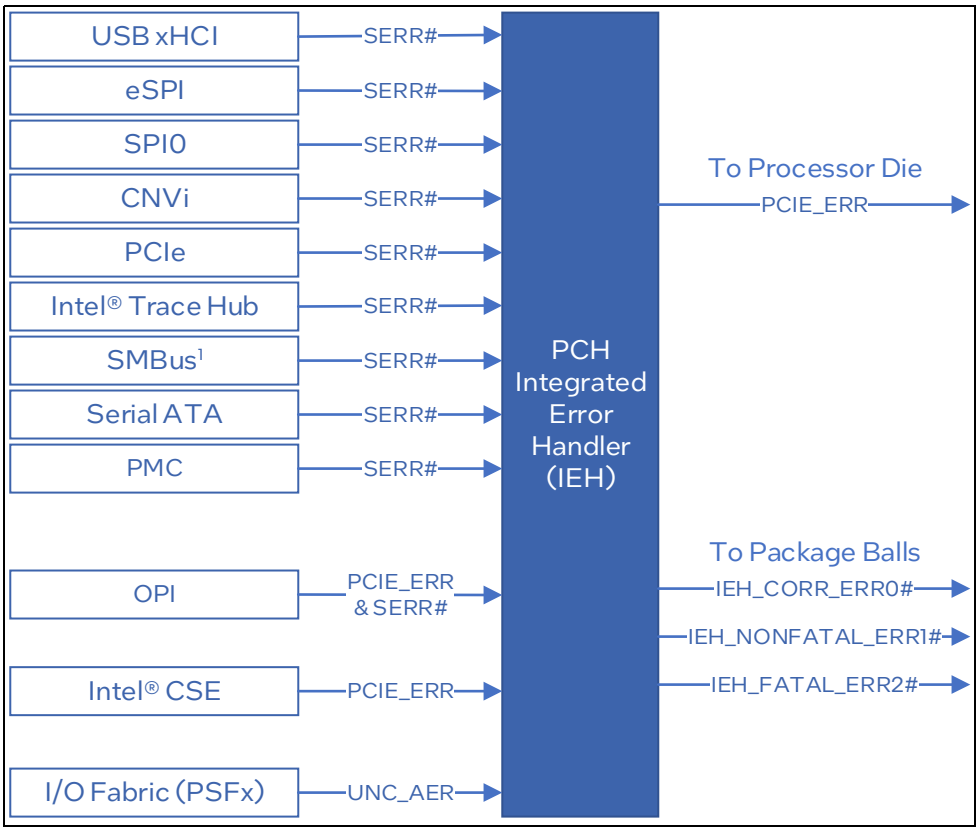
20.3.2.2 Enabled Mode

The IEH maps all PCH detectable errors, including legacy errors, to:

- A PCIE_ERROR message that is routed to the processor die, over the IOSF-SB bus.
- Assertion of the IEH_CORR_ERR0#, IEH_NONFATAL_ERR1#, IEH_FATAL_ERR2# signals.

Note: The state of the ERR# signals are cleared at warm reset but the error that caused the signal assertion will remain logged, since all status registers are sticky.

Figure 17. IEH Enabled Mode



Note: The SMBus controller can also generate a SERR# in response to a SERR# message received over the On Package Interface (OPI) from the processor die.

20.3.3 THERMTRIP#

Refer to Section 10.4.8 of the Datasheet Volume 1 (RDC# 759603) for further information.

20.3.4 FUSA_DIAGTEST_EN, FUSA_DIAGTEST_MODE

These signals are driven by an external device to configure the FuSa diagnostic testing mode, as described in Table 42 below.

Note: The state of FUSA_DIAGTEST_EN & FUSA_DIAGTEST_MODE is sampled by the processor during an S5 - S0 state transition.

Table 42. FuSa Diagnostic Test Configuration

FUSA_DIAGTEST_EN	FUSA_DIAGTEST_MODE	Configuration
0	0 or 1	Not in FuSa diagnostic test mode
1	0	FuSa BIOS diagnostic testing mode
1	1	FuSa pre- BIOS diagnostic testing mode

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21.0 Registers

21.1 Integrated Gigabit Ethernet Controller Configuration Registers Summary

Note: These registers are only applicable for the Intel Atom® x7000 processor series.

This chapter documents the registers in Bus: 0, Device: 30, Function: 4.

DID Values:

GbE Controller:- D30: F4 - 54ACh

Table 43. Summary of Bus: 0, Device: 30, Function: 4 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID Register (DEVVENDID)	54AC0000h
4h	4	Status And Command (STATUSCOMMAND)	00100000h
8h	4	Revision Id And Class Code (REVCLASSCODE)	00000000h
Ch	4	Cache Line Latency Header And Bist (CLLATHEADERBIST)	00000000h
10h	4	Base Address Register (BAR)	00000000h
14h	4	Base Address Register High (BAR_HIGH)	00000000h
18h	4	Base Address Register1 (BAR1)	00000000h
1Ch	4	Base Address Register1 High (BAR1_HIGH)	00000000h
2Ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	00000000h
30h	4	EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)	00000000h
34h	4	Capabilities Pointer (CAPABILITYPTR)	00000080h
3Ch	4	Interrupt Register (INTERRUPTREG)	00000100h
40h	4	Pcie Capabilities Register (PCIECAPREG)	00920010h
44h	4	Pcie Device Capability Register (DEVCAPREG)	10008FC0h
48h	4	Pcie Device Control Status Register (DEVCTRLSTAT)	00000000h
64h	4	Pcie Device Capability2 Register (DEVCAPREG2)	00000000h
68h	4	Pcie Device Control2 Status Register (DEVCTRLSTAT2)	00000000h
80h	4	PowerManagement Capability Id (POWERCAPID)	48030001h
84h	4	Power Management Control And Status Register (PMECTRLSTATUS)	00000008h
90h	4	Pci Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)	01400010h
98h	4	Software Ltr Update Mmio Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	00000000h
9Ch	4	Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG)	00000000h
A0h	4	D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)	00000800h
B0h	4	General Purpose Read Write Register1 (GEN_PCI_REGRW1)	00000000h
C0h	4	General Purpose Input Register (GEN_INPUT_REG)	00000000h
D0h	4	Msi Capability Register (MSI_CAP_REG)	01800005h
D4h	4	Msi Message Low Address (MSI_ADDR_LOW)	00000000h
D8h	4	Msi Message High Address (MSI_ADDR_HIGH)	00000000h
DCh	4	Msi Message Data (MSI_MSG_DATA)	00000000h
E0h	4	MSI Mask Register (MSI_MASK)	00000000h
E4h	4	MSI Pending Register (MSI_PENDING)	00000000h
F8h	4	Manufacturers ID (MANID)	00000000h

21.1.1 Device ID and Vendor ID Register (DEVVENDID) — Offset 0h

Device ID and Vendor ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 0h	54AC0000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	54ACh RO/P	**Device ID Field (DEVICEID):** Device ID identifies the particular PCI device
15:0	0000h RO	**Vendor ID Field (VENDORID):** Vendor ID is a unique ID provided by the PCI SIG which identifies the manufacturer of the device

21.1.2 Status and Command (STATUSCOMMAND) — Offset 4h

Command register and Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DPE):** Detected Parity Error
30	0h RW/1C	**Signaled System Error (SSE):** Signaled System Error
29	0h RW/1C	**RMA Field (RMA):** Received Master Abort
28	0h RW/1C	**RTA Field (RTA):** Received Target Abort
27:25	0h RO	**Reserved**
24	0h RW/1C	**Master Data Parity Error (MDPE):** Master Data Parity Error
23:21	0h RO	**Reserved**
20	1h RO	**Cap List Field (CAPLIST):** Capabilities List: Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status Field (INTR_STATUS):** Interrupt Status: This bit reflects state of interrupt in the device
18:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Interrupt Disable
9	0h RO	**Reserved**
8	0h RW	**SERR Enable Field (SERR_ENABLE):** SERR Enable Not implemented
7	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Parity Error Response Enable (PERE):** Parity Error Response Enable
5:3	0h RO	**Reserved**
2	0h RW	**BME Field (BME):** Bus Master Enable
1	0h RW	**MSE Field (MSE):** Memory Space Enable
0	0h RO	**Reserved**

21.1.3 Revision ID and Class Code (REVCLASSCODE) — Offset 8h

Revision ID register and Class Code register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RO	**Revision ID Field (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	00h RO/P	**Class Code Field (RID):** Revision ID identifies the revision of particular PCI device.

21.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST) — Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23	0h RO	**MultiFunction Device Field (MULFNDEV):** Multi-Function Device
22:16	00h RO	**Header Type Field (HEADERTYPE):** Header Type: Implements Type 0 Configuration header
15:8	00h RO	**Latency Timer Field (LATTIMER):** Latency Timer:. This register is implemented as R/W with default as 0
7:0	00h RW/P	**Cache Line Size Field (CACHELINE_SIZE):** Cacheline Size

21.1.5 Base Address Register (BAR) — Offset 10h

Base Address Register low [31:2] type [2:1] in 32bit or 64bit address range and memory space indicator [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR):** Base Address Register Low Base address of the AXI fabric memory space. Taken from Strap values as ones
11:4	00h RO	**Size Field (SIZEINDICATOR):** Size Indicator RO Always returns 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable Field (PREFETCHABLE):** Prefetchable: Indicates that this BAR is not prefetchable
2:1	0h RO	**Type Field (TYPE0):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** Memory Space Indicator: 0 indicates this BAR is present in the memory space.

21.1.6 Base Address Register High (BAR_HIGH) — Offset 14h

Base Address Register High enabled if [2:1] of BAR_HIGH is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR_HIGH):** Base Address high - MSB

21.1.7 Base Address Register1 (BAR1) — Offset 18h

Base Address Register1 accesses to PCI configuration space and is always 4K type in [2:1] and memory space indicator in [0].

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Base Address Field (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.

Bit Range	Default & Access	Field Name (ID): Description
11:4	00h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** Prefetchable: Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** Memory Space Indicator: 0 Indicates this BAR is present in the memory space

21.1.8 Base Address Register1 High (BAR1_HIGH) — Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**Base Address High Field (BASEADDR1_HIGH):** Base Address: Base address of the AXI fabric memory space. Taken from Strap values as ones

21.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID) — Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** Subsystem ID: This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** Subsystem Vendor ID: This register must be implemented for any function that can be instantiated more than once in a given system

21.1.10 EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR) — Offset 30h

EXPANSION ROM Base Address register is a RO indicates support for expansion ROMs.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

21.1.11 Capabilities Pointer (CAPABILITYPTR) — Offset 34h

Capabilities Pointer register indicates what the next capability is.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 34h	00000080h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Capabilities Pointer: Indicates what the next capability is.

21.1.12 Interrupt Register (INTERRUPTREG) — Offset 3Ch

Interrupt line Register isn't used in Bridge directly Interrupt Pin register reflects the IPIN value in private configuration space. MIN_GNT register indicating the requirement of latency timers and MAX_LAT register max latency.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 3Ch	00000100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h RO	**Min GNT Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	**Reserved**
11:8	1h RO	**Interrupt Pin Field (INTPIN):** Interrupt Pin: Value in this register is reflected from the IPIN value in the private configuration space.
7:0	00h RW/P	**Int Line Field (INTLINE):** Interrupt Line: It is used to communicate to software the interrupt line to which the interrupt pin is connected

21.1.13 PCIe Capabilities Register (PCIECAPREG) — Offset 40h

PCIe Capabilities register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 40h	00920010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO	**Int Msg Num Field (INTR_MSG_NUM):** PCIE Interrupt Message Number
24	0h RO	**Slot Implemented Field (SLOT_IMPLEMENTED):** Slot Implemented. Tied to 0
23:20	9h RO	**Dev Port Type Field (DEV_PORT_TYPE):** Device Port Type. Taken from strap
19:16	2h RO	**Cap Version Field (CAP_VER):** PCI Capability Version
15:8	00h RO/V	**Next Capability Pointer Field (NEXT_CAP_PTR):** Next Capability Pointer
7:0	10h RO	**Capability ID Field (PCIE_CAP_ID):** PCIE Capability ID

21.1.14 PCIe Device Capability Register (DEVCAPREG) — Offset 44h

PCIe Device Capability register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 44h	10008FC0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO	**FLR Capability Field (FLR_CAP):** FLR Capability
27:26	0h RO	**Capl slot power limit scale Field (CAP_SLOT_PWR_LIM_SCALE):** Captured Slot Power Limit Scale. Tied to 0
25:18	00h RO	**Capl slot power limit value Field (CAP_SLOT_PWR_LIM_VAL):** Captured Slot Power Limit Value. Tied to 0
17:16	0h RO	**Reserved**
15	1h RO	**RB error ptr Field (RB_ERR_RPTR):** Role Based Error Reporting
14:12	0h RO	**Reserved**
11:9	7h RO	**EP L01 Acc Latency Field (EP_L1_ACC_LAT):** L1 Acceptable Latency
8:6	7h RO	**EP L0 Acc Latency Field (EP_L0_ACC_LAT):** L0 Acceptable Latency

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**ETF Support Field (ETF_SUPPORT):** Extended Tag Field Support
4:3	0h RO	**Phantom Func Support Field (PHANTOM_FUNC_SUPPORT):** Phantom Functions support. NA for Bridge
2:0	0h RO	**Max Pl Size Support Field (MAX_PL_SIZE_SUPPORT):** Max Payload Size

21.1.15 PCIe Device Control Status Register (DEVCTRLSTAT) — Offset 48h

PCIe Device Status register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RO/V	**Txn Pending Field (TXN_PENDING):** Transaction Pending bit
20	0h RO	**Aux Power Det Field (AUX_PWR_DETECTED):** Aux Power Detected. Always tied to 0
19	0h RW/1C	**UR Field (UR_DETECTED):** Unsupported Request Detected
18	0h RW/1C	**Fatal Error Det Field (FER_DETECTED):** Fatal Error Detected
17	0h RO	**Non Fatal Err Det Field (NFER_DETECTED):** Non Fatal Error Detected
16	0h RO	**Correctable Error Det Field (CER_DETECTED):** Correctable Error Detected
15	0h WO	**Initiate FLR Field (INITIATE_FLR):** Initiate Function Level Reset
14:12	0h RO	**Max Read Request Size Field (MAX_RD_REQ_SIZE):** Max Read Request Size
11	0h RW	**Enable NoSnoop Field (EN_NS):** Enable No Snoop
10	0h RO	**Aux Power Det Field (AUX_PWR_PM_EN):** Aux Power Enable
9	0h RO	**Phantom Function En Field (PHANTOM_FUNC_EN):** Phantom Function Enable. Not support by Bridge
8	0h RW	**ETF En Field (ETF_EN):** Extended Tag Field Enable
7:5	0h RO	**Max Payload Size Field (MAX_PL_SIZE):** Maximum Payload Size
4	0h RW	**Enable Relaxed Ordering Field (EN_RO):** Enable Relaxed Ordering

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW	**UR Reporting En Field (URR_EN):** Unsupported Request Reporting Enable
2	0h RW	**Fatal Err Reporting En Field (FER_EN):** Fatal Error Reporting Enable
1	0h RW	**Non Fatal Err Reporting En Field (NFER_EN):** Non Fatal Error Reporting Enable
0	0h RW	**Correctable Error Reporting En Field (CER_EN):** Correctable Error Reporting Enable

21.1.16 PCIe Device Capability2 Register (DEVCAPREG2) — Offset 64h

PCIe Device Cap Register 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RO	**Max End2End TLP Prefix Field (MAX_EE_TLP_PREFIXES):** Max End2End TLP Prefixes
21	0h RO	**End2End TLP Prefix Supported Field (EE_TLP_PREFIX_SUPPORT):** End2End TLP Prefixes Support
20	0h RO	**Ext Format Support Field (EXTD_FMT_SUPPORT):** Extended Format Support
19:18	0h RO	**OBFF Support Field (OBFF_SUPPORT):** PCI OBFF Support
17:14	0h RO	**Reserved**
13:12	0h RO	**TPH Completer Supported Field (TPH_CPL_SUPPORT):** TPH Completer Support
11	0h RO	**LTR Support Field (LTR_SUPPORT):** LTR Support
10	0h RO	**NO RO Enable Field (NRO_EN_PRPR_PASS):** No RO based PR-PR Passing
9	0h RO	**CAS CPL 128 Support Field (CAS_CPL_SUPPORT_128):** CAS128 Support
8	0h RO	**CAS CPL 64 Support Field (ATM_OP_CPL_SUPPORT_64):** CAS64 Completion Support
7	0h RO	**CAS CPL 32 Support Field (ATM_OP_CPL_SUPPORT_32):** CAS32 Completion Support
6	0h RO	**Atomic Operation Routing Field (ATOR_SUPPORT):** Atomic Operation Routing Support
5	0h RO	**PCI ARI Forwarding Support Field (ARI_FWD_SUPPORT):** ARI Forwarding Support

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**CPL Timeout Disable Support Field (CPL_TO_DIS_SUPPORT):** Completion Timeout Disable Support
3:0	0h RO	**CPL Timeout Range Support Field (CPL_TO_RNG_SUPPORT):** Completion Timeout Ranges Support

21.1.17 PCIe Device Control2 Status Register (DEVCTRLSTAT2) — Offset 68h

PCIe Device Status Register 2.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO	**End2End TLP Prefix Blocking Field (EE_TLP_PREFIX_EN):** End2End TLP Prefixes Blocking
14:13	0h RO	**OBFF Enable Field (OBFF_EN):** OBFF Enable
12:11	0h RO	**Reserved**
10	0h RW	**LTR Mechanism Enable Field (LTR_MECH_EN):** LTR Mechanism Enable
9	0h RO	**IDO Based CPL Enable Field (IDO_CPL_EN):** IDO Completion Enable
8	0h RO	**IDO Based Request Enable Field (IDO_REQ_EN):** IDO Request Enable
7	0h RO	**Atomic OP Egress Blocking Field (ATM_OP_EGR_BLK):** Atomic Operation Egress Blocking
6	0h RO	**Atomic OP Req Enable Field (ATM_OP_REQ_EN):** Actomic Operation Requester Enable
5	0h RO	**ARI Fwd Enable Field (ARI_FWD_EN):** ARI Forwarding Enable
4	0h RW	**CPL Timeout Disable Field (CPL_TO_DIS):** Completion Timeout Disable Support
3:0	0h RW	**CPL Timeout Value Field (CPL_TO_VAL):** Completion Timeout Value

21.1.18 Power Management Capability ID (POWERCAPID) — Offset 80h

Power Management Capability ID register points to next capability structure and power management capability with power management capabilities register for PME support and version.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 80h	48030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	09h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	**Reserved**
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	00h RO	**Next Cap Field (NXTCAP):** Next Capability: Points to the next capability structure.
7:0	01h RO	**Power Capability ID Field (POWER_CAP):** Power Management Capability: Indicates this is power management capability

21.1.19 Power Management Control and Status Register (PMECTRLSTATUS) — Offset 84h

Power Management Control and Status register to set and read PME status PME enable No Soft reset and power state.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 84h	00000008h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW/1C/P	**PME Status Field (PMESTATUS):** PME Status
14:9	0h RO	**Reserved**
8	0h RW/P	**PME Enable Field (PMEENABLE):** PME Enable
7:4	0h RO	**Reserved**
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	**Reserved**
1:0	0h RW	**Power State Field (POWERSTATE):** Power State: This field is used both to determine the current power state and to set a new power state

21.1.20 PCI Device Idle Vendor Capability Register (PCIDEVIDLE_CAP_RECORD) — Offset 90h

PCI Device Vendor Specific Capability register defines Vendor specific Capability ID revision length next capability and CAPID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 90h	F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision IDField (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	00h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	09h RO	**Capability ID Field (CAPID):** Capability ID

21.1.21 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG) — Offset 94h

Extended Vendor Capability register for VSEC Length revision and ID.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 94h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	0010h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

21.1.22 Software LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) — Offset 98h

Software Location Pointer in MMIO space as an offset specified by BAR.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

21.1.23 Device Idle Pointer Register (DEVICE_IDLE_POINTER_REG) — Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Bar num: Indicates that the D0i3 MMIO location is always at BAR0
0	0h RO	**D0i3 Valid Field (VALID):** Valid: This value is reflected from the D0i3 valid strap at the top level.

21.1.24 D0i3 and Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG) — Offset A0h

D0idle_Max_Power_On_Latency register set at boot and Power control enable register to enable communication with the PGCB block below the Bridge.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + A0h	00000800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW/P	**HAE Field (HAE):** Hardware Autonomous Enable
20	0h RO	**Reserved**
19	0h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If ?1? then the function will power gate when idle and the DevIdle register (DevIdleC[2] = ?1?) is set.
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If ?1? then function will power gate when idle and the PMCSR[1:0] register in the function =?11? (D3).
15:13	0h RO	**Reserved**
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	000h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency value

21.1.25 General Purpose Read Write Register1 (GEN_PCI_REGRW1) — Offset B0h

General Purpose PCI Read Write Register1.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**General Purpose Read Write:** Spare Register Bit available for General Purpose
30	0h RW	**PM_Override_Power_On:** 1'b0: No override 1'b1: Disable low power mode entry
29	0h RW	**PM_Override_Force_Clock_On:** 1'b0: No override 1'b1: Disable clock gating during low power mode
28	0h RW	**General Purpose Read Write:** Spare Register Bit available for General Purpose
27	0h RW	**CG_Disable_MAC:** 1'b0: Enable MAC Clock Gating 1'b1: Disable MAC Clock Gating
26	0h RW	**MGBE_PushPull_MDIO:** 1'b0: MDIO is open drain 1'b1: MDIO is push pull
25:0	0h RW	**General Purpose Read Write:** Spare Register Bit available for General Purpose

21.1.26 General Purpose Input Register (GEN_INPUT_REG) — Offset C0h

General Purpose Input Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register: This register value reflects the value of GEN_REG_INPUT_RW

21.1.27 MSI Capability Register (MSI_CAP_REG) — Offset D0h

MSI Capability Register.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D0h	01800005h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	1h RO	**Per Vector Masking Capability Field (PER_VECTOR_MSK_CAP):** Per Vector Masking Capability
23	1h RO	**MSI Capability Field (MSI_CAP_64B):** 64 bit message address capability
22:20	0h RW	**Multi Message En Field (MUL_MSG_EN):** Multiple Message Enable
19:17	0h RO	**Multi Message Cap Field (MUL_MSG_CAP):** Multiple Message Capable
16	0h RW	**MSI Enable Field (MSG_MSI_ENABLE):** MSI Enable
15:8	00h RO	**Next Pointer Field (MSG_NXT_PTR):** Next Capability Pointer
7:0	05h RO	**MSI Capability Field (MSG_CAP_ID):** MSI Capability ID

21.1.28 MSI Message Low Address (MSI_ADDR_LOW) — Offset D4h

MSI Message Low Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**MSI Message Low Address Field (MSI_ADDR_LOW):** MSI Message Low Address

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RO	**Reserved**

21.1.29 MSI Message High Address (MSI_ADDR_HIGH) — Offset D8h

MSI Message High Address.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + D8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Message High Address Field (MSI_ADDR_HIGH):** MSI Message High Address

21.1.30 MSI Message Data (MSI_MSG_DATA) — Offset DCh

MSI Message Data.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**MSI Message Data Field (MSI_MSG_DATA):** MSI Message Data

21.1.31 MSI Mask Register (MSI_MASK) — Offset E0h

MSI Mask bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + E0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MSI Mask Field (MSI_MASK):** MSI Mask bits

21.1.32 MSI Pending Register (MSI_PENDING) — Offset E4h

MSI Pending bits.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MSI Pending Field (MSI_PENDING):** MSI Pending bits

21.1.33 Manufacturers ID (MANID) — Offset F8h

Manufacturers ID register

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:30, F:4] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/P	**Manufacturers ID Field (MANID):** Manufacturer ID: Default value comes from straps.

21.2 GbE Controller Memory Mapped Registers Summary

Note: These registers are only applicable for the Intel Atom® x7000 processor series.

These are the I/O Registers in Memory Space for this Function that are accessible to BIOS and software running on the Host Root (RS0) processor. The Base Address Register (BAR) is located at offset 10h in PCI Configuration Space.

Table 44. Summary of GbE Controller Memory Mapped Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	MAC_CONFIGURATION DWC_ETHER_QOS (MAC_CONFIGURATION)	00000000h
4h	4	MAC_EXT_CONFIGURATION DWC_ETHER_QOS (MAC_EXT_CONFIGURATION)	00000000h
8h	4	MAC_PACKET_FILTER DWC_ETHER_QOS (MAC_PACKET_FILTER)	00000000h
Ch	4	MAC_WATCHDOG_TIMEOUT DWC_ETHER_QOS (MAC_WATCHDOG_TIMEOUT)	00000000h
10h	4	MAC_HASH_TABLE_REG0 DWC_ETHER_QOS (MAC_HASH_TABLE_REG0)	00000000h
14h	4	MAC_HASH_TABLE_REG1 DWC_ETHER_QOS (MAC_HASH_TABLE_REG1)	00000000h
50h	4	MAC_VLAN_TAG_CTRL DWC_ETHER_QOS (MAC_VLAN_TAG_CTRL)	00000000h
54h	4	MAC_VLAN_TAG_DATA DWC_ETHER_QOS (MAC_VLAN_TAG_DATA)	00000000h
58h	4	MAC_VLAN_HASH_TABLE DWC_ETHER_QOS (MAC_VLAN_HASH_TABLE)	00000000h
60h	4	MAC_VLAN_INCL DWC_ETHER_QOS (MAC_VLAN_INCL)	00000000h
64h	4	MAC_INNER_VLAN_INCL DWC_ETHER_QOS (MAC_INNER_VLAN_INCL)	00000000h
70h	4	MAC_Q0_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q0_TX_FLOW_CTRL)	00000000h
74h	4	MAC_Q1_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q1_TX_FLOW_CTRL)	00000000h
78h	4	MAC_Q2_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q2_TX_FLOW_CTRL)	00000000h
7Ch	4	MAC_Q3_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q3_TX_FLOW_CTRL)	00000000h
80h	4	MAC_Q4_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q4_TX_FLOW_CTRL)	00000000h
84h	4	MAC_Q5_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q5_TX_FLOW_CTRL)	00000000h
90h	4	MAC_RX_FLOW_CTRL DWC_ETHER_QOS (MAC_RX_FLOW_CTRL)	00000000h
94h	4	MAC_RXQ_CTRL4 DWC_ETHER_QOS (MAC_RXQ_CTRL4)	00000000h
98h	4	MAC_TXQ_PRTY_MAP0 DWC_ETHER_QOS (MAC_TXQ_PRTY_MAP0)	00000000h
A0h	4	MAC_RXQ_CTRL0 DWC_ETHER_QOS (MAC_RXQ_CTRL0)	00000000h
A4h	4	MAC_RXQ_CTRL1 DWC_ETHER_QOS (MAC_RXQ_CTRL1)	00000000h
A8h	4	MAC_RXQ_CTRL2 DWC_ETHER_QOS (MAC_RXQ_CTRL2)	00000000h
ACh	4	MAC_RXQ_CTRL3 DWC_ETHER_QOS (MAC_RXQ_CTRL3)	00000000h
B0h	4	MAC_INTERRUPT_STATUS DWC_ETHER_QOS (MAC_INTERRUPT_STATUS)	00000000h
B4h	4	MAC_INTERRUPT_ENABLE DWC_ETHER_QOS (MAC_INTERRUPT_ENABLE)	00000000h
B8h	4	MAC_RX_TX_STATUS DWC_ETHER_QOS (MAC_RX_TX_STATUS)	00000000h
C0h	4	MAC_PMT_CONTROL_STATUS DWC_ETHER_QOS (MAC_PMT_CONTROL_STATUS)	00000000h
C4h	4	MAC_RWK_PACKET_FILTER DWC_ETHER_QOS (MAC_RWK_PACKET_FILTER)	00000000h
D0h	4	MAC_LPI_CONTROL_STATUS DWC_ETHER_QOS (MAC_LPI_CONTROL_STATUS)	00000000h
D4h	4	MAC_LPI_TIMERS_CONTROL DWC_ETHER_QOS (MAC_LPI_TIMERS_CONTROL)	03E80000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D8h	4	MAC_LPI_ENTRY_TIMER DWC_ETHER_QOS (MAC_LPI_ENTRY_TIMER)	00000000h
DCh	4	MAC_1US_TIC_COUNTER DWC_ETHER_QOS (MAC_1US_TIC_COUNTER)	00000063h
F8h	4	MAC_PHYIF_CONTROL_STATUS DWC_ETHER_QOS (MAC_PHYIF_CONTROL_STATUS)	00000000h
110h	4	MAC_VERSION DWC_ETHER_QOS (MAC_VERSION)	00005151h
114h	4	MAC_DEBUG DWC_ETHER_QOS (MAC_DEBUG)	00000000h
11Ch	4	MAC_HW_FEATURE0 DWC_ETHER_QOS (MAC_HW_FEATURE0)	0EFD73F7h
120h	4	MAC_HW_FEATURE1 DWC_ETHER_QOS (MAC_HW_FEATURE1)	119F79C8h
124h	4	MAC_HW_FEATURE2 DWC_ETHER_QOS (MAC_HW_FEATURE2)	220C50C5h
128h	4	MAC_HW_FEATURE3 DWC_ETHER_QOS (MAC_HW_FEATURE3)	3C390231h
140h	4	MAC_DPP_FSM_INTERRUPT_STATUS DWC_ETHER_QOS (MAC_DPP_FSM_INTERRUPT_STATUS)	00000000h
144h	4	MAC_AXI_SLV_DPE_ADDR_STATUS DWC_ETHER_QOS (MAC_AXI_SLV_DPE_ADDR_STATUS)	00000000h
148h	4	MAC_FSM_CONTROL DWC_ETHER_QOS (MAC_FSM_CONTROL)	00000000h
14Ch	4	MAC_FSM_ACT_TIMER DWC_ETHER_QOS (MAC_FSM_ACT_TIMER)	00000000h
150h	4	SNPS_SCS_REG1 DWC_ETHER_QOS (SNPS_SCS_REG1)	00000000h
200h	4	MAC_MDIO_ADDRESS DWC_ETHER_QOS (MAC_MDIO_ADDRESS)	00000000h
204h	4	MAC_MDIO_DATA DWC_ETHER_QOS (MAC_MDIO_DATA)	00000000h
208h	4	MAC_GPIO_CONTROL DWC_ETHER_QOS (MAC_GPIO_CONTROL)	00000000h
20Ch	4	MAC_GPIO_STATUS DWC_ETHER_QOS (MAC_GPIO_STATUS)	00000000h
210h	4	MAC_ARP_ADDRESS DWC_ETHER_QOS (MAC_ARP_ADDRESS)	00000000h
230h	4	MAC_CSR_SW_CTRL DWC_ETHER_QOS (MAC_CSR_SW_CTRL)	00000000h
234h	4	MAC_FPE_CTRL_STS DWC_ETHER_QOS (MAC_FPE_CTRL_STS)	00000000h
238h	4	MAC_EXT_CFG1 DWC_ETHER_QOS (MAC_EXT_CFG1)	00000002h
240h	4	MAC_PRESN_TIME_NS DWC_ETHER_QOS (MAC_PRESN_TIME_NS)	00000000h
244h	4	MAC_PRESN_TIME_UPDT DWC_ETHER_QOS (MAC_PRESN_TIME_UPDT)	00000000h
300h	4	MAC_ADDRESS0_HIGH DWC_ETHER_QOS (MAC_ADDRESS0_HIGH)	8000FFFFh
304h	4	MAC_ADDRESS0_LOW DWC_ETHER_QOS (MAC_ADDRESS0_LOW)	FFFFFFFFh
308h	4	MAC_ADDRESS1_HIGH DWC_ETHER_QOS (MAC_ADDRESS1_HIGH)	0000FFFFh
30Ch	4	MAC_ADDRESS1_LOW DWC_ETHER_QOS (MAC_ADDRESS1_LOW)	FFFFFFFFh
310h	4	MAC_ADDRESS2_HIGH DWC_ETHER_QOS (MAC_ADDRESS2_HIGH)	0000FFFFh
314h	4	MAC_ADDRESS2_LOW DWC_ETHER_QOS (MAC_ADDRESS2_LOW)	FFFFFFFFh
318h	4	MAC_ADDRESS3_HIGH DWC_ETHER_QOS (MAC_ADDRESS3_HIGH)	0000FFFFh
31Ch	4	MAC_ADDRESS3_LOW DWC_ETHER_QOS (MAC_ADDRESS3_LOW)	FFFFFFFFh
320h	4	MAC_ADDRESS4_HIGH DWC_ETHER_QOS (MAC_ADDRESS4_HIGH)	0000FFFFh
324h	4	MAC_ADDRESS4_LOW DWC_ETHER_QOS (MAC_ADDRESS4_LOW)	FFFFFFFFh
328h	4	MAC_ADDRESS5_HIGH DWC_ETHER_QOS (MAC_ADDRESS5_HIGH)	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
32Ch	4	MAC_ADDRESS5_LOW DWC_ETHER_QOS (MAC_ADDRESS5_LOW)	FFFFFFFFh
330h	4	MAC_ADDRESS6_HIGH DWC_ETHER_QOS (MAC_ADDRESS6_HIGH)	0000FFFFh
334h	4	MAC_ADDRESS6_LOW DWC_ETHER_QOS (MAC_ADDRESS6_LOW)	FFFFFFFFh
338h	4	MAC_ADDRESS7_HIGH DWC_ETHER_QOS (MAC_ADDRESS7_HIGH)	0000FFFFh
33Ch	4	MAC_ADDRESS7_LOW DWC_ETHER_QOS (MAC_ADDRESS7_LOW)	FFFFFFFFh
340h	4	MAC_ADDRESS8_HIGH DWC_ETHER_QOS (MAC_ADDRESS8_HIGH)	0000FFFFh
344h	4	MAC_ADDRESS8_LOW DWC_ETHER_QOS (MAC_ADDRESS8_LOW)	FFFFFFFFh
348h	4	MAC_ADDRESS9_HIGH DWC_ETHER_QOS (MAC_ADDRESS9_HIGH)	0000FFFFh
34Ch	4	MAC_ADDRESS9_LOW DWC_ETHER_QOS (MAC_ADDRESS9_LOW)	FFFFFFFFh
350h	4	MAC_ADDRESS10_HIGH DWC_ETHER_QOS (MAC_ADDRESS10_HIGH)	0000FFFFh
354h	4	MAC_ADDRESS10_LOW DWC_ETHER_QOS (MAC_ADDRESS10_LOW)	FFFFFFFFh
358h	4	MAC_ADDRESS11_HIGH DWC_ETHER_QOS (MAC_ADDRESS11_HIGH)	0000FFFFh
35Ch	4	MAC_ADDRESS11_LOW DWC_ETHER_QOS (MAC_ADDRESS11_LOW)	FFFFFFFFh
360h	4	MAC_ADDRESS12_HIGH DWC_ETHER_QOS (MAC_ADDRESS12_HIGH)	0000FFFFh
364h	4	MAC_ADDRESS12_LOW DWC_ETHER_QOS (MAC_ADDRESS12_LOW)	FFFFFFFFh
368h	4	MAC_ADDRESS13_HIGH DWC_ETHER_QOS (MAC_ADDRESS13_HIGH)	0000FFFFh
36Ch	4	MAC_ADDRESS13_LOW DWC_ETHER_QOS (MAC_ADDRESS13_LOW)	FFFFFFFFh
370h	4	MAC_ADDRESS14_HIGH DWC_ETHER_QOS (MAC_ADDRESS14_HIGH)	0000FFFFh
374h	4	MAC_ADDRESS14_LOW DWC_ETHER_QOS (MAC_ADDRESS14_LOW)	FFFFFFFFh
378h	4	MAC_ADDRESS15_HIGH DWC_ETHER_QOS (MAC_ADDRESS15_HIGH)	0000FFFFh
37Ch	4	MAC_ADDRESS15_LOW DWC_ETHER_QOS (MAC_ADDRESS15_LOW)	FFFFFFFFh
380h	4	MAC_ADDRESS16_HIGH DWC_ETHER_QOS (MAC_ADDRESS16_HIGH)	0000FFFFh
384h	4	MAC_ADDRESS16_LOW DWC_ETHER_QOS (MAC_ADDRESS16_LOW)	FFFFFFFFh
388h	4	MAC_ADDRESS17_HIGH DWC_ETHER_QOS (MAC_ADDRESS17_HIGH)	0000FFFFh
38Ch	4	MAC_ADDRESS17_LOW DWC_ETHER_QOS (MAC_ADDRESS17_LOW)	FFFFFFFFh
390h	4	MAC_ADDRESS18_HIGH DWC_ETHER_QOS (MAC_ADDRESS18_HIGH)	0000FFFFh
394h	4	MAC_ADDRESS18_LOW DWC_ETHER_QOS (MAC_ADDRESS18_LOW)	FFFFFFFFh
398h	4	MAC_ADDRESS19_HIGH DWC_ETHER_QOS (MAC_ADDRESS19_HIGH)	0000FFFFh
39Ch	4	MAC_ADDRESS19_LOW DWC_ETHER_QOS (MAC_ADDRESS19_LOW)	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3A0h	4	MAC_ADDRESS20_HIGH DWC_ETHER_QOS (MAC_ADDRESS20_HIGH)	0000FFFFh
3A4h	4	MAC_ADDRESS20_LOW DWC_ETHER_QOS (MAC_ADDRESS20_LOW)	FFFFFFFFh
3A8h	4	MAC_ADDRESS21_HIGH DWC_ETHER_QOS (MAC_ADDRESS21_HIGH)	0000FFFFh
3ACh	4	MAC_ADDRESS21_LOW DWC_ETHER_QOS (MAC_ADDRESS21_LOW)	FFFFFFFFh
3B0h	4	MAC_ADDRESS22_HIGH DWC_ETHER_QOS (MAC_ADDRESS22_HIGH)	0000FFFFh
3B4h	4	MAC_ADDRESS22_LOW DWC_ETHER_QOS (MAC_ADDRESS22_LOW)	FFFFFFFFh
3B8h	4	MAC_ADDRESS23_HIGH DWC_ETHER_QOS (MAC_ADDRESS23_HIGH)	0000FFFFh
3BCh	4	MAC_ADDRESS23_LOW DWC_ETHER_QOS (MAC_ADDRESS23_LOW)	FFFFFFFFh
3C0h	4	MAC_ADDRESS24_HIGH DWC_ETHER_QOS (MAC_ADDRESS24_HIGH)	0000FFFFh
3C4h	4	MAC_ADDRESS24_LOW DWC_ETHER_QOS (MAC_ADDRESS24_LOW)	FFFFFFFFh
3C8h	4	MAC_ADDRESS25_HIGH DWC_ETHER_QOS (MAC_ADDRESS25_HIGH)	0000FFFFh
3CCh	4	MAC_ADDRESS25_LOW DWC_ETHER_QOS (MAC_ADDRESS25_LOW)	FFFFFFFFh
3D0h	4	MAC_ADDRESS26_HIGH DWC_ETHER_QOS (MAC_ADDRESS26_HIGH)	0000FFFFh
3D4h	4	MAC_ADDRESS26_LOW DWC_ETHER_QOS (MAC_ADDRESS26_LOW)	FFFFFFFFh
3D8h	4	MAC_ADDRESS27_HIGH DWC_ETHER_QOS (MAC_ADDRESS27_HIGH)	0000FFFFh
3DCh	4	MAC_ADDRESS27_LOW DWC_ETHER_QOS (MAC_ADDRESS27_LOW)	FFFFFFFFh
3E0h	4	MAC_ADDRESS28_HIGH DWC_ETHER_QOS (MAC_ADDRESS28_HIGH)	0000FFFFh
3E4h	4	MAC_ADDRESS28_LOW DWC_ETHER_QOS (MAC_ADDRESS28_LOW)	FFFFFFFFh
3E8h	4	MAC_ADDRESS29_HIGH DWC_ETHER_QOS (MAC_ADDRESS29_HIGH)	0000FFFFh
3ECh	4	MAC_ADDRESS29_LOW DWC_ETHER_QOS (MAC_ADDRESS29_LOW)	FFFFFFFFh
3F0h	4	MAC_ADDRESS30_HIGH DWC_ETHER_QOS (MAC_ADDRESS30_HIGH)	0000FFFFh
3F4h	4	MAC_ADDRESS30_LOW DWC_ETHER_QOS (MAC_ADDRESS30_LOW)	FFFFFFFFh
3F8h	4	MAC_ADDRESS31_HIGH DWC_ETHER_QOS (MAC_ADDRESS31_HIGH)	0000FFFFh
3FCh	4	MAC_ADDRESS31_LOW DWC_ETHER_QOS (MAC_ADDRESS31_LOW)	FFFFFFFFh
400h	4	MAC_ADDRESS32_HIGH DWC_ETHER_QOS (MAC_ADDRESS32_HIGH)	0000FFFFh
404h	4	MAC_ADDRESS32_LOW DWC_ETHER_QOS (MAC_ADDRESS32_LOW)	FFFFFFFFh
408h	4	MAC_ADDRESS33_HIGH DWC_ETHER_QOS (MAC_ADDRESS33_HIGH)	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40Ch	4	MAC_ADDRESS33_LOW DWC_ETHER_QOS (MAC_ADDRESS33_LOW)	FFFFFFFFh
410h	4	MAC_ADDRESS34_HIGH DWC_ETHER_QOS (MAC_ADDRESS34_HIGH)	0000FFFFh
414h	4	MAC_ADDRESS34_LOW DWC_ETHER_QOS (MAC_ADDRESS34_LOW)	FFFFFFFFh
418h	4	MAC_ADDRESS35_HIGH DWC_ETHER_QOS (MAC_ADDRESS35_HIGH)	0000FFFFh
41Ch	4	MAC_ADDRESS35_LOW DWC_ETHER_QOS (MAC_ADDRESS35_LOW)	FFFFFFFFh
420h	4	MAC_ADDRESS36_HIGH DWC_ETHER_QOS (MAC_ADDRESS36_HIGH)	0000FFFFh
424h	4	MAC_ADDRESS36_LOW DWC_ETHER_QOS (MAC_ADDRESS36_LOW)	FFFFFFFFh
428h	4	MAC_ADDRESS37_HIGH DWC_ETHER_QOS (MAC_ADDRESS37_HIGH)	0000FFFFh
42Ch	4	MAC_ADDRESS37_LOW DWC_ETHER_QOS (MAC_ADDRESS37_LOW)	FFFFFFFFh
430h	4	MAC_ADDRESS38_HIGH DWC_ETHER_QOS (MAC_ADDRESS38_HIGH)	0000FFFFh
434h	4	MAC_ADDRESS38_LOW DWC_ETHER_QOS (MAC_ADDRESS38_LOW)	FFFFFFFFh
438h	4	MAC_ADDRESS39_HIGH DWC_ETHER_QOS (MAC_ADDRESS39_HIGH)	0000FFFFh
43Ch	4	MAC_ADDRESS39_LOW DWC_ETHER_QOS (MAC_ADDRESS39_LOW)	FFFFFFFFh
440h	4	MAC_ADDRESS40_HIGH DWC_ETHER_QOS (MAC_ADDRESS40_HIGH)	0000FFFFh
444h	4	MAC_ADDRESS40_LOW DWC_ETHER_QOS (MAC_ADDRESS40_LOW)	FFFFFFFFh
448h	4	MAC_ADDRESS41_HIGH DWC_ETHER_QOS (MAC_ADDRESS41_HIGH)	0000FFFFh
44Ch	4	MAC_ADDRESS41_LOW DWC_ETHER_QOS (MAC_ADDRESS41_LOW)	FFFFFFFFh
450h	4	MAC_ADDRESS42_HIGH DWC_ETHER_QOS (MAC_ADDRESS42_HIGH)	0000FFFFh
454h	4	MAC_ADDRESS42_LOW DWC_ETHER_QOS (MAC_ADDRESS42_LOW)	FFFFFFFFh
458h	4	MAC_ADDRESS43_HIGH DWC_ETHER_QOS (MAC_ADDRESS43_HIGH)	0000FFFFh
45Ch	4	MAC_ADDRESS43_LOW DWC_ETHER_QOS (MAC_ADDRESS43_LOW)	FFFFFFFFh
460h	4	MAC_ADDRESS44_HIGH DWC_ETHER_QOS (MAC_ADDRESS44_HIGH)	0000FFFFh
464h	4	MAC_ADDRESS44_LOW DWC_ETHER_QOS (MAC_ADDRESS44_LOW)	FFFFFFFFh
468h	4	MAC_ADDRESS45_HIGH DWC_ETHER_QOS (MAC_ADDRESS45_HIGH)	0000FFFFh
46Ch	4	MAC_ADDRESS45_LOW DWC_ETHER_QOS (MAC_ADDRESS45_LOW)	FFFFFFFFh
470h	4	MAC_ADDRESS46_HIGH DWC_ETHER_QOS (MAC_ADDRESS46_HIGH)	0000FFFFh
474h	4	MAC_ADDRESS46_LOW DWC_ETHER_QOS (MAC_ADDRESS46_LOW)	FFFFFFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
478h	4	MAC_ADDRESS47_HIGH DWC_ETHER_QOS (MAC_ADDRESS47_HIGH)	0000FFFFh
47Ch	4	MAC_ADDRESS47_LOW DWC_ETHER_QOS (MAC_ADDRESS47_LOW)	FFFFFFFFh
480h	4	MAC_ADDRESS48_HIGH DWC_ETHER_QOS (MAC_ADDRESS48_HIGH)	0000FFFFh
484h	4	MAC_ADDRESS48_LOW DWC_ETHER_QOS (MAC_ADDRESS48_LOW)	FFFFFFFFh
488h	4	MAC_ADDRESS49_HIGH DWC_ETHER_QOS (MAC_ADDRESS49_HIGH)	0000FFFFh
48Ch	4	MAC_ADDRESS49_LOW DWC_ETHER_QOS (MAC_ADDRESS49_LOW)	FFFFFFFFh
490h	4	MAC_ADDRESS50_HIGH DWC_ETHER_QOS (MAC_ADDRESS50_HIGH)	0000FFFFh
494h	4	MAC_ADDRESS50_LOW DWC_ETHER_QOS (MAC_ADDRESS50_LOW)	FFFFFFFFh
498h	4	MAC_ADDRESS51_HIGH DWC_ETHER_QOS (MAC_ADDRESS51_HIGH)	0000FFFFh
49Ch	4	MAC_ADDRESS51_LOW DWC_ETHER_QOS (MAC_ADDRESS51_LOW)	FFFFFFFFh
4A0h	4	MAC_ADDRESS52_HIGH DWC_ETHER_QOS (MAC_ADDRESS52_HIGH)	0000FFFFh
4A4h	4	MAC_ADDRESS52_LOW DWC_ETHER_QOS (MAC_ADDRESS52_LOW)	FFFFFFFFh
4A8h	4	MAC_ADDRESS53_HIGH DWC_ETHER_QOS (MAC_ADDRESS53_HIGH)	0000FFFFh
4ACh	4	MAC_ADDRESS53_LOW DWC_ETHER_QOS (MAC_ADDRESS53_LOW)	FFFFFFFFh
4B0h	4	MAC_ADDRESS54_HIGH DWC_ETHER_QOS (MAC_ADDRESS54_HIGH)	0000FFFFh
4B4h	4	MAC_ADDRESS54_LOW DWC_ETHER_QOS (MAC_ADDRESS54_LOW)	FFFFFFFFh
4B8h	4	MAC_ADDRESS55_HIGH DWC_ETHER_QOS (MAC_ADDRESS55_HIGH)	0000FFFFh
4BCh	4	MAC_ADDRESS55_LOW DWC_ETHER_QOS (MAC_ADDRESS55_LOW)	FFFFFFFFh
4C0h	4	MAC_ADDRESS56_HIGH DWC_ETHER_QOS (MAC_ADDRESS56_HIGH)	0000FFFFh
4C4h	4	MAC_ADDRESS56_LOW DWC_ETHER_QOS (MAC_ADDRESS56_LOW)	FFFFFFFFh
4C8h	4	MAC_ADDRESS57_HIGH DWC_ETHER_QOS (MAC_ADDRESS57_HIGH)	0000FFFFh
4CCh	4	MAC_ADDRESS57_LOW DWC_ETHER_QOS (MAC_ADDRESS57_LOW)	FFFFFFFFh
4D0h	4	MAC_ADDRESS58_HIGH DWC_ETHER_QOS (MAC_ADDRESS58_HIGH)	0000FFFFh
4D4h	4	MAC_ADDRESS58_LOW DWC_ETHER_QOS (MAC_ADDRESS58_LOW)	FFFFFFFFh
4D8h	4	MAC_ADDRESS59_HIGH DWC_ETHER_QOS (MAC_ADDRESS59_HIGH)	0000FFFFh
4DCh	4	MAC_ADDRESS59_LOW DWC_ETHER_QOS (MAC_ADDRESS59_LOW)	FFFFFFFFh
4E0h	4	MAC_ADDRESS60_HIGH DWC_ETHER_QOS (MAC_ADDRESS60_HIGH)	0000FFFFh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4E4h	4	MAC_ADDRESS60_LOW DWC_ETHER_QOS (MAC_ADDRESS60_LOW)	FFFFFFFFh
4E8h	4	MAC_ADDRESS61_HIGH DWC_ETHER_QOS (MAC_ADDRESS61_HIGH)	0000FFFFh
4ECh	4	MAC_ADDRESS61_LOW DWC_ETHER_QOS (MAC_ADDRESS61_LOW)	FFFFFFFFh
4F0h	4	MAC_ADDRESS62_HIGH DWC_ETHER_QOS (MAC_ADDRESS62_HIGH)	0000FFFFh
4F4h	4	MAC_ADDRESS62_LOW DWC_ETHER_QOS (MAC_ADDRESS62_LOW)	FFFFFFFFh
4F8h	4	MAC_ADDRESS63_HIGH DWC_ETHER_QOS (MAC_ADDRESS63_HIGH)	0000FFFFh
4FCh	4	MAC_ADDRESS63_LOW DWC_ETHER_QOS (MAC_ADDRESS63_LOW)	FFFFFFFFh
700h	4	MMC_CONTROL DWC_ETHER_QOS (MMC_CONTROL)	00000000h
704h	4	MMC_RX_INTERRUPT DWC_ETHER_QOS (MMC_RX_INTERRUPT)	00000000h
708h	4	MMC_TX_INTERRUPT DWC_ETHER_QOS (MMC_TX_INTERRUPT)	00000000h
70Ch	4	MMC_RX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_RX_INTERRUPT_MASK)	00000000h
710h	4	MMC_TX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_TX_INTERRUPT_MASK)	00000000h
714h	4	TX_OCTET_COUNT_GOOD_BAD DWC_ETHER_QOS (TX_OCTET_COUNT_GOOD_BAD)	00000000h
718h	4	TX_PACKET_COUNT_GOOD_BAD DWC_ETHER_QOS (TX_PACKET_COUNT_GOOD_BAD)	00000000h
71Ch	4	TX_BROADCAST_PACKETS_GOOD DWC_ETHER_QOS (TX_BROADCAST_PACKETS_GOOD)	00000000h
720h	4	TX_MULTICAST_PACKETS_GOOD DWC_ETHER_QOS (TX_MULTICAST_PACKETS_GOOD)	00000000h
724h	4	TX_64OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_64OCTETS_PACKETS_GOOD_BAD)	00000000h
728h	4	TX_65TO127OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_65TO127OCTETS_PACKETS_GOOD_BAD)	00000000h
72Ch	4	TX_128TO255OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_128TO255OCTETS_PACKETS_GOOD_BAD)	00000000h
730h	4	TX_256TO511OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_256TO511OCTETS_PACKETS_GOOD_BAD)	00000000h
734h	4	TX_512TO1023OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_512TO1023OCTETS_PACKETS_GOOD_BAD)	00000000h
738h	4	TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD)	00000000h
73Ch	4	TX_UNICAST_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_UNICAST_PACKETS_GOOD_BAD)	00000000h
740h	4	TX_MULTICAST_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_MULTICAST_PACKETS_GOOD_BAD)	00000000h
744h	4	TX_BROADCAST_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_BROADCAST_PACKETS_GOOD_BAD)	00000000h
748h	4	TX_UNDERFLOW_ERROR_PACKETS DWC_ETHER_QOS (TX_UNDERFLOW_ERROR_PACKETS)	00000000h
74Ch	4	TX_SINGLE_COLLISION_GOOD_PACKETS DWC_ETHER_QOS (TX_SINGLE_COLLISION_GOOD_PACKETS)	00000000h
750h	4	TX_MULTIPLE_COLLISION_GOOD_PACKETS DWC_ETHER_QOS (TX_MULTIPLE_COLLISION_GOOD_PACKETS)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
754h	4	TX_DEFERRED_PACKETS DWC_ETHER_QOS (TX_DEFERRED_PACKETS)	00000000h
758h	4	TX_LATE_COLLISION_PACKETS DWC_ETHER_QOS (TX_LATE_COLLISION_PACKETS)	00000000h
75Ch	4	TX_EXCESSIVE_COLLISION_PACKETS DWC_ETHER_QOS (TX_EXCESSIVE_COLLISION_PACKETS)	00000000h
760h	4	TX_CARRIER_ERROR_PACKETS DWC_ETHER_QOS (TX_CARRIER_ERROR_PACKETS)	00000000h
764h	4	TX_OCTET_COUNT_GOOD DWC_ETHER_QOS (TX_OCTET_COUNT_GOOD)	00000000h
768h	4	TX_PACKET_COUNT_GOOD DWC_ETHER_QOS (TX_PACKET_COUNT_GOOD)	00000000h
76Ch	4	TX_EXCESSIVE_DEFERRAL_ERROR DWC_ETHER_QOS (TX_EXCESSIVE_DEFERRAL_ERROR)	00000000h
770h	4	TX_PAUSE_PACKETS DWC_ETHER_QOS (TX_PAUSE_PACKETS)	00000000h
774h	4	TX_VLAN_PACKETS_GOOD DWC_ETHER_QOS (TX_VLAN_PACKETS_GOOD)	00000000h
778h	4	TX_OSIZE_PACKETS_GOOD DWC_ETHER_QOS (TX_OSIZE_PACKETS_GOOD)	00000000h
780h	4	RX_PACKETS_COUNT_GOOD_BAD DWC_ETHER_QOS (RX_PACKETS_COUNT_GOOD_BAD)	00000000h
784h	4	RX_OCTET_COUNT_GOOD_BAD DWC_ETHER_QOS (RX_OCTET_COUNT_GOOD_BAD)	00000000h
788h	4	RX_OCTET_COUNT_GOOD DWC_ETHER_QOS (RX_OCTET_COUNT_GOOD)	00000000h
78Ch	4	RX_BROADCAST_PACKETS_GOOD DWC_ETHER_QOS (RX_BROADCAST_PACKETS_GOOD)	00000000h
790h	4	RX_MULTICAST_PACKETS_GOOD DWC_ETHER_QOS (RX_MULTICAST_PACKETS_GOOD)	00000000h
794h	4	RX_CRC_ERROR_PACKETS DWC_ETHER_QOS (RX_CRC_ERROR_PACKETS)	00000000h
798h	4	RX_ALIGNMENT_ERROR_PACKETS DWC_ETHER_QOS (RX_ALIGNMENT_ERROR_PACKETS)	00000000h
79Ch	4	RX_RUNT_ERROR_PACKETS DWC_ETHER_QOS (RX_RUNT_ERROR_PACKETS)	00000000h
7A0h	4	RX_JABBER_ERROR_PACKETS DWC_ETHER_QOS (RX_JABBER_ERROR_PACKETS)	00000000h
7A4h	4	RX_UNDERSIZE_PACKETS_GOOD DWC_ETHER_QOS (RX_UNDERSIZE_PACKETS_GOOD)	00000000h
7A8h	4	RX_OVERSIZE_PACKETS_GOOD DWC_ETHER_QOS (RX_OVERSIZE_PACKETS_GOOD)	00000000h
7ACh	4	RX_64OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_64OCTETS_PACKETS_GOOD_BAD)	00000000h
7B0h	4	RX_65TO127OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_65TO127OCTETS_PACKETS_GOOD_BAD)	00000000h
7B4h	4	RX_128TO255OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_128TO255OCTETS_PACKETS_GOOD_BAD)	00000000h
7B8h	4	RX_256TO511OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_256TO511OCTETS_PACKETS_GOOD_BAD)	00000000h
7BCh	4	RX_512TO1023OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_512TO1023OCTETS_PACKETS_GOOD_BAD)	00000000h
7C0h	4	RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7C4h	4	RX_UNICAST_PACKETS_GOOD DWC_ETHER_QOS (RX_UNICAST_PACKETS_GOOD)	00000000h
7C8h	4	RX_LENGTH_ERROR_PACKETS DWC_ETHER_QOS (RX_LENGTH_ERROR_PACKETS)	00000000h
7CCh	4	RX_OUT_OF_RANGE_TYPE_PACKETS DWC_ETHER_QOS (RX_OUT_OF_RANGE_TYPE_PACKETS)	00000000h
7D0h	4	RX_PAUSE_PACKETS DWC_ETHER_QOS (RX_PAUSE_PACKETS)	00000000h
7D4h	4	RX_FIFO_OVERFLOW_PACKETS DWC_ETHER_QOS (RX_FIFO_OVERFLOW_PACKETS)	00000000h
7D8h	4	RX_VLAN_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_VLAN_PACKETS_GOOD_BAD)	00000000h
7DCh	4	RX_WATCHDOG_ERROR_PACKETS DWC_ETHER_QOS (RX_WATCHDOG_ERROR_PACKETS)	00000000h
7E0h	4	RX_RECEIVE_ERROR_PACKETS DWC_ETHER_QOS (RX_RECEIVE_ERROR_PACKETS)	00000000h
7E4h	4	RX_CONTROL_PACKETS_GOOD DWC_ETHER_QOS (RX_CONTROL_PACKETS_GOOD)	00000000h
7ECh	4	TX_LPI_USEC_CNTR DWC_ETHER_QOS (TX_LPI_USEC_CNTR)	00000000h
7F0h	4	TX_LPI_TRAN_CNTR DWC_ETHER_QOS (TX_LPI_TRAN_CNTR)	00000000h
7F4h	4	RX_LPI_USEC_CNTR DWC_ETHER_QOS (RX_LPI_USEC_CNTR)	00000000h
7F8h	4	RX_LPI_TRAN_CNTR DWC_ETHER_QOS (RX_LPI_TRAN_CNTR)	00000000h
800h	4	MMC_IPC_RX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_IPC_RX_INTERRUPT_MASK)	00000000h
808h	4	MMC_IPC_RX_INTERRUPT DWC_ETHER_QOS (MMC_IPC_RX_INTERRUPT)	00000000h
810h	4	RXIPV4_GOOD_PACKETS DWC_ETHER_QOS (RXIPV4_GOOD_PACKETS)	00000000h
814h	4	RXIPV4_HEADER_ERROR_PACKETS DWC_ETHER_QOS (RXIPV4_HEADER_ERROR_PACKETS)	00000000h
818h	4	RXIPV4_NO_PAYLOAD_PACKETS DWC_ETHER_QOS (RXIPV4_NO_PAYLOAD_PACKETS)	00000000h
81Ch	4	RXIPV4_FRAGMENTED_PACKETS DWC_ETHER_QOS (RXIPV4_FRAGMENTED_PACKETS)	00000000h
820h	4	RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS DWC_ETHER_QOS (RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS)	00000000h
824h	4	RXIPV6_GOOD_PACKETS DWC_ETHER_QOS (RXIPV6_GOOD_PACKETS)	00000000h
828h	4	RXIPV6_HEADER_ERROR_PACKETS DWC_ETHER_QOS (RXIPV6_HEADER_ERROR_PACKETS)	00000000h
82Ch	4	RXIPV6_NO_PAYLOAD_PACKETS DWC_ETHER_QOS (RXIPV6_NO_PAYLOAD_PACKETS)	00000000h
830h	4	RXUDP_GOOD_PACKETS DWC_ETHER_QOS (RXUDP_GOOD_PACKETS)	00000000h
834h	4	RXUDP_ERROR_PACKETS DWC_ETHER_QOS (RXUDP_ERROR_PACKETS)	00000000h
838h	4	RXTCP_GOOD_PACKETS DWC_ETHER_QOS (RXTCP_GOOD_PACKETS)	00000000h
83Ch	4	RXTCP_ERROR_PACKETS DWC_ETHER_QOS (RXTCP_ERROR_PACKETS)	00000000h
840h	4	RXICMP_GOOD_PACKETS DWC_ETHER_QOS (RXICMP_GOOD_PACKETS)	00000000h
844h	4	RXICMP_ERROR_PACKETS DWC_ETHER_QOS (RXICMP_ERROR_PACKETS)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
850h	4	RXIPV4_GOOD_OCTETS DWC_ETHER_QOS (RXIPV4_GOOD_OCTETS)	00000000h
854h	4	RXIPV4_HEADER_ERROR_OCTETS DWC_ETHER_QOS (RXIPV4_HEADER_ERROR_OCTETS)	00000000h
858h	4	RXIPV4_NO_PAYLOAD_OCTETS DWC_ETHER_QOS (RXIPV4_NO_PAYLOAD_OCTETS)	00000000h
85Ch	4	RXIPV4_FRAGMENTED_OCTETS DWC_ETHER_QOS (RXIPV4_FRAGMENTED_OCTETS)	00000000h
860h	4	RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS DWC_ETHER_QOS (RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS)	00000000h
864h	4	RXIPV6_GOOD_OCTETS DWC_ETHER_QOS (RXIPV6_GOOD_OCTETS)	00000000h
868h	4	RXIPV6_HEADER_ERROR_OCTETS DWC_ETHER_QOS (RXIPV6_HEADER_ERROR_OCTETS)	00000000h
86Ch	4	RXIPV6_NO_PAYLOAD_OCTETS DWC_ETHER_QOS (RXIPV6_NO_PAYLOAD_OCTETS)	00000000h
870h	4	RXUDP_GOOD_OCTETS DWC_ETHER_QOS (RXUDP_GOOD_OCTETS)	00000000h
874h	4	RXUDP_ERROR_OCTETS DWC_ETHER_QOS (RXUDP_ERROR_OCTETS)	00000000h
878h	4	RXTCP_GOOD_OCTETS DWC_ETHER_QOS (RXTCP_GOOD_OCTETS)	00000000h
87Ch	4	RXTCP_ERROR_OCTETS DWC_ETHER_QOS (RXTCP_ERROR_OCTETS)	00000000h
880h	4	RXICMP_GOOD_OCTETS DWC_ETHER_QOS (RXICMP_GOOD_OCTETS)	00000000h
884h	4	RXICMP_ERROR_OCTETS DWC_ETHER_QOS (RXICMP_ERROR_OCTETS)	00000000h
8A0h	4	MMC_FPE_TX_INTERRUPT DWC_ETHER_QOS (MMC_FPE_TX_INTERRUPT)	00000000h
8A4h	4	MMC_FPE_TX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_FPE_TX_INTERRUPT_MASK)	00000000h
8A8h	4	MMC_TX_FPE_FRAGMENT_CNTR DWC_ETHER_QOS (MMC_TX_FPE_FRAGMENT_CNTR)	00000000h
8ACh	4	MMC_TX_HOLD_REQ_CNTR DWC_ETHER_QOS (MMC_TX_HOLD_REQ_CNTR)	00000000h
8C0h	4	MMC_FPE_RX_INTERRUPT DWC_ETHER_QOS (MMC_FPE_RX_INTERRUPT)	00000000h
8C4h	4	MMC_FPE_RX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_FPE_RX_INTERRUPT_MASK)	00000000h
8C8h	4	MMC_RX_PACKET_ASSEMBLY_ERR_CNTR DWC_ETHER_QOS (MMC_RX_PACKET_ASSEMBLY_ERR_CNTR)	00000000h
8CCh	4	MMC_RX_PACKET_SMD_ERR_CNTR DWC_ETHER_QOS (MMC_RX_PACKET_SMD_ERR_CNTR)	00000000h
8D0h	4	MMC_RX_PACKET_ASSEMBLY_OK_CNTR DWC_ETHER_QOS (MMC_RX_PACKET_ASSEMBLY_OK_CNTR)	00000000h
8D4h	4	MMC_RX_FPE_FRAGMENT_CNTR DWC_ETHER_QOS (MMC_RX_FPE_FRAGMENT_CNTR)	00000000h
900h	4	MAC_L3_L4_CONTROL0 DWC_ETHER_QOS (MAC_L3_L4_CONTROL0)	00000000h
904h	4	MAC_LAYER4_ADDRESS0 DWC_ETHER_QOS (MAC_LAYER4_ADDRESS0)	00000000h
910h	4	MAC_LAYER3_ADDR0_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR0_REG0)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
914h	4	MAC_LAYER3_ADDR1_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR1_REG0)	00000000h
918h	4	MAC_LAYER3_ADDR2_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR2_REG0)	00000000h
91Ch	4	MAC_LAYER3_ADDR3_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR3_REG0)	00000000h
930h	4	MAC_L3_L4_CONTROL1 DWC_ETHER_QOS (MAC_L3_L4_CONTROL1)	00000000h
934h	4	MAC_LAYER4_ADDRESS1 DWC_ETHER_QOS (MAC_LAYER4_ADDRESS1)	00000000h
940h	4	MAC_LAYER3_ADDR0_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR0_REG1)	00000000h
944h	4	MAC_LAYER3_ADDR1_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR1_REG1)	00000000h
948h	4	MAC_LAYER3_ADDR2_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR2_REG1)	00000000h
94Ch	4	MAC_LAYER3_ADDR3_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR3_REG1)	00000000h
B00h	4	MAC_TIMESTAMP_CONTROL DWC_ETHER_QOS (MAC_TIMESTAMP_CONTROL)	00002000h
B04h	4	MAC_SUB_SECOND_INCREMENT DWC_ETHER_QOS (MAC_SUB_SECOND_INCREMENT)	00000000h
B08h	4	MAC_SYSTEM_TIME_SECONDS DWC_ETHER_QOS (MAC_SYSTEM_TIME_SECONDS)	00000000h
B0Ch	4	MAC_SYSTEM_TIME_NANOSECONDS DWC_ETHER_QOS (MAC_SYSTEM_TIME_NANOSECONDS)	00000000h
B10h	4	MAC_SYSTEM_TIME_SECONDS_UPDATE DWC_ETHER_QOS (MAC_SYSTEM_TIME_SECONDS_UPDATE)	00000000h
B14h	4	MAC_SYSTEM_TIME_NANOSECONDS_UPDATE DWC_ETHER_QOS (MAC_SYSTEM_TIME_NANOSECONDS_UPDATE)	00000000h
B18h	4	MAC_TIMESTAMP_ADDEND DWC_ETHER_QOS (MAC_TIMESTAMP_ADDEND)	00000000h
B1Ch	4	MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS DWC_ETHER_QOS (MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS)	00000000h
B20h	4	MAC_TIMESTAMP_STATUS DWC_ETHER_QOS (MAC_TIMESTAMP_STATUS)	00000000h
B30h	4	MAC_TX_TIMESTAMP_STATUS_NANOSECONDS DWC_ETHER_QOS (MAC_TX_TIMESTAMP_STATUS_NANOSECONDS)	00000000h
B34h	4	MAC_TX_TIMESTAMP_STATUS_SECONDS DWC_ETHER_QOS (MAC_TX_TIMESTAMP_STATUS_SECONDS)	00000000h
B40h	4	MAC_AUXILIARY_CONTROL DWC_ETHER_QOS (MAC_AUXILIARY_CONTROL)	00000000h
B48h	4	MAC_AUXILIARY_TIMESTAMP_NANOSECONDS DWC_ETHER_QOS (MAC_AUXILIARY_TIMESTAMP_NANOSECONDS)	00000000h
B4Ch	4	MAC_AUXILIARY_TIMESTAMP_SECONDS DWC_ETHER_QOS (MAC_AUXILIARY_TIMESTAMP_SECONDS)	00000000h
B50h	4	MAC_TIMESTAMP_INGRESS_ASYM_CORR DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_ASYM_CORR)	00000000h
B54h	4	MAC_TIMESTAMP_EGRESS_ASYM_CORR DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_ASYM_CORR)	00000000h
B58h	4	MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
B5Ch	4	MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND)	00000000h
B60h	4	MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC)	00000000h
B64h	4	MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC)	00000000h
B68h	4	MAC_TIMESTAMP_INGRESS_LATENCY DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_LATENCY)	00000000h
B6Ch	4	MAC_TIMESTAMP_EGRESS_LATENCY DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_LATENCY)	00000000h
B70h	4	MAC_PPS_CONTROL DWC_ETHER_QOS (MAC_PPS_CONTROL)	00000000h
B80h	4	MAC_PPS0_TARGET_TIME_SECONDS DWC_ETHER_QOS (MAC_PPS0_TARGET_TIME_SECONDS)	00000000h
B84h	4	MAC_PPS0_TARGET_TIME_NANOSECONDS DWC_ETHER_QOS (MAC_PPS0_TARGET_TIME_NANOSECONDS)	00000000h
B88h	4	MAC_PPS0_INTERVAL DWC_ETHER_QOS (MAC_PPS0_INTERVAL)	00000000h
B8Ch	4	MAC_PPS0_WIDTH DWC_ETHER_QOS (MAC_PPS0_WIDTH)	00000000h
B90h	4	MAC_PPS1_TARGET_TIME_SECONDS DWC_ETHER_QOS (MAC_PPS1_TARGET_TIME_SECONDS)	00000000h
B94h	4	MAC_PPS1_TARGET_TIME_NANOSECONDS DWC_ETHER_QOS (MAC_PPS1_TARGET_TIME_NANOSECONDS)	00000000h
B98h	4	MAC_PPS1_INTERVAL DWC_ETHER_QOS (MAC_PPS1_INTERVAL)	00000000h
B9Ch	4	MAC_PPS1_WIDTH DWC_ETHER_QOS (MAC_PPS1_WIDTH)	00000000h
BC0h	4	MAC_PTO_CONTROL DWC_ETHER_QOS (MAC_PTO_CONTROL)	00000000h
BC4h	4	MAC_SOURCE_PORT_IDENTITY0 DWC_ETHER_QOS (MAC_SOURCE_PORT_IDENTITY0)	00000000h
BC8h	4	MAC_SOURCE_PORT_IDENTITY1 DWC_ETHER_QOS (MAC_SOURCE_PORT_IDENTITY1)	00000000h
BCCh	4	MAC_SOURCE_PORT_IDENTITY2 DWC_ETHER_QOS (MAC_SOURCE_PORT_IDENTITY2)	00000000h
BD0h	4	MAC_LOG_MESSAGE_INTERVAL DWC_ETHER_QOS (MAC_LOG_MESSAGE_INTERVAL)	00000000h
C00h	4	MTL_OPERATION_MODE DWC_ETHER_QOS (MTL_OPERATION_MODE)	00000000h
C08h	4	MTL_DBG_CTL DWC_ETHER_QOS (MTL_DBG_CTL)	00000000h
C0Ch	4	MTL_DBG_STS DWC_ETHER_QOS (MTL_DBG_STS)	00000018h
C10h	4	MTL_FIFO_DEBUG_DATA DWC_ETHER_QOS (MTL_FIFO_DEBUG_DATA)	00000000h
C20h	4	MTL_INTERRUPT_STATUS DWC_ETHER_QOS (MTL_INTERRUPT_STATUS)	00000000h
C30h	4	MTL_RXQ_DMA_MAP0 DWC_ETHER_QOS (MTL_RXQ_DMA_MAP0)	00000000h
C34h	4	MTL_RXQ_DMA_MAP1 DWC_ETHER_QOS (MTL_RXQ_DMA_MAP1)	00000000h
C40h	4	MTL_TBS_CTRL DWC_ETHER_QOS (MTL_TBS_CTRL)	00000000h
C50h	4	MTL_EST_CONTROL DWC_ETHER_QOS (MTL_EST_CONTROL)	00000000h
C58h	4	MTL_EST_STATUS DWC_ETHER_QOS (MTL_EST_STATUS)	00000000h
C60h	4	MTL_EST_SCH_ERROR DWC_ETHER_QOS (MTL_EST_SCH_ERROR)	00000000h
C64h	4	MTL_EST_FRM_SIZE_ERROR DWC_ETHER_QOS (MTL_EST_FRM_SIZE_ERROR)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C68h	4	MTL_EST_FRM_SIZE_CAPTURE DWC_ETHER_QOS (MTL_EST_FRM_SIZE_CAPTURE)	00000000h
C70h	4	MTL_EST_INTR_ENABLE DWC_ETHER_QOS (MTL_EST_INTR_ENABLE)	00000000h
C80h	4	MTL_EST_GCL_CONTROL DWC_ETHER_QOS (MTL_EST_GCL_CONTROL)	00000000h
C84h	4	MTL_EST_GCL_DATA DWC_ETHER_QOS (MTL_EST_GCL_DATA)	00000000h
C90h	4	MTL_FPE_CTRL_STS DWC_ETHER_QOS (MTL_FPE_CTRL_STS)	00000000h
C94h	4	MTL_FPE_ADVANCE DWC_ETHER_QOS (MTL_FPE_ADVANCE)	00000000h
CC0h	4	MTL_ECC_CONTROL DWC_ETHER_QOS (MTL_ECC_CONTROL)	00000000h
CC4h	4	MTL_SAFETY_INTERRUPT_STATUS DWC_ETHER_QOS (MTL_SAFETY_INTERRUPT_STATUS)	00000000h
CC8h	4	MTL_ECC_INTERRUPT_ENABLE DWC_ETHER_QOS (MTL_ECC_INTERRUPT_ENABLE)	00000000h
CCCh	4	MTL_ECC_INTERRUPT_STATUS DWC_ETHER_QOS (MTL_ECC_INTERRUPT_STATUS)	00000000h
CD0h	4	MTL_ECC_ERR_STS_RCTL DWC_ETHER_QOS (MTL_ECC_ERR_STS_RCTL)	00000000h
CD4h	4	MTL_ECC_ERR_ADDR_STATUS DWC_ETHER_QOS (MTL_ECC_ERR_ADDR_STATUS)	00000000h
CD8h	4	MTL_ECC_ERR_CNTR_STATUS DWC_ETHER_QOS (MTL_ECC_ERR_CNTR_STATUS)	00000000h
CE0h	4	MTL_DPP_CONTROL DWC_ETHER_QOS (MTL_DPP_CONTROL)	00000000h
D00h	4	MTL_TXQ0_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ0_OPERATION_MODE)	00000000h
D04h	4	MTL_TXQ0_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ0_UNDERFLOW)	00000000h
D08h	4	MTL_TXQ0_DEBUG DWC_ETHER_QOS (MTL_TXQ0_DEBUG)	00000000h
D14h	4	MTL_TXQ0_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ0_ETS_STATUS)	00000000h
D18h	4	MTL_TXQ0_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ0_QUANTUM_WEIGHT)	00000000h
D2Ch	4	MTL_Q0_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q0_INTERRUPT_CONTROL_STATUS)	00000000h
D30h	4	MTL_RXQ0_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ0_OPERATION_MODE)	00000000h
D34h	4	MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT)	00000000h
D38h	4	MTL_RXQ0_DEBUG DWC_ETHER_QOS (MTL_RXQ0_DEBUG)	00000000h
D3Ch	4	MTL_RXQ0_CONTROL DWC_ETHER_QOS (MTL_RXQ0_CONTROL)	00000000h
D40h	4	MTL_TXQ1_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ1_OPERATION_MODE)	00000000h
D44h	4	MTL_TXQ1_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ1_UNDERFLOW)	00000000h
D48h	4	MTL_TXQ1_DEBUG DWC_ETHER_QOS (MTL_TXQ1_DEBUG)	00000000h
D50h	4	MTL_TXQ1_ETS_CONTROL DWC_ETHER_QOS (MTL_TXQ1_ETS_CONTROL)	00000000h
D54h	4	MTL_TXQ1_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ1_ETS_STATUS)	00000000h
D58h	4	MTL_TXQ1_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ1_QUANTUM_WEIGHT)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
D5Ch	4	MTL_TXQ1_SENDSLOPECREDIT DWC_ETHER_QOS (MTL_TXQ1_SENDSLOPECREDIT)	00000000h
D60h	4	MTL_TXQ1_HICREDIT DWC_ETHER_QOS (MTL_TXQ1_HICREDIT)	00000000h
D64h	4	MTL_TXQ1_LOCREDIT DWC_ETHER_QOS (MTL_TXQ1_LOCREDIT)	00000000h
D6Ch	4	MTL_Q1_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q1_INTERRUPT_CONTROL_STATUS)	00000000h
D70h	4	MTL_RXQ1_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ1_OPERATION_MODE)	00000000h
D74h	4	MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT)	00000000h
D78h	4	MTL_RXQ1_DEBUG DWC_ETHER_QOS (MTL_RXQ1_DEBUG)	00000000h
D7Ch	4	MTL_RXQ1_CONTROL DWC_ETHER_QOS (MTL_RXQ1_CONTROL)	00000000h
D80h	4	MTL_TXQ2_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ2_OPERATION_MODE)	00000000h
D84h	4	MTL_TXQ2_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ2_UNDERFLOW)	00000000h
D88h	4	MTL_TXQ2_DEBUG DWC_ETHER_QOS (MTL_TXQ2_DEBUG)	00000000h
D90h	4	MTL_TXQ2_ETS_CONTROL DWC_ETHER_QOS (MTL_TXQ2_ETS_CONTROL)	00000000h
D94h	4	MTL_TXQ2_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ2_ETS_STATUS)	00000000h
D98h	4	MTL_TXQ2_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ2_QUANTUM_WEIGHT)	00000000h
D9Ch	4	MTL_TXQ2_SENDSLOPECREDIT DWC_ETHER_QOS (MTL_TXQ2_SENDSLOPECREDIT)	00000000h
DA0h	4	MTL_TXQ2_HICREDIT DWC_ETHER_QOS (MTL_TXQ2_HICREDIT)	00000000h
DA4h	4	MTL_TXQ2_LOCREDIT DWC_ETHER_QOS (MTL_TXQ2_LOCREDIT)	00000000h
DACh	4	MTL_Q2_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q2_INTERRUPT_CONTROL_STATUS)	00000000h
DB0h	4	MTL_RXQ2_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ2_OPERATION_MODE)	00000000h
DB4h	4	MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT)	00000000h
DB8h	4	MTL_RXQ2_DEBUG DWC_ETHER_QOS (MTL_RXQ2_DEBUG)	00000000h
DBCh	4	MTL_RXQ2_CONTROL DWC_ETHER_QOS (MTL_RXQ2_CONTROL)	00000000h
DC0h	4	MTL_TXQ3_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ3_OPERATION_MODE)	00000000h
DC4h	4	MTL_TXQ3_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ3_UNDERFLOW)	00000000h
DC8h	4	MTL_TXQ3_DEBUG DWC_ETHER_QOS (MTL_TXQ3_DEBUG)	00000000h
DD0h	4	MTL_TXQ3_ETS_CONTROL DWC_ETHER_QOS (MTL_TXQ3_ETS_CONTROL)	00000000h
DD4h	4	MTL_TXQ3_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ3_ETS_STATUS)	00000000h
DD8h	4	MTL_TXQ3_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ3_QUANTUM_WEIGHT)	00000000h
DDCh	4	MTL_TXQ3_SENDSLOPECREDIT DWC_ETHER_QOS (MTL_TXQ3_SENDSLOPECREDIT)	00000000h
DE0h	4	MTL_TXQ3_HICREDIT DWC_ETHER_QOS (MTL_TXQ3_HICREDIT)	00000000h
DE4h	4	MTL_TXQ3_LOCREDIT DWC_ETHER_QOS (MTL_TXQ3_LOCREDIT)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
DECh	4	MTL_Q3_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q3_INTERRUPT_CONTROL_STATUS)	00000000h
DF0h	4	MTL_RXQ3_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ3_OPERATION_MODE)	00000000h
DF4h	4	MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT)	00000000h
DF8h	4	MTL_RXQ3_DEBUG DWC_ETHER_QOS (MTL_RXQ3_DEBUG)	00000000h
DFCh	4	MTL_RXQ3_CONTROL DWC_ETHER_QOS (MTL_RXQ3_CONTROL)	00000000h
E2Ch	4	MTL_Q4_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q4_INTERRUPT_CONTROL_STATUS)	00000000h
E30h	4	MTL_RXQ4_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ4_OPERATION_MODE)	00000000h
E34h	4	MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT)	00000000h
E38h	4	MTL_RXQ4_DEBUG DWC_ETHER_QOS (MTL_RXQ4_DEBUG)	00000000h
E3Ch	4	MTL_RXQ4_CONTROL DWC_ETHER_QOS (MTL_RXQ4_CONTROL)	00000000h
E6Ch	4	MTL_Q5_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q5_INTERRUPT_CONTROL_STATUS)	00000000h
E70h	4	MTL_RXQ5_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ5_OPERATION_MODE)	00000000h
E74h	4	MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT)	00000000h
E78h	4	MTL_RXQ5_DEBUG DWC_ETHER_QOS (MTL_RXQ5_DEBUG)	00000000h
E7Ch	4	MTL_RXQ5_CONTROL DWC_ETHER_QOS (MTL_RXQ5_CONTROL)	00000000h
1000h	4	DMA_MODE DWC_ETHER_QOS (DMA_MODE)	00000000h
1004h	4	DMA_SYSBUS_MODE DWC_ETHER_QOS (DMA_SYSBUS_MODE)	01010000h
1008h	4	DMA_INTERRUPT_STATUS DWC_ETHER_QOS (DMA_INTERRUPT_STATUS)	00000000h
100Ch	4	DMA_DEBUG_STATUS0 DWC_ETHER_QOS (DMA_DEBUG_STATUS0)	00000000h
1010h	4	DMA_DEBUG_STATUS1 DWC_ETHER_QOS (DMA_DEBUG_STATUS1)	00000000h
1020h	4	AXI4_TX_AR_ACE_CONTROL DWC_ETHER_QOS (AXI4_TX_AR_ACE_CONTROL)	00000000h
1024h	4	AXI4_RX_AW_ACE_CONTROL DWC_ETHER_QOS (AXI4_RX_AW_ACE_CONTROL)	00000000h
1028h	4	AXI4_TXRX_AWAR_ACE_CONTROL DWC_ETHER_QOS (AXI4_TXRX_AWAR_ACE_CONTROL)	00000000h
1040h	4	AXI_LPI_ENTRY_INTERVAL DWC_ETHER_QOS (AXI_LPI_ENTRY_INTERVAL)	00000000h
1050h	4	DMA_TBS_CTRL DWC_ETHER_QOS (DMA_TBS_CTRL)	00000000h
1080h	4	DMA_SAFETY_INTERRUPT_STATUS DWC_ETHER_QOS (DMA_SAFETY_INTERRUPT_STATUS)	00000000h
1084h	4	DMA_ECC_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_ECC_INTERRUPT_ENABLE)	00000000h
1088h	4	DMA_ECC_INTERRUPT_STATUS DWC_ETHER_QOS (DMA_ECC_INTERRUPT_STATUS)	00000000h
1100h	4	DMA_CH0_CONTROL DWC_ETHER_QOS (DMA_CH0_CONTROL)	00000000h
1104h	4	DMA_CH0_TX_CONTROL DWC_ETHER_QOS (DMA_CH0_TX_CONTROL)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1108h	4	DMA_CH0_RX_CONTROL DWC_ETHER_QOS (DMA_CH0_RX_CONTROL)	00000000h
1110h	4	DMA_CH0_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH0_TXDESC_LIST_HADDRESS)	00000000h
1114h	4	DMA_CH0_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH0_TXDESC_LIST_ADDRESS)	00000000h
1118h	4	DMA_CH0_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH0_RXDESC_LIST_HADDRESS)	00000000h
111Ch	4	DMA_CH0_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH0_RXDESC_LIST_ADDRESS)	00000000h
1120h	4	DMA_CH0_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH0_TXDESC_TAIL_POINTER)	00000000h
1128h	4	DMA_CH0_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH0_RXDESC_TAIL_POINTER)	00000000h
112Ch	4	DMA_CH0_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH0_TXDESC_RING_LENGTH)	00000000h
1130h	4	DMA_CH0_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH0_RXDESC_RING_LENGTH)	00000000h
1134h	4	DMA_CH0_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH0_INTERRUPT_ENABLE)	00000000h
1138h	4	DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER)	00000000h
113Ch	4	DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS)	000007C0h
1144h	4	DMA_CH0_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_TXDESC)	00000000h
114Ch	4	DMA_CH0_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_RXDESC)	00000000h
1150h	4	DMA_CH0_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_TXBUFFER_H)	00000000h
1154h	4	DMA_CH0_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_TXBUFFER)	00000000h
1158h	4	DMA_CH0_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_RXBUFFER_H)	00000000h
115Ch	4	DMA_CH0_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_RXBUFFER)	00000000h
1160h	4	DMA_CH0_STATUS DWC_ETHER_QOS (DMA_CH0_STATUS)	00000000h
1164h	4	DMA_CH0_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH0_MISS_FRAME_CNT)	00000000h
116Ch	4	DMA_CH0_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH0_RX_ERI_CNT)	00000000h
1180h	4	DMA_CH1_CONTROL DWC_ETHER_QOS (DMA_CH1_CONTROL)	00000000h
1184h	4	DMA_CH1_TX_CONTROL DWC_ETHER_QOS (DMA_CH1_TX_CONTROL)	00000000h
1188h	4	DMA_CH1_RX_CONTROL DWC_ETHER_QOS (DMA_CH1_RX_CONTROL)	00000000h
1190h	4	DMA_CH1_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH1_TXDESC_LIST_HADDRESS)	00000000h
1194h	4	DMA_CH1_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH1_TXDESC_LIST_ADDRESS)	00000000h
1198h	4	DMA_CH1_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH1_RXDESC_LIST_HADDRESS)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
119Ch	4	DMA_CH1_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH1_RXDESC_LIST_ADDRESS)	00000000h
11A0h	4	DMA_CH1_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH1_TXDESC_TAIL_POINTER)	00000000h
11A8h	4	DMA_CH1_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH1_RXDESC_TAIL_POINTER)	00000000h
11ACh	4	DMA_CH1_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH1_TXDESC_RING_LENGTH)	00000000h
11B0h	4	DMA_CH1_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH1_RXDESC_RING_LENGTH)	00000000h
11B4h	4	DMA_CH1_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH1_INTERRUPT_ENABLE)	00000000h
11B8h	4	DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER)	00000000h
11BCh	4	DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS)	000007C0h
11C4h	4	DMA_CH1_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_TXDESC)	00000000h
11CCh	4	DMA_CH1_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_RXDESC)	00000000h
11D0h	4	DMA_CH1_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_TXBUFFER_H)	00000000h
11D4h	4	DMA_CH1_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_TXBUFFER)	00000000h
11D8h	4	DMA_CH1_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_RXBUFFER_H)	00000000h
11DCh	4	DMA_CH1_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_RXBUFFER)	00000000h
11E0h	4	DMA_CH1_STATUS DWC_ETHER_QOS (DMA_CH1_STATUS)	00000000h
11E4h	4	DMA_CH1_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH1_MISS_FRAME_CNT)	00000000h
11ECh	4	DMA_CH1_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH1_RX_ERI_CNT)	00000000h
1200h	4	DMA_CH2_CONTROL DWC_ETHER_QOS (DMA_CH2_CONTROL)	00000000h
1204h	4	DMA_CH2_TX_CONTROL DWC_ETHER_QOS (DMA_CH2_TX_CONTROL)	00000000h
1208h	4	DMA_CH2_RX_CONTROL DWC_ETHER_QOS (DMA_CH2_RX_CONTROL)	00000000h
1210h	4	DMA_CH2_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH2_TXDESC_LIST_HADDRESS)	00000000h
1214h	4	DMA_CH2_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH2_TXDESC_LIST_ADDRESS)	00000000h
1218h	4	DMA_CH2_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH2_RXDESC_LIST_HADDRESS)	00000000h
121Ch	4	DMA_CH2_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH2_RXDESC_LIST_ADDRESS)	00000000h
1220h	4	DMA_CH2_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH2_TXDESC_TAIL_POINTER)	00000000h
1228h	4	DMA_CH2_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH2_RXDESC_TAIL_POINTER)	00000000h
122Ch	4	DMA_CH2_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH2_TXDESC_RING_LENGTH)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1230h	4	DMA_CH2_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH2_RXDESC_RING_LENGTH)	00000000h
1234h	4	DMA_CH2_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH2_INTERRUPT_ENABLE)	00000000h
1238h	4	DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER)	00000000h
123Ch	4	DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS)	000007C0h
1244h	4	DMA_CH2_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_TXDESC)	00000000h
124Ch	4	DMA_CH2_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_RXDESC)	00000000h
1250h	4	DMA_CH2_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_TXBUFFER_H)	00000000h
1254h	4	DMA_CH2_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_TXBUFFER)	00000000h
1258h	4	DMA_CH2_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_RXBUFFER_H)	00000000h
125Ch	4	DMA_CH2_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_RXBUFFER)	00000000h
1260h	4	DMA_CH2_STATUS DWC_ETHER_QOS (DMA_CH2_STATUS)	00000000h
1264h	4	DMA_CH2_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH2_MISS_FRAME_CNT)	00000000h
126Ch	4	DMA_CH2_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH2_RX_ERI_CNT)	00000000h
1280h	4	DMA_CH3_CONTROL DWC_ETHER_QOS (DMA_CH3_CONTROL)	00000000h
1284h	4	DMA_CH3_TX_CONTROL DWC_ETHER_QOS (DMA_CH3_TX_CONTROL)	00000000h
1288h	4	DMA_CH3_RX_CONTROL DWC_ETHER_QOS (DMA_CH3_RX_CONTROL)	00000000h
1290h	4	DMA_CH3_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH3_TXDESC_LIST_HADDRESS)	00000000h
1294h	4	DMA_CH3_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH3_TXDESC_LIST_ADDRESS)	00000000h
1298h	4	DMA_CH3_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH3_RXDESC_LIST_HADDRESS)	00000000h
129Ch	4	DMA_CH3_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH3_RXDESC_LIST_ADDRESS)	00000000h
12A0h	4	DMA_CH3_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH3_TXDESC_TAIL_POINTER)	00000000h
12A8h	4	DMA_CH3_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH3_RXDESC_TAIL_POINTER)	00000000h
12ACh	4	DMA_CH3_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH3_TXDESC_RING_LENGTH)	00000000h
12B0h	4	DMA_CH3_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH3_RXDESC_RING_LENGTH)	00000000h
12B4h	4	DMA_CH3_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH3_INTERRUPT_ENABLE)	00000000h
12B8h	4	DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER)	00000000h
12BCh	4	DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS)	000007C0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
12C4h	4	DMA_CH3_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_TXDESC)	00000000h
12CCh	4	DMA_CH3_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_RXDESC)	00000000h
12D0h	4	DMA_CH3_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_TXBUFFER_H)	00000000h
12D4h	4	DMA_CH3_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_TXBUFFER)	00000000h
12D8h	4	DMA_CH3_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_RXBUFFER_H)	00000000h
12DCh	4	DMA_CH3_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_RXBUFFER)	00000000h
12E0h	4	DMA_CH3_STATUS DWC_ETHER_QOS (DMA_CH3_STATUS)	00000000h
12E4h	4	DMA_CH3_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH3_MISS_FRAME_CNT)	00000000h
12ECh	4	DMA_CH3_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH3_RX_ERI_CNT)	00000000h
1300h	4	DMA_CH4_CONTROL DWC_ETHER_QOS (DMA_CH4_CONTROL)	00000000h
1308h	4	DMA_CH4_RX_CONTROL DWC_ETHER_QOS (DMA_CH4_RX_CONTROL)	00000000h
1318h	4	DMA_CH4_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH4_RXDESC_LIST_HADDRESS)	00000000h
131Ch	4	DMA_CH4_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH4_RXDESC_LIST_ADDRESS)	00000000h
1328h	4	DMA_CH4_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH4_RXDESC_TAIL_POINTER)	00000000h
1330h	4	DMA_CH4_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH4_RXDESC_RING_LENGTH)	00000000h
1334h	4	DMA_CH4_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH4_INTERRUPT_ENABLE)	00000000h
1338h	4	DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER)	00000000h
134Ch	4	DMA_CH4_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH4_CURRENT_APP_RXDESC)	00000000h
1358h	4	DMA_CH4_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH4_CURRENT_APP_RXBUFFER_H)	00000000h
135Ch	4	DMA_CH4_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH4_CURRENT_APP_RXBUFFER)	00000000h
1360h	4	DMA_CH4_STATUS DWC_ETHER_QOS (DMA_CH4_STATUS)	00000000h
1364h	4	DMA_CH4_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH4_MISS_FRAME_CNT)	00000000h
136Ch	4	DMA_CH4_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH4_RX_ERI_CNT)	00000000h
1380h	4	DMA_CH5_CONTROL DWC_ETHER_QOS (DMA_CH5_CONTROL)	00000000h
1388h	4	DMA_CH5_RX_CONTROL DWC_ETHER_QOS (DMA_CH5_RX_CONTROL)	00000000h
1398h	4	DMA_CH5_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH5_RXDESC_LIST_HADDRESS)	00000000h
139Ch	4	DMA_CH5_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH5_RXDESC_LIST_ADDRESS)	00000000h
13A8h	4	DMA_CH5_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH5_RXDESC_TAIL_POINTER)	00000000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
13B0h	4	DMA_CH5_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH5_RXDESC_RING_LENGTH)	00000000h
13B4h	4	DMA_CH5_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH5_INTERRUPT_ENABLE)	00000000h
13B8h	4	DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER)	00000000h
13CCh	4	DMA_CH5_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH5_CURRENT_APP_RXDESC)	00000000h
13D8h	4	DMA_CH5_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH5_CURRENT_APP_RXBUFFER_H)	00000000h
13DCh	4	DMA_CH5_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH5_CURRENT_APP_RXBUFFER)	00000000h
13E0h	4	DMA_CH5_STATUS DWC_ETHER_QOS (DMA_CH5_STATUS)	00000000h
13E4h	4	DMA_CH5_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH5_MISS_FRAME_CNT)	00000000h
13ECh	4	DMA_CH5_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH5_RX_ERI_CNT)	00000000h

21.2.1 MAC_CONFIGURATION DWC_ETHER_QOS (MAC_CONFIGURATION) — Offset 0h

The MAC Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ARPEN DWC_ETHER_QOS (ARPEN):** ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected.

Bit Range	Default & Access	Field Name (ID): Description
30:28	0h RW	**SARC DWC_ETHER_QOS (SARC):** Source Address Insertion or Replacement Control This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: - The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: - If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: - If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. - If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. Note: - Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.
27	0h RW	**IPC DWC_ETHER_QOS (IPC):** Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit.
26:24	0h RW	**IPG DWC_ETHER_QOS (IPG):** Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register.
23	0h RW	**GPSLCE DWC_ETHER_QOS (GPSLCE):** Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status.
22	0h RW	**S2KP DWC_ETHER_QOS (S2KP):** IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. For more information about how the setting of this bit and the JE bit impact the Giant packet status, see the Table, Gaint Packet Status based on S2KP and JE Bits. Note: When the JE bit is set, setting this bit has no effect on the giant packet status.
21	0h RW	**CST DWC_ETHER_QOS (CST):** CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**ACS DWC_ETHER_QOS (ACS):** Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. Note: For information about how the settings of CST bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit.
19	0h RW	**WD DWC_ETHER_QOS (WD):** Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes.
18	0h RW	**BE DWC_ETHER_QOS (BE):** Packet Burst Enable When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode.
17	0h RW	**JD DWC_ETHER_QOS (JD):** Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet.
16	0h RW	**JE DWC_ETHER_QOS (JE):** Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status.
15	0h RW	**PS DWC_ETHER_QOS (PS):** Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit.
14	0h RW	**FES DWC_ETHER_QOS (FES):** Speed This bit selects the speed mode. The mac_speed_o[0] signal reflects the value of this bit.
13	0h RW	**DM DWC_ETHER_QOS (DM):** Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations.
12	0h RW	**LM DWC_ETHER_QOS (LM):** Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back.
11	0h RW	**ECRSFD DWC_ETHER_QOS (ECRSFD):** Enable Carrier Sense Before Transmission in Full-Duplex Mode When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal.
10	0h RW	**DO DWC_ETHER_QOS (DO):** Disable Receive Own When this bit is set, the MAC disables the reception of packets when the gmii_txen_o is asserted in the half-duplex mode. When this bit is reset, the MAC receives all packets given by the PHY. This bit is not applicable in the full-duplex mode.
9	0h RW	**DCRS DWC_ETHER_QOS (DCRS):** Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**DR DWC_ETHER_QOS (DR):** Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode.
7	0h RO	**Reserved**
6:5	0h RW	**BL DWC_ETHER_QOS (BL):** Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode.
4	0h RW	**DC DWC_ETHER_QOS (DC):** Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode.
3:2	0h RW	**PRELEN DWC_ETHER_QOS (PRELEN):** Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode.
1	0h RW	**TE DWC_ETHER_QOS (TE):** Transmitter Enable When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets.
0	0h RW	**RE DWC_ETHER_QOS (RE):** Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface.

21.2.2 MAC_EXT_CONFIGURATION DWC_ETHER_QOS (MAC_EXT_CONFIGURATION) — Offset 4h

The MAC Extended Configuration Register establishes the operating mode of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RW	**EIPG DWC_ETHER_QOS (EIPG):** Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	0h RW	**EIPGEN DWC_ETHER_QOS (EIPGEN):** Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode.
23	0h RO	**Reserved**
22:20	0h RW	**HDSMS DWC_ETHER_QOS (HDSMS):** Maximum Size for Splitting the Header Data These bits indicate the maximum header size allowed for splitting the header data in the received packet.
19	0h RW	**PDC DWC_ETHER_QOS (PDC):** Packet Duplication Control When this bit is set, the received packet with Multicast/ Broadcast Destination address is routed to multiple Receive DMA Channels. The Receive DMA Channels is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Multicast/Broadcast Destination address in the received packet. The DCS field is interpreted to be a one-hot value, each bit corresponding to the Receive DMA Channel. When this bit is reset, the received packet is routed to single Receive DMA Channel. The Receive DMA Channel is identified by the DCS field of MAC_Address(#i)_High register corresponding to the MAC Address register that matches the Destination address in the received packet. The DCS field is interpreted as a binary value.
18	0h RW	**USP DWC_ETHER_QOS (USP):** Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5.
17	0h RW	**SPEN DWC_ETHER_QOS (SPEN):** Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets.
16	0h RW	**DCRCC DWC_ETHER_QOS (DCRCC):** Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets.

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:0	0000h RW	**GPSL DWC_ETHER_QOS (GPSL):** Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

21.2.3 MAC_PACKET_FILTER DWC_ETHER_QOS (MAC_PACKET_FILTER) — Offset 8h

The MAC Packet Filter register contains the filter controls for receiving packets. Some of the controls from this register go to the address check block of the MAC which performs the first level of address filtering. The second level of filtering is performed on the incoming packet based on other controls such as Pass Bad Packets and Pass Control Packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RA DWC_ETHER_QOS (RA):** Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter.
30:22	0h RO	**Reserved**
21	0h RW	**DNTU DWC_ETHER_QOS (DNTU):** Drop Non-TCP/UDP over IP Packets When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets.
20	0h RW	**IPFE DWC_ETHER_QOS (IPFE):** Layer 3 and Layer 4 Filter Enable When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields.
19:17	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**VTFE DWC_ETHER_QOS (VTFE):** VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag.
15:11	0h RO	**Reserved**
10	0h RW	**HPF DWC_ETHER_QOS (HPF):** Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter.
9	0h RW	**SAF DWC_ETHER_QOS (SAF):** Source Address Filter Enable When this bit is set, the MAC compares the SA field of the received packets with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in DWC_ether_qos, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.
8	0h RW	**SAIF DWC_ETHER_QOS (SAIF):** SA Inverse Filtering When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter.
7:6	0h RW	**PCF DWC_ETHER_QOS (PCF):** Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets).
5	0h RW	**DBF DWC_ETHER_QOS (DBF):** Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets.
4	0h RW	**PM DWC_ETHER_QOS (PM):** Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit.
3	0h RW	**DAIF DWC_ETHER_QOS (DAIF):** DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed.
2	0h RW	**HMC DWC_ETHER_QOS (HMC):** Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers.
1	0h RW	**HUC DWC_ETHER_QOS (HUC):** Hash Unicast When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers.
0	0h RW	**PR DWC_ETHER_QOS (PR):** Promiscuous Mode When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set.

21.2.4 MAC_WATCHDOG_TIMEOUT DWC_ETHER_QOS (MAC_WATCHDOG_TIMEOUT) — Offset Ch

The Watchdog Timeout register controls the watchdog timeout for received packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**PWE DWC_ETHER_QOS (PWE):** Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register.
7:4	0h RO	**Reserved**
3:0	0h RW	**WTO DWC_ETHER_QOS (WTO):** Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped.

21.2.5 MAC_HASH_TABLE_REG0 DWC_ETHER_QOS (MAC_HASH_TABLE_REG0) — Offset 10h

The Hash Table Register 0 contains the first 32 bits of the hash table, when the width of the hash table is 128 or 256 bits. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way: - Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32). - Perform bitwise reversal for the value obtained in Step 1. - Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written. If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**HT31T0 DWC_ETHER_QOS (HT31T0):** MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table.

21.2.6 MAC_HASH_TABLE_REG1 DWC_ETHER_QOS (MAC_HASH_TABLE_REG1) — Offset 14h

The Hash Table Register 1 contains the second 32 bits of the hash table. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way: - Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32). - Perform bitwise reversal for the value obtained in Step 1. - Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written. If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**HT63T32 DWC_ETHER_QOS (HT63T32):** MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.

21.2.7 MAC_VLAN_TAG_CTRL DWC_ETHER_QOS (MAC_VLAN_TAG_CTRL) — Offset 50h

This register is the redefined format of the MAC VLAN Tag Register. It is used for indirect addressing. It contains the address offset, command type and Busy Bit for CSR access of the Per VLAN Tag registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**EIVLRXS DWC_ETHER_QOS (EIVLRXS):** Enable Inner VLAN Tag in Rx Status When this bit is set, the MAC provides the inner VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the inner VLAN Tag in Rx status.
30	0h RO	**Reserved**
29:28	0h RW	**EIVLS DWC_ETHER_QOS (EIVLS):** Enable Inner VLAN Tag Stripping on Receive This field indicates the stripping operation on inner VLAN Tag in received packet.
27	0h RW	**ERIVLT DWC_ETHER_QOS (ERIVLT):** DWC_ether_qos register
26	0h RW	**EDVLP DWC_ETHER_QOS (EDVLP):** Enable Double VLAN Processing When this bit is set, the MAC enables processing of up to two VLAN Tags on Tx and Rx (if present). When this bit is reset, the MAC enables processing of up to one VLAN Tag on Tx and Rx (if present).
25	0h RW	**VTHM DWC_ETHER_QOS (VTHM):** VLAN Tag Hash Table Match Enable When this bit is set, the most significant four bits of CRC of VLAN Tag (ones-complement of most significant four bits of CRC of VLAN Tag when ETV bit is reset) are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the ones-complement of the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed.
24	0h RW	**EVLRXS DWC_ETHER_QOS (EVLRXS):** Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status.
23	0h RO	**Reserved**
22:21	0h RW	**EVLS DWC_ETHER_QOS (EVLS):** Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet.
20:19	0h RO	**Reserved**
18	0h RW	**ESVL DWC_ETHER_QOS (ESVL):** Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets.

Bit Range	Default & Access	Field Name (ID): Description
17	0h RW	**VTIM DWC_ETHER_QOS (VTIM):** VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched.
16:7	0h RO	**Reserved**
6:2	00h RW	**OFS DWC_ETHER_QOS (OFS):** Offset This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access. The width of the field depends on the number of MAC VLAN Tag Registers enabled.
1	0h RW	**CT DWC_ETHER_QOS (CT):** Command Type This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation.
0	0h RW	**OB DWC_ETHER_QOS (OB):** Operation Busy This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset.

21.2.8 MAC_VLAN_TAG_DATA DWC_ETHER_QOS (MAC_VLAN_TAG_DATA) — Offset 54h

This register holds the read/write data for Indirect Access of the Per VLAN Tag registers. During the read access, this field contains valid read data only after the OB bit is reset. During the write access, this field should be valid prior to setting the OB bit in the MAC_VLAN_Tag_Ctrl Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:25	0h RW	**DMACHN DWC_ETHER_QOS (DMACHN):** DMA Channel Number The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed.
24	0h RW	**DMACHEN DWC_ETHER_QOS (DMACHEN):** DMA Channel Number Enable This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing.

Bit Range	Default & Access	Field Name (ID): Description
23:21	0h RO	**Reserved**
20	0h RW	**ERIVLT DWC_ETHER_QOS (ERIVLT):** Enable Inner VLAN Tag Comparison This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit and the EDVLP field are set, the MAC receiver enables operation on the inner VLAN Tag (if present). When this bit is reset, the MAC receiver enables operation on the outer VLAN Tag (if present).
19	0h RW	**ERSVLM DWC_ETHER_QOS (ERSVLM):** Enable S-VLAN Match for received Frames This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets.
18	0h RW	**DOVLTC DWC_ETHER_QOS (DOVLTC):** Disable VLAN Type Comparison This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit.
17	0h RW	**ETV DWC_ETHER_QOS (ETV):** 12bits or 16bits VLAN comparison This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet.
16	0h RW	**VEN DWC_ETHER_QOS (VEN):** VLAN Tag Enable This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields.
15:0	0000h RW	**VID DWC_ETHER_QOS (VID):** VLAN Tag ID This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set.

21.2.9 MAC_VLAN_HASH_TABLE DWC_ETHER_QOS (MAC_VLAN_HASH_TABLE) — Offset 58h

When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. When ETV bit of MAC_VLAN_Tag register is set, the upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. When ETV bit of MAC_VLAN_Tag register is reset, the ones-complement of upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, when ETV bit is set a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table, whereas when ETV bit is reset a hash value of 4b'1000 selects Bit 7 of the VLAN Hash table. The hash value of the destination address is calculated in the following way: - Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3). - Perform bitwise reversal for the value obtained in step 1. - Take the upper four bits from the value obtained in step 2. If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] (in little-endian mode) or Bits[7:0] (in big-endian mode) of this register are written. - If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**VLHT DWC_ETHER_QOS (VLHT):** VLAN Hash Table This field contains the 16-bit VLAN Hash Table.

21.2.10 MAC_VLAN_INCL DWC_ETHER_QOS (MAC_VLAN_INCL) — Offset 60h

The VLAN Tag Inclusion or Replacement register contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**BUSY DWC_ETHER_QOS (BUSY):** Busy This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset. The application must make sure that this bit is reset before attempting subsequent access to this register.
30	0h RW	**RDWR DWC_ETHER_QOS (RDWR):** Read write control This bit controls the read or write operation for indirectly accessing the queue/channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation. This does not have any effect when CBTI is reset.
29:26	0h RO	**Reserved**
25:24	0h RW	**ADDR DWC_ETHER_QOS (ADDR):** Address This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset.
23:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW	**CBTI DWC_ETHER_QOS (CBTI):** Channel based tag insertion When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register.
20	0h RW	**VLTI DWC_ETHER_QOS (VLTI):** VLAN Tag Input When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor
19	0h RW	**CSVL DWC_ETHER_QOS (CSVL):** C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets.
18	0h RW	**VLP DWC_ETHER_QOS (VLP):** VLAN Priority Control When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored.
17:16	0h RW	**VLC DWC_ETHER_QOS (VLC):** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.
15:0	0000h RW	**VLT DWC_ETHER_QOS (VLT):** VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

21.2.11 MAC_INNER_VLAN_INCL DWC_ETHER_QOS (MAC_INNER_VLAN_INCL) — Offset 64h

The Inner VLAN Tag Inclusion or Replacement register contains the inner VLAN tag to be inserted or replaced in the Transmit packet. It also contains the inner VLAN tag insertion controls.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW	**VLTI DWC_ETHER_QOS (VLTI):** VLAN Tag Input When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: - The Tx descriptor
19	0h RW	**CSVL DWC_ETHER_QOS (CSVL):** C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets.
18	0h RW	**VLP DWC_ETHER_QOS (VLP):** VLAN Priority Control When this bit is set, the VLC field is used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and the VLC field is ignored.
17:16	0h RW	**VLC DWC_ETHER_QOS (VLC):** VLAN Tag Control in Transmit Packets - 2'b00: No VLAN tag deletion, insertion, or replacement - 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 17 and 18) and VLAN tag (bytes 19 and 20) of all transmitted packets with VLAN tags. - 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 19 and 20 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 17 and 18. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. - 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 19 and 20 of all VLAN-type transmitted packets (Bytes 17 and 18 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.
15:0	0000h RW	**VLT DWC_ETHER_QOS (VLT):** VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: - Bits[15:13]: User Priority - Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) - Bits[11:0]: VLAN Identifier (VID) field of VLAN tag

21.2.12 MAC_Q0_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q0_TX_FLOW_CTRL) — Offset 70h

The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC. A Write to a register with the Busy bit set to 1 triggers the Flow Control block to generate a Pause packet. The fields of the control packet are selected as specified in the 802.3x specification, and the Pause Time value from this register is used in the Pause Time field of the control packet. The Busy bit remains set until the control packet is transferred onto the cable. The application must make sure that the Busy bit is cleared before writing to the register. When the PFCE bit in the MAC_Rx_Flow_Ctrl register is enabled, this register controls the generation of Priority Flow Control (PFC) frames with priorities mapped according to PSRQ0 in the MAC_RxQ_Ctrl2 register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**PT DWC_ETHER_QOS (PT):** Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**DZPQ DWC_ETHER_QOS (DZPQ):** Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled.
6:4	0h RW	**PLT DWC_ETHER_QOS (PLT):** Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times.
3:2	0h RO	**Reserved**
1	0h RW	**TFE DWC_ETHER_QOS (TFE):** Transmit Flow Control Enable Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled.
0	0h RW	**FCB_BPA DWC_ETHER_QOS (FCB_BPA):** Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.13 MAC_Q1_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q1_TX_FLOW_CTRL) — Offset 74h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**PT DWC_ETHER_QOS (PT):** Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	0h RO	**Reserved**
7	0h RW	**DZPQ DWC_ETHER_QOS (DZPQ):** Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled.
6:4	0h RW	**PLT DWC_ETHER_QOS (PLT):** Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times.
3:2	0h RO	**Reserved**
1	0h RW	**TFE DWC_ETHER_QOS (TFE):** Transmit Flow Control Enable When this bit is set in full-duplex mode, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets.
0	0h RW	**FCB_BPA DWC_ETHER_QOS (FCB_BPA):** Flow Control Busy This bit initiates a PFC packet if the TFE bit is set. To initiate a PFC packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When PFC packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.14 MAC_Q2_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q2_TX_FLOW_CTRL) — Offset 78h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 74h.

21.2.15 MAC_Q3_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q3_TX_FLOW_CTRL) — Offset 7Ch

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 74h.

21.2.16 MAC_Q4_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q4_TX_FLOW_CTRL) — Offset 80h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 74h.

21.2.17 MAC_Q5_TX_FLOW_CTRL DWC_ETHER_QOS (MAC_Q5_TX_FLOW_CTRL) — Offset 84h

This register controls the generation of PFC Control packets of priorities mapped as per the PSRQi field in the MAC_RxQ_Ctrl2/MAC_RxQ_Ctrl3 registers.

Note: Bit definitions are the same as MAC_Q1_TX_FLOW_CTRL, offset 74h.

21.2.18 MAC_RX_FLOW_CTRL DWC_ETHER_QOS (MAC_RX_FLOW_CTRL) — Offset 90h

The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**PFCE DWC_ETHER_QOS (PFCE):** Priority Based Flow Control Enable When this bit is set, it enables generation and reception of priority-based flow control (PFC) packets. When this bit is reset, it enables generation and reception of 802.3x Pause control packets.
7:2	0h RO	**Reserved**
1	0h RW	**UP DWC_ETHER_QOS (UP):** Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011.
0	0h RW	**RFE DWC_ETHER_QOS (RFE):** Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time.

21.2.19 MAC_RXQ_CTRL4 DWC_ETHER_QOS (MAC_RXQ_CTRL4) — Offset 94h

The Receive Queue Control 4 register controls the routing of unicast and multicast packets that fail the Destination or Source address filter to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:17	0h RW	**VFFQ DWC_ETHER_QOS (VFFQ):** VLAN Tag Filter Fail Packets Queue This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
16	0h RW	**VFFQE DWC_ETHER_QOS (VFFQE):** VLAN Tag Filter Fail Packets Queuing Enable When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:9	0h RW	**MFFQ DWC_ETHER_QOS (MFFQ):** Multicast Address Filter Fail Packets Queue. This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.
8	0h RW	**MFFQE DWC_ETHER_QOS (MFFQE):** Multicast Address Filter Fail Packets Queuing Enable. When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.
7:4	0h RO	**Reserved**
3:1	0h RW	**UFFQ DWC_ETHER_QOS (UFFQ):** Unicast Address Filter Fail Packets Queue. This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
0	0h RW	**UFFQE DWC_ETHER_QOS (UFFQE):** Unicast Address Filter Fail Packets Queuing Enable. When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.

21.2.20 MAC_TXQ_PRTY_MAP0 DWC_ETHER_QOS (MAC_TXQ_PRTY_MAP0) — Offset 98h

The Transmit Queue Priority Mapping 0 register contains the priority values assigned to Tx Queue 0 through Tx Queue 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**PSTQ3 DWC_ETHER_QOS (PSTQ3):** Priorities Selected in Transmit Queue 3 This bit is similar to the PSTQ0 bit.
23:16	00h RW	**PSTQ2 DWC_ETHER_QOS (PSTQ2):** Priorities Selected in Transmit Queue 2 This bit is similar to the PSTQ0 bit.
15:8	00h RW	**PSTQ1 DWC_ETHER_QOS (PSTQ1):** Priorities Selected in Transmit Queue 1 This bit is similar to the PSTQ0 bit.

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**PSTQ0 DWC_ETHER_QOS (PSTQ0):** Priorities Selected in Transmit Queue 0 This field holds the priorities assigned to Tx Queue 0 by the software. This field determines if Tx Queue 0 should be blocked from transmitting specified pause time when a PFC packet is received with priorities matching the priorities programmed in this field. If the content of this field is not mutually exclusive to corresponding fields of other Transmit queues, that is, same priority is mapped to multiple Tx queues, the MAC blocks all queues with matching priority for specified time.

21.2.21 MAC_RXQ_CTRL0 DWC_ETHER_QOS (MAC_RXQ_CTRL0) — Offset A0h

The Receive Queue Control 0 register controls the queue management in the MAC Receiver. Note: In multiple Rx queues configuration, all the queues are disabled by default. Enable the Rx queue by programming the corresponding field in this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:10	0h RW	**RXQ5EN DWC_ETHER_QOS (RXQ5EN):** Receive Queue 5 Enable This field is similar to the RXQ0EN field.
9:8	0h RW	**RXQ4EN DWC_ETHER_QOS (RXQ4EN):** Receive Queue 4 Enable This field is similar to the RXQ0EN field.
7:6	0h RW	**RXQ3EN DWC_ETHER_QOS (RXQ3EN):** Receive Queue 3 Enable This field is similar to the RXQ0EN field.
5:4	0h RW	**RXQ2EN DWC_ETHER_QOS (RXQ2EN):** Receive Queue 2 Enable This field is similar to the RXQ0EN field.
3:2	0h RW	**RXQ1EN DWC_ETHER_QOS (RXQ1EN):** Receive Queue 1 Enable This field is similar to the RXQ0EN field.
1:0	0h RW	**RXQ0EN DWC_ETHER_QOS (RXQ0EN):** Receive Queue 0 Enable This field indicates whether Rx Queue 0 is enabled for AV or DCB.

21.2.22 MAC_RXQ_CTRL1 DWC_ETHER_QOS (MAC_RXQ_CTRL1) — Offset A4h

The Receive Queue Control 1 register controls the routing of multicast, broadcast, AV, DCB, and untagged packets to the Rx queues.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:24	0h RW	**FPRQ DWC_ETHER_QOS (FPRQ):** Frame Preemption Residue Queue This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.
23:22	0h RW	**TPQC DWC_ETHER_QOS (TPQC):** Tagged PTP over Ethernet Packets Queuing Control. This field controls the routing of the VLAN Tagged PTPoE packets. If DWC_EQOS_AV_ENABLE is selected in the configuration, the following programmable options are allowed. - 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). - 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). - 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. - 2'b11: Reserved If DWC_EQOS_AV_ENABLE is not selected in the configuration, the following programmable options are allowed. - 1'b0: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for DCB/ Generic enabled Rx Queues). - 1'b1: VLAN Tagged PTPoE packets are routed to Rx Queues specified by PTPQ field.
21	0h RW	**TACPQE DWC_ETHER_QOS (TACPQE):** Tagged AV Control Packets Queuing Enable. When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers.
20	0h RW	**MCBCQEN DWC_ETHER_QOS (MCBCQEN):** Multicast and Broadcast Queue Enable This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field.
19	0h RO	**Reserved**
18:16	0h RW	**MCBCQ DWC_ETHER_QOS (MCBCQ):** Multicast and Broadcast Queue This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets.
15	0h RO	**Reserved**
14:12	0h RW	**UPQ DWC_ETHER_QOS (UPQ):** Untagged Packet Queue This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets.
11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:8	0h RW	**DCBCPQ DWC_ETHER_QOS (DCBCPQ):** DCB Control Packets Queue This field specifies the Rx queue on which the received DCB control packets are routed. The DCB data packets are routed based on the PSRQ field of the Transmit Flow Control Register of corresponding queue.
7	0h RO	**Reserved**
6:4	0h RW	**PTPQ DWC_ETHER_QOS (PTPQ):** PTP Packets Queue This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue.
3	0h RO	**Reserved**
2:0	0h RW	**AVCPQ DWC_ETHER_QOS (AVCPQ):** AV Untagged Control Packets Queue This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field.

21.2.23 MAC_RXQ_CTRL2 DWC_ETHER_QOS (MAC_RXQ_CTRL2) — Offset A8h

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 0 to 3.

Type	Size	Offset	Default
MMIO	32 bit	BAR + A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**PSRQ3 DWC_ETHER_QOS (PSRQ3):** Priorities Selected in the Receive Queue 3 This field decides the priorities assigned to Rx Queue 3. All packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 3 crosses the flow control threshold settings.
23:16	00h RW	**PSRQ2 DWC_ETHER_QOS (PSRQ2):** Priorities Selected in the Receive Queue 2 This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2. For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 2 crosses the flow control threshold settings.

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RW	**PSRQ1 DWC_ETHER_QOS (PSRQ1):** Priorities Selected in the Receive Queue 1 This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 1 crosses the flow control threshold settings.
7:0	00h RW	**PSRQ0 DWC_ETHER_QOS (PSRQ0):** Priorities Selected in the Receive Queue 0 This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 0 crosses the flow control threshold settings.

21.2.24 MAC_RXQ_CTRL3 DWC_ETHER_QOS (MAC_RXQ_CTRL3) — Offset ACh

This register controls the routing of tagged packets based on the USP (user Priority) field of the received packets to the RxQueues 4 to 7.

Type	Size	Offset	Default
MMIO	32 bit	BAR + ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**PSRQ5 DWC_ETHER_QOS (PSRQ5):** Priorities Selected in the Receive Queue 5 This field decides the priorities assigned to Rx Queue 5. All packets with priorities that match the values set in this field are routed to Rx Queue 5. For example, if PSRQ5[6] is set, packets with USP field equal to 6 are routed to Rx Queue 5. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 5 crosses the flow control threshold settings.
7:0	00h RW	**PSRQ4 DWC_ETHER_QOS (PSRQ4):** Priorities Selected in the Receive Queue 4 This field decides the priorities assigned to Rx Queue 4. All packets with priorities that match the values set in this field are routed to Rx Queue 4. For example, if PSRQ4[7:4] is set, packets with USP field equal to 7, 6, 5, or 4 are routed to Rx Queue 4. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. this field also determines the priorities to be included in the PFC packet sent to remote station when Rx Queue 4 crosses the flow control threshold settings.

21.2.25 MAC_INTERRUPT_STATUS DWC_ETHER_QOS (MAC_INTERRUPT_STATUS) — Offset B0h

The Interrupt Status register contains the status of interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RO/V	**MFRIS DWC_ETHER_QOS (MFRIS):** MMC FPE Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support.
19	0h RO/V	**MFTIS DWC_ETHER_QOS (MFTIS):** MMC FPE Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support.
18	0h RO/V	**MDIOIS DWC_ETHER_QOS (MDIOIS):** MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
17	0h RO/V	**FPEIS DWC_ETHER_QOS (FPEIS):** Frame Preemption Interrupt Status This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt.
16	0h RO	**Reserved**
15	0h RO/V	**GPIIS DWC_ETHER_QOS (GPIIS):** GPI Interrupt Status When the GPIO feature is enabled, this bit is set when any active event (LL or LH) occurs on the GPIS field of the MAC_GPIO_Status register and the corresponding GPIE bit is enabled in the MAC_GPIO_Control register. This bit is cleared on reading lane 0 (GPIS) of the MAC_GPIO_Status register.
14	0h RO/V	**RXSTSIS DWC_ETHER_QOS (RXSTSIS):** Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO/V	**TXSTSIS DWC_ETHER_QOS (TXSTSIS):** Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: - Excessive Collision (EXCOL) - Late Collision (LCOL) - Excessive Deferral (EXDEF) - Loss of Carrier (LCARR) - No Carrier (NCARR) - Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.
12	0h RO/V	**TSIS DWC_ETHER_QOS (TSIS):** Timestamp Interrupt Status If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: - The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. - There is an overflow in the Seconds register. - The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register.
11	0h RO/V	**MMCRXIPIS DWC_ETHER_QOS (MMCRXIPIS):** MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options.
10	0h RO/V	**MMCTXIS DWC_ETHER_QOS (MMCTXIS):** MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.
9	0h RO/V	**MMCRXIS DWC_ETHER_QOS (MMCRXIS):** MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.
8	0h RO/V	**MMCIS DWC_ETHER_QOS (MMCIS):** MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.
7:6	0h RO	**Reserved**
5	0h RO/V	**LPIIS DWC_ETHER_QOS (LPIIS):** LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set).
4	0h RO/V	**PMTIS DWC_ETHER_QOS (PMTIS):** PMT Interrupt Status This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**PHYIS DWC_ETHER_QOS (PHYIS):** PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set).
2:1	0h RO	**Reserved**
0	0h RO/V	**RGSMIIIS DWC_ETHER_QOS (RGSMIIIS):** RGMII or SMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface.

21.2.26 MAC_INTERRUPT_ENABLE DWC_ETHER_QOS (MAC_INTERRUPT_ENABLE) — Offset B4h

The Interrupt Enable register contains the masks for generating the interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RW	**MDIOIE DWC_ETHER_QOS (MDIOIE):** MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register.
17	0h RW	**FPEIE DWC_ETHER_QOS (FPEIE):** Frame Preemption Interrupt Enable When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register.
16:15	0h RO	**Reserved**
14	0h RW	**RXSTSIE DWC_ETHER_QOS (RXSTSIE):** Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register.
13	0h RW	**TXSTSIE DWC_ETHER_QOS (TXSTSIE):** Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register.
12	0h RW	**TSIE DWC_ETHER_QOS (TSIE):** Timestamp Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register.
11:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**LPIIE DWC_ETHER_QOS (LPIIE):** LPI Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register.
4	0h RW	**PMTIE DWC_ETHER_QOS (PMTIE):** PMT Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register.
3	0h RW	**PHYIE DWC_ETHER_QOS (PHYIE):** PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register.
2:1	0h RO	**Reserved**
0	0h RW	**RGSMIIIE DWC_ETHER_QOS (RGSMIIIE):** RGMII or SMII Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register.

21.2.27 MAC_RX_TX_STATUS DWC_ETHER_QOS (MAC_RX_TX_STATUS) — Offset B8h

The Receive Transmit Status register contains the Receive and Transmit Error status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RO/V	**RWT DWC_ETHER_QOS (RWT):** Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
7:6	0h RO	**Reserved**
5	0h RO/V	**EXCOL DWC_ETHER_QOS (EXCOL):** Excessive Collisions When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**LCOL DWC_ETHER_QOS (LCOL):** Late Collision When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
3	0h RO/V	**EXDEF DWC_ETHER_QOS (EXDEF):** Excessive Deferral When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
2	0h RO/V	**LCARR DWC_ETHER_QOS (LCARR):** Loss of Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
1	0h RO/V	**NCARR DWC_ETHER_QOS (NCARR):** No Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
0	0h RO/V	**TJT DWC_ETHER_QOS (TJT):** Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.

21.2.28 MAC_PMT_CONTROL_STATUS DWC_ETHER_QOS (MAC_PMT_CONTROL_STATUS) — Offset C0h

The PMT Control and Status Register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RWKFILTRST DWC_ETHER_QOS (RWKFILTRST):** Remote Wake-Up Packet Filter Register Pointer Reset When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
30:29	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
28:24	00h RO/V	**RWKPTR DWC_ETHER_QOS (RWKPTR):** Remote Wake-up FIFO Pointer This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	0h RO	**Reserved**
10	0h RW	**RWKPFE DWC_ETHER_QOS (RWKPFE):** Remote Wake-up Packet Forwarding Enable When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
9	0h RW	**GLBLUCAST DWC_ETHER_QOS (GLBLUCAST):** Global Unicast When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet.
8:7	0h RO	**Reserved**
6	0h RO/V	**RWKPRCVD DWC_ETHER_QOS (RWKPRCVD):** Remote Wake-Up Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
5	0h RO/V	**MGKPRCVD DWC_ETHER_QOS (MGKPRCVD):** Magic Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
4:3	0h RO	**Reserved**
2	0h RW	**RWKPKTEN DWC_ETHER_QOS (RWKPKTEN):** Remote Wake-Up Packet Enable When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet.
1	0h RW	**MGKPKTEN DWC_ETHER_QOS (MGKPKTEN):** Magic Packet Enable When this bit is set, a power management event is generated when the MAC receives a magic packet.
0	0h RW	**PWRDWN DWC_ETHER_QOS (PWRDWN):** Power Down When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.29 MAC_RWK_PACKET_FILTER DWC_ETHER_QOS (MAC_RWK_PACKET_FILTER) — Offset C4h

The Remote Wakeup Filter registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register. When the Remote Wakeup Filters are to be programmed, the entire set of wkuppktfilter_reg registers must be written. The wkuppktfilter_reg register is programmed by sequentially writing the eight, sixteen or thirty-two register values in MAC_RWK_Packet_Filter register for wkuppktfilter_reg0, wkuppktfilter_reg1, ..., wkuppktfilter_reg31 respectively. The wkuppktfilter_reg register is read in a similar way. The MAC updates the wkuppktfilter_reg register current pointer value in RWKPTR field of MAC_PMT_Control_Status register. The Remote Wakeup Filters are arranged in blocks of 4 filters each and each such block have eight 32-bit wide registers, viz. wkuppktfilter_reg0-7, wkuppktfilter_reg8-15, wkuppktfilter_reg16-23 and wkuppktfilter_reg24-31. The fields of Remote Wakeup Filter are described as follows: Filter i Byte Mask: The filter i byte mask register defines the bytes of the packet that are examined by filter i (0, 1, 2, 3, .., 15) to determine whether or not a packet is a wake-up packet. - The MSB (31st bit) must be zero. - Bit j[30:0] is the byte mask. - If Bit j (byte number) of the byte mask is set, the CRC block processes the Filter i Offset + j of the incoming packet; otherwise Filter i Offset + j is ignored. Filter i Command: The 4-bit filter i command controls the filter i operation. - Bit 3 specifies the address type, defining the destination address type of the pattern. When the bit is set, the pattern applies to only multicast packets; when the bit is reset, the pattern applies only to unicast packet. - Bit 2 (Inverse Mode), when set, reverses the logic of the CRC16 hash function signal, to reject a packet with matching CRC-16 value. Bit 2, along with Bit 1, allows a MAC to reject a subset of remote wake-up packets by creating filter logic such as "Pattern 1 AND NOT Pattern 2". - Bit 1 (And_Previous) implements the Boolean logic. When set, the result of the current entry is logically ANDed with the result of the previous filter. This AND logic allows a filter pattern longer than 32 bytes by splitting the mask among two, three, or four filters. This depends on the number of filters that have the And_Previous bit set. The details are provided below: -- The And_Previous bit setting is applicable within a set of 4 filters. -- Setting of And_Previous bit of filter that is not enabled has no effect, that is setting And_Previous bit of lowest number filter in the set of 4 filters has no effect. For example, setting of And_Previous bit of Filter 0 has no effect. -- If And_Previous bit is set for filter to form AND chained filter, the AND chain breaks at the point any filter is not enabled. For example: If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set) but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 1 is not enabled (bit 0 in Filter 1 command is reset), then only Filter 2 result ANDed with Filter 3 result is considered. If Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 3 And_Previous bit is set (bit 1 in Filter 3 command is set), but Filter 2 is not enabled (bit 0 in Filter 2 command is reset), then since setting of Filter 2 And_Previous bit has no effect only Filter 1 result ORed with Filter 3 result is considered. -- If filters chained by And_Previous bit setting have complementary programming, then a frame may never pass the AND chained filter. For example, if Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 1 Address_Type bit is set (bit 3 in Filter 1 command is set) indicating multicast detection and Filter 2 Address_Type bit is reset (bit 3 in Filter 2 command is reset) indicating unicast detection or vice versa, a remote wakeup frame does not pass the AND chained filter as a remote wakeup frame cannot be of both unicast and multicast address type. - Bit 0 is the enable for filter i. If Bit 0 is not set, filter i is disabled. Filter i Offset: The filter i offset register defines the offset (within the packet) from which the filter i examines the packets. - This 8-bit pattern-offset is the offset for the filter i first byte to be examined. - The minimum allowed offset is 12, which refers to the 13th byte of the packet. - The offset value 0 refers to the first byte of the packet. Filter i CRC-16: The filter i CRC-16 register contains the CRC-16 value calculated from the pattern and the byte mask programmed in the Remote Wakeup filter register. - The 16-bit CRC calculation uses the following

polynomial: G(x) = x^16 + x^15 + x^2 + 1 - Each mask, used in the hash function calculation, is compared with a 16-bit value associated with that mask. Each filter has the following: -- 32-bit Mask: Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC-16 calculation. -- 8-bit Offset Pointer: Specifies the byte to start the CRC-16 computation. The pointer and the mask are used together to locate the bytes to be used in the CRC-16 calculations. The structure of the RWK Filter registers is shown in "Figure 10-11 Remote Wake-Up Packet Filter Register".

Type	Size	Offset	Default
MMIO	32 bit	BAR + C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**WKUPFRMFTR DWC_ETHER_QOS (WKUPFRMFTR):** RWK Packet Filter This field contains the various controls of RWK Packet filter.

21.2.30 MAC_LPI_CONTROL_STATUS DWC_ETHER_QOS (MAC_LPI_CONTROL_STATUS) — Offset D0h

The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21	0h RW	**LPITCSE DWC_ETHER_QOS (LPITCSE):** LPI Tx Clock Stop Enable When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**LPIATE DWC_ETHER_QOS (LPIATE):** LPI Timer Enable This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions.
19	0h RW	**LPITXA DWC_ETHER_QOS (LPITXA):** LPI Tx Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode.
18	0h RW	**PLSEN DWC_ETHER_QOS (PLSEN):** PHY Link Status Enable This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit.
17	0h RW	**PLS DWC_ETHER_QOS (PLS):** PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down.
16	0h RW	**LPIEN DWC_ETHER_QOS (LPIEN):** LPI Enable When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission.
15:10	0h RO	**Reserved**
9	0h RO/V	**RLPIST DWC_ETHER_QOS (RLPIST):** Receive LPI State When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface.
8	0h RO/V	**TLPIST DWC_ETHER_QOS (TLPIST):** Transmit LPI State When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface.
7:4	0h RO	**Reserved**
3	0h RO/V	**RLPIEX DWC_ETHER_QOS (RLPIEX):** Receive LPI Exit When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.
2	0h RO/V	**RLPIEN DWC_ETHER_QOS (RLPIEN):** Receive LPI Entry When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RO/V	**TLPIEX DWC_ETHER_QOS (TLPIEX):** Transmit LPI Exit When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).
0	0h RO/V	**TLPIEN DWC_ETHER_QOS (TLPIEN):** Transmit LPI Entry When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).

21.2.31 MAC_LPI_TIMERS_CONTROL DWC_ETHER_QOS (MAC_LPI_TIMERS_CONTROL) — Offset D4h

The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D4h	03E80000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:16	3E8h RW	**LST DWC_ETHER_QOS (LST):** LPI LS Timer This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	0000h RW	**TWT DWC_ETHER_QOS (TWT):** LPI TW Timer This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

21.2.32 MAC_LPI_ENTRY_TIMER DWC_ETHER_QOS (MAC_LPI_ENTRY_TIMER) — Offset D8h

This register controls the Tx LPI entry timer. This counter is enabled only when bit[20](LPITE) bit of MAC_LPI_Control_Status is set to 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:3	00000h RW	**LPIET DWC_ETHER_QOS (LPIET):** LPI Entry Timer This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	0h RO	**Reserved**

21.2.33 MAC_1US_TIC_COUNTER DWC_ETHER_QOS (MAC_1US_TIC_COUNTER) — Offset DCh

This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially.

Type	Size	Offset	Default
MMIO	32 bit	BAR + DCh	00000063h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	063h RW	**TIC_1US_CNTR DWC_ETHER_QOS (TIC_1US_CNTR):** 1US TIC Counter The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

21.2.34 MAC_PHYIF_CONTROL_STATUS DWC_ETHER_QOS (MAC_PHYIF_CONTROL_STATUS) — Offset F8h

The PHY Interface Control and Status register indicates the status signals received by the SGMII, RGMII, or SMII interface (selected at reset) from the PHY. This register is optional.

Type	Size	Offset	Default
MMIO	32 bit	BAR + F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RO/V	**LNKSTS DWC_ETHER_QOS (LNKSTS):** Link Status This bit indicates whether the link is up (1'b1) or down (1'b0).
18:17	0h RO/V	**LNKSPEED DWC_ETHER_QOS (LNKSPEED):** Link Speed This bit indicates the current speed of the link.
16	0h RO/V	**LNKMOD DWC_ETHER_QOS (LNKMOD):** Link Mode This bit indicates the current mode of operation of the link.
15:2	0h RO	**Reserved**
1	0h RW	**LUD DWC_ETHER_QOS (LUD):** Link Up or Down This bit indicates whether the link is up or down during transmission of configuration in the RGMII, SGMII, or SMII interface.
0	0h RW	**TC DWC_ETHER_QOS (TC):** Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: - "Reduced Gigabit Media Independent Interface" - "Serial Media Independent Interface" - "Serial Gigabit Media Independent Interface"

21.2.35 MAC_VERSION DWC_ETHER_QOS (MAC_VERSION) — Offset 110h

The version register identifies the version of the DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 110h	00005151h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	51h RO/V	**USERVER DWC_ETHER_QOS (USERVER):** User-defined Version
7:0	51h RO/V	**SNPSVER DWC_ETHER_QOS (SNPSVER):** IP defined Version

21.2.36 MAC_DEBUG DWC_ETHER_QOS (MAC_DEBUG) — Offset 114h

The Debug register provides the debug status of various MAC blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RO/V	**TFCSTS DWC_ETHER_QOS (TFCSTS):** MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module.
16	0h RO/V	**TPESTS DWC_ETHER_QOS (TPESTS):** MAC GMII or MII Transmit Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state.
15:3	0h RO	**Reserved**
2:1	0h RO/V	**RFCFCSTS DWC_ETHER_QOS (RFCFCSTS):** MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	0h RO/V	**RPESTS DWC_ETHER_QOS (RPESTS):** MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state.

21.2.37 MAC_HW_FEATURE0 DWC_ETHER_QOS (MAC_HW_FEATURE0) — Offset 11Ch

This register indicates the presence of first set of the optional features or functions of the DWC_ether_qos. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 11Ch	0EFD73F7h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	0h RO/V	**ACTPHYSEL DWC_ETHER_QOS (ACTPHYSEL):** Active PHY Selected When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion.
27	1h RO/V	**SAVLANINS DWC_ETHER_QOS (SAVLANINS):** Source Address or VLAN Insertion Enable This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected
26:25	3h RO/V	**TSSTSSEL DWC_ETHER_QOS (TSSTSSEL):** Timestamp System Time Source This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected
24	0h RO/V	**MACADR64SEL DWC_ETHER_QOS (MACADR64SEL):** MAC Addresses 64-127 Selected This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selected
23	1h RO/V	**MACADR32SEL DWC_ETHER_QOS (MACADR32SEL):** MAC Addresses 32-63 Selected This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected
22:18	1Fh RO/V	**ADDMACADRSEL DWC_ETHER_QOS (ADDMACADRSEL):** MAC Addresses 1-31 Selected This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option
17	0h RO	**Reserved**
16	1h RO/V	**RXCOESEL DWC_ETHER_QOS (RXCOESEL):** Receive Checksum Offload Enabled This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected
15	0h RO	**Reserved**
14	1h RO/V	**TXCOESEL DWC_ETHER_QOS (TXCOESEL):** Transmit Checksum Offload Enabled This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selected
13	1h RO/V	**EEESEL DWC_ETHER_QOS (EEESEL):** Energy Efficient Ethernet Enabled This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected
12	1h RO/V	**TSSEL DWC_ETHER_QOS (TSSEL):** IEEE 1588-2008 Timestamp Enabled This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected
11:10	0h RO	**Reserved**
9	1h RO/V	**ARPOFFSEL DWC_ETHER_QOS (ARPOFFSEL):** ARP Offload Enabled This bit is set to 1 when the Enable IPv4 ARP Offload option is selected

Bit Range	Default & Access	Field Name (ID): Description
8	1h RO/V	**MMCSEL DWC_ETHER_QOS (MMCSEL):** RMON Module Enable This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected
7	1h RO/V	**MGKSEL DWC_ETHER_QOS (MGKSEL):** PMT Magic Packet Enable This bit is set to 1 when the Enable Magic Packet Detection option is selected
6	1h RO/V	**RWKSEL DWC_ETHER_QOS (RWKSEL):** PMT Remote Wake-up Packet Enable This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected
5	1h RO/V	**SMASEL DWC_ETHER_QOS (SMASEL):** SMA (MDIO) Interface This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected
4	1h RO/V	**VLHASH DWC_ETHER_QOS (VLHASH):** VLAN Hash Filter Selected This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected
3	0h RO/V	**PCSSEL DWC_ETHER_QOS (PCSSEL):** PCS Registers (TBI, SGMII, or RTBI PHY interface) This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected
2	1h RO/V	**HDSEL DWC_ETHER_QOS (HDSEL):** Half-duplex Support This bit is set to 1 when the half-duplex mode is selected
1	1h RO/V	**GMIISEL DWC_ETHER_QOS (GMIISEL):** 1000 Mbps Support This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation
0	1h RO/V	**MIISEL DWC_ETHER_QOS (MIISEL):** 10 or 100 Mbps Support This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation

21.2.38 MAC_HW_FEATURE1 DWC_ETHER_QOS (MAC_HW_FEATURE1) — Offset 120h

This register indicates the presence of second set of the optional features or functions of the DWC_ether_qos. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 120h	119F79C8h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:27	2h RO/V	**L3L4FNUM DWC_ETHER_QOS (L3L4FNUM):** Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters:
26	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
25:24	1h RO/V	**HASHTBLSZ DWC_ETHER_QOS (HASHTBLSZ):** Hash Table Size This field indicates the size of the hash table:
23	1h RO/V	**POUOST DWC_ETHER_QOS (POUOST):** One Step for PTP over UDP/IP Feature Enable This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected.
22	0h RO	**Reserved**
21	0h RO/V	**RAVSEL DWC_ETHER_QOS (RAVSEL):** Rx Side Only AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected.
20	1h RO/V	**AVSEL DWC_ETHER_QOS (AVSEL):** AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option is selected.
19	1h RO/V	**DBGMEMA DWC_ETHER_QOS (DBGMEMA):** DMA Debug Registers Enable This bit is set to 1 when the Debug Mode Enable option is selected
18	1h RO/V	**TSOEN DWC_ETHER_QOS (TSOEN):** TCP Segmentation Offload Enable This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected
17	1h RO/V	**SPHEN DWC_ETHER_QOS (SPHEN):** Split Header Feature Enable This bit is set to 1 when the Enable Split Header Structure option is selected
16	1h RO/V	**DCBEN DWC_ETHER_QOS (DCBEN):** DCB Feature Enable This bit is set to 1 when the Enable Data Center Bridging option is selected
15:14	1h RO/V	**ADDR64 DWC_ETHER_QOS (ADDR64):** Address Width. This field indicates the configured address width:
13	1h RO/V	**ADVTHWORD DWC_ETHER_QOS (ADVTHWORD):** IEEE 1588 High Word Register Enable This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selected
12	1h RO/V	**PTOEN DWC_ETHER_QOS (PTOEN):** PTP Offload Enable This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected.
11	1h RO/V	**OSTEN DWC_ETHER_QOS (OSTEN):** One-Step Timestamping Enable This bit is set to 1 when the Enable One-Step Timestamp Feature is selected.
10:6	07h RO/V	**TXFIFOSIZE DWC_ETHER_QOS (TXFIFOSIZE):** MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7:
5	0h RO/V	**SPRAM DWC_ETHER_QOS (SPRAM):** Single Port RAM Enable This bit is set to 1 when the Use single port RAM Feature is selected.
4:0	08h RO/V	**RXFIFOSIZE DWC_ETHER_QOS (RXFIFOSIZE):** MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7:

21.2.39 MAC_HW_FEATURE2 DWC_ETHER_QOS (MAC_HW_FEATURE2) — Offset 124h

This register indicates the presence of third set of the optional features or functions of the DWC_ether_qos. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 124h	220C50C5h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:28	2h RO/V	**AUXSNAPNUM DWC_ETHER_QOS (AUXSNAPNUM):** Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs:
27	0h RO	**Reserved**
26:24	2h RO/V	**PPSOUTNUM DWC_ETHER_QOS (PPSOUTNUM):** Number of PPS Outputs This field indicates the number of PPS outputs:
23:22	0h RO	**Reserved**
21:18	3h RO/V	**TXCHCNT DWC_ETHER_QOS (TXCHCNT):** Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels:
17:16	0h RO	**Reserved**
15:12	5h RO/V	**RXCHCNT DWC_ETHER_QOS (RXCHCNT):** Number of DMA Receive Channels This field indicates the number of DMA Receive channels:
11:10	0h RO	**Reserved**
9:6	3h RO/V	**TXQCNT DWC_ETHER_QOS (TXQCNT):** Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues:
5:4	0h RO	**Reserved**
3:0	5h RO/V	**RXQCNT DWC_ETHER_QOS (RXQCNT):** Number of MTL Receive Queues This field indicates the number of MTL Receive queues:

21.2.40 MAC_HW_FEATURE3 DWC_ETHER_QOS (MAC_HW_FEATURE3) — Offset 128h

This register indicates the presence of fourth set the optional features or functions of the DWC_ether_qos. The software driver can use this register to dynamically enable or disable the programs related to the optional blocks.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 128h	3C390231h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	3h RO/V	**ASP DWC_ETHER_QOS (ASP):** Automotive Safety Package Following are the encoding for the different Safety features
27	1h RO/V	**TBSSEL DWC_ETHER_QOS (TBSSEL):** Time Based Scheduling Enable This bit is set to 1 when the Time Based Scheduling feature is selected.
26	1h RO/V	**FPESEL DWC_ETHER_QOS (FPESEL):** Frame Preemption Enable This bit is set to 1 when the Enable Frame preemption feature is selected.
25:22	0h RO	**Reserved**
21:20	3h RO/V	**ESTWID DWC_ETHER_QOS (ESTWID):** Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval Field
19:17	4h RO/V	**ESTDEP DWC_ETHER_QOS (ESTDEP):** Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(DWC_EQOS_EST_DEP)-5
16	1h RO/V	**ESTSEL DWC_ETHER_QOS (ESTSEL):** Enhancements to Scheduling Traffic Enable This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected.
15	0h RO	**Reserved**
14:13	0h RO/V	**FRPES DWC_ETHER_QOS (FRPES):** Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser.
12:11	0h RO/V	**FRPBS DWC_ETHER_QOS (FRPBS):** Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser.
10	0h RO/V	**FRPSEL DWC_ETHER_QOS (FRPSEL):** Flexible Receive Parser Selected This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected.
9	1h RO/V	**PDUPSEL DWC_ETHER_QOS (PDUPSEL):** Broadcast/Multicast Packet Duplication This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected.
8:6	0h RO	**Reserved**
5	1h RO/V	**DVLAN DWC_ETHER_QOS (DVLAN):** Double VLAN Tag Processing Selected This bit is set to 1 when the Enable Double VLAN Processing Feature is selected.
4	1h RO/V	**CBTISEL DWC_ETHER_QOS (CBTISEL):** Queue/Channel based VLAN tag insertion on Tx Enable This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Reserved**
2:0	1h RO/V	**NRVF DWC_ETHER_QOS (NRVF):** Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected:

21.2.41 MAC_DPP_FSM_INTERRUPT_STATUS DWC_ETHER_QOS (MAC_DPP_FSM_INTERRUPT_STATUS) — Offset 140h

This register contains the status of Automotive Safety related Data Path Parity Errors, Interface Timeout Errors, FSM State Parity Errors and FSM State Timeout Errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 140h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**FSMPES DWC_ETHER_QOS (FSMPES):** FSM State Parity Error Status This field when set indicates one of the FSMs State registers has a parity error detected.
23:18	0h RO	**Reserved**
17	0h RW	**SLVTES DWC_ETHER_QOS (SLVTES):** Slave Read/Write Timeout Error Status This field when set indicates that an Application/CSR Timeout has occurred on the AXI slave interface.
16	0h RW	**MSTTES DWC_ETHER_QOS (MSTTES):** Master Read/Write Timeout Error Status This field when set indicates that an Application/CSR Timeout has occurred on the master (AXI/AHB/ARI/ATI) interface.
15:13	0h RO	**Reserved**
12	0h RW	**PTES DWC_ETHER_QOS (PTES):** PTP FSM Timeout Error Status This field when set indicates that one of the PTP FSM Timeout has occurred.
11	0h RW	**ATES DWC_ETHER_QOS (ATES):** APP FSM Timeout Error Status This field when set indicates that one of the APP FSM Timeout has occurred.
10	0h RO	**Reserved**
9	0h RW	**RTES DWC_ETHER_QOS (RTES):** Rx FSM Timeout Error Status This field when set indicates that one of the Rx FSM Timeout has occurred.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**TTES DWC_ETHER_QOS (TTES):** Tx FSM Timeout Error Status This field when set indicates that one of the Tx FSM Timeout has occurred.
7	0h RW	**ASRPES DWC_ETHER_QOS (ASRPES):** AXI Slave Read data path Parity checker Error Status This bit when set indicates that parity error is detected at the AXI Slave read data interface on "rdata_s_o" or at PC9 checker as shown in the Fig.AXI slave Interface Data path parity protection.
6	0h RW	**CWPES DWC_ETHER_QOS (CWPES):** CSR Write data path Parity checker Error Status This bit when set indicates that parity error is detected at the CSR write data interface on mci_wdata_i (or at PC8 checker as shown in Fig.AXI slave Interface Data path parity protection). When EPSI bit of MTL_DPP_Control register is set and if any parity mis-match is detected on the input slave parity ports (or at PC7 checker as shown in the Fig.AXI slave Interface Data path parity protection) will set this bit to one.
5	0h RW	**ARPES DWC_ETHER_QOS (ARPES):** Application Receive interface data path Parity Error Status This bit when set indicates that a parity error is detected at following checkers based on the system configuration as described below - In MTL configuration (DWC_EQOS_SYS=1), parity checker (PC6 as shown in Fig.Receive Data path Parity protection) at ARI interface. - In DMA configuration (DWC_EQOS_SYS=2), parity checker (PC6 as shown in Fig.Receive Data path Parity protection) at DMA application interface. - In AHB configuration (DWC_EQOS_SYS=3), parity checker (PC6 as shown in Fig.Receive Data path Parity protection) at AHB master interface. - In AXI configuration (DWC_EQOS_SYS=4), parity checker (PC6 as shown in Fig.Receive Data path Parity protection) at AXI master interface.
4	0h RW	**MTSPES DWC_ETHER_QOS (MTSPES):** MTL TX Status data path Parity checker Error Status This filed when set indicates that, parity error is detected on the MTL TX Status data on ati interface (or at PC5 as shown in Fig.Transmit data path parity protection).
3	0h RW	**MPES DWC_ETHER_QOS (MPES):** MTL data path Parity checker Error Status This bit when set indicates that a parity error is detected at the MTL transmit write controller parity checker (or at PC4 as shown in Fig.Transmit data path parity protection).
2	0h RW	**RDPES DWC_ETHER_QOS (RDPES):** Read Descriptor Parity checker Error Status This bit when set indicates that a parity error is detected at the DMA Read descriptor parity checker (or at PC3 as shown in Fig.Transmit data path parity protection).
1	0h RW	**TPES DWC_ETHER_QOS (TPES):** TSO data path Parity checker Error Status This bit when set indicates that a parity error is detected at the DMA TSO parity checker (or at PC2 as shown in Fig.Transmit data path parity protection).
0	0h RW	**ATPES DWC_ETHER_QOS (ATPES):** Application Transmit Interface Parity checker Error Status This bit when set indicates that a parity error is detected on the AXI/AHB Master read data parity checker. This bit when set indicates that a parity error is detected on the interface port parity checker. Following are the checkers located based on the system configuration, - In MTL configuration (DWC_EQOS_SYS=1), parity checker (PC1 as shown in Fig.Transmit data path parity protection) at ATI interface. - In DMA configuration (DWC_EQOS_SYS=2), parity checker (PC1 as shown in Fig.Transmit data path parity protection) at DMA application interface. - In AHB configuration (DWC_EQOS_SYS=3), parity checker (PC1 as shown in Fig.Transmit data path parity protection) at AHB master interface. - In AXI configuration (DWC_EQOS_SYS=4), parity checker (PC1 as shown in Fig.Transmit data path parity protection) at AXI master interface.

21.2.42 MAC_AXI_SLV_DPE_ADDR_STATUS DWC_ETHER_QOS (MAC_AXI_SLV_DPE_ADDR_STATUS) — Offset 144h

This register indicates the CSR address corresponding to the CSR write data on which parity error occured.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RO/V	**ASPEAS DWC_ETHER_QOS (ASPEAS):** AXI Slave data path Parity Error Address Status This field holds the CSR address for which parity error is detected on the CSR write data. This field holds the first address for which parity error is detected on the write data and will be cleared on read.

21.2.43 MAC_FSM_CONTROL DWC_ETHER_QOS (MAC_FSM_CONTROL) — Offset 148h

This register is used to control the FSM State parity and timeout error injection in Debug mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 148h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**PLGRNML DWC_ETHER_QOS (PLGRNML):** PTP Large/Normal Mode Select This field when set indicates that large mode tic generation is used for PTP domain, else normal mode tic generation is used.
27	0h RW	**ALGRNML DWC_ETHER_QOS (ALGRNML):** APP Large/Normal Mode Select This field when set indicates that large mode tic generation is used for APP domain, else normal mode tic generation is used.
26	0h RO	**Reserved**
25	0h RW	**RLGRNML DWC_ETHER_QOS (RLGRNML):** Rx Large/Normal Mode Select This field when set indicates that large mode tic generation is used for Rx domain, else normal mode tic generation is used.
24	0h RW	**TLGRNML DWC_ETHER_QOS (TLGRNML):** Tx Large/Normal Mode Select This field when set indicates that large mode tic generation is used for Tx domain, else normal mode tic generation is used.
23:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**PPEIN DWC_ETHER_QOS (PPEIN):** PTP FSM Parity Error Injection This field when set indicates that Error Injection for PTP FSM Parity is enabled.
19	0h RW	**APEIN DWC_ETHER_QOS (APEIN):** APP FSM Parity Error Injection This field when set indicates that Error Injection for APP FSM Parity is enabled.
18	0h RO	**Reserved**
17	0h RW	**RPEIN DWC_ETHER_QOS (RPEIN):** Rx FSM Parity Error Injection This field when set indicates that Error Injection for RX FSM Parity is enabled.
16	0h RW	**TPEIN DWC_ETHER_QOS (TPEIN):** Tx FSM Parity Error Injection This field when set indicates that Error Injection for TX FSM Parity is enabled.
15:13	0h RO	**Reserved**
12	0h RW	**PTEIN DWC_ETHER_QOS (PTEIN):** PTP FSM Timeout Error Injection This field when set indicates that Error Injection for PTP FSM timeout is enabled.
11	0h RW	**ATEIN DWC_ETHER_QOS (ATEIN):** APP FSM Timeout Error Injection This field when set indicates that Error Injection for APP FSM timeout is enabled.
10	0h RO	**Reserved**
9	0h RW	**RTEIN DWC_ETHER_QOS (RTEIN):** Rx FSM Timeout Error Injection This field when set indicates that Error Injection for RX FSM timeout is enabled.
8	0h RW	**TTEIN DWC_ETHER_QOS (TTEIN):** Tx FSM Timeout Error Injection This field when set indicates that Error Injection for TX FSM timeout is enabled.
7:2	0h RO	**Reserved**
1	0h RW	**PRTYEN DWC_ETHER_QOS (PRTYEN):** This bit when set indicates that the FSM parity feature is enabled.
0	0h RW	**TMOUTEN DWC_ETHER_QOS (TMOUTEN):** This bit when set indicates that the FSM timeout feature is enabled.

21.2.44 MAC_FSM_ACT_TIMER DWC_ETHER_QOS (MAC_FSM_ACT_TIMER) — Offset 14Ch

This register is used to select the FSM and Interface Timeout values.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 14Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:20	0h RW	**LTMRMD DWC_ETHER_QOS (LTMRMD):** This field provides the mode value to be used for large mode FSM and other interface time outs. The timeout duration based on the mode value is given below
19:16	0h RW	**NTMRMD DWC_ETHER_QOS (NTMRMD):** This field provides the value to be used for normal mode FSM and other interface time outs. The timeout duration based on the mode value is given below
15:10	0h RO	**Reserved**
9:0	000h RW	**TMR DWC_ETHER_QOS (TMR):** This field indicates the number of CSR clocks required to generate 1us tic.

21.2.45 MAC_MDIO_ADDRESS DWC_ETHER_QOS (MAC_MDIO_ADDRESS) — Offset 200h

The MDIO Address register controls the management cycles to external PHY through a management interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 200h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**PSE DWC_ETHER_QOS (PSE):** Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW	**BTB DWC_ETHER_QOS (BTB):** Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0.
25:21	00h RW	**PA DWC_ETHER_QOS (PA):** Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.
20:16	00h RW	**RDA DWC_ETHER_QOS (RDA):** Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	0h RO	**Reserved**
14:12	0h RW	**NTC DWC_ETHER_QOS (NTC):** Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	0h RW	**CR DWC_ETHER_QOS (CR):** CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: - 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 - 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 - 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 - 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 - 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 - 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 - 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 - 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz freqency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: - 1000: CSR clock/4 - 1001: CSR clock/6 - 1010: CSR clock/8 - 1011: CSR clock/10 - 1100: CSR clock/12 - 1101: CSR clock/14 - 1110: CSR clock/16 - 1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface.
7:5	0h RO	**Reserved**
4	0h RW	**SKAP DWC_ETHER_QOS (SKAP):** Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set.
3	0h RW	**GOC_1 DWC_ETHER_QOS (GOC_1):** GMII Operation Command 1 This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows: - 00: Reserved - 01: Write - 10: Post Read Increment Address for Clause 45 PHY - 11: Read When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid.
2	0h RW	**GOC_0 DWC_ETHER_QOS (GOC_0):** GMII Operation Command 0 This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1.

Bit Range	Default & Access	Field Name (ID): Description
1	0h RW	**C45E DWC_ETHER_QOS (C45E):** Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO.
0	0h RW	**GB DWC_ETHER_QOS (GB):** GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDI field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.46 MAC_MDIO_DATA DWC_ETHER_QOS (MAC_MDIO_DATA) — Offset 204h

The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address. This register also stores the Read data from the PHY register located at the address specified by MDIO Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 204h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RA DWC_ETHER_QOS (RA):** Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	0000h RW	**GD DWC_ETHER_QOS (GD):** GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

21.2.47 MAC_GPIO_CONTROL DWC_ETHER_QOS (MAC_GPIO_CONTROL) — Offset 208h

The GPIO Control register controls the GPIO.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 208h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RW	**GPIT DWC_ETHER_QOS (GPIT):** GPI Type When this bit is set, it indicates that the corresponding GPIS bit in MAC_GPIO_Status register is of latched-low (LL) type. When this bit is reset, it indicates that the corresponding GPIS is of latched-high (LH) type. The number of bits available in this field depends on the GP Input Signal Width option. Other bits are not used (reserved and always reset).
15:4	0h RO	**Reserved**
3:0	0h RW	**GPIE DWC_ETHER_QOS (GPIE):** GPI Interrupt Enable When this bit is set and the programmed event (LL or LH) occurs on the corresponding GPIS bit of MAC_GPIO_Status register, the GPIIS bit of DMA_Interrupt_Status register is set and an interrupt is generated on the mci_intr_o or sbd_intr_o signal. The GPIIS bit is cleared when the application reads the Bits[7:0] of MAC_GPIO_Status register. When this bit is reset, the GPIIS bit is not set when any event occurs on the corresponding GPIS bits.

21.2.48 MAC_GPIO_STATUS DWC_ETHER_QOS (MAC_GPIO_STATUS) — Offset 20Ch

The General Purpose IO register provides the control to drive the following: up to 16 bits of output ports (GPO) and status of up to 16 input ports (GPIS).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 20Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RW	**GPO DWC_ETHER_QOS (GPO):** General Purpose Output When this bit is set, it directly drives the gpo_o output ports. When this bit is reset, it does not directly drive the gpo_o output ports. The number of bits available in this field depends on the GP Input Signal Width option. Other bits are not used (reserved and always reset).
15:4	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**GPIS DWC_ETHER_QOS (GPIS):** General Purpose Input Status This field gives the status of the signals connected to the gpi_i port. This field is of the following types based on the setting of the corresponding GPIT field of MAC_GPIO_Control register: - Latched-low (LL): This field is cleared when the corresponding gpi_i input becomes low. This field remains low until the application reads this field after which this field reflects the current value of gpi_i input. - Latched-high (LH): This field is set when the corresponding gpi_i input becomes high. This field remains high until the application reads this field after which this field reflects the current value of gpi_i input. The number of bits available in this field depends on the GP Input Signal Width option. Other bits are not used (reserved and always reset). 0000H

21.2.49 MAC_ARP_ADDRESS DWC_ETHER_QOS (MAC_ARP_ADDRESS) — Offset 210h

The ARP Address register contains the IPv4 Destination Address of the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 210h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**ARPPA DWC_ETHER_QOS (ARPPA):** ARP Protocol Address This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

21.2.50 MAC_CSR_SW_CTRL DWC_ETHER_QOS (MAC_CSR_SW_CTRL) — Offset 230h

This register contains SW programmable controls for changing the CSR access response and status bits clearing.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 230h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**SEEN DWC_ETHER_QOS (SEEN):** Slave Error Response Enable When this bit is set, the MAC responds with Slave Error for accesses to reserved registers in CSR space. When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space.
7:1	0h RO	**Reserved**
0	0h RW	**RCWE DWC_ETHER_QOS (RCWE):** Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read.

21.2.51 MAC_FPE_CTRL_STS DWC_ETHER_QOS (MAC_FPE_CTRL_STS) — Offset 234h

This register controls the operation of Frame Preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 234h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19	0h RW	**TRSP DWC_ETHER_QOS (TRSP):** Transmitted Respond Frame Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
18	0h RW	**TVER DWC_ETHER_QOS (TVER):** Transmitted Verify Frame Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
17	0h RW	**RRSP DWC_ETHER_QOS (RRSP):** Received Respond Frame Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
16	0h RW	**RVER DWC_ETHER_QOS (RVER):** Received Verify Frame Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
15:4	0h RO	**Reserved**
3	0h RW	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**SRSP DWC_ETHER_QOS (SRSP):** Send Respond mPacket When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
1	0h RW	**SVER DWC_ETHER_QOS (SVER):** Send Verify mPacket When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
0	0h RW	**EFPE DWC_ETHER_QOS (EFPE):** Enable Tx Frame Preemption When set Frame Preemption Tx functionality is enabled.

21.2.52 MAC_EXT_CFG1 DWC_ETHER_QOS (MAC_EXT_CFG1) — Offset 238h

This register contains Split mode control field and offset field for Split Header feature.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 238h	00000002h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:8	0h RW	**SPLM DWC_ETHER_QOS (SPLM):** Split Mode These bits indicate the mode of splitting the incoming Rx packets. They are
7	0h RO	**Reserved**
6:0	02h RW	**SPLOFST DWC_ETHER_QOS (SPLOFST):** Split Offset These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

21.2.53 MAC_PRESN_TIME_NS DWC_ETHER_QOS (MAC_PRESN_TIME_NS) — Offset 240h

This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns Exists when DWC_EQOS_FLEXI_PPS_OUT_EN is configured

Type	Size	Offset	Default
MMIO	32 bit	BAR + 240h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**MPTN DWC_ETHER_QOS (MPTN):** MAC 1722 Presentation Time in ns These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns

21.2.54 MAC_PRESN_TIME_UPDT DWC_ETHER_QOS (MAC_PRESN_TIME_UPDT) — Offset 244h

This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). Exists when DWC_EQOS_FLEXI_PPS_OUT_EN is configured

Type	Size	Offset	Default
MMIO	32 bit	BAR + 244h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**MPTU DWC_ETHER_QOS (MPTU):** MAC 1722 Presentation Time Update This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction

21.2.55 MAC_ADDRESS0_HIGH DWC_ETHER_QOS (MAC_ADDRESS0_HIGH) — Offset 300h

The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station. The first DA byte that is received on the (G)MII interface corresponds to the LS byte (Bits [7:0]) of the MAC Address Low register. For example, if 0x112233445566 is received (0x11 in lane 0 of the first column) on the (G)MII as the destination address, then the MacAddress0 Register [47:0] is compared with 0x665544332211. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, then the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC

Address0 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 300h	8000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO/V	**AE DWC_ETHER_QOS (AE):** Address Enable This bit is always set to 1.
30:22	0h RO	**Reserved**
21:16	00h RW	**DCS DWC_ETHER_QOS (DCS):** DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
15:0	FFFFh RW	**ADDRHI DWC_ETHER_QOS (ADDRHI):** MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

21.2.56 MAC_ADDRESS0_LOW DWC_ETHER_QOS (MAC_ADDRESS0_LOW) — Offset 304h

The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 304h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**ADDRLO DWC_ETHER_QOS (ADDRLO):** MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

21.2.57 MAC_ADDRESS1_HIGH DWC_ETHER_QOS (MAC_ADDRESS1_HIGH) — Offset 308h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 308h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**AE DWC_ETHER_QOS (AE):** Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.
30	0h RW	**SA DWC_ETHER_QOS (SA):** Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet.
29:24	00h RW	**MBC DWC_ETHER_QOS (MBC):** Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: - Bit 29: MAC_Address${i}_High[15:8] - Bit 28: MAC_Address${i}_High[7:0] - Bit 27: MAC_Address${i}_Low[31:24] - .. - Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.
23:22	0h RO	**Reserved**
21:16	00h RW	**DCS DWC_ETHER_QOS (DCS):** DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed.
15:0	FFFFh RW	**ADDRHI DWC_ETHER_QOS (ADDRHI):** MAC Address1 [47:32] This field contains the upper 16 bits[47:32] of the second 6-byte MAC address.

21.2.58 MAC_ADDRESS1_LOW DWC_ETHER_QOS (MAC_ADDRESS1_LOW) — Offset 30Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 30Ch	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**ADDRLO DWC_ETHER_QOS (ADDRLO):** MAC Address1 [31:0] This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined until loaded by the application after the initialization process.

21.2.59 MAC_ADDRESS2_HIGH DWC_ETHER_QOS (MAC_ADDRESS2_HIGH) — Offset 310h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.60 MAC_ADDRESS2_LOW DWC_ETHER_QOS (MAC_ADDRESS2_LOW) — Offset 314h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.61 MAC_ADDRESS3_HIGH DWC_ETHER_QOS (MAC_ADDRESS3_HIGH) — Offset 318h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.62 MAC_ADDRESS3_LOW DWC_ETHER_QOS (MAC_ADDRESS3_LOW) — Offset 31Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.63 MAC_ADDRESS4_HIGH DWC_ETHER_QOS (MAC_ADDRESS4_HIGH) — Offset 320h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.64 MAC_ADDRESS4_LOW DWC_ETHER_QOS (MAC_ADDRESS4_LOW) — Offset 324h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.65 MAC_ADDRESS5_HIGH DWC_ETHER_QOS (MAC_ADDRESS5_HIGH) — Offset 328h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.66 MAC_ADDRESS5_LOW DWC_ETHER_QOS (MAC_ADDRESS5_LOW) — Offset 32Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.67 MAC_ADDRESS6_HIGH DWC_ETHER_QOS (MAC_ADDRESS6_HIGH) — Offset 330h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.68 MAC_ADDRESS6_LOW DWC_ETHER_QOS (MAC_ADDRESS6_LOW) — Offset 334h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.69 MAC_ADDRESS7_HIGH DWC_ETHER_QOS (MAC_ADDRESS7_HIGH) — Offset 338h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.70 MAC_ADDRESS7_LOW DWC_ETHER_QOS (MAC_ADDRESS7_LOW) — Offset 33Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.71 MAC_ADDRESS8_HIGH DWC_ETHER_QOS (MAC_ADDRESS8_HIGH) — Offset 340h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.72 MAC_ADDRESS8_LOW DWC_ETHER_QOS (MAC_ADDRESS8_LOW) — Offset 344h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.73 MAC_ADDRESS9_HIGH DWC_ETHER_QOS (MAC_ADDRESS9_HIGH) — Offset 348h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.74 MAC_ADDRESS9_LOW DWC_ETHER_QOS (MAC_ADDRESS9_LOW) — Offset 34Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.75 MAC_ADDRESS10_HIGH DWC_ETHER_QOS (MAC_ADDRESS10_HIGH) — Offset 350h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.76 MAC_ADDRESS10_LOW DWC_ETHER_QOS (MAC_ADDRESS10_LOW) — Offset 354h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.77 MAC_ADDRESS11_HIGH DWC_ETHER_QOS (MAC_ADDRESS11_HIGH) — Offset 358h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.78 MAC_ADDRESS11_LOW DWC_ETHER_QOS (MAC_ADDRESS11_LOW) — Offset 35Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.79 MAC_ADDRESS12_HIGH DWC_ETHER_QOS (MAC_ADDRESS12_HIGH) — Offset 360h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.80 MAC_ADDRESS12_LOW DWC_ETHER_QOS (MAC_ADDRESS12_LOW) — Offset 364h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.81 MAC_ADDRESS13_HIGH DWC_ETHER_QOS (MAC_ADDRESS13_HIGH) — Offset 368h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.82 MAC_ADDRESS13_LOW DWC_ETHER_QOS (MAC_ADDRESS13_LOW) — Offset 36Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.83 MAC_ADDRESS14_HIGH DWC_ETHER_QOS (MAC_ADDRESS14_HIGH) — Offset 370h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.84 MAC_ADDRESS14_LOW DWC_ETHER_QOS (MAC_ADDRESS14_LOW) — Offset 374h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.85 MAC_ADDRESS15_HIGH DWC_ETHER_QOS (MAC_ADDRESS15_HIGH) — Offset 378h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.86 MAC_ADDRESS15_LOW DWC_ETHER_QOS (MAC_ADDRESS15_LOW) — Offset 37Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.87 MAC_ADDRESS16_HIGH DWC_ETHER_QOS (MAC_ADDRESS16_HIGH) — Offset 380h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.88 MAC_ADDRESS16_LOW DWC_ETHER_QOS (MAC_ADDRESS16_LOW) — Offset 384h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.89 MAC_ADDRESS17_HIGH DWC_ETHER_QOS (MAC_ADDRESS17_HIGH) — Offset 388h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.90 MAC_ADDRESS17_LOW DWC_ETHER_QOS (MAC_ADDRESS17_LOW) — Offset 38Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.91 MAC_ADDRESS18_HIGH DWC_ETHER_QOS (MAC_ADDRESS18_HIGH) — Offset 390h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.92 MAC_ADDRESS18_LOW DWC_ETHER_QOS (MAC_ADDRESS18_LOW) — Offset 394h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.93 MAC_ADDRESS19_HIGH DWC_ETHER_QOS (MAC_ADDRESS19_HIGH) — Offset 398h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.94 MAC_ADDRESS19_LOW DWC_ETHER_QOS (MAC_ADDRESS19_LOW) — Offset 39Ch

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.95 MAC_ADDRESS20_HIGH DWC_ETHER_QOS (MAC_ADDRESS20_HIGH) — Offset 3A0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.96 MAC_ADDRESS20_LOW DWC_ETHER_QOS (MAC_ADDRESS20_LOW) — Offset 3A4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.97 MAC_ADDRESS21_HIGH DWC_ETHER_QOS (MAC_ADDRESS21_HIGH) — Offset 3A8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.98 MAC_ADDRESS21_LOW DWC_ETHER_QOS (MAC_ADDRESS21_LOW) — Offset 3ACh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.99 MAC_ADDRESS22_HIGH DWC_ETHER_QOS (MAC_ADDRESS22_HIGH) — Offset 3B0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.100 MAC_ADDRESS22_LOW DWC_ETHER_QOS (MAC_ADDRESS22_LOW) — Offset 3B4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.101 MAC_ADDRESS23_HIGH DWC_ETHER_QOS (MAC_ADDRESS23_HIGH) — Offset 3B8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.102 MAC_ADDRESS23_LOW DWC_ETHER_QOS (MAC_ADDRESS23_LOW) — Offset 3BCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.103 MAC_ADDRESS24_HIGH DWC_ETHER_QOS (MAC_ADDRESS24_HIGH) — Offset 3C0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.104 MAC_ADDRESS24_LOW DWC_ETHER_QOS (MAC_ADDRESS24_LOW) — Offset 3C4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.105 MAC_ADDRESS25_HIGH DWC_ETHER_QOS (MAC_ADDRESS25_HIGH) — Offset 3C8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.106 MAC_ADDRESS25_LOW DWC_ETHER_QOS (MAC_ADDRESS25_LOW) — Offset 3CCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.107 MAC_ADDRESS26_HIGH DWC_ETHER_QOS (MAC_ADDRESS26_HIGH) — Offset 3D0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.108 MAC_ADDRESS26_LOW DWC_ETHER_QOS (MAC_ADDRESS26_LOW) — Offset 3D4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.109 MAC_ADDRESS27_HIGH DWC_ETHER_QOS (MAC_ADDRESS27_HIGH) — Offset 3D8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.110 MAC_ADDRESS27_LOW DWC_ETHER_QOS (MAC_ADDRESS27_LOW) — Offset 3DCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.111 MAC_ADDRESS28_HIGH DWC_ETHER_QOS (MAC_ADDRESS28_HIGH) — Offset 3E0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.112 MAC_ADDRESS28_LOW DWC_ETHER_QOS (MAC_ADDRESS28_LOW) — Offset 3E4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.113 MAC_ADDRESS29_HIGH DWC_ETHER_QOS (MAC_ADDRESS29_HIGH) — Offset 3E8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.114 MAC_ADDRESS29_LOW DWC_ETHER_QOS (MAC_ADDRESS29_LOW) — Offset 3ECh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.115 MAC_ADDRESS30_HIGH DWC_ETHER_QOS (MAC_ADDRESS30_HIGH) — Offset 3F0h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.116 MAC_ADDRESS30_LOW DWC_ETHER_QOS (MAC_ADDRESS30_LOW) — Offset 3F4h

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.117 MAC_ADDRESS31_HIGH DWC_ETHER_QOS (MAC_ADDRESS31_HIGH) — Offset 3F8h

The MAC Address1 High register holds the upper 16 bits of the second 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address1 Low Register are written. For proper synchronization updates, the consecutive writes to this Address Low Register should be performed after at least four clock cycles in the destination clock domain.

Note: Bit definitions are the same as MAC_ADDRESS1_HIGH, offset 308h.

21.2.118 MAC_ADDRESS31_LOW DWC_ETHER_QOS (MAC_ADDRESS31_LOW) — Offset 3FCh

The MAC Address1 Low register holds the lower 32 bits of the second 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS1_LOW, offset 30Ch.

21.2.119 MAC_ADDRESS32_HIGH DWC_ETHER_QOS (MAC_ADDRESS32_HIGH) — Offset 400h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 400h	0000FFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**AE DWC_ETHER_QOS (AE):** Address Enable When this bit is set, the Address filter module uses the 33rd MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.
30:19	0h RO	**Reserved**
18:16	0h RW	**DCS DWC_ETHER_QOS (DCS):** DMA Channel Select This field contains the DMA Channel number to which an Rx packet whose DA matches the MAC Address32 content is routed.
15:0	FFFFh RW	**ADDRHI DWC_ETHER_QOS (ADDRHI):** MAC Address32 [47:32] This field contains the upper 16 bits (47:32) of the 33rd 6-byte MAC address.

21.2.120 MAC_ADDRESS32_LOW DWC_ETHER_QOS (MAC_ADDRESS32_LOW) — Offset 404h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 404h	FFFFFFFFh

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW	**ADDRLO DWC_ETHER_QOS (ADDRLO):** MAC Address32 [31:0] This field contains the lower 32 bits of the 33rd 6-byte MAC address. The content of this field is undefined until loaded by the Application after the initialization process.

21.2.121 MAC_ADDRESS33_HIGH DWC_ETHER_QOS (MAC_ADDRESS33_HIGH) — Offset 408h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.122 MAC_ADDRESS33_LOW DWC_ETHER_QOS (MAC_ADDRESS33_LOW) — Offset 40Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.123 MAC_ADDRESS34_HIGH DWC_ETHER_QOS (MAC_ADDRESS34_HIGH) — Offset 410h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.124 MAC_ADDRESS34_LOW DWC_ETHER_QOS (MAC_ADDRESS34_LOW) — Offset 414h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.125 MAC_ADDRESS35_HIGH DWC_ETHER_QOS (MAC_ADDRESS35_HIGH) — Offset 418h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.126 MAC_ADDRESS35_LOW DWC_ETHER_QOS (MAC_ADDRESS35_LOW) — Offset 41Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.127 MAC_ADDRESS36_HIGH DWC_ETHER_QOS (MAC_ADDRESS36_HIGH) — Offset 420h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.128 MAC_ADDRESS36_LOW DWC_ETHER_QOS (MAC_ADDRESS36_LOW) — Offset 424h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.129 MAC_ADDRESS37_HIGH DWC_ETHER_QOS (MAC_ADDRESS37_HIGH) — Offset 428h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.130 MAC_ADDRESS37_LOW DWC_ETHER_QOS (MAC_ADDRESS37_LOW) — Offset 42Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.131 MAC_ADDRESS38_HIGH DWC_ETHER_QOS (MAC_ADDRESS38_HIGH) — Offset 430h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.132 MAC_ADDRESS38_LOW DWC_ETHER_QOS (MAC_ADDRESS38_LOW) — Offset 434h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.133 MAC_ADDRESS39_HIGH DWC_ETHER_QOS (MAC_ADDRESS39_HIGH) — Offset 438h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.134 MAC_ADDRESS39_LOW DWC_ETHER_QOS (MAC_ADDRESS39_LOW) — Offset 43Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.135 MAC_ADDRESS40_HIGH DWC_ETHER_QOS (MAC_ADDRESS40_HIGH) — Offset 440h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.136 MAC_ADDRESS40_LOW DWC_ETHER_QOS (MAC_ADDRESS40_LOW) — Offset 444h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.137 MAC_ADDRESS41_HIGH DWC_ETHER_QOS (MAC_ADDRESS41_HIGH) — Offset 448h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.138 MAC_ADDRESS41_LOW DWC_ETHER_QOS (MAC_ADDRESS41_LOW) — Offset 44Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.139 MAC_ADDRESS42_HIGH DWC_ETHER_QOS (MAC_ADDRESS42_HIGH) — Offset 450h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.140 MAC_ADDRESS42_LOW DWC_ETHER_QOS (MAC_ADDRESS42_LOW) — Offset 454h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.141 MAC_ADDRESS43_HIGH DWC_ETHER_QOS (MAC_ADDRESS43_HIGH) — Offset 458h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.142 MAC_ADDRESS43_LOW DWC_ETHER_QOS (MAC_ADDRESS43_LOW) — Offset 45Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.143 MAC_ADDRESS44_HIGH DWC_ETHER_QOS (MAC_ADDRESS44_HIGH) — Offset 460h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.144 MAC_ADDRESS44_LOW DWC_ETHER_QOS (MAC_ADDRESS44_LOW) — Offset 464h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.145 MAC_ADDRESS45_HIGH DWC_ETHER_QOS (MAC_ADDRESS45_HIGH) — Offset 468h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.146 MAC_ADDRESS45_LOW DWC_ETHER_QOS (MAC_ADDRESS45_LOW) — Offset 46Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.147 MAC_ADDRESS46_HIGH DWC_ETHER_QOS (MAC_ADDRESS46_HIGH) — Offset 470h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.148 MAC_ADDRESS46_LOW DWC_ETHER_QOS (MAC_ADDRESS46_LOW) — Offset 474h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.149 MAC_ADDRESS47_HIGH DWC_ETHER_QOS (MAC_ADDRESS47_HIGH) — Offset 478h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.150 MAC_ADDRESS47_LOW DWC_ETHER_QOS (MAC_ADDRESS47_LOW) — Offset 47Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.151 MAC_ADDRESS48_HIGH DWC_ETHER_QOS (MAC_ADDRESS48_HIGH) — Offset 480h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.152 MAC_ADDRESS48_LOW DWC_ETHER_QOS (MAC_ADDRESS48_LOW) — Offset 484h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.153 MAC_ADDRESS49_HIGH DWC_ETHER_QOS (MAC_ADDRESS49_HIGH) — Offset 488h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.154 MAC_ADDRESS49_LOW DWC_ETHER_QOS (MAC_ADDRESS49_LOW) — Offset 48Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.155 MAC_ADDRESS50_HIGH DWC_ETHER_QOS (MAC_ADDRESS50_HIGH) — Offset 490h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.156 MAC_ADDRESS50_LOW DWC_ETHER_QOS (MAC_ADDRESS50_LOW) — Offset 494h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.157 MAC_ADDRESS51_HIGH DWC_ETHER_QOS (MAC_ADDRESS51_HIGH) — Offset 498h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.158 MAC_ADDRESS51_LOW DWC_ETHER_QOS (MAC_ADDRESS51_LOW) — Offset 49Ch

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.159 MAC_ADDRESS52_HIGH DWC_ETHER_QOS (MAC_ADDRESS52_HIGH) — Offset 4A0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.160 MAC_ADDRESS52_LOW DWC_ETHER_QOS (MAC_ADDRESS52_LOW) — Offset 4A4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.161 MAC_ADDRESS53_HIGH DWC_ETHER_QOS (MAC_ADDRESS53_HIGH) — Offset 4A8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.162 MAC_ADDRESS53_LOW DWC_ETHER_QOS (MAC_ADDRESS53_LOW) — Offset 4ACh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.163 MAC_ADDRESS54_HIGH DWC_ETHER_QOS (MAC_ADDRESS54_HIGH) — Offset 4B0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.164 MAC_ADDRESS54_LOW DWC_ETHER_QOS (MAC_ADDRESS54_LOW) — Offset 4B4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.165 MAC_ADDRESS55_HIGH DWC_ETHER_QOS (MAC_ADDRESS55_HIGH) — Offset 4B8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.166 MAC_ADDRESS55_LOW DWC_ETHER_QOS (MAC_ADDRESS55_LOW) — Offset 4BCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.167 MAC_ADDRESS56_HIGH DWC_ETHER_QOS (MAC_ADDRESS56_HIGH) — Offset 4C0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.168 MAC_ADDRESS56_LOW DWC_ETHER_QOS (MAC_ADDRESS56_LOW) — Offset 4C4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.169 MAC_ADDRESS57_HIGH DWC_ETHER_QOS (MAC_ADDRESS57_HIGH) — Offset 4C8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.170 MAC_ADDRESS57_LOW DWC_ETHER_QOS (MAC_ADDRESS57_LOW) — Offset 4CCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.171 MAC_ADDRESS58_HIGH DWC_ETHER_QOS (MAC_ADDRESS58_HIGH) — Offset 4D0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.172 MAC_ADDRESS58_LOW DWC_ETHER_QOS (MAC_ADDRESS58_LOW) — Offset 4D4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.173 MAC_ADDRESS59_HIGH DWC_ETHER_QOS (MAC_ADDRESS59_HIGH) — Offset 4D8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.174 MAC_ADDRESS59_LOW DWC_ETHER_QOS (MAC_ADDRESS59_LOW) — Offset 4DCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.175 MAC_ADDRESS60_HIGH DWC_ETHER_QOS (MAC_ADDRESS60_HIGH) — Offset 4E0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.176 MAC_ADDRESS60_LOW DWC_ETHER_QOS (MAC_ADDRESS60_LOW) — Offset 4E4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.177 MAC_ADDRESS61_HIGH DWC_ETHER_QOS (MAC_ADDRESS61_HIGH) — Offset 4E8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.178 MAC_ADDRESS61_LOW DWC_ETHER_QOS (MAC_ADDRESS61_LOW) — Offset 4ECh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.179 MAC_ADDRESS62_HIGH DWC_ETHER_QOS (MAC_ADDRESS62_HIGH) — Offset 4F0h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.180 MAC_ADDRESS62_LOW DWC_ETHER_QOS (MAC_ADDRESS62_LOW) — Offset 4F4h

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.181 MAC_ADDRESS63_HIGH DWC_ETHER_QOS (MAC_ADDRESS63_HIGH) — Offset 4F8h

The MAC Address32 High register holds the upper 16 bits of the 33rd 6-byte MAC address of the station. If the MAC address registers are configured to be double-synchronized to the (G)MII clock domains, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the MAC Address Low Register are written. For proper synchronization updates, you should perform the consecutive writes to the MAC Address Low Register after at least four clock cycles of the destination clock.

Note: Bit definitions are the same as MAC_ADDRESS32_HIGH, offset 400h.

21.2.182 MAC_ADDRESS63_LOW DWC_ETHER_QOS (MAC_ADDRESS63_LOW) — Offset 4FCh

The MAC Address32 Low register holds the lower 16 bits of the 33rd 6-byte MAC address of the station.

Note: Bit definitions are the same as MAC_ADDRESS32_LOW, offset 404h.

21.2.183 MMC_CONTROL DWC_ETHER_QOS (MMC_CONTROL) — Offset 700h

This register establishes the operating mode of MMC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 700h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**UCDBC DWC_ETHER_QOS (UCDBC):** Update MMC Counters for Dropped Broadcast Packets Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets.
7:6	0h RO	**Reserved**
5	0h RW	**CNTPRSTLVL DWC_ETHER_QOS (CNTPRSTLVL):** Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2kBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2kBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0.
4	0h RW	**CNTPRST DWC_ETHER_QOS (CNTPRST):** Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.
3	0h RW	**CNTFREEZ DWC_ETHER_QOS (CNTFREEZ):** MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode.
2	0h RW	**RSTONRD DWC_ETHER_QOS (RSTONRD):** Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read.
1	0h RW	**CNTSTOPRO DWC_ETHER_QOS (CNTSTOPRO):** Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value.
0	0h RW	**CNTRST DWC_ETHER_QOS (CNTRST):** Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.

21.2.184 MMC_RX_INTERRUPT DWC_ETHER_QOS (MMC_RX_INTERRUPT) — Offset 704h

This register maintains the interrupts generated from all Receive statistics counters. The MMC Receive Interrupt register maintains the interrupts that are generated when the following occur: - Receive statistic counters reach half of their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter). - Receive statistic counters cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When the Counter Stop Rollover is set, interrupts are set but the counter remains at all-ones. The MMC Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit. Note: R_SS_RC means that this register bit is set internally, and it is cleared when the Counter register is read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 704h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO/V	**RXLPITRCIS DWC_ETHER_QOS (RXLPITRCIS):** MMC Receive LPI transition counter interrupt status This bit is set when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
26	0h RO/V	**RXLPIUSCIS DWC_ETHER_QOS (RXLPIUSCIS):** MMC Receive LPI microsecond counter interrupt status This bit is set when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
25	0h RO/V	**RXCTRLPIS DWC_ETHER_QOS (RXCTRLPIS):** MMC Receive Control Packet Counter Interrupt Status This bit is set when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
24	0h RO/V	**RXRCVERRPIS DWC_ETHER_QOS (RXRCVERRPIS):** MMC Receive Error Packet Counter Interrupt Status This bit is set when the rxrcverror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
23	0h RO/V	**RXWDOGPIS DWC_ETHER_QOS (RXWDOGPIS):** MMC Receive Watchdog Error Packet Counter Interrupt Status This bit is set when the rxwatchdog error counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
22	0h RO/V	**RXVLANGBPIS DWC_ETHER_QOS (RXVLANGBPIS):** MMC Receive VLAN Good Bad Packet Counter Interrupt Status This bit is set when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
21	0h RO/V	**RXFOVPIS DWC_ETHER_QOS (RXFOVPIS):** MMC Receive FIFO Overflow Packet Counter Interrupt Status This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RO/V	**RXPAUSPIS DWC_ETHER_QOS (RXPAUSPIS):** MMC Receive Pause Packet Counter Interrupt Status This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
19	0h RO/V	**RXORANGEPIS DWC_ETHER_QOS (RXORANGEPIS):** MMC Receive Out Of Range Error Packet Counter Interrupt Status. This bit is set when the rxoutofrangetype counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
18	0h RO/V	**RXLENERPIS DWC_ETHER_QOS (RXLENERPIS):** MMC Receive Length Error Packet Counter Interrupt Status This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
17	0h RO/V	**RXUCGPIS DWC_ETHER_QOS (RXUCGPIS):** MMC Receive Unicast Good Packet Counter Interrupt Status This bit is set when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
16	0h RO/V	**RX1024TMAXOCTGBPIS DWC_ETHER_QOS (RX1024TMAXOCTGBPIS):** MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15	0h RO/V	**RX512T1023OCTGBPIS DWC_ETHER_QOS (RX512T1023OCTGBPIS):** MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
14	0h RO/V	**RX256T511OCTGBPIS DWC_ETHER_QOS (RX256T511OCTGBPIS):** MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
13	0h RO/V	**RX128T255OCTGBPIS DWC_ETHER_QOS (RX128T255OCTGBPIS):** MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
12	0h RO/V	**RX65T127OCTGBPIS DWC_ETHER_QOS (RX65T127OCTGBPIS):** MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
11	0h RO/V	**RX64OCTGBPIS DWC_ETHER_QOS (RX64OCTGBPIS):** MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
10	0h RO/V	**RXOSIZEGPIS DWC_ETHER_QOS (RXOSIZEGPIS):** MMC Receive Oversize Good Packet Counter Interrupt Status This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
9	0h RO/V	**RXUSIZEGPIS DWC_ETHER_QOS (RXUSIZEGPIS):** MMC Receive Undersize Good Packet Counter Interrupt Status This bit is set when the rxundersize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
8	0h RO/V	**RXJABERPIS DWC_ETHER_QOS (RXJABERPIS):** MMC Receive Jabber Error Packet Counter Interrupt Status This bit is set when the rxjabbererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO/V	**RXRUNTPIS DWC_ETHER_QOS (RXRUNTPIS):** MMC Receive Runt Packet Counter Interrupt Status This bit is set when the rxrunterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
6	0h RO/V	**RXALGNERPIS DWC_ETHER_QOS (RXALGNERPIS):** MMC Receive Alignment Error Packet Counter Interrupt Status This bit is set when the rxalignmenterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
5	0h RO/V	**RXCRCERPIS DWC_ETHER_QOS (RXCRCERPIS):** MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
4	0h RO/V	**RXMCGPIS DWC_ETHER_QOS (RXMCGPIS):** MMC Receive Multicast Good Packet Counter Interrupt Status This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
3	0h RO/V	**RXBCGPIS DWC_ETHER_QOS (RXBCGPIS):** MMC Receive Broadcast Good Packet Counter Interrupt Status This bit is set when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
2	0h RO/V	**RXGOCTIS DWC_ETHER_QOS (RXGOCTIS):** MMC Receive Good Octet Counter Interrupt Status This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
1	0h RO/V	**RXGBOCTIS DWC_ETHER_QOS (RXGBOCTIS):** MMC Receive Good Bad Octet Counter Interrupt Status This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
0	0h RO/V	**RXGBPKTIS DWC_ETHER_QOS (RXGBPKTIS):** MMC Receive Good Bad Packet Counter Interrupt Status This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

21.2.185 MMC_TX_INTERRUPT DWC_ETHER_QOS (MMC_TX_INTERRUPT) — Offset 708h

This register maintains the interrupts generated from all Transmit statistics counters. The MMC Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 708h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO/V	**TXLPITRCIS DWC_ETHER_QOS (TXLPITRCIS):** MMC Transmit LPI transition counter interrupt status This bit is set when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
26	0h RO/V	**TXLPIUSCIS DWC_ETHER_QOS (TXLPIUSCIS):** MMC Transmit LPI microsecond counter interrupt status This bit is set when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
25	0h RO/V	**TXOSIZEGPIS DWC_ETHER_QOS (TXOSIZEGPIS):** MMC Transmit Oversize Good Packet Counter Interrupt Status This bit is set when the txoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
24	0h RO/V	**TXVLANGPIS DWC_ETHER_QOS (TXVLANGPIS):** MMC Transmit VLAN Good Packet Counter Interrupt Status This bit is set when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
23	0h RO/V	**TXPAUSPIS DWC_ETHER_QOS (TXPAUSPIS):** MMC Transmit Pause Packet Counter Interrupt Status This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
22	0h RO/V	**TXEXDEFPIS DWC_ETHER_QOS (TXEXDEFPIS):** MMC Transmit Excessive Deferral Packet Counter Interrupt Status This bit is set when the txexcessdef counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
21	0h RO/V	**TXGPKTIS DWC_ETHER_QOS (TXGPKTIS):** MMC Transmit Good Packet Counter Interrupt Status This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
20	0h RO/V	**TXGOCTIS DWC_ETHER_QOS (TXGOCTIS):** MMC Transmit Good Octet Counter Interrupt Status This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
19	0h RO/V	**TXCARERPIS DWC_ETHER_QOS (TXCARERPIS):** MMC Transmit Carrier Error Packet Counter Interrupt Status This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
18	0h RO/V	**TXEXCOLPIS DWC_ETHER_QOS (TXEXCOLPIS):** MMC Transmit Excessive Collision Packet Counter Interrupt Status This bit is set when the txexesscol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
17	0h RO/V	**TXLATCOLPIS DWC_ETHER_QOS (TXLATCOLPIS):** MMC Transmit Late Collision Packet Counter Interrupt Status This bit is set when the txlatecol counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO/V	**TXDEFPIS DWC_ETHER_QOS (TXDEFPIS):** MMC Transmit Deferred Packet Counter Interrupt Status This bit is set when the txdeferred counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15	0h RO/V	**TXMCOLGPIS DWC_ETHER_QOS (TXMCOLGPIS):** MMC Transmit Multiple Collision Good Packet Counter Interrupt Status This bit is set when the txmulticol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
14	0h RO/V	**TXSCOLGPIS DWC_ETHER_QOS (TXSCOLGPIS):** MMC Transmit Single Collision Good Packet Counter Interrupt Status This bit is set when the txsinglecol_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
13	0h RO/V	**TXUFLOWERPIS DWC_ETHER_QOS (TXUFLOWERPIS):** MMC Transmit Underflow Error Packet Counter Interrupt Status This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
12	0h RO/V	**TXBCGBPIS DWC_ETHER_QOS (TXBCGBPIS):** MMC Transmit Broadcast Good Bad Packet Counter Interrupt Status This bit is set when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
11	0h RO/V	**TXMCGBPIS DWC_ETHER_QOS (TXMCGBPIS):** MMC Transmit Multicast Good Bad Packet Counter Interrupt Status The bit is set when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
10	0h RO/V	**TXUCGBPIS DWC_ETHER_QOS (TXUCGBPIS):** MMC Transmit Unicast Good Bad Packet Counter Interrupt Status This bit is set when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
9	0h RO/V	**TX1024TMAXOCTGBPIS DWC_ETHER_QOS (TX1024TMAXOCTGBPIS):** MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status This bit is set when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
8	0h RO/V	**TX512T1023OCTGBPIS DWC_ETHER_QOS (TX512T1023OCTGBPIS):** MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Status This bit is set when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
7	0h RO/V	**TX256T511OCTGBPIS DWC_ETHER_QOS (TX256T511OCTGBPIS):** MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Status This bit is set when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
6	0h RO/V	**TX128T255OCTGBPIS DWC_ETHER_QOS (TX128T255OCTGBPIS):** MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Status This bit is set when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
5	0h RO/V	**TX65T127OCTGBPIS DWC_ETHER_QOS (TX65T127OCTGBPIS):** MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Status This bit is set when the tx65to127octets_gb counter reaches half the maximum value, and also when it reaches the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
4	0h RO/V	**TX64OCTGBPIS DWC_ETHER_QOS (TX64OCTGBPIS):** MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Status This bit is set when the tx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**TXMCGPIS DWC_ETHER_QOS (TXMCGPIS):** MMC Transmit Multicast Good Packet Counter Interrupt Status This bit is set when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
2	0h RO/V	**TXBCGPIS DWC_ETHER_QOS (TXBCGPIS):** MMC Transmit Broadcast Good Packet Counter Interrupt Status This bit is set when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
1	0h RO/V	**TXGBPKTIS DWC_ETHER_QOS (TXGBPKTIS):** MMC Transmit Good Bad Packet Counter Interrupt Status This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
0	0h RO/V	**TXGBOCTIS DWC_ETHER_QOS (TXGBOCTIS):** MMC Transmit Good Bad Octet Counter Interrupt Status This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

21.2.186 MMC_RX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_RX_INTERRUPT_MASK) — Offset 70Ch

This register maintains the masks for interrupts generated from all Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 70Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**RXLPITRCIM DWC_ETHER_QOS (RXLPITRCIM):** MMC Receive LPI transition counter interrupt Mask Setting this bit masks the interrupt when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value.
26	0h RW	**RXLPIUSCIM DWC_ETHER_QOS (RXLPIUSCIM):** MMC Receive LPI microsecond counter interrupt Mask Setting this bit masks the interrupt when the Rx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value.
25	0h RW	**RXCTRLPIM DWC_ETHER_QOS (RXCTRLPIM):** MMC Receive Control Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value.
24	0h RW	**RXRCVERRPIM DWC_ETHER_QOS (RXRCVERRPIM):** MMC Receive Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxrcverror counter reaches half of the maximum value or the maximum value.

Bit Range	Default & Access	Field Name (ID): Description
23	0h RW	**RXWDOGPIM DWC_ETHER_QOS (RXWDOGPIM):** MMC Receive Watchdog Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxwatchdog counter reaches half of the maximum value or the maximum value.
22	0h RW	**RXVLANGBPIM DWC_ETHER_QOS (RXVLANGBPIM):** MMC Receive VLAN Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value.
21	0h RW	**RXFOVPIM DWC_ETHER_QOS (RXFOVPIM):** MMC Receive FIFO Overflow Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value.
20	0h RW	**RXPAUSPIM DWC_ETHER_QOS (RXPAUSPIM):** MMC Receive Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value.
19	0h RW	**RXORANGEPIM DWC_ETHER_QOS (RXORANGEPIM):** MMC Receive Out Of Range Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoutofrangetype counter reaches half of the maximum value or the maximum value.
18	0h RW	**RXLENERPIM DWC_ETHER_QOS (RXLENERPIM):** MMC Receive Length Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value.
17	0h RW	**RXUCGPIM DWC_ETHER_QOS (RXUCGPIM):** MMC Receive Unicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value.
16	0h RW	**RX1024TMAXOCTGBPIM DWC_ETHER_QOS (RX1024TMAXOCTGBPIM):** MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask. Setting this bit masks the interrupt when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value.
15	0h RW	**RX512T1023OCTGBPIM DWC_ETHER_QOS (RX512T1023OCTGBPIM):** MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value.
14	0h RW	**RX256T511OCTGBPIM DWC_ETHER_QOS (RX256T511OCTGBPIM):** MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value.
13	0h RW	**RX128T255OCTGBPIM DWC_ETHER_QOS (RX128T255OCTGBPIM):** MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value.
12	0h RW	**RX65T127OCTGBPIM DWC_ETHER_QOS (RX65T127OCTGBPIM):** MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value.
11	0h RW	**RX64OCTGBPIM DWC_ETHER_QOS (RX64OCTGBPIM):** MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx64octets_gb counter reaches half of the maximum value or the maximum value.
10	0h RW	**RXOSIZEGPIM DWC_ETHER_QOS (RXOSIZEGPIM):** MMC Receive Oversize Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**RXUSIZEGPIM DWC_ETHER_QOS (RXUSIZEGPIM):** MMC Receive Undersize Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxundersize_g counter reaches half of the maximum value or the maximum value.
8	0h RW	**RXJABERPIM DWC_ETHER_QOS (RXJABERPIM):** MMC Receive Jabber Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxjabbererror counter reaches half of the maximum value or the maximum value.
7	0h RW	**RXRUNTPIM DWC_ETHER_QOS (RXRUNTPIM):** MMC Receive Runt Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxrunterror counter reaches half of the maximum value or the maximum value.
6	0h RW	**RXALGNERPIM DWC_ETHER_QOS (RXALGNERPIM):** MMC Receive Alignment Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxalignmenterror counter reaches half of the maximum value or the maximum value.
5	0h RW	**RXCRCERPIM DWC_ETHER_QOS (RXCRCERPIM):** MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value.
4	0h RW	**RXMCGPIM DWC_ETHER_QOS (RXMCGPIM):** MMC Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value.
3	0h RW	**RXBCGPIM DWC_ETHER_QOS (RXBCGPIM):** MMC Receive Broadcast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value.
2	0h RW	**RXGOCTIM DWC_ETHER_QOS (RXGOCTIM):** MMC Receive Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value.
1	0h RW	**RXGBOCTIM DWC_ETHER_QOS (RXGBOCTIM):** MMC Receive Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value.
0	0h RW	**RXGBPKTIM DWC_ETHER_QOS (RXGBPKTIM):** MMC Receive Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value.

21.2.187 MMC_TX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_TX_INTERRUPT_MASK) — Offset 710h

This register maintains the masks for interrupts generated from all Transmit statistics counters. The MMC Transmit Interrupt Mask register maintains the masks for the interrupts generated when the transmit statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 710h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RW	**TXLPITRCIM DWC_ETHER_QOS (TXLPITRCIM):** MMC Transmit LPI transition counter interrupt Mask Setting this bit masks the interrupt when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value.
26	0h RW	**TXLPIUSCIM DWC_ETHER_QOS (TXLPIUSCIM):** MMC Transmit LPI microsecond counter interrupt Mask Setting this bit masks the interrupt when the Tx_LPI_USEC_Cntr counter reaches half of the maximum value or the maximum value.
25	0h RW	**TXOSIZEGPIM DWC_ETHER_QOS (TXOSIZEGPIM):** MMC Transmit Oversize Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txoversize_g counter reaches half of the maximum value or the maximum value.
24	0h RW	**TXVLANGPIM DWC_ETHER_QOS (TXVLANGPIM):** MMC Transmit VLAN Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txvlanpackets_g counter reaches half of the maximum value or the maximum value.
23	0h RW	**TXPAUSPIM DWC_ETHER_QOS (TXPAUSPIM):** MMC Transmit Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value.
22	0h RW	**TXEXDEFPIM DWC_ETHER_QOS (TXEXDEFPIM):** MMC Transmit Excessive Deferral Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txexcessdef counter reaches half of the maximum value or the maximum value.
21	0h RW	**TXGPKTIM DWC_ETHER_QOS (TXGPKTIM):** MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value.
20	0h RW	**TXGOCTIM DWC_ETHER_QOS (TXGOCTIM):** MMC Transmit Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value.
19	0h RW	**TXCARERPIM DWC_ETHER_QOS (TXCARERPIM):** MMC Transmit Carrier Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value.
18	0h RW	**TXEXCOLPIM DWC_ETHER_QOS (TXEXCOLPIM):** MMC Transmit Excessive Collision Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txexcesscol counter reaches half of the maximum value or the maximum value.
17	0h RW	**TXLATCOLPIM DWC_ETHER_QOS (TXLATCOLPIM):** MMC Transmit Late Collision Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txlatecol counter reaches half of the maximum value or the maximum value.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**TXDEFPIM DWC_ETHER_QOS (TXDEFPIM):** MMC Transmit Deferred Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txdeferred counter reaches half of the maximum value or the maximum value.
15	0h RW	**TXMCOLGPIM DWC_ETHER_QOS (TXMCOLGPIM):** MMC Transmit Multiple Collision Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txmulticol_g counter reaches half of the maximum value or the maximum value.
14	0h RW	**TXSCOLGPIM DWC_ETHER_QOS (TXSCOLGPIM):** MMC Transmit Single Collision Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txsinglecol_g counter reaches half of the maximum value or the maximum value.
13	0h RW	**TXUFLOWERPIM DWC_ETHER_QOS (TXUFLOWERPIM):** MMC Transmit Underflow Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value.
12	0h RW	**TXBCGBPIM DWC_ETHER_QOS (TXBCGBPIM):** MMC Transmit Broadcast Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txbroadcastpackets_gb counter reaches half of the maximum value or the maximum value.
11	0h RW	**TXMCGBPIM DWC_ETHER_QOS (TXMCGBPIM):** MMC Transmit Multicast Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txmulticastpackets_gb counter reaches half of the maximum value or the maximum value.
10	0h RW	**TXUCGBPIM DWC_ETHER_QOS (TXUCGBPIM):** MMC Transmit Unicast Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunicastpackets_gb counter reaches half of the maximum value or the maximum value.
9	0h RW	**TX1024TMAXOCTGBPIM DWC_ETHER_QOS (TX1024TMAXOCTGBPIM):** MMC Transmit 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the tx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value.
8	0h RW	**TX512T1023OCTGBPIM DWC_ETHER_QOS (TX512T1023OCTGBPIM):** MMC Transmit 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the tx512to1023octets_gb counter reaches half of the maximum value or the maximum value.
7	0h RW	**TX256T511OCTGBPIM DWC_ETHER_QOS (TX256T511OCTGBPIM):** MMC Transmit 256 to 511 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the tx256to511octets_gb counter reaches half of the maximum value or the maximum value.
6	0h RW	**TX128T255OCTGBPIM DWC_ETHER_QOS (TX128T255OCTGBPIM):** MMC Transmit 128 to 255 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the tx128to255octets_gb counter reaches half of the maximum value or the maximum value.
5	0h RW	**TX65T127OCTGBPIM DWC_ETHER_QOS (TX65T127OCTGBPIM):** MMC Transmit 65 to 127 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the tx65to127octets_gb counter reaches half of the maximum value or the maximum value.
4	0h RW	**TX64OCTGBPIM DWC_ETHER_QOS (TX64OCTGBPIM):** MMC Transmit 64 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the tx64octets_gb counter reaches half of the maximum value or the maximum value.
3	0h RW	**TXMCGPIM DWC_ETHER_QOS (TXMCGPIM):** MMC Transmit Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**TXBCGPIM DWC_ETHER_QOS (TXBCGPIM):** MMC Transmit Broadcast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value.
1	0h RW	**TXGBPKTIM DWC_ETHER_QOS (TXGBPKTIM):** MMC Transmit Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value.
0	0h RW	**TXGBOCTIM DWC_ETHER_QOS (TXGBOCTIM):** MMC Transmit Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value.

21.2.188 TX_OCTET_COUNT_GOOD_BAD DWC_ETHER_QOS (TX_OCTET_COUNT_GOOD_BAD) — Offset 714h

This register provides the number of bytes transmitted by the DWC_ether_qos, exclusive of preamble and retried bytes, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 714h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXOCTGB DWC_ETHER_QOS (TXOCTGB):** Tx Octet Count Good Bad This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

21.2.189 TX_PACKET_COUNT_GOOD_BAD DWC_ETHER_QOS (TX_PACKET_COUNT_GOOD_BAD) — Offset 718h

This register provides the number of good and bad packets transmitted by DWC_ether_qos, exclusive of retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 718h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXPKTGB DWC_ETHER_QOS (TXPKTGB):** Tx Packet Count Good Bad This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

21.2.190 TX_BROADCAST_PACKETS_GOOD DWC_ETHER_QOS (TX_BROADCAST_PACKETS_GOOD) — Offset 71Ch

This register provides the number of good broadcast packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 71Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXBCASTG DWC_ETHER_QOS (TXBCASTG):** Tx Broadcast Packets Good This field indicates the number of good broadcast packets transmitted.

21.2.191 TX_MULTICAST_PACKETS_GOOD DWC_ETHER_QOS (TX_MULTICAST_PACKETS_GOOD) — Offset 720h

This register provides the number of good multicast packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 720h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXMCASTG DWC_ETHER_QOS (TXMCASTG):** Tx Multicast Packets Good This field indicates the number of good multicast packets transmitted.

21.2.192 TX_64OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_64OCTETS_PACKETS_GOOD_BAD) — Offset 724h

This register provides the number of good and bad packets transmitted by DWC_ether_qos with length 64 bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 724h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TX64OCTGB DWC_ETHER_QOS (TX64OCTGB):** Tx 64Octets Packets Good_Bad This field indicates the number of good and bad packets transmitted with length 64 bytes, exclusive of preamble and retried packets.

21.2.193 TX_65TO127OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_65TO127OCTETS_PACKETS_GOOD_BAD) — Offset 728h

This register provides the number of good and bad packets transmitted by DWC_ether_qos with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 728h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TX65_127OCTGB DWC_ETHER_QOS (TX65_127OCTGB):** Tx 65To127Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 65 and 127 (inclusive) bytes, exclusive of preamble and retried packets.

21.2.194 TX_128TO255OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_128TO255OCTETS_PACKETS_GOOD_BAD) — Offset 72Ch

This register provides the number of good and bad packets transmitted by DWC_ether_qos with length between 128 to 255 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 72Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TX128_255OCTGB DWC_ETHER_QOS (TX128_255OCTGB):** Tx 128To255Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 128 and 255 (inclusive) bytes, exclusive of preamble and retried packets.

21.2.195 TX_256TO511OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_256TO511OCTETS_PACKETS_GOOD_BAD) — Offset 730h

This register provides the number of good and bad packets transmitted by DWC_ether_qos with length between 256 to 511 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 730h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TX256_511OCTGB DWC_ETHER_QOS (TX256_511OCTGB):** Tx 256To511Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 256 and 511 (inclusive) bytes, exclusive of preamble and retried packets.

21.2.196 TX_512TO1023OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_512TO1023OCTETS_PACKETS_GOOD_BAD) — Offset 734h

This register provides the number of good and bad packets transmitted by DWC_ether_qos with length 512 to 1023 (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 734h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TX512_1023OCTGB DWC_ETHER_QOS (TX512_1023OCTGB):** Tx 512To1023Octets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 512 and 1023 (inclusive) bytes, exclusive of preamble and retried packets.

21.2.197 TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD) — Offset 738h

This register provides the number of good and bad packets transmitted by DWC_ether_qos with length 1024 to maxsize (inclusive) bytes, exclusive of preamble and retried packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 738h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TX1024_MAXOCTGB DWC_ETHER_QOS (TX1024_MAXOCTGB):** Tx 1024ToMaxOctets Packets Good Bad This field indicates the number of good and bad packets transmitted with length between 1024 and maxsize (inclusive) bytes, exclusive of preamble and retried packets.

21.2.198 TX_UNICAST_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_UNICAST_PACKETS_GOOD_BAD) — Offset 73Ch

This register provides the number of good and bad unicast packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 73Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXUCASTGB DWC_ETHER_QOS (TXUCASTGB):** Tx Unicast Packets Good Bad This field indicates the number of good and bad unicast packets transmitted.

21.2.199 TX_MULTICAST_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_MULTICAST_PACKETS_GOOD_BAD) — Offset 740h

This register provides the number of good and bad multicast packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 740h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXMCASTGB DWC_ETHER_QOS (TXMCASTGB):** Tx Multicast Packets Good Bad This field indicates the number of good and bad multicast packets transmitted.

21.2.200 TX_BROADCAST_PACKETS_GOOD_BAD DWC_ETHER_QOS (TX_BROADCAST_PACKETS_GOOD_BAD) — Offset 744h

This register provides the number of good and bad broadcast packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 744h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXBCASTGB DWC_ETHER_QOS (TXBCASTGB):** Tx Broadcast Packets Good Bad This field indicates the number of good and bad broadcast packets transmitted.

21.2.201 TX_UNDERFLOW_ERROR_PACKETS DWC_ETHER_QOS (TX_UNDERFLOW_ERROR_PACKETS) — Offset 748h

This register provides the number of packets aborted by DWC_ether_qos because of packets underflow error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 748h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXUNDRFLW DWC_ETHER_QOS (TXUNDRFLW):** Tx Underflow Error Packets This field indicates the number of packets aborted because of packets underflow error.

21.2.202 TX_SINGLE_COLLISION_GOOD_PACKETS DWC_ETHER_QOS (TX_SINGLE_COLLISION_GOOD_PACKETS) — Offset 74Ch

This register provides the number of successfully transmitted packets by DWC_ether_qos after a single collision in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 74Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXSNGLCOLG DWC_ETHER_QOS (TXSNGLCOLG):** Tx Single Collision Good Packets This field indicates the number of successfully transmitted packets after a single collision in the half-duplex mode.

21.2.203 TX_MULTIPLE_COLLISION_GOOD_PACKETS DWC_ETHER_QOS (TX_MULTIPLE_COLLISION_GOOD_PACKETS) — Offset 750h

This register provides the number of successfully transmitted packets by DWC_ether_qos after multiple collisions in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 750h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXMULTCOLG DWC_ETHER_QOS (TXMULTCOLG):** Tx Multiple Collision Good Packets This field indicates the number of successfully transmitted packets after multiple collisions in the half-duplex mode.

21.2.204 TX_DEFERRED_PACKETS DWC_ETHER_QOS (TX_DEFERRED_PACKETS) — Offset 754h

This register provides the number of successfully transmitted by DWC_ether_qos after a deferral in the half-duplex mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 754h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXDEFRD DWC_ETHER_QOS (TXDEFRD):** Tx Deferred Packets This field indicates the number of successfully transmitted after a deferral in the half-duplex mode.

21.2.205 TX_LATE_COLLISION_PACKETS DWC_ETHER_QOS (TX_LATE_COLLISION_PACKETS) — Offset 758h

This register provides the number of packets aborted by DWC_ether_qos because of late collision error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 758h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXLATECOL DWC_ETHER_QOS (TXLATECOL):** Tx Late Collision Packets This field indicates the number of packets aborted because of late collision error.

21.2.206 TX_EXCESSIVE_COLLISION_PACKETS DWC_ETHER_QOS (TX_EXCESSIVE_COLLISION_PACKETS) — Offset 75Ch

This register provides the number of packets aborted by DWC_ether_qos because of excessive (16) collision errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 75Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXEXSCOL DWC_ETHER_QOS (TXEXSCOL):** Tx Excessive Collision Packets This field indicates the number of packets aborted because of excessive (16) collision errors.

21.2.207 TX_CARRIER_ERROR_PACKETS DWC_ETHER_QOS (TX_CARRIER_ERROR_PACKETS) — Offset 760h

This register provides the number of packets aborted by DWC_ether_qos because of carrier sense error (no carrier or loss of carrier).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 760h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXCARR DWC_ETHER_QOS (TXCARR):** Tx Carrier Error Packets This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

21.2.208 TX_OCTET_COUNT_GOOD DWC_ETHER_QOS (TX_OCTET_COUNT_GOOD) — Offset 764h

This register provides the number of bytes transmitted by DWC_ether_qos, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 764h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXOCTG DWC_ETHER_QOS (TXOCTG):** Tx Octet Count Good This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

21.2.209 TX_PACKET_COUNT_GOOD DWC_ETHER_QOS (TX_PACKET_COUNT_GOOD) — Offset 768h

This register provides the number of good packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 768h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXPKTG DWC_ETHER_QOS (TXPKTG):** Tx Packet Count Good This field indicates the number of good packets transmitted.

21.2.210 TX_EXCESSIVE_DEFERRAL_ERROR DWC_ETHER_QOS (TX_EXCESSIVE_DEFERRAL_ERROR) — Offset 76Ch

This register provides the number of packets aborted by DWC_ether_qos because of excessive deferral error (deferred for more than two max-sized packet times).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 76Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXEXSDEF DWC_ETHER_QOS (TXEXSDEF):** Tx Excessive Deferral Error This field indicates the number of packets aborted because of excessive deferral error (deferred for more than two max-sized packet times).

21.2.211 TX_PAUSE_PACKETS DWC_ETHER_QOS (TX_PAUSE_PACKETS) — Offset 770h

This register provides the number of good Pause packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 770h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXPAUSE DWC_ETHER_QOS (TXPAUSE):** Tx Pause Packets This field indicates the number of good Pause packets transmitted.

21.2.212 TX_VLAN_PACKETS_GOOD DWC_ETHER_QOS (TX_VLAN_PACKETS_GOOD) — Offset 774h

This register provides the number of good VLAN packets transmitted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 774h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXVLANG DWC_ETHER_QOS (TXVLANG):** Tx VLAN Packets Good This field provides the number of good VLAN packets transmitted.

21.2.213 TX_OSIZE_PACKETS_GOOD DWC_ETHER_QOS (TX_OSIZE_PACKETS_GOOD) — Offset 778h

This register provides the number of packets transmitted by DWC_ether_qos without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 778h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXOSIZG DWC_ETHER_QOS (TXOSIZG):** Tx OSize Packets Good This field indicates the number of packets transmitted without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register).

21.2.214 RX_PACKETS_COUNT_GOOD_BAD DWC_ETHER_QOS (RX_PACKETS_COUNT_GOOD_BAD) — Offset 780h

This register provides the number of good and bad packets received by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 780h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXPKTGB DWC_ETHER_QOS (RXPKTGB):** Rx Packets Count Good Bad This field indicates the number of good and bad packets received.

21.2.215 RX_OCTET_COUNT_GOOD_BAD DWC_ETHER_QOS (RX_OCTET_COUNT_GOOD_BAD) — Offset 784h

This register provides the number of bytes received by DWC_ther_qos, exclusive of preamble, in good and bad packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 784h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXOCTGB DWC_ETHER_QOS (RXOCTGB):** Rx Octet Count Good Bad This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

21.2.216 RX_OCTET_COUNT_GOOD DWC_ETHER_QOS (RX_OCTET_COUNT_GOOD) — Offset 788h

This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, only in good packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 788h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXOCTG DWC_ETHER_QOS (RXOCTG):** Rx Octet Count Good This field indicates the number of bytes received, exclusive of preamble, only in good packets.

21.2.217 RX_BROADCAST_PACKETS_GOOD DWC_ETHER_QOS (RX_BROADCAST_PACKETS_GOOD) — Offset 78Ch

This register provides the number of good broadcast packets received by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 78Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXBCASTG DWC_ETHER_QOS (RXBCASTG):** Rx Broadcast Packets Good This field indicates the number of good broadcast packets received.

21.2.218 RX_MULTICAST_PACKETS_GOOD DWC_ETHER_QOS (RX_MULTICAST_PACKETS_GOOD) — Offset 790h

This register provides the number of good multicast packets received by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 790h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXMCASTG DWC_ETHER_QOS (RXMCASTG):** Rx Multicast Packets Good This field indicates the number of good multicast packets received.

21.2.219 RX_CRC_ERROR_PACKETS DWC_ETHER_QOS (RX_CRC_ERROR_PACKETS) — Offset 794h

This register provides the number of packets received by DWC_ether_qos with CRC error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 794h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXCRCERR DWC_ETHER_QOS (RXCRCERR):** Rx CRC Error Packets This field indicates the number of packets received with CRC error.

21.2.220 RX_ALIGNMENT_ERROR_PACKETS DWC_ETHER_QOS (RX_ALIGNMENT_ERROR_PACKETS) — Offset 798h

This register provides the number of packets received by DWC_ether_qos with alignment (dribble) error. It is valid only in 10/100 mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 798h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXALGNERR DWC_ETHER_QOS (RXALGNERR):** Rx Alignment Error Packets This field indicates the number of packets received with alignment (dribble) error. It is valid only in 10/100 mode.

21.2.221 RX_RUNT_ERROR_PACKETS DWC_ETHER_QOS (RX_RUNT_ERROR_PACKETS) — Offset 79Ch

This register provides the number of packets received by DWC_ether_qos with runt (length less than 64 bytes and CRC error) error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 79Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXRUNTERR DWC_ETHER_QOS (RXRUNTERR):** Rx Runt Error Packets This field indicates the number of packets received with runt (length less than 64 bytes and CRC error) error.

21.2.222 RX_JABBER_ERROR_PACKETS DWC_ETHER_QOS (RX_JABBER_ERROR_PACKETS) — Offset 7A0h

This register provides the number of giant packets received by DWC_ether_qos with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXJABERR DWC_ETHER_QOS (RXJABERR):** Rx Jabber Error Packets This field indicates the number of giant packets received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets.

21.2.223 RX_UNDERSIZE_PACKETS_GOOD DWC_ETHER_QOS (RX_UNDERSIZE_PACKETS_GOOD) — Offset 7A4h

This register provides the number of packets received by DWC_ether_qos with length less than 64 bytes, without any errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXUNDERSZG DWC_ETHER_QOS (RXUNDERSZG):** Rx Undersize Packets Good This field indicates the number of packets received with length less than 64 bytes, without any errors.

21.2.224 RX_OVERSIZE_PACKETS_GOOD DWC_ETHER_QOS (RX_OVERSIZE_PACKETS_GOOD) — Offset 7A8h

This register provides the number of packets received by DWC_ether_qos without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXOVERSZG DWC_ETHER_QOS (RXOVERSZG):** Rx Oversize Packets Good This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register).

21.2.225 RX_64OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_64OCTETS_PACKETS_GOOD_BAD) — Offset 7ACh

This register provides the number of good and bad packets received by DWC_ether_qos with length 64 bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RX64OCTGB DWC_ETHER_QOS (RX64OCTGB):** Rx 64 Octets Packets Good Bad This field indicates the number of good and bad packets received with length 64 bytes, exclusive of the preamble.

21.2.226 RX_65TO127OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_65TO127OCTETS_PACKETS_GOOD_BAD) — Offset 7B0h

This register provides the number of good and bad packets received by DWC_ether_qos with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RX65_127OCTGB DWC_ETHER_QOS (RX65_127OCTGB):** Rx 65-127 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 65 and 127 (inclusive) bytes, exclusive of the preamble.

21.2.227 RX_128TO255OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_128TO255OCTETS_PACKETS_GOOD_BAD) — Offset 7B4h

This register provides the number of good and bad packets received by DWC_ether_qos with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RX128_255OCTGB DWC_ETHER_QOS (RX128_255OCTGB):** Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble.

21.2.228 RX_256TO511OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_256TO511OCTETS_PACKETS_GOOD_BAD) — Offset 7B8h

This register provides the number of good and bad packets received by DWC_ether_qos with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7B8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RX256_511OCTGB DWC_ETHER_QOS (RX256_511OCTGB):** Rx 256-511 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 256 and 511 (inclusive) bytes, exclusive of the preamble.

21.2.229 RX_512TO1023OCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_512TO1023OCTETS_PACKETS_GOOD_BAD) — Offset 7BCh

This register provides the number of good and bad packets received by DWC_ether_qos with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7BCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RX512_1023OCTGB DWC_ETHER_QOS (RX512_1023OCTGB):** RX 512-1023 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble.

21.2.230 RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD) — Offset 7C0h

This register provides the number of good and bad packets received by DWC_ether_qos with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RX1024_MAXOCTGB DWC_ETHER_QOS (RX1024_MAXOCTGB):** Rx 1024-Max Octets Good Bad This field indicates the number of good and bad packets received with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble.

21.2.231 RX_UNICAST_PACKETS_GOOD DWC_ETHER_QOS (RX_UNICAST_PACKETS_GOOD) — Offset 7C4h

This register provides the number of good unicast packets received by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXUCASTG DWC_ETHER_QOS (RXUCASTG):** Rx Unicast Packets Good This field indicates the number of good unicast packets received.

21.2.232 RX_LENGTH_ERROR_PACKETS DWC_ETHER_QOS (RX_LENGTH_ERROR_PACKETS) — Offset 7C8h

This register provides the number of packets received by DWC_ether_qos with length error (Length Type field not equal to packet size), for all packets with valid length field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXLENERR DWC_ETHER_QOS (RXLENERR):** Rx Length Error Packets This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

21.2.233 RX_OUT_OF_RANGE_TYPE_PACKETS DWC_ETHER_QOS (RX_OUT_OF_RANGE_TYPE_PACKETS) — Offset 7CCh

This register provides the number of packets received by DWC_ether_qos with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXOUTOFRNG DWC_ETHER_QOS (RXOUTOFRNG):** Rx Out of Range Type Packet This field indicates the number of packets received with length field not equal to the valid packet size (greater than 1,500 but less than 1,536).

21.2.234 RX_PAUSE_PACKETS DWC_ETHER_QOS (RX_PAUSE_PACKETS) — Offset 7D0h

This register provides the number of good and valid Pause packets received by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXPAUSEPKT DWC_ETHER_QOS (RXPAUSEPKT):** Rx Pause Packets This field indicates the number of good and valid Pause packets received.

21.2.235 RX_FIFO_OVERFLOW_PACKETS DWC_ETHER_QOS (RX_FIFO_OVERFLOW_PACKETS) — Offset 7D4h

This register provides the number of missed received packets because of FIFO overflow in DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXFIFOOVFL DWC_ETHER_QOS (RXFIFOOVFL):** Rx FIFO Overflow Packets This field indicates the number of missed received packets because of FIFO overflow.

21.2.236 RX_VLAN_PACKETS_GOOD_BAD DWC_ETHER_QOS (RX_VLAN_PACKETS_GOOD_BAD) — Offset 7D8h

This register provides the number of good and bad VLAN packets received by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7D8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXVLANPKTGB DWC_ETHER_QOS (RXVLANPKTGB):** Rx VLAN Packets Good Bad This field indicates the number of good and bad VLAN packets received.

21.2.237 RX_WATCHDOG_ERROR_PACKETS DWC_ETHER_QOS (RX_WATCHDOG_ERROR_PACKETS) — Offset 7DCh

This register provides the number of packets received by DWC_ether_qos with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7DCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXWDGERR DWC_ETHER_QOS (RXWDGERR):** Rx Watchdog Error Packets This field indicates the number of packets received with error because of watchdog timeout error (packets with a data load larger than 2,048 bytes (when JE and WD bits are reset in MAC_Configuration register), 10,240 bytes (when JE bit is set and WD bit is reset in MAC_Configuration register), 16,384 bytes (when WD bit is set in MAC_Configuration register) or the value programmed in the MAC_Watchdog_Timeout register).

21.2.238 RX_RECEIVE_ERROR_PACKETS DWC_ETHER_QOS (RX_RECEIVE_ERROR_PACKETS) — Offset 7E0h

This register provides the number of packets received by DWC_ether_qos with Receive error or Packet Extension error on the GMII or MII interface.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXRCVERR DWC_ETHER_QOS (RXRCVERR):** Rx Receive Error Packets This field indicates the number of packets received with Receive error or Packet Extension error on the GMII or MII interface.

21.2.239 RX_CONTROL_PACKETS_GOOD DWC_ETHER_QOS (RX_CONTROL_PACKETS_GOOD) — Offset 7E4h

This register provides the number of good control packets received by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7E4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXCTRLG DWC_ETHER_QOS (RXCTRLG):** Rx Control Packets Good This field indicates the number of good control packets received.

21.2.240 TX_LPI_USEC_CNTR DWC_ETHER_QOS (TX_LPI_USEC_CNTR) — Offset 7ECh

This register provides the number of microseconds Tx LPI is asserted by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7ECh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXLPIUSC DWC_ETHER_QOS (TXLPIUSC):** Tx LPI Microseconds Counter This field indicates the number of microseconds Tx LPI is asserted. For every Tx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

21.2.241 TX_LPI_TRAN_CNTR DWC_ETHER_QOS (TX_LPI_TRAN_CNTR) — Offset 7F0h

This register provides the number of times DWC_ether_qos has entered Tx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXLPITRC DWC_ETHER_QOS (TXLPITRC):** Tx LPI Transition counter This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter will increment.

21.2.242 RX_LPI_USEC_CNTR DWC_ETHER_QOS (RX_LPI_USEC_CNTR) — Offset 7F4h

This register provides the number of microseconds Rx LPI is sampled by DWC_ether_qos.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXLPIUSC DWC_ETHER_QOS (RXLPIUSC):** Rx LPI Microseconds Counter This field indicates the number of microseconds Rx LPI is asserted. For every Rx LPI Entry and Exit, the Timer value can have an error of +/- 1 microsecond.

21.2.243 RX_LPI_TRAN_CNTR DWC_ETHER_QOS (RX_LPI_TRAN_CNTR) — Offset 7F8h

This register provides the number of times DWC_ether_qos has entered Rx LPI.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 7F8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXLPITRC DWC_ETHER_QOS (RXLPITRC):** Rx LPI Transition counter This field indicates the number of times Rx LPI Entry has occurred.

21.2.244 MMC_IPC_RX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_IPC_RX_INTERRUPT_MASK) — Offset 800h

This register maintains the mask for the interrupt generated from the receive IPC statistic counters. The MMC Receive Checksum Off load Interrupt Mask register maintains the masks for the interrupts generated when the receive IPC (Checksum Off load) statistic counters reach half their maximum value, and when they reach their maximum values. This register is 32 bits wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 800h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW	**RXICMPEROIM DWC_ETHER_QOS (RXICMPEROIM):** MMC Receive ICMP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value.
28	0h RW	**RXICMPGOIM DWC_ETHER_QOS (RXICMPGOIM):** MMC Receive ICMP Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value.
27	0h RW	**RXTCPEROIM DWC_ETHER_QOS (RXTCPEROIM):** MMC Receive TCP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value.
26	0h RW	**RXTCPGOIM DWC_ETHER_QOS (RXTCPGOIM):** MMC Receive TCP Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value.

Bit Range	Default & Access	Field Name (ID): Description
25	0h RW	**RXUDPEROIM DWC_ETHER_QOS (RXUDPEROIM):** MMC Receive UDP Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value.
24	0h RW	**RXUDPGOIM DWC_ETHER_QOS (RXUDPGOIM):** MMC Receive IPV6 No Payload Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value.
23	0h RW	**RXIPV6NOPAYOIM DWC_ETHER_QOS (RXIPV6NOPAYOIM):** MMC Receive IPV6 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value.
22	0h RW	**RXIPV6HEROIM DWC_ETHER_QOS (RXIPV6HEROIM):** MMC Receive IPV6 Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value.
21	0h RW	**RXIPV6GOIM DWC_ETHER_QOS (RXIPV6GOIM):** MMC Receive IPV6 Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value.
20	0h RW	**RXIPV4UDSBLOIM DWC_ETHER_QOS (RXIPV4UDSBLOIM):** MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value.
19	0h RW	**RXIPV4FRAGOIM DWC_ETHER_QOS (RXIPV4FRAGOIM):** MMC Receive IPV4 Fragmented Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value.
18	0h RW	**RXIPV4NOPAYOIM DWC_ETHER_QOS (RXIPV4NOPAYOIM):** MMC Receive IPV4 No Payload Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value.
17	0h RW	**RXIPV4HEROIM DWC_ETHER_QOS (RXIPV4HEROIM):** MMC Receive IPV4 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value.
16	0h RW	**RXIPV4GOIM DWC_ETHER_QOS (RXIPV4GOIM):** MMC Receive IPV4 Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value.
15:14	0h RO	**Reserved**
13	0h RW	**RXICMPERPIM DWC_ETHER_QOS (RXICMPERPIM):** MMC Receive ICMP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value.
12	0h RW	**RXICMPGPIM DWC_ETHER_QOS (RXICMPGPIM):** MMC Receive ICMP Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value.
11	0h RW	**RXTCPERPIM DWC_ETHER_QOS (RXTCPERPIM):** MMC Receive TCP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**RXTCPGPIM DWC_ETHER_QOS (RXTCPGPIM):** MMC Receive TCP Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value.
9	0h RW	**RXUDPERPIM DWC_ETHER_QOS (RXUDPERPIM):** MMC Receive UDP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value.
8	0h RW	**RXUDPGPIM DWC_ETHER_QOS (RXUDPGPIM):** MMC Receive UDP Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value.
7	0h RW	**RXIPV6NOPAYPIM DWC_ETHER_QOS (RXIPV6NOPAYPIM):** MMC Receive IPV6 No Payload Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value.
6	0h RW	**RXIPV6HERPIM DWC_ETHER_QOS (RXIPV6HERPIM):** MMC Receive IPV6 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value.
5	0h RW	**RXIPV6GPIM DWC_ETHER_QOS (RXIPV6GPIM):** MMC Receive IPV6 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value.
4	0h RW	**RXIPV4UDSBLPIM DWC_ETHER_QOS (RXIPV4UDSBLPIM):** MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value.
3	0h RW	**RXIPV4FRAGPIM DWC_ETHER_QOS (RXIPV4FRAGPIM):** MMC Receive IPV4 Fragmented Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value.
2	0h RW	**RXIPV4NOPAYPIM DWC_ETHER_QOS (RXIPV4NOPAYPIM):** MMC Receive IPV4 No Payload Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value.
1	0h RW	**RXIPV4HERPIM DWC_ETHER_QOS (RXIPV4HERPIM):** MMC Receive IPV4 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value.
0	0h RW	**RXIPV4GPIM DWC_ETHER_QOS (RXIPV4GPIM):** MMC Receive IPV4 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value.

21.2.245 MMC_IPC_RX_INTERRUPT DWC_ETHER_QOS (MMC_IPC_RX_INTERRUPT) — Offset 808h

This register maintains the interrupt that the receive IPC statistic counters generate. The MMC Receive Checksum Offload Interrupt register maintains the interrupts generated when receive IPC statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32 bit counter and 0xFFFF for 16 bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC Receive Checksum Offload Interrupt register is 32 bit wide. When

the MMC IPC counter that caused the interrupt is read, its corresponding interrupt bit is cleared. The counter's least-significant byte lane (Bits[7:0]) must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 808h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RO/V	**RXICMPEROIS DWC_ETHER_QOS (RXICMPEROIS):** MMC Receive ICMP Error Octet Counter Interrupt Status This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
28	0h RO/V	**RXICMPGOIS DWC_ETHER_QOS (RXICMPGOIS):** MMC Receive ICMP Good Octet Counter Interrupt Status This bit is set when the rxicmp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
27	0h RO/V	**RXTCPEROIS DWC_ETHER_QOS (RXTCPEROIS):** MMC Receive TCP Error Octet Counter Interrupt Status This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
26	0h RO/V	**RXTCPGOIS DWC_ETHER_QOS (RXTCPGOIS):** MMC Receive TCP Good Octet Counter Interrupt Status This bit is set when the rxtcp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
25	0h RO/V	**RXUDPEROIS DWC_ETHER_QOS (RXUDPEROIS):** MMC Receive UDP Error Octet Counter Interrupt Status This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
24	0h RO/V	**RXUDPGOIS DWC_ETHER_QOS (RXUDPGOIS):** MMC Receive UDP Good Octet Counter Interrupt Status This bit is set when the rxudp_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
23	0h RO/V	**RXIPV6NOPAYOIS DWC_ETHER_QOS (RXIPV6NOPAYOIS):** MMC Receive IPV6 No Payload Octet Counter Interrupt Status This bit is set when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
22	0h RO/V	**RXIPV6HEROIS DWC_ETHER_QOS (RXIPV6HEROIS):** MMC Receive IPV6 Header Error Octet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
21	0h RO/V	**RXIPV6GOIS DWC_ETHER_QOS (RXIPV6GOIS):** MMC Receive IPV6 Good Octet Counter Interrupt Status This bit is set when the rxipv6_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
20	0h RO/V	**RXIPV4UDSBLOIS DWC_ETHER_QOS (RXIPV4UDSBLOIS):** MMC Receive IPV4 UDP Checksum Disabled Octet Counter Interrupt Status This bit is set when the rxipv4_udsbl_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO/V	**RXIPV4FRAGOIS DWC_ETHER_QOS (RXIPV4FRAGOIS):** MMC Receive IPV4 Fragmented Octet Counter Interrupt Status This bit is set when the rxipv4_frag_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
18	0h RO/V	**RXIPV4NOPAYOIS DWC_ETHER_QOS (RXIPV4NOPAYOIS):** MMC Receive IPV4 No Payload Octet Counter Interrupt Status This bit is set when the rxipv4_nopay_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
17	0h RO/V	**RXIPV4HEROIS DWC_ETHER_QOS (RXIPV4HEROIS):** MMC Receive IPV4 Header Error Octet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
16	0h RO/V	**RXIPV4GOIS DWC_ETHER_QOS (RXIPV4GOIS):** MMC Receive IPV4 Good Octet Counter Interrupt Status This bit is set when the rxipv4_gd_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:14	0h RO	**Reserved**
13	0h RO/V	**RXICMPERPIS DWC_ETHER_QOS (RXICMPERPIS):** MMC Receive ICMP Error Packet Counter Interrupt Status This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
12	0h RO/V	**RXICMPGPIS DWC_ETHER_QOS (RXICMPGPIS):** MMC Receive ICMP Good Packet Counter Interrupt Status This bit is set when the rxicmp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
11	0h RO/V	**RXTCPERPIS DWC_ETHER_QOS (RXTCPERPIS):** MMC Receive TCP Error Packet Counter Interrupt Status This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
10	0h RO/V	**RXTCPGPIS DWC_ETHER_QOS (RXTCPGPIS):** MMC Receive TCP Good Packet Counter Interrupt Status This bit is set when the rxtcp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
9	0h RO/V	**RXUDPERPIS DWC_ETHER_QOS (RXUDPERPIS):** MMC Receive UDP Error Packet Counter Interrupt Status This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
8	0h RO/V	**RXUDPGPIS DWC_ETHER_QOS (RXUDPGPIS):** MC Receive UDP Good Packet Counter Interrupt Status This bit is set when the rxudp_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
7	0h RO/V	**RXIPV6NOPAYPIS DWC_ETHER_QOS (RXIPV6NOPAYPIS):** MMC Receive IPV6 No Payload Packet Counter Interrupt Status This bit is set when the rxipv6_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
6	0h RO/V	**RXIPV6HERPIS DWC_ETHER_QOS (RXIPV6HERPIS):** MMC Receive IPV6 Header Error Packet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
5	0h RO/V	**RXIPV6GPIS DWC_ETHER_QOS (RXIPV6GPIS):** MMC Receive IPV6 Good Packet Counter Interrupt Status This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO/V	**RXIPV4UDSBLPIS DWC_ETHER_QOS (RXIPV4UDSBLPIS):** MMC Receive IPV4 UDP Checksum Disabled Packet Counter Interrupt Status This bit is set when the rxipv4_udsbl_pkts counter reaches half of the maximum value or the maximum value.
3	0h RO/V	**RXIPV4FRAGPIS DWC_ETHER_QOS (RXIPV4FRAGPIS):** MMC Receive IPV4 Fragmented Packet Counter Interrupt Status This bit is set when the rxipv4_frag_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
2	0h RO/V	**RXIPV4NOPAYPIS DWC_ETHER_QOS (RXIPV4NOPAYPIS):** MMC Receive IPV4 No Payload Packet Counter Interrupt Status This bit is set when the rxipv4_nopay_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
1	0h RO/V	**RXIPV4HERPIS DWC_ETHER_QOS (RXIPV4HERPIS):** MMC Receive IPV4 Header Error Packet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.
0	0h RO/V	**RXIPV4GPIS DWC_ETHER_QOS (RXIPV4GPIS):** MMC Receive IPV4 Good Packet Counter Interrupt Status This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.

21.2.246 RXIPV4_GOOD_PACKETS DWC_ETHER_QOS (RXIPV4_GOOD_PACKETS) — Offset 810h

This register provides the number of good IPv4 datagrams received by DWC_ether_qos with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 810h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4GDPKT DWC_ETHER_QOS (RXIPV4GDPKT):** RxIPv4 Good Packets This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

21.2.247 RXIPV4_HEADER_ERROR_PACKETS DWC_ETHER_QOS (RXIPV4_HEADER_ERROR_PACKETS) — Offset 814h

RxIPv4 Header Error Packets This register provides the number of IPv4 datagrams received by DWC_ether_qos with header (checksum, length, or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 814h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4HDRERRPKT DWC_ETHER_QOS (RXIPV4HDRERRPKT):** RxIPv4 Header Error Packets This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

21.2.248 RXIPV4_NO_PAYLOAD_PACKETS DWC_ETHER_QOS (RXIPV4_NO_PAYLOAD_PACKETS) — Offset 818h

This register provides the number of IPv4 datagram packets received by DWC_ether_qos that did not have a TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 818h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4NOPAYPKT DWC_ETHER_QOS (RXIPV4NOPAYPKT):** RxIPv4 Payload Packets This field indicates the number of IPv4 datagram packets received that did not have a TCP, UDP, or ICMP payload.

21.2.249 RXIPV4_FRAGMENTED_PACKETS DWC_ETHER_QOS (RXIPV4_FRAGMENTED_PACKETS) — Offset 81Ch

This register provides the number of good IPv4 datagrams received by DWC_ether_qos with fragmentation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 81Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4FRAGPKT DWC_ETHER_QOS (RXIPV4FRAGPKT):** RxIPv4 Fragmented Packets This field indicates the number of good IPv4 datagrams received with fragmentation.

21.2.250 RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS DWC_ETHER_QOS (RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS) — Offset 820h

This register provides the number of good IPv4 datagrams received by DWC_ether_qos that had a UDP payload with checksum disabled.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 820h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4UDSBLPKT DWC_ETHER_QOS (RXIPV4UDSBLPKT):** RxIPv4 UDP Checksum Disabled Packets This field indicates the number of good IPv4 datagrams received that had a UDP payload with checksum disabled.

21.2.251 RXIPV6_GOOD_PACKETS DWC_ETHER_QOS (RXIPV6_GOOD_PACKETS) — Offset 824h

This register provides the number of good IPv6 datagrams received by DWC_ether_qos with the TCP, UDP, or ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 824h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV6GDPKT DWC_ETHER_QOS (RXIPV6GDPKT):** RxIPv6 Good Packets This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

21.2.252 RXIPV6_HEADER_ERROR_PACKETS DWC_ETHER_QOS (RXIPV6_HEADER_ERROR_PACKETS) — Offset 828h

This register provides the number of IPv6 datagrams received by DWC_ether_qos with header (length or version mismatch) errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 828h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV6HDRERRPKT DWC_ETHER_QOS (RXIPV6HDRERRPKT):** RxIPv6 Header Error Packets This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

21.2.253 RXIPV6_NO_PAYLOAD_PACKETS DWC_ETHER_QOS (RXIPV6_NO_PAYLOAD_PACKETS) — Offset 82Ch

This register provides the number of IPv6 datagram packets received by DWC_ether_qos that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 82Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV6NOPAYPKT DWC_ETHER_QOS (RXIPV6NOPAYPKT):** RxIPv6 Payload Packets This field indicates the number of IPv6 datagram packets received that did not have a TCP, UDP, or ICMP payload. This includes all IPv6 datagrams with fragmentation or security extension headers.

21.2.254 RXUDP_GOOD_PACKETS DWC_ETHER_QOS (RXUDP_GOOD_PACKETS) — Offset 830h

This register provides the number of good IP datagrams received by DWC_ether_qos with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 830h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXUDPGDPKT DWC_ETHER_QOS (RXUDPGDPKT):** RxUDP Good Packets This field indicates the number of good IP datagrams received with a good UDP payload. This counter is not updated when the RxIPv4_UDP_Checksum_Disabled_Packets counter is incremented.

21.2.255 RXUDP_ERROR_PACKETS DWC_ETHER_QOS (RXUDP_ERROR_PACKETS) — Offset 834h

This register provides the number of good IP datagrams received by DWC_ether_qos whose UDP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 834h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXUDPERRPKT DWC_ETHER_QOS (RXUDPERRPKT):** RxUDP Error Packets This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

21.2.256 RXTCP_GOOD_PACKETS DWC_ETHER_QOS (RXTCP_GOOD_PACKETS) — Offset 838h

This register provides the number of good IP datagrams received by DWC_ether_qos with a good TCP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 838h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXTCPGDPKT DWC_ETHER_QOS (RXTCPGDPKT):** RxTCP Good Packets This field indicates the number of good IP datagrams received with a good TCP payload.

21.2.257 RXTCP_ERROR_PACKETS DWC_ETHER_QOS (RXTCP_ERROR_PACKETS) — Offset 83Ch

This register provides the number of good IP datagrams received by DWC_ether_qos whose TCP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 83Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXTCPERRPKT DWC_ETHER_QOS (RXTCPERRPKT):** RxTCP Error Packets This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

21.2.258 RXICMP_GOOD_PACKETS DWC_ETHER_QOS (RXICMP_GOOD_PACKETS) — Offset 840h

This register provides the number of good IP datagrams received by DWC_ether_qos with a good ICMP payload.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 840h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXICMPGDPKT DWC_ETHER_QOS (RXICMPGDPKT):** RxICMP Good Packets This field indicates the number of good IP datagrams received with a good ICMP payload.

21.2.259 RXICMP_ERROR_PACKETS DWC_ETHER_QOS (RXICMP_ERROR_PACKETS) — Offset 844h

This register provides the number of good IP datagrams received by DWC_ether_qos whose ICMP payload has a checksum error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 844h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXICMPERRPKT DWC_ETHER_QOS (RXICMPERRPKT):** RxICMP Error Packets This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

21.2.260 RXIPV4_GOOD_OCTETS DWC_ETHER_QOS (RXIPV4_GOOD_OCTETS) — Offset 850h

This register provides the number of bytes received by DWC_ether_qos in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 850h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4GDOCT DWC_ETHER_QOS (RXIPV4GDOCT):** RxIPv4 Good Octets This field indicates the number of bytes received in good IPv4 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.261 RXIPV4_HEADER_ERROR_OCTETS DWC_ETHER_QOS (RXIPV4_HEADER_ERROR_OCTETS) — Offset 854h

This register provides the number of bytes received by DWC_ether_qos in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 854h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4HDRERROCT DWC_ETHER_QOS (RXIPV4HDRERROCT):** RxIPv4 Header Error Octets This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.262 RXIPV4_NO_PAYLOAD_OCTETS DWC_ETHER_QOS (RXIPV4_NO_PAYLOAD_OCTETS) — Offset 858h

This register provides the number of bytes received by DWC_ether_qos in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 858h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4NOPAYOCT DWC_ETHER_QOS (RXIPV4NOPAYOCT):** RxIPv4 Payload Octets This field indicates the number of bytes received in IPv4 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.263 RXIPV4_FRAGMENTED_OCTETS DWC_ETHER_QOS (RXIPV4_FRAGMENTED_OCTETS) — Offset 85Ch

This register provides the number of bytes received by DWC_ether_qos in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 85Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4FRAGOCT DWC_ETHER_QOS (RXIPV4FRAGOCT):** RxIPv4 Fragmented Octets This field indicates the number of bytes received in fragmented IPv4 datagrams. The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.264 RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS DWC_ETHER_QOS (RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS) — Offset 860h

This register provides the number of bytes received by DWC_ether_qos in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 860h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV4UDSBLOCT DWC_ETHER_QOS (RXIPV4UDSBLOCT):** RxIPv4 UDP Checksum Disable Octets This field indicates the number of bytes received in a UDP segment that had the UDP checksum disabled. This counter does not count IP Header bytes. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.265 RXIPV6_GOOD_OCTETS DWC_ETHER_QOS (RXIPV6_GOOD_OCTETS) — Offset 864h

This register provides the number of bytes received by DWC_ether_qos in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 864h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV6GDOCT DWC_ETHER_QOS (RXIPV6GDOCT):** RxIPv6 Good Octets This field indicates the number of bytes received in good IPv6 datagrams encapsulating TCP, UDP, or ICMP data. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.266 RXIPV6_HEADER_ERROR_OCTETS DWC_ETHER_QOS (RXIPV6_HEADER_ERROR_OCTETS) — Offset 868h

This register provides the number of bytes received by DWC_ether_qos in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 868h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV6HDRERROCT DWC_ETHER_QOS (RXIPV6HDRERROCT):** RxIPv6 Header Error Octets This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.267 RXIPV6_NO_PAYLOAD_OCTETS DWC_ETHER_QOS (RXIPV6_NO_PAYLOAD_OCTETS) — Offset 86Ch

This register provides the number of bytes received by DWC_ether_qos in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 86Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXIPV6NOPAYOCT DWC_ETHER_QOS (RXIPV6NOPAYOCT):** RxIPv6 Payload Octets This field indicates the number of bytes received in IPv6 datagrams that did not have a TCP, UDP, or ICMP payload. The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

21.2.268 RXUDP_GOOD_OCTETS DWC_ETHER_QOS (RXUDP_GOOD_OCTETS) — Offset 870h

This register provides the number of bytes received by DWC_ether_qos in a good UDP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 870h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXUDPGDOCT DWC_ETHER_QOS (RXUDPGDOCT):** RxUDP Good Octets This field indicates the number of bytes received in a good UDP segment. This counter does not count IP header bytes.

21.2.269 RXUDP_ERROR_OCTETS DWC_ETHER_QOS (RXUDP_ERROR_OCTETS) — Offset 874h

This register provides the number of bytes received by DWC_ether_qos in a UDP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 874h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXUDPERROCT DWC_ETHER_QOS (RXUDPERROCT):** RxUDP Error Octets This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

21.2.270 RXTCP_GOOD_OCTETS DWC_ETHER_QOS (RXTCP_GOOD_OCTETS) — Offset 878h

This register provides the number of bytes received by DWC_ether_qos in a good TCP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 878h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXTCPGDOCT DWC_ETHER_QOS (RXTCPGDOCT):** RxTCP Good Octets This field indicates the number of bytes received in a good TCP segment. This counter does not count IP header bytes.

21.2.271 RXTCP_ERROR_OCTETS DWC_ETHER_QOS (RXTCP_ERROR_OCTETS) — Offset 87Ch

This register provides the number of bytes received by DWC_ether_qos in a TCP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 87Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXTCPERROCT DWC_ETHER_QOS (RXTCPERROCT):** RxTCP Error Octets This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

21.2.272 RXICMP_GOOD_OCTETS DWC_ETHER_QOS (RXICMP_GOOD_OCTETS) — Offset 880h

This register provides the number of bytes received by DWC_ether_qos in a good ICMP segment. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 880h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXICMPGDOCT DWC_ETHER_QOS (RXICMPGDOCT):** RxICMP Good Octets This field indicates the number of bytes received in a good ICMP segment. This counter does not count IP header bytes.

21.2.273 RXICMP_ERROR_OCTETS DWC_ETHER_QOS (RXICMP_ERROR_OCTETS) — Offset 884h

This register provides the number of bytes received by DWC_ether_qos in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 884h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**RXICMPERROCT DWC_ETHER_QOS (RXICMPERROCT):** RxICMP Error Octets This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

21.2.274 MMC_FPE_TX_INTERRUPT DWC_ETHER_QOS (MMC_FPE_TX_INTERRUPT) — Offset 8A0h

This register maintains the interrupts generated from all FPE related Transmit statistics counters. The MMC FPE Transmit Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Transmit Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RO/V	**HRCIS DWC_ETHER_QOS (HRCIS):** MMC Tx Hold Request Counter Interrupt Status This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.
0	0h RO/V	**FCIS DWC_ETHER_QOS (FCIS):** MMC Tx FPE Fragment Counter Interrupt status This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.275 MMC_FPE_TX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_FPE_TX_INTERRUPT_MASK) — Offset 8A4h

This register maintains the masks for interrupts generated from all FPE related Transmit statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Reserved**
1	0h RW	**HRCIM DWC_ETHER_QOS (HRCIM):** MMC Transmit Hold Request Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.
0	0h RW	**FCIM DWC_ETHER_QOS (FCIM):** MMC Transmit Fragment Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.276 MMC_TX_FPE_FRAGMENT_CNTR DWC_ETHER_QOS (MMC_TX_FPE_FRAGMENT_CNTR) — Offset 8A8h

This register provides the number of additional mPackets transmitted due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8A8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXFFC DWC_ETHER_QOS (TXFFC):** Tx FPE Fragment counter This field indicates the number of additional mPackets that has been transmitted due to preemption Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.277 MMC_TX_HOLD_REQ_CNTR DWC_ETHER_QOS (MMC_TX_HOLD_REQ_CNTR) — Offset 8ACh

This register provides the count of number of times a hold request is given to MAC

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8ACh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXHRC DWC_ETHER_QOS (TXHRC):** Tx Hold Request Counter This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.

21.2.278 MMC_FPE_RX_INTERRUPT DWC_ETHER_QOS (MMC_FPE_RX_INTERRUPT) — Offset 8C0h

This register maintains the interrupts generated from all FPE related Receive statistics counters. The MMC FPE Receive Interrupt register maintains the interrupts generated when transmit statistic counters reach half their maximum values (0x8000_0000 for 32 bit counter and 0x8000 for 16 bit counter), and when they cross their maximum values (0xFFFF_FFFF for 32-bit counter and 0xFFFF for 16-bit counter). When Counter Stop Rollover is set, the interrupts are set but the counter remains at all-ones. The MMC FPE Receive Interrupt register is a 32 bit register. An interrupt bit is cleared when the respective MMC counter that caused the interrupt is read. The least significant byte lane (Bits[7:0]) of the respective counter must be read to clear the interrupt bit.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RO/V	**FCIS DWC_ETHER_QOS (FCIS):** MMC Rx FPE Fragment Counter Interrupt Status This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**PAOCIS DWC_ETHER_QOS (PAOCIS):** MMC Rx Packet Assembly OK Counter Interrupt Status This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.
1	0h RO/V	**PSECIS DWC_ETHER_QOS (PSECIS):** MMC Rx Packet SMD Error Counter Interrupt Status This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.
0	0h RO/V	**PAECIS DWC_ETHER_QOS (PAECIS):** MMC Rx Packet Assembly Error Counter Interrupt Status This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.279 MMC_FPE_RX_INTERRUPT_MASK DWC_ETHER_QOS (MMC_FPE_RX_INTERRUPT_MASK) — Offset 8C4h

This register maintains the masks for interrupts generated from all FPE related Receive statistics counters. The MMC Receive Interrupt Mask register maintains the masks for the interrupts generated when FPE related receive statistic counters reach half of their maximum value or the maximum values. This register is 32 bit wide.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**FCIM DWC_ETHER_QOS (FCIM):** MMC Rx FPE Fragment Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.
2	0h RW	**PAOCIM DWC_ETHER_QOS (PAOCIM):** MMC Rx Packet Assembly OK Counter Interrupt Mask Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.
1	0h RW	**PSECIM DWC_ETHER_QOS (PSECIM):** MMC Rx Packet SMD Error Counter Interrupt Mask Setting this bit masks the interrupt when the R Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**PAECIM DWC_ETHER_QOS (PAECIM):** MMC Rx Packet Assembly Error Counter Interrupt Mask Setting this bit masks the interrupt when the R Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.280 MMC_RX_PACKET_ASSEMBLY_ERR_CNTR DWC_ETHER_QOS (MMC_RX_PACKET_ASSEMBLY_ERR_CNTR) — Offset 8C8h

This register provides the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8C8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**PAEC DWC_ETHER_QOS (PAEC):** Rx Packet Assembly Error Counter This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.281 MMC_RX_PACKET_SMD_ERR_CNTR DWC_ETHER_QOS (MMC_RX_PACKET_SMD_ERR_CNTR) — Offset 8CCh

This register provides the number of received MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8CCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**PSEC DWC_ETHER_QOS (PSEC):** Rx Packet SMD Error Counter This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.282 MMC_RX_PACKET_ASSEMBLY_OK_CNTR DWC_ETHER_QOS (MMC_RX_PACKET_ASSEMBLY_OK_CNTR) — Offset 8D0h

This register provides the number of MAC frames that were successfully reassembled and delivered to MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**PAOC DWC_ETHER_QOS (PAOC):** Rx Packet Assembly OK Counter This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.283 MMC_RX_FPE_FRAGMENT_CNTR DWC_ETHER_QOS (MMC_RX_FPE_FRAGMENT_CNTR) — Offset 8D4h

This register provides the number of additional mPackets received due to preemption.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 8D4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**FFC DWC_ETHER_QOS (FFC):** Rx FPE Fragment Counter This field indicates the number of additional mPackets received due to preemption Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration.

21.2.284 MAC_L3_L4_CONTROL0 DWC_ETHER_QOS (MAC_L3_L4_CONTROL0) — Offset 900h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 900h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMCHEN0 DWC_ETHER_QOS (DMCHEN0):** DMA Channel Select Enable When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter.
27	0h RO	**Reserved**
26:24	0h RW	**DMCHN0 DWC_ETHER_QOS (DMCHN0):** DMA Channel Number When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**L4DPIM0 DWC_ETHER_QOS (L4DPIM0):** Layer 4 Destination Port Inverse Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high.
20	0h RW	**L4DPM0 DWC_ETHER_QOS (L4DPM0):** Layer 4 Destination Port Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching.
19	0h RW	**L4SPIM0 DWC_ETHER_QOS (L4SPIM0):** Layer 4 Source Port Inverse Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high.
18	0h RW	**L4SPM0 DWC_ETHER_QOS (L4SPM0):** Layer 4 Source Port Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching.
17	0h RO	**Reserved**
16	0h RW	**L4PEN0 DWC_ETHER_QOS (L4PEN0):** Layer 4 Protocol Enable When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set.

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RW	**L3HDBM0 DWC_ETHER_QOS (L3HDBM0):** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM0 DWC_ETHER_QOS (L3HSBM0):** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**L3DAIM0 DWC_ETHER_QOS (L3DAIM0):** Layer 3 IP DA Inverse Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high.
4	0h RW	**L3DAM0 DWC_ETHER_QOS (L3DAM0):** Layer 3 IP DA Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering.
3	0h RW	**L3SAIM0 DWC_ETHER_QOS (L3SAIM0):** Layer 3 IP SA Inverse Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set.
2	0h RW	**L3SAM0 DWC_ETHER_QOS (L3SAM0):** Layer 3 IP SA Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering.
1	0h RO	**Reserved**
0	0h RW	**L3PEN0 DWC_ETHER_QOS (L3PEN0):** Layer 3 Protocol Enable When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set.

21.2.285 MAC_LAYER4_ADDRESS0 DWC_ETHER_QOS (MAC_LAYER4_ADDRESS0) — Offset 904h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core. You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian

mode) of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 904h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**L4DP0 DWC_ETHER_QOS (L4DP0):** Layer 4 Destination Port Number Field When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**L4SP0 DWC_ETHER_QOS (L4SP0):** Layer 4 Source Port Number Field When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

21.2.286 MAC_LAYER3_ADDR0_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR0_REG0) — Offset 910h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 910h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A00 DWC_ETHER_QOS (L3A00):** Layer 3 Address 0 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

21.2.287 MAC_LAYER3_ADDR1_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR1_REG0) — Offset 914h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 914h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A10 DWC_ETHER_QOS (L3A10):** Layer 3 Address 1 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

21.2.288 MAC_LAYER3_ADDR2_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR2_REG0) — Offset 918h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 918h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A20 DWC_ETHER_QOS (L3A20):** Layer 3 Address 2 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

21.2.289 MAC_LAYER3_ADDR3_REG0 DWC_ETHER_QOS (MAC_LAYER3_ADDR3_REG0) — Offset 91Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 91Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A30 DWC_ETHER_QOS (L3A30):** Layer 3 Address 3 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

21.2.290 MAC_L3_L4_CONTROL1 DWC_ETHER_QOS (MAC_L3_L4_CONTROL1) — Offset 930h

The Layer 3 and Layer 4 Control register controls the operations of filter 0 of Layer 3 and Layer 4.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 930h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**DMCHEN1 DWC_ETHER_QOS (DMCHEN1):** DMA Channel Select Enable When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter.
27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:24	0h RW	**DMCHN1 DWC_ETHER_QOS (DMCHN1):** DMA Channel Number When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration.
23:22	0h RO	**Reserved**
21	0h RW	**L4DPIM1 DWC_ETHER_QOS (L4DPIM1):** Layer 4 Destination Port Inverse Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high.
20	0h RW	**L4DPM1 DWC_ETHER_QOS (L4DPM1):** Layer 4 Destination Port Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching.
19	0h RW	**L4SPIM1 DWC_ETHER_QOS (L4SPIM1):** Layer 4 Source Port Inverse Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high.
18	0h RW	**L4SPM1 DWC_ETHER_QOS (L4SPM1):** Layer 4 Source Port Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching.
17	0h RO	**Reserved**
16	0h RW	**L4PEN1 DWC_ETHER_QOS (L4PEN1):** Layer 4 Protocol Enable When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the L4SPM0 or L4DPM0 bit is set.
15:11	00h RW	**L3HDBM1 DWC_ETHER_QOS (L3HDBM1):** Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: - 0: No bits are masked. - 1: LSb[0] is masked. - 2: Two LSbs [1:0] are masked - .. - 127: All bits except MSb are masked. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set.
10:6	00h RW	**L3HSBM1 DWC_ETHER_QOS (L3HSBM1):** Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: - 0: No bits are masked. - 1: LSb[0] is masked - 2: Two LSbs [1:0] are masked - .. - 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high.
5	0h RW	**L3DAIM1 DWC_ETHER_QOS (L3DAIM1):** Layer 3 IP DA Inverse Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**L3DAM1 DWC_ETHER_QOS (L3DAM1):** Layer 3 IP DA Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering.
3	0h RW	**L3SAIM1 DWC_ETHER_QOS (L3SAIM1):** Layer 3 IP SA Inverse Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set.
2	0h RW	**L3SAM1 DWC_ETHER_QOS (L3SAM1):** Layer 3 IP SA Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering.
1	0h RO	**Reserved**
0	0h RW	**L3PEN1 DWC_ETHER_QOS (L3PEN1):** Layer 3 Protocol Enable When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set.

21.2.291 MAC_LAYER4_ADDRESS1 DWC_ETHER_QOS (MAC_LAYER4_ADDRESS1) — Offset 934h

The MAC_Layer4_Address(#i), MAC_L3_L4_Control(#i), MAC_Layer3_Addr0_Reg(#i), MAC_Layer3_Addr1_Reg(#i), MAC_Layer3_Addr2_Reg(#i) and MAC_Layer3_Addr3_Reg(#i) registers are reserved (RO with default value) if Enable Layer 3 and Layer 4 Packet Filter option is not selected while configuring the core. You can configure the Layer 3 and Layer 4 Address Registers to be double-synchronized by selecting the Synchronize Layer 3 and Layer 4 Address Registers to Rx Clock Domain option while configuring the core. When you select this option, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Layer 3 and Layer 4 Address Registers are written. For proper synchronization updates, you should perform consecutive writes to same Layer 3 and Layer 4 Address Registers after at least four clock cycles delay of the destination clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 934h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**L4DP1 DWC_ETHER_QOS (L4DP1):** Layer 4 Destination Port Number Field When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets.
15:0	0000h RW	**L4SP1 DWC_ETHER_QOS (L4SP1):** Layer 4 Source Port Number Field When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets.

21.2.292 MAC_LAYER3_ADDR0_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR0_REG1) — Offset 940h

For IPv4 packets, the Layer 3 Address 0 Register 0 register contains the 32-bit IP Source Address field. For IPv6 packets, it contains Bits[31:0] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 940h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A01 DWC_ETHER_QOS (L3A01):** Layer 3 Address 0 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets.

21.2.293 MAC_LAYER3_ADDR1_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR1_REG1) — Offset 944h

For IPv4 packets, the Layer 3 Address 1 Register 0 register contains the 32-bit IP Destination Address field. For IPv6 packets, it contains Bits[63:32] of the 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 944h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A11 DWC_ETHER_QOS (L3A11):** Layer 3 Address 1 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets.

21.2.294 MAC_LAYER3_ADDR2_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR2_REG1) — Offset 948h

The Layer 3 Address 2 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[95:64] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 948h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A21 DWC_ETHER_QOS (L3A21):** Layer 3 Address 2 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

21.2.295 MAC_LAYER3_ADDR3_REG1 DWC_ETHER_QOS (MAC_LAYER3_ADDR3_REG1) — Offset 94Ch

The Layer 3 Address 3 Register 0 register is reserved for IPv4 packets. For IPv6 packets, it contains Bits[127:96] of 128-bit IP Source Address or Destination Address field.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 94Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**L3A31 DWC_ETHER_QOS (L3A31):** Layer 3 Address 3 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used.

21.2.296 MAC_TIMESTAMP_CONTROL DWC_ETHER_QOS (MAC_TIMESTAMP_CONTROL) — Offset B00h

This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B00h	00002000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**AV8021ASMEN DWC_ETHER_QOS (AV8021ASMEN):** AV 802.1AS Mode Enable When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit.
27:25	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**TXTSSTSM DWC_ETHER_QOS (TXTSSTSM):** Transmit Timestamp Status Mode When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register.
23:21	0h RO	**Reserved**
20	0h RW	**ESTI DWC_ETHER_QOS (ESTI):** External System Time Input When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: - To take the timestamp provided as status - To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time.
19	0h RW	**CSC DWC_ETHER_QOS (CSC):** Enable checksum correction during OST for PTP over UDP/IPv4 packets When this bit is set, the last two bytes of PTP message sent over UDP/IPv4 is updated to keep the UDP checksum correct, for changes made to origin timestamp and/or correction field as part of one step timestamp operation. The application shall form the packet with these two dummy bytes. When reset, no updates are done to keep the UDP checksum correct. The application shall form the packet with UDP checksum set to 0.
18	0h RW	**TSENMACADDR DWC_ETHER_QOS (TSENMACADDR):** Enable MAC Address for PTP Packet Filtering When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching.
17:16	0h RW	**SNAPTYPSEL DWC_ETHER_QOS (SNAPTYPSEL):** Select PTP packets for Taking Snapshots These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	0h RW	**TSMSTRENA DWC_ETHER_QOS (TSMSTRENA):** Enable Snapshot for Messages Relevant to Master When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node.
14	0h RW	**TSEVNTENA DWC_ETHER_QOS (TSEVNTENA):** Enable Timestamp Snapshot for Event Messages When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table.
13	1h RW	**TSIPV4ENA DWC_ETHER_QOS (TSIPV4ENA):** Enable Processing of PTP Packets Sent over IPv4-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default.
12	0h RW	**TSIPV6ENA DWC_ETHER_QOS (TSIPV6ENA):** Enable Processing of PTP Packets Sent over IPv6-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets.
11	0h RW	**TSIPENA DWC_ETHER_QOS (TSIPENA):** Enable Processing of PTP over Ethernet Packets When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**TSVER2ENA DWC_ETHER_QOS (TSVER2ENA):** Enable PTP Packet Processing for Version 2 Format When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'.
9	0h RW	**TSCTRLSSR DWC_ETHER_QOS (TSCTRLSSR):** Timestamp Digital or Binary Rollover Control When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit.
8	0h RW	**TSENALL DWC_ETHER_QOS (TSENALL):** Enable Timestamp for All Packets When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC.
7	0h RO	**Reserved**
6	0h RW	**PTGE DWC_ETHER_QOS (PTGE):** Presentation Time Generation Enable When this bit is set the Presentation Time generation will be enabled.
5	0h RW	**TSADDREG DWC_ETHER_QOS (TSADDREG):** Update Addend Register When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
4	0h RO	**Reserved**
3	0h RW	**TSUPDT DWC_ETHER_QOS (TSUPDT):** Update Timestamp When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated. When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
2	0h RW	**TSINIT DWC_ETHER_QOS (TSINIT):** Initialize Timestamp When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
1	0h RW	**TSCFUPDT DWC_ETHER_QOS (TSCFUPDT):** Fine or Coarse Timestamp Update When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp.
0	0h RW	**TSENA DWC_ETHER_QOS (TSENA):** Enable Timestamp When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set.

21.2.297 MAC_SUB_SECOND_INCREMENT DWC_ETHER_QOS (MAC_SUB_SECOND_INCREMENT) — Offset B04h

This register specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	00h RW	**SSINC DWC_ETHER_QOS (SSINC):** Sub-second Increment Value The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:8	00h RW	**SNSINC DWC_ETHER_QOS (SNSINC):** Sub-nanosecond Increment Value This field contains the sub-nanosecond increment value, represented in nanoseconds multiplied by 2^8. This value is accumulated with the sub-nanoseconds field of the subsecond register. For example, when TSCTRLSSR field in the MAC_Timestamp_Control register is set. and if the required increment is 5.3ns, then SSINC should be 0x05 and SNSINC should be 0x4C.
7:0	0h RO	**Reserved**

21.2.298 MAC_SYSTEM_TIME_SECONDS DWC_ETHER_QOS (MAC_SYSTEM_TIME_SECONDS) — Offset B08h

The System Time Seconds register, along with System Time Nanoseconds register, indicates the current value of the system time maintained by the MAC. Though it is updated on a continuous basis, there is some delay from the actual time because of clock domain transfer latencies (from clk_ptp_ref_i to CSR clock).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TSS DWC_ETHER_QOS (TSS):** Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

21.2.299 MAC_SYSTEM_TIME_NANOSECONDS DWC_ETHER_QOS (MAC_SYSTEM_TIME_NANOSECONDS) — Offset B0Ch

The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B0Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30:0	00000000h RO/V	**TSSS DWC_ETHER_QOS (TSSS):** Timestamp Sub Seconds The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

21.2.300 MAC_SYSTEM_TIME_SECONDS_UPDATE DWC_ETHER_QOS (MAC_SYSTEM_TIME_SECONDS_UPDATE) — Offset B10h

The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC. You must write both registers before setting the TSINIT or TSUPDT bits in DWC_eqos_top_map/EQOS_MAC/MAC_Timestamp_Control.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TSS DWC_ETHER_QOS (TSS):** Timestamp Seconds The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

21.2.301 MAC_SYSTEM_TIME_NANOSECONDS_UPDATE DWC_ETHER_QOS (MAC_SYSTEM_TIME_NANOSECONDS_UPDATE) — Offset B14h

MAC System Time Nanoseconds Update register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ADDSUB DWC_ETHER_QOS (ADDSUB):** Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register.
30:0	00000000h RW	**TSSS DWC_ETHER_QOS (TSSS):** Timestamp Sub Seconds The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register. When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 -. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 -. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

21.2.302 MAC_TIMESTAMP_ADDEND DWC_ETHER_QOS (MAC_TIMESTAMP_ADDEND) — Offset B18h

Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register). The content of this register is added to a 32-bit accumulator in every clock cycle (of clk_ptp_ref_i) and the system time is updated whenever the accumulator overflows.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TSAR DWC_ETHER_QOS (TSAR):** Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

21.2.303 MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS DWC_ETHER_QOS (MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS) — Offset B1Ch

System Time - Higher Word Seconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B1Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**TSHWR DWC_ETHER_QOS (TSHWR):** Timestamp Higher Word Register This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears.

21.2.304 MAC_TIMESTAMP_STATUS DWC_ETHER_QOS (MAC_TIMESTAMP_STATUS) — Offset B20h

Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:25	00h RO/V	**ATSNS DWC_ETHER_QOS (ATSNS):** Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
24	0h RO/V	**ATSSTM DWC_ETHER_QOS (ATSSTM):** Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.
23:20	0h RO	**Reserved**
19:16	0h RO/V	**ATSSTN DWC_ETHER_QOS (ATSSTN):** Auxiliary Timestamp Snapshot Trigger Identifier These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: - Bit 16: Auxiliary trigger 0 - Bit 17: Auxiliary trigger 1 - Bit 18: Auxiliary trigger 2 - Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15	0h RO/V	**TXTSSIS DWC_ETHER_QOS (TXTSSIS):** Tx Timestamp Status Interrupt Status In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set).
14:6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**TSTRGTERR1 DWC_ETHER_QOS (TSTRGTERR1):** Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
4	0h RO/V	**TSTARGT1 DWC_ETHER_QOS (TSTARGT1):** Timestamp Target Time Reached for Target Time PPS1 When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds registers. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
3	0h RO/V	**TSTRGTERR0 DWC_ETHER_QOS (TSTRGTERR0):** Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
2	0h RO/V	**AUXTSTRIG DWC_ETHER_QOS (AUXTSTRIG):** Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
1	0h RO/V	**TSTARGT0 DWC_ETHER_QOS (TSTARGT0):** Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.
0	0h RO/V	**TSSOVF DWC_ETHER_QOS (TSSOVF):** Timestamp Seconds Overflow When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.

21.2.305 MAC_TX_TIMESTAMP_STATUS_NANOSECONDS DWC_ETHER_QOS (MAC_TX_TIMESTAMP_STATUS_NANOSECONDS) — Offset B30h

This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled. The MAC_Tx_Timestamp_Status_Nanoseconds register, along with MAC_Tx_Timestamp_Status_Seconds, gives the 64-bit timestamp captured for the PTP packet successfully transmitted by the MAC. This value is considered to be read by the application when the last byte of MAC_Tx_Timestamp_Status_Nanoseconds is read. In the little-endian mode, this means when bits[31:24] are read; in big-endian mode, bits[7:0] are read. If the application does not read these registers and timestamp of another packet is captured, then either the current timestamp is lost (overwritten) or the new timestamp is lost (dropped), depending on the setting of the TXTSSTSM bit of the MAC_Timestamp_Control register. The status bit TXTSC bit [15] in MAC_Timestamp_Status register is set whenever the MAC transmitter captures the timestamp.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**TXTSSMIS DWC_ETHER_QOS (TXTSSMIS):** Transmit Timestamp Status Missed When this bit is set, it indicates one of the following: - The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset - The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event.
30:0	00000000h RO/V	**TXTSSLO DWC_ETHER_QOS (TXTSSLO):** Transmit Timestamp Status Low This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

21.2.306 MAC_TX_TIMESTAMP_STATUS_SECONDS DWC_ETHER_QOS (MAC_TX_TIMESTAMP_STATUS_SECONDS) — Offset B34h

The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**TXTSSHI DWC_ETHER_QOS (TXTSSHI):** Transmit Timestamp Status High This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

21.2.307 MAC_AUXILIARY_CONTROL DWC_ETHER_QOS (MAC_AUXILIARY_CONTROL) — Offset B40h

The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**ATSEN1 DWC_ETHER_QOS (ATSEN1):** Auxiliary Snapshot 1 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored.
4	0h RW	**ATSEN0 DWC_ETHER_QOS (ATSEN0):** Auxiliary Snapshot 0 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored.
3:1	0h RO	**Reserved**
0	0h RW	**ATSFC DWC_ETHER_QOS (ATSFC):** Auxiliary Snapshot FIFO Clear When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.308 MAC_AUXILIARY_TIMESTAMP_NANOSECONDS DWC_ETHER_QOS (MAC_AUXILIARY_TIMESTAMP_NANOSECONDS) — Offset B48h

The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot. These two registers form the read port of a 64-bit wide FIFO with a depth of 4, 8, or 16 as selected while configuring the core. You can store multiple snapshots in this FIFO. Bits[29:25] in MAC_Timestamp_Status indicate the fill-level of the FIFO. The top of the FIFO is removed only when the last byte of MAC_Auxiliary_Timestamp_Seconds register is read. In the little-endian mode, this means when Bits[31:24] are read and in big-endian mode, Bits[7:0] are read.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B48h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
30:0	00000000h RO/V	**AUXTSLO DWC_ETHER_QOS (AUXTSLO):** Auxiliary Timestamp Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

21.2.309 MAC_AUXILIARY_TIMESTAMP_SECONDS DWC_ETHER_QOS (MAC_AUXILIARY_TIMESTAMP_SECONDS) — Offset B4Ch

The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B4Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**AUXTSHI DWC_ETHER_QOS (AUXTSHI):** Auxiliary Timestamp Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

21.2.310 MAC_TIMESTAMP_INGRESS_ASYM_CORR DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_ASYM_CORR) — Offset B50h

The MAC Timestamp Ingress Asymmetry Correction register contains the Ingress Asymmetry Correction value to be used while updating correction field in PDelay_Resp PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OSTIAC DWC_ETHER_QOS (OSTIAC):** One-Step Timestamp Ingress Asymmetry Correction This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^16. For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit.

21.2.311 MAC_TIMESTAMP_EGRESS_ASYM_CORR DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_ASYM_CORR) — Offset B54h

The MAC Timestamp Egress Asymmetry Correction register contains the Egress Asymmetry Correction value to be used while updating the correction field in PDelay_Req PTP messages.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**OSTEAC DWC_ETHER_QOS (OSTEAC):** One-Step Timestamp Egress Asymmetry Correction This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^16. For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFD_8000, which is the 2's complement of 0x0002_8000(2.5 * 216). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC (3.3 * 216).

21.2.312 MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND) — Offset B58h

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TSIC DWC_ETHER_QOS (TSIC):** Timestamp Ingress Correction This field contains the ingress path correction value as defined by the Ingress Correction expression.

21.2.313 MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND) — Offset B5Ch

This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TSEC DWC_ETHER_QOS (TSEC):** Timestamp Egress Correction This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

21.2.314 MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC) — Offset B60h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for ingress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**TSICSNS DWC_ETHER_QOS (TSICSNS):** Timestamp Ingress Correction, sub-nanoseconds This field contains the sub-nanoseconds part of the ingress path correction value as defined by the "Ingress Correction" expression.
7:0	0h RO	**Reserved**

21.2.315 MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC) — Offset B64h

This register contains the sub-nanosecond part of the correction value to be used with the captured timestamp value, for egress direction.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**TSECSNS DWC_ETHER_QOS (TSECSNS):** Timestamp Egress Correction, sub-nanoseconds This field contains the sub-nanoseconds part of the egress path correction value as defined by the "Egress Correction" expression.
7:0	0h RO	**Reserved**

21.2.316 MAC_TIMESTAMP_INGRESS_LATENCY DWC_ETHER_QOS (MAC_TIMESTAMP_INGRESS_LATENCY) — Offset B68h

This register holds the Ingress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO/V	**ITLNS DWC_ETHER_QOS (ITLNS):** Ingress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	00h RO/V	**ITLSNS DWC_ETHER_QOS (ITLSNS):** Ingress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	0h RO	**Reserved**

21.2.317 MAC_TIMESTAMP_EGRESS_LATENCY DWC_ETHER_QOS (MAC_TIMESTAMP_EGRESS_LATENCY) — Offset B6Ch

This register holds the Egress MAC latency.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B6Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27:16	000h RO/V	**ETLNS DWC_ETHER_QOS (ETLNS):** Egress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
15:8	00h RO/V	**ETLSNS DWC_ETHER_QOS (ETLSNS):** Egress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	0h RO	**Reserved**

21.2.318 MAC_PPS_CONTROL DWC_ETHER_QOS (MAC_PPS_CONTROL) — Offset B70h

PPS Control register. Bits[30:24] of this register are valid only when four Flexible PPS outputs are selected. Bits[22:16] are valid only when three or more Flexible PPS outputs are selected. Bits[14:8] are valid only when two or more Flexible PPS outputs are selected. Bits[6:4] are valid only when Flexible PPS feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**MCGREN1 DWC_ETHER_QOS (MCGREN1):** MCGR Mode Enable for PPS1 Output This field enables the 1st PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode.
14:13	0h RW	**TRGTMODSEL1 DWC_ETHER_QOS (TRGTMODSEL1):** Target Time Register Mode for PPS1 Output This field indicates the Target Time registers (MAC_PPS1_Target_Time_Seconds and MAC_PPS1_Target_Time_Nanoseconds) mode for PPS1 output signal.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO	**Reserved**
11:8	0h RW	**PPSCMD1 DWC_ETHER_QOS (PPSCMD1):** Flexible PPS1 Output Control This field controls the flexible PPS1 output (ptp_pps_o[1]) signal. This field is similar to the PPSCMD0 field. If MCGREN1 is set, then PPSCMD1 indicated by these 4 bits [11:8] are taken as Presentation Time Control bits for media clock generation and recovery for comparator instance 1. This field is similar to the PPSCMD0 Presentation Time Control bits. If MCGREN1 is not set then only 3 bits from [10:8] is used as PPSCMD1 and the 4th bit is to be set as 0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
7	0h RW	**MCGREN0 DWC_ETHER_QOS (MCGREN0):** MCGR Mode Enable for PPS0 Output This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode.
6:5	0h RW	**TRGTMODSEL0 DWC_ETHER_QOS (TRGTMODSEL0):** Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal:
4	0h RW	**PPSEN0 DWC_ETHER_QOS (PPSEN0):** Flexible PPS Output Mode Enable When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode).

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**PPSCTRL_PPSCMD DWC_ETHER_QOS (PPSCTRL_PPSCMD):** PPS Output Frequency Control This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: - 0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. - 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. - 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. - 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. - .. - 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: - When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms - When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high) - When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high) This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register. or Flexible PPS Output (ptp_pps_o[0]) Control Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: - 0000: No Command - 0001: START Single Pulse This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register. - 0010: START Pulse Train This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. - 0011: Cancel START This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. - 0100: STOP Pulse train at time This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. - 0101: STOP Pulse Train immediately This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). - 110: Cancel STOP Pulse train This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. - 0111-1111: Reserved or Presentation Time Control If MCGREN0 is set then these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0: - 0000: No Operation related to MCGR will be carried out. If set to this value in the mid of clock recovery or generation all the processing inputs will be flushed. - 0001: Capture the Presentation time at rising edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0010: Capture the Presentation time at falling edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0011: Capture the Presentation time at both edges of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register - 0100-1000: Reserved - 1001: Toggle output on compare - 1010: Pulse output low on compare for one PTP-clock cycle - 1011: Pulse output high on compare for one PTP-clock cycle - 1100-1111: Reserved

21.2.319 MAC_PPS0_TARGET_TIME_SECONDS DWC_ETHER_QOS (MAC_PPS0_TARGET_TIME_SECONDS) — Offset B80h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TSTRH0 DWC_ETHER_QOS (TSTRH0):** PPS Target Time Seconds Register This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

21.2.320 MAC_PPS0_TARGET_TIME_NANOSECONDS DWC_ETHER_QOS (MAC_PPS0_TARGET_TIME_NANOSECONDS) — Offset B84h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TRGTBUSY0 DWC_ETHER_QOS (TRGTBUSY0):** PPS Target Time Register Busy The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted.
30:0	00000000h RW	**TTSL0 DWC_ETHER_QOS (TTSL0):** Target Time Low for PPS Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.321 MAC_PPS0_INTERVAL DWC_ETHER_QOS (MAC_PPS0_INTERVAL) — Offset B88h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B88h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPSINT0 DWC_ETHER_QOS (PPSINT0):** PPS Output Signal Interval These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

21.2.322 MAC_PPS0_WIDTH DWC_ETHER_QOS (MAC_PPS0_WIDTH) — Offset B8Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B8Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPSWIDTH0 DWC_ETHER_QOS (PPSWIDTH0):** PPS Output Signal Width These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

21.2.323 MAC_PPS1_TARGET_TIME_SECONDS DWC_ETHER_QOS (MAC_PPS1_TARGET_TIME_SECONDS) — Offset B90h

The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**TSTRH1 DWC_ETHER_QOS (TSTRH1):** PPS Target Time Seconds Register This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

21.2.324 MAC_PPS1_TARGET_TIME_NANOSECONDS DWC_ETHER_QOS (MAC_PPS1_TARGET_TIME_NANOSECONDS) — Offset B94h

PPS0 Target Time Nanoseconds register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + B94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**TRGTBUSY1 DWC_ETHER_QOS (TRGTBUSY1):** PPS Target Time Register Busy The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain. The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed time gets corrupted.

Bit Range	Default & Access	Field Name (ID): Description
30:0	00000000h RW	**TTSL1 DWC_ETHER_QOS (TTSL1):** Target Time Low for PPS Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.325 MAC_PPS1_INTERVAL DWC_ETHER_QOS (MAC_PPS1_INTERVAL) — Offset B98h

The PPS0 Interval register contains the number of units of sub-second increment value between the rising edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B98h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPSINT1 DWC_ETHER_QOS (PPSINT1):** PPS Output Signal Interval These bits store the interval between the rising edges of PPS0 signal output. The interval is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if the PTP reference clock is 50 MHz (period of 20 ns), and desired interval between the rising edges of PPS0 signal output is 100 ns (that is, 5 units of sub-second increment value), you should program value 4 (5-1) in this register.

21.2.326 MAC_PPS1_WIDTH DWC_ETHER_QOS (MAC_PPS1_WIDTH) — Offset B9Ch

The PPS0 Width register contains the number of units of sub-second increment value between the rising and corresponding falling edges of PPS0 signal output (ptp_pps_o[0]).

Type	Size	Offset	Default
MMIO	32 bit	BAR + B9Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**PPSWIDTH1 DWC_ETHER_QOS (PPSWIDTH1):** PPS Output Signal Width These bits store the width between the rising edge and corresponding falling edge of PPS0 signal output. The width is stored in terms of number of units of sub-second increment value. You need to program one value less than the required interval. For example, if PTP reference clock is 50 MHz (period of 20 ns), and width between the rising and corresponding falling edges of PPS0 signal output is 80 ns (that is, four units of sub-second increment value), you should program value 3 (4-1) in this register. Note: The value programmed in this register must be lesser than the value programmed in MAC_PPS0_Interval.

21.2.327 MAC_PTO_CONTROL DWC_ETHER_QOS (MAC_PTO_CONTROL) — Offset BC0h

This register controls the PTP Offload Engine operation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**DN DWC_ETHER_QOS (DN):** Domain Number This field indicates the domain Number in which the PTP node is operating.
7	0h RW	**PDRDIS DWC_ETHER_QOS (PDRDIS):** Disable Peer Delay Response response generation When this bit is set, the Peer Delay Response (Pdelay_Resp) response is not be generated for received Peer Delay Request (Pdelay_Req) request packet, as required by the programmed mode. Note: Setting this bit to 1 affects the normal PTP Offload operation and the time synchronization. So, this bit must be set only if there is problem with Pdelay_Resp generation in Hardware and/or Pdelay_Resp generation is handled by Software.
6	0h RW	**DRRDIS DWC_ETHER_QOS (DRRDIS):** Disable PTO Delay Request/Response response generation When this bit is set, the Delay Request and Delay response is not generated for received SYNC and Delay request packet respectively, as required by the programmed mode.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**APDREQTRIG DWC_ETHER_QOS (APDREQTRIG):** Automatic PTP Pdelay_Req message Trigger When this bit is set, one PTP Pdelay_Req message is transmitted. This bit is automatically cleared after the PTP Pdelay_Req message is transmitted. The application should set the APDREQEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
4	0h RW	**ASYNCTRIG DWC_ETHER_QOS (ASYNCTRIG):** Automatic PTP SYNC message Trigger When this bit is set, one PTP SYNC message is transmitted. This bit is automatically cleared after the PTP SYNC message is transmitted. The application should set the ASYNCEN bit for this operation. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
3	0h RO	**Reserved**
2	0h RW	**APDREQEN DWC_ETHER_QOS (APDREQEN):** Automatic PTP Pdelay_Req message Enable When this bit is set, PTP Pdelay_Req message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Peer-to-Peer Transparent mode.
1	0h RW	**ASYNCEN DWC_ETHER_QOS (ASYNCEN):** Automatic PTP SYNC message Enable When this bit is set, PTP SYNC message is generated periodically based on interval programmed or trigger from application, when the MAC is programmed to be in Clock Master mode.
0	0h RW	**PTOEN DWC_ETHER_QOS (PTOEN):** PTP Offload Enable When this bit is set, the PTP Offload feature is enabled.

21.2.328 MAC_SOURCE_PORT_IDENTITY0 DWC_ETHER_QOS (MAC_SOURCE_PORT_IDENTITY0) — Offset BC4h

This register contains Bits[31:0] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SPI0 DWC_ETHER_QOS (SPI0):** Source Port Identity 0 This field indicates bits [31:0] of sourcePortIdentity of PTP node.

21.2.329 MAC_SOURCE_PORT_IDENTITY1 DWC_ETHER_QOS (MAC_SOURCE_PORT_IDENTITY1) — Offset BC8h

This register contains Bits[63:32] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BC8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**SPI1 DWC_ETHER_QOS (SPI1):** Source Port Identity 1 This field indicates bits [63:32] of sourcePortIdentity of PTP node.

21.2.330 MAC_SOURCE_PORT_IDENTITY2 DWC_ETHER_QOS (MAC_SOURCE_PORT_IDENTITY2) — Offset BCCh

This register contains Bits[79:64] of the 80-bit Source Port Identity of the PTP node. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BCCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**SPI2 DWC_ETHER_QOS (SPI2):** Source Port Identity 2 This field indicates bits [79:64] of sourcePortIdentity of PTP node.

21.2.331 MAC_LOG_MESSAGE_INTERVAL DWC_ETHER_QOS (MAC_LOG_MESSAGE_INTERVAL) — Offset BD0h

This register contains the periodic intervals for automatic PTP packet generation. This register is available only when the Enable PTP Timestamp Offload feature is selected.

Type	Size	Offset	Default
MMIO	32 bit	BAR + BD0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**LMPDRI DWC_ETHER_QOS (LMPDRI):** Log Min Pdelay_Req Interval This field indicates logMinPdelayReqInterval of PTP node. This is used to schedule the periodic Pdelay request packet transmission. Allowed values are -15 to 15.Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.
23:11	0h RO	**Reserved**
10:8	0h RW	**DRSYNCR DWC_ETHER_QOS (DRSYNCR):** Delay_Req to SYNC Ratio In Slave mode, it is used for controlling frequency of Delay_Req messages transmitted. - 0: DelayReq generated for every received SYNC - 1: DelayReq generated every alternate reception of SYNC - 2: for every 4 SYNC messages - 3: for every 8 SYNC messages - 4: for every 16 SYNC messages - 5: for every 32 SYNC messages - 6-7: Reserved The master sends this information (logMinDelayReqInterval) in the DelayResp PTP messages to the slave. The DWC_ether_qos Receiver processes this value from the received DelayResp messages and updates this field accordingly. In the Slave mode, the host must not write/update this register unless it has to override the received value. In Master mode, the sum of this field and logSyncInterval (LSI) field is provided in the logMinDelayReqInterval field of the generated multicast Delay_Resp PTP message. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears.
7:0	00h RW	**LSI DWC_ETHER_QOS (LSI):** Log Sync Interval This field indicates the periodicity of the automatically generated SYNC message when the PTP node is Master. Allowed values are -15 to 15. Negative value must be represented in 2's-complement form. For example, if the required value is -1, the value programmed must be 0xFF.

21.2.332 MTL_OPERATION_MODE DWC_ETHER_QOS (MTL_OPERATION_MODE) — Offset C00h

The Operation Mode register establishes the Transmit and Receive operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**CNTCLR DWC_ETHER_QOS (CNTCLR):** Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
8	0h RW	**CNTPRST DWC_ETHER_QOS (CNTPRST):** Counters Preset When this bit is set, - MTL_TxQ[0-7]_Underflow register is initialized/ preset to 12'h7F0. - Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
7	0h RO	**Reserved**
6:5	0h RW	**SCHALG DWC_ETHER_QOS (SCHALG):** Tx Scheduling Algorithm This field indicates the algorithm for Tx scheduling:
4:3	0h RO	**Reserved**
2	0h RW	**RAA DWC_ETHER_QOS (RAA):** Receive Arbitration Algorithm This field is used to select the arbitration algorithm for the Rx side. - 0: Strict priority (SP) Queue 0 has the lowest priority and the last queue has the highest priority. - 1: Weighted Strict Priority (WSP)
1	0h RW	**DTXSTS DWC_ETHER_QOS (DTXSTS):** Drop Transmit Status When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application.
0	0h RO	**Reserved**

21.2.333 MTL_DBG_CTL DWC_ETHER_QOS (MTL_DBG_CTL) — Offset C08h

The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18:17	0h RW	**EIEC DWC_ETHER_QOS (EIEC):** ECC Inject Error Control for Tx, Rx and TSO memories When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field.
16	0h RW	**EIEE DWC_ETHER_QOS (EIEE):** ECC Inject Error Enable for Tx, Rx and TSO memories When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**STSIE DWC_ETHER_QOS (STSIE):** Transmit Status Available Interrupt Status Enable When this bit is set, an interrupt is generated when Transmit status is available in slave mode.
14	0h RW	**PKTIE DWC_ETHER_QOS (PKTIE):** Receive Packet Available Interrupt Status Enable When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO.
13:12	0h RW	**FIFOSEL DWC_ETHER_QOS (FIFOSEL):** FIFO Selected for Access This field indicates the FIFO selected for debug access:
11	0h RW	**FIFOWREN DWC_ETHER_QOS (FIFOWREN):** FIFO Write Enable When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.
10	0h RW	**FIFORDEN DWC_ETHER_QOS (FIFORDEN):** FIFO Read Enable When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.
9	0h RW	**RSTSEL DWC_ETHER_QOS (RSTSEL):** Reset Pointers of Selected FIFO When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.
8	0h RW	**RSTALL DWC_ETHER_QOS (RSTALL):** Reset All Pointers When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.
7	0h RO	**Reserved**
6:5	0h RW	**PKTSTATE DWC_ETHER_QOS (PKTSTATE):** Encoded Packet State This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP
4	0h RO	**Reserved**
3:2	0h RW	**BYTEEN DWC_ETHER_QOS (BYTEEN):** Byte Enables This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected.
1	0h RW	**DBGMOD DWC_ETHER_QOS (DBGMOD):** Debug Mode Access to FIFO When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: - Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO - Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: - Write access to the Tx FIFO - Read access to the Rx FIFO and Tx Status FIFO
0	0h RW	**FDBGEN DWC_ETHER_QOS (FDBGEN):** FIFO Debug Access Enable When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface.

21.2.334 MTL_DBG_STS DWC_ETHER_QOS (MTL_DBG_STS) — Offset C0Ch

The FIFO Debug Status register contains the status of FIFO debug access.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C0Ch	00000018h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:15	00000h RO/V	**LOCR DWC_ETHER_QOS (LOCR):** Remaining Locations in the FIFO Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively. Reset: In single Tx Queue configurations, (DWC_EQOS_TXFIFO_SIZE/ (DWC_EQOS_DATAWIDTH/8)), Otherwise 0000H
14:10	0h RO	**Reserved**
9	0h RW	**STSI DWC_ETHER_QOS (STSI):** Transmit Status Available Interrupt Status When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit.
8	0h RW	**PKTI DWC_ETHER_QOS (PKTI):** Receive Packet Available Interrupt Status When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit.
7:5	0h RO	**Reserved**
4:3	3h RO/V	**BYTEEN DWC_ETHER_QOS (BYTEEN):** Byte Enables This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected.
2:1	0h RO/V	**PKTSTATE DWC_ETHER_QOS (PKTSTATE):** Encoded Packet State This field is used to get the control or status information of the selected FIFO. Tx FIFO: - 00: Packet Data - 01: Control Word - 10: SOP Data - 11: EOP Data Rx FIFO: - 00: Packet Data - 01: Normal Status - 10: Last Status - 11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation.
0	0h RO/V	**FIFOBUSY DWC_ETHER_QOS (FIFOBUSY):** FIFO Busy When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: - All other fields of this register - All fields of the MTL_FIFO_Debug_Data register

21.2.335 MTL_FIFO_DEBUG_DATA DWC_ETHER_QOS (MTL_FIFO_DEBUG_DATA) — Offset C10h

The FIFO Debug Data register contains the data to be written to or read from the FIFOs.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C10h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**FDBGDATA DWC_ETHER_QOS (FDBGDATA):** FIFO Debug Data During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

21.2.336 MTL_INTERRUPT_STATUS DWC_ETHER_QOS (MTL_INTERRUPT_STATUS) — Offset C20h

The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C20h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	**Reserved**
18	0h RO/V	**ESTIS DWC_ETHER_QOS (ESTIS):** EST (TAS- 802.1Qbv) Interrupt Status This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt.
17	0h RO/V	**DBGIS DWC_ETHER_QOS (DBGIS):** Debug Interrupt status This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source.
16:6	0h RO	**Reserved**
5	0h RO/V	**Q5IS DWC_ETHER_QOS (Q5IS):** Queue 5 Interrupt status This bit indicates that there is an interrupt from Queue 5. To reset this bit, the application must read the MTL_Q5_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.
4	0h RO/V	**Q4IS DWC_ETHER_QOS (Q4IS):** Queue 4 Interrupt status This bit indicates that there is an interrupt from Queue 4. To reset this bit, the application must read the MTL_Q4_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO/V	**Q3IS DWC_ETHER_QOS (Q3IS):** Queue 3 Interrupt status This bit indicates that there is an interrupt from Queue 3. To reset this bit, the application must read the MTL_Q3_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.
2	0h RO/V	**Q2IS DWC_ETHER_QOS (Q2IS):** Queue 2 Interrupt status This bit indicates that there is an interrupt from Queue 2. To reset this bit, the application must read the MTL_Q2_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.
1	0h RO/V	**Q1IS DWC_ETHER_QOS (Q1IS):** Queue 1 Interrupt status This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.
0	0h RO/V	**Q0IS DWC_ETHER_QOS (Q0IS):** Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source.

21.2.337 MTL_RXQ_DMA_MAP0 DWC_ETHER_QOS (MTL_RXQ_DMA_MAP0) — Offset C30h

The Receive Queue and DMA Channel Mapping 0 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**Q3DDMACH DWC_ETHER_QOS (Q3DDMACH):** Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection When set, this bit indicates that the packets received in Queue 3 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 3 are routed to the DMA Channel programmed in the Q3MDMACH field (Bits[26:24]).
27	0h RO	**Reserved**
26:24	0h RW	**Q3MDMACH DWC_ETHER_QOS (Q3MDMACH):** Queue 3 Mapped to DMA Channel This field controls the routing of the received packet in Queue 3 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q3DDMACH field is reset. Note: The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved
23:21	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**Q2DDMACH DWC_ETHER_QOS (Q2DDMACH):** Queue 2 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 2 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 2 are routed to the DMA Channel programmed in the Q2MDMACH field (Bits[18:16]).
19	0h RO	**Reserved**
18:16	0h RW	**Q2MDMACH DWC_ETHER_QOS (Q2MDMACH):** Queue 2 Mapped to DMA Channel This field controls the routing of the received packet in Queue 2 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q2DDMACH field is reset.
15:13	0h RO	**Reserved**
12	0h RW	**Q1DDMACH DWC_ETHER_QOS (Q1DDMACH):** Queue 1 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA Channel programmed in the Q1MDMACH field (Bits[10:8]).
11	0h RO	**Reserved**
10:8	0h RW	**Q1MDMACH DWC_ETHER_QOS (Q1MDMACH):** Queue 1 Mapped to DMA Channel This field controls the routing of the received packet in Queue 1 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**
4	0h RW	**Q0DDMACH DWC_ETHER_QOS (Q0DDMACH):** Queue 0 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field.
3	0h RO	**Reserved**
2:0	0h RW	**Q0MDMACH DWC_ETHER_QOS (Q0MDMACH):** Queue 0 Mapped to DMA Channel This field controls the routing of the packet received in Queue 0 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

21.2.338 MTL_RXQ_DMA_MAP1 DWC_ETHER_QOS (MTL_RXQ_DMA_MAP1) — Offset C34h

The Receive Queue and DMA Channel Mapping 1 register is reserved in EQOS-CORE and EQOS-MTL configurations.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW	**Q5DDMACH DWC_ETHER_QOS (Q5DDMACH):** Queue 5 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 5 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 5 are routed to the DMA Channel programmed in the Q5MDMACH field.
11	0h RO	**Reserved**
10:8	0h RW	**Q5MDMACH DWC_ETHER_QOS (Q5MDMACH):** Queue 5 Mapped to DMA Channel This field controls the routing of the packets received in Queue 5 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q5DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.
7:5	0h RO	**Reserved**
4	0h RW	**Q4DDMACH DWC_ETHER_QOS (Q4DDMACH):** Queue 4 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 4 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 4 are routed to the DMA Channel programmed in the Q4MDMACH field.
3	0h RO	**Reserved**
2:0	0h RW	**Q4MDMACH DWC_ETHER_QOS (Q4MDMACH):** Queue 4 Mapped to DMA Channel This field controls the routing of the packet received in Queue 4 to the DMA channel: - 000: DMA Channel 0 - 001: DMA Channel 1 - 010: DMA Channel 2 - 011: DMA Channel 3 - 100: DMA Channel 4 - 101: DMA Channel 5 - 110: DMA Channel 6 - 111: DMA Channel 7 This field is valid when the Q4DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved.

21.2.339 MTL_TBS_CTRL DWC_ETHER_QOS (MTL_TBS_CTRL) — Offset C40h

This register controls the operation of Time Based Scheduling.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**LEOS DWC_ETHER_QOS (LEOS):** Launch Expiry Offset The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**LEGOS DWC_ETHER_QOS (LEGOS):** Launch Expiry GSN Offset The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set.
3:2	0h RO	**Reserved**
1	0h RW	**LEOV DWC_ETHER_QOS (LEOV):** Launch Expiry Offset Valid When set indicates the LEOS field is valid. When not set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time.
0	0h RW	**ESTM DWC_ETHER_QOS (ESTM):** EST offset Mode When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8].

21.2.340 MTL_EST_CONTROL DWC_ETHER_QOS (MTL_EST_CONTROL) — Offset C50h

This register controls the operation of Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	00h RW	**PTOV DWC_ETHER_QOS (PTOV):** PTP Time Offset Value The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL.
23:12	000h RW	**CTOV DWC_ETHER_QOS (CTOV):** Current Time Offset Value Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible).
11	0h RO	**Reserved**
10:8	0h RW	**TILS DWC_ETHER_QOS (TILS):** Time Interval Left Shift Amount This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists. - 000: No left shift needed (equal to x1ns) - 001: Left shift TI by 1 bit (equal to x2ns) - 010: Left shift TI by 2 bits (equal to x4ns) -. -. - 100: Left shift TI by 7 bits (equal to x128ns) Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only.
7:6	0h RW	**LCSE DWC_ETHER_QOS (LCSE):** Loop Count to report Scheduling Error Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register.
5	0h RW	**DFBS DWC_ETHER_QOS (DFBS):** Drop Frames causing Scheduling Error When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped.
4	0h RW	**DDBF DWC_ETHER_QOS (DDBF):** Do not Drop frames during Frame Size Error When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register).
3:2	0h RO	**Reserved**
1	0h RW	**SSWL DWC_ETHER_QOS (SSWL):** Switch to S/W owned list When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared but SWOL is not updated as the switch was not successful. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.
0	0h RW	**EEST DWC_ETHER_QOS (EEST):** Enable EST When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set. When DWC_EQOS_ASP_ECC is selected during the configuration, if any uncorrectable error is detected in the EST memory the hardware will reset this bit and disable the EST function.

21.2.341 MTL_EST_STATUS DWC_ETHER_QOS (MTL_EST_STATUS) — Offset C58h

This register provides Status related to Enhancements to Scheduled Transmission (IEEE802.1Qbv).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO/V	**CGSN DWC_ETHER_QOS (CGSN):** Current GCL Slot Number Indicates the slot number of the GCL list. Slot number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental.
15:12	0h RO	**Reserved**
11:8	0h RO/V	**BTRL DWC_ETHER_QOS (BTRL):** BTR Error Loop Count Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "1111" indicates the iterations exceeded the value of 8 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared.
7	0h RO/V	**SWOL DWC_ETHER_QOS (SWOL):** S/W owned list When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/ writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default.
6:5	0h RO	**Reserved**
4	0h RW	**CGCE DWC_ETHER_QOS (CGCE):** Constant Gate Control Error This error occurs when the list length (LLR) is 1 and the programmed Time Interval (TI) value after the optional Left Shifting is less than or equal to the Cycle Time (CTR). The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
3	0h RO/V	**HLBS DWC_ETHER_QOS (HLBS):** Head-Of-Line Blocking due to Scheduling Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO/V	**HLBF DWC_ETHER_QOS (HLBF):** Head-Of-Line Blocking due to Frame Size Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros.
1	0h RW	**BTRE DWC_ETHER_QOS (BTRE):** BTR Error When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "1111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "1111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
0	0h RW	**SWLC DWC_ETHER_QOS (SWLC):** Switch to S/W owned list Complete When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

21.2.342 MTL_EST_SCH_ERROR DWC_ETHER_QOS (MTL_EST_SCH_ERROR) — Offset C60h

This register provides the One Hot encoded Queue Numbers that are having the Scheduling related error (timeout).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**SEQN DWC_ETHER_QOS (SEQN):** Schedule Error Queue Number The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

21.2.343 MTL_EST_FRM_SIZE_ERROR DWC_ETHER_QOS (MTL_EST_FRM_SIZE_ERROR) — Offset C64h

This register provides the One Hot encoded Queue Numbers that are having the Frame Size related error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**FEQN DWC_ETHER_QOS (FEQN):** Frame Size Error Queue Number The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

21.2.344 MTL_EST_FRM_SIZE_CAPTURE DWC_ETHER_QOS (MTL_EST_FRM_SIZE_CAPTURE) — Offset C68h

This register captures the Frame Size and Queue Number of the first occurrence of the Frame Size related error. Up on clearing it captures the data of immediate next occurrence of a similar error.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C68h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RO/V	**HBFQ DWC_ETHER_QOS (HBFQ):** Queue Number of HLBF Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros.
15	0h RO	**Reserved**
14:0	0000h RO/V	**HBFS DWC_ETHER_QOS (HBFS):** Frame Size of HLBF Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register is all zeros.

21.2.345 MTL_EST_INTR_ENABLE DWC_ETHER_QOS (MTL_EST_INTR_ENABLE) — Offset C70h

This register implements the Interrupt Enable bits for the various events that generate an interrupt. Bit positions have a 1 to 1 correlation with the status bit positions in MTL_ETS_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C70h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4	0h RW	**CGCE DWC_ETHER_QOS (CGCE):** Interrupt Enable for CGCE When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interrupt
3	0h RW	**IEHS DWC_ETHER_QOS (IEHS):** Interrupt Enable for HLBS When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt.
2	0h RW	**IEHF DWC_ETHER_QOS (IEHF):** Interrupt Enable for HLBF When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt.
1	0h RW	**IEBE DWC_ETHER_QOS (IEBE):** Interrupt Enable for BTR Error When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt.
0	0h RW	**IECC DWC_ETHER_QOS (IECC):** Interrupt Enable for Switch List When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt.

21.2.346 MTL_EST_GCL_CONTROL DWC_ETHER_QOS (MTL_EST_GCL_CONTROL) — Offset C80h

This register provides the control information for reading/writing to the Gate Control lists.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C80h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:22	0h RW	**ESTEIEC DWC_ETHER_QOS (ESTEIEC):** ECC Inject Error Control for EST Memory When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. This filed will be valid only if DWC_EQOS_ASP_ECC feature is selected during the configuration, else it will be reserved.
21	0h RW	**ESTEIEE DWC_ETHER_QOS (ESTEIEE):** EST ECC Inject Error Enable When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature.
20	0h RW	**ERR0 DWC_ETHER_QOS (ERR0):** When set indicates the last write operation was aborted as software writes to GCL and GCL registers is prohibited when SSWL bit of MTL_EST_Control Register is set. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
19:17	0h RO	**Reserved**
16:8	000h RW	**ADDR DWC_ETHER_QOS (ADDR):** Gate Control List Address: (GCLA when GCRR is "0"). Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. The width of this field is dependent on DWC_EQOS_EST_DEP; unused bits should be treated as read only. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares. - 000: BTR Low (31:0) - 001: BTR High (63:31) - 010: CTR Low (31:0) - 011: CTR High (39:32) - 100: TER (31:0) - 101: LLR (n:0) (where n is (log{DWC_EQOS_EST_DEP} / log2)) - Others: Reserved
7:6	0h RO	**Reserved**
5	0h RW	**DBGB DWC_ETHER_QOS (DBGB):** Debug Mode Bank Select When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used.
4	0h RW	**DBGM DWC_ETHER_QOS (DBGM):** Debug Mode When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use.
3	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GCRR DWC_ETHER_QOS (GCRR):** Gate Control Related Registers When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA.
1	0h RW	**R1W0 DWC_ETHER_QOS (R1W0):** Read '1', Write '0': When set to '1': Read Operation When set to '0': Write Operation.
0	0h RW	**SRWO DWC_ETHER_QOS (SRWO):** Start Read/Write Op When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.347 MTL_EST_GCL_DATA DWC_ETHER_QOS (MTL_EST_GCL_DATA) — Offset C84h

This register holds the read data or write data in case of reads and writes respectively.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C84h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RW	**GCD DWC_ETHER_QOS (GCD):** Gate Control Data The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations.

21.2.348 MTL_FPE_CTRL_STS DWC_ETHER_QOS (MTL_FPE_CTRL_STS) — Offset C90h

This register controls the operation of, and provides status for Frame Preemption (IEEE802.1Qbu/802.3br).

Type	Size	Offset	Default
MMIO	32 bit	BAR + C90h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RO/V	**HRS DWC_ETHER_QOS (HRS):** Hold/Release Status - 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. - 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State.
27:12	0h RO	**Reserved**
11:8	0h RW	**PEC DWC_ETHER_QOS (PEC):** Preemption Classification When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List.
7:2	0h RO	**Reserved**
1:0	0h RW	**AFSZ DWC_ETHER_QOS (AFSZ):** Additional Fragment Size used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 bytes

21.2.349 MTL_FPE_ADVANCE DWC_ETHER_QOS (MTL_FPE_ADVANCE) — Offset C94h

This register holds the Hold and Release Advance time.

Type	Size	Offset	Default
MMIO	32 bit	BAR + C94h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RW	**RADV DWC_ETHER_QOS (RADV):** Release Advance The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission.

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**HADV DWC_ETHER_QOS (HADV):** Hold Advance The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission.

21.2.350 MTL_ECC_CONTROL DWC_ETHER_QOS (MTL_ECC_CONTROL) — Offset CC0h

The MTL_ECC_Control register establishes the operating mode of ECC related to MTL memories.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**MEEAO DWC_ETHER_QOS (MEEAO):** MTL ECC Error Address Status Over-ride When set, the following error address fields will hold the last valid address where the error is detected. When reset, the following error address fields will hold the first address where the error is detected. EUEAS/ ECEAS of MTL_ECC_Err_Addr_Status register.
7:5	0h RO	**Reserved**
4	0h RW	**TSOEE DWC_ETHER_QOS (TSOEE):** TSO memory ECC Enable When set to 1, enables the ECC feature for TSO memory in DMA. When set to zero, disables the ECC feature for TSO memory in DMA.
3	0h RO	**Reserved**
2	0h RW	**MESTEE DWC_ETHER_QOS (MESTEE):** MTL EST ECC Enable When set to 1, enables the ECC feature for EST memory. When set to zero, disables the ECC feature for EST memory.
1	0h RW	**MRXEE DWC_ETHER_QOS (MRXEE):** MTL Rx FIFO ECC Enable When set to 1, enables the ECC feature for MTL Rx FIFO memory. When set to zero, disables the ECC feature for MTL Rx FIFO memory.
0	0h RW	**MTXEE DWC_ETHER_QOS (MTXEE):** MTL Tx FIFO ECC Enable When set to 1, enables the ECC feature for MTL Tx FIFO memory. When set to zero, disables the ECC feature for MTL Tx FIFO memory.

21.2.351 MTL_SAFETY_INTERRUPT_STATUS DWC_ETHER_QOS (MTL_SAFETY_INTERRUPT_STATUS) — Offset CC4h

The MTL_Safety_Interrupt_Status registers provides Safety interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**MCSIS DWC_ETHER_QOS (MCSIS):** MAC Safety Uncorrectable Interrupt Status Indicates an uncorrectable Safety-related Interrupt is set in the MAC module. MAC_DPP_FSM_Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC.
30:2	0h RO	**Reserved**
1	0h RO/V	**MEUIS DWC_ETHER_QOS (MEUIS):** MTL ECC Uncorrectable error Interrupt Status This bit indicates that an uncorrectable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register.
0	0h RO/V	**MECIS DWC_ETHER_QOS (MECIS):** MTL ECC Correctable error Interrupt Status This bit indicates that a correctable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register.

21.2.352 MTL_ECC_INTERRUPT_ENABLE DWC_ETHER_QOS (MTL_ECC_INTERRUPT_ENABLE) — Offset CC8h

The MTL_ECC_Interrupt_Enable register provides enable bits for the ECC interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CC8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**ECEIE DWC_ETHER_QOS (ECEIE):** EST memory Correctable Error Interrupt Enable When set, generates an interrupt when a correctable error is detected at the MTL EST memory interface. It is indicated in the ECES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt.
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**RXCEIE DWC_ETHER_QOS (RXCEIE):** Rx memory Correctable Error Interrupt Enable When set, generates an interrupt when a correctable error is detected at the MTL Rx memory interface. It is indicated in the RXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt.
3:1	0h RO	**Reserved**
0	0h RW	**TXCEIE DWC_ETHER_QOS (TXCEIE):** Tx memory Correctable Error Interrupt Enable When set, generates an interrupt when a correctable error is detected at the MTL Tx memory interface. It is indicated in the TXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt.

21.2.353 MTL_ECC_INTERRUPT_STATUS DWC_ETHER_QOS (MTL_ECC_INTERRUPT_STATUS) — Offset CCCh

The MTL_ECC_Interrupt_Status register provides MTL ECC Interrupt Status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CCCh	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	**Reserved**
10	0h RW	**EUES DWC_ETHER_QOS (EUES):** MTL EST memory Uncorrectable Error Status When set, indicates that an uncorrectable error is detected at MTL EST memory interface.
9	0h RW	**EAMS DWC_ETHER_QOS (EAMS):** MTL EST memory Address Mismatch Status This bit when set indicates that address mismatch is found for address bus of MTL EST memory.
8	0h RW	**ECES DWC_ETHER_QOS (ECES):** MTL EST memory Correctable Error Status This bit when set indicates that correctable error is detected at the MTL EST memory.
7	0h RO	**Reserved**
6	0h RW	**RXUES DWC_ETHER_QOS (RXUES):** MTL Rx memory Uncorrectable Error Status When set, indicates that an uncorrectable error is detected at the MTL Rx memory interface.
5	0h RW	**RXAMS DWC_ETHER_QOS (RXAMS):** MTL Rx memory Address Mismatch Status This bit when set indicates that address mismatch is found for address bus of the MTL Rx memory.
4	0h RW	**RXCES DWC_ETHER_QOS (RXCES):** MTL Rx memory Correctable Error Status This bit when set indicates that correctable error is detected at the MTL Rx memory.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Reserved**
2	0h RW	**TXUES DWC_ETHER_QOS (TXUES):** MTL Tx memory Uncorrectable Error Status When set, indicates that an uncorrectable error is detected at the MTL TX memory interface.
1	0h RW	**TXAMS DWC_ETHER_QOS (TXAMS):** MTL Tx memory Address Mismatch Status This bit when set indicates that address mismatch is found for address bus of the MTL Tx memory.
0	0h RW	**TXCES DWC_ETHER_QOS (TXCES):** MTL Tx memory Correctable Error Status This bit when set indicates that a correctable error is detected at the MTL Tx memory.

21.2.354 MTL_ECC_ERR_STS_RCTL DWC_ETHER_QOS (MTL_ECC_ERR_STS_RCTL) — Offset CD0h

The MTL_ECC_Err_Sts_Rctl register establishes the control for ECC Error status capture.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	**Reserved**
5	0h RW	**CUES DWC_ETHER_QOS (CUES):** Clear Uncorrectable Error Status When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's uncorrectable error address and uncorrectable error count values will be cleared upon reading. Hardware resets this bit when all the error status values are cleared.
4	0h RW	**CCES DWC_ETHER_QOS (CCES):** Clear Correctable Error Status When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's correctable error address and correctable error count values will be cleared upon reading. Hardware resets this bit when all the error status values are cleared.
3:1	0h RW	**EMS DWC_ETHER_QOS (EMS):** MTL ECC Memory Selection When EESRE bit of this register is set, this field indicates which memory's error status value to be read. The memory selection encoding is as described below.
0	0h RW	**EESRE DWC_ETHER_QOS (EESRE):** MTL ECC Error Status Read Enable When this bit is set, based on the EMS field of this register, the respective memory's error status values will be captured as described below - The correctable and uncorrectable error count values will be captured into MTL_ECC_Err_Cnt_Status register - The address location's of correctable and uncorrectable errors will be captured into MTL_ECC_Err_Addr_Status register. Hardware resets this bit when all the status values are captured into the MTL_ECC_Err_Cnt_Status and MTL_ECC_Err_Addr_Status registers.

21.2.355 MTL_ECC_ERR_ADDR_STATUS DWC_ETHER_QOS (MTL_ECC_ERR_ADDR_STATUS) — Offset CD4h

The MTL_ECC_Err_Addr_Status register provides the memory addresses for the correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD4h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**EUEAS DWC_ETHER_QOS (EUEAS):** MTL ECC Uncorrectable Error Address Status Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which an uncorrectable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which either an uncorrectable error or an address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which either an uncorrectable error or address mismatch is detected.
15:0	0000h RO/V	**ECEAS DWC_ETHER_QOS (ECEAS):** MTL ECC Correctable Error Address Status Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which a correctable error is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which correctable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which correctable error is detected.

21.2.356 MTL_ECC_ERR_CNTR_STATUS DWC_ETHER_QOS (MTL_ECC_ERR_CNTR_STATUS) — Offset CD8h

The MTL_ECC_Err_Cntr_Status register provides ECC Error count for Correctable and uncorrectable errors.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CD8h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
19:16	0h RO/V	**EUECS DWC_ETHER_QOS (EUECS):** MTL ECC Uncorrectable Error Counter Status Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's uncorrectable error count value.
15:8	0h RO	**Reserved**
7:0	00h RO/V	**ECECS DWC_ETHER_QOS (ECECS):** MTL ECC Correctable Error Counter Status Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's correctable error count value.

21.2.357 MTL_DPP_CONTROL DWC_ETHER_QOS (MTL_DPP_CONTROL) — Offset CE0h

The MTL_DPP_Control establishes the operating mode of Data Parity protection and error injection.

Type	Size	Offset	Default
MMIO	32 bit	BAR + CE0h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW	**IPECW DWC_ETHER_QOS (IPECW):** Insert Parity error in CSR Read data parity generator When set to 1, parity bit of first valid data generated by the CSR parity generator (or at PG10 as shown in Fig.AXI slave Interface Data path parity protection) is flipped. Hardware will clear this bit once respective parity bit is flipped.
12	0h RW	**IPEASW DWC_ETHER_QOS (IPEASW):** Insert Parity error in AXI Slave Write data parity generator When set to 1, parity bit of first valid data generated by the AXI parity generator is (or at PG9 as shown in Fig.AXI slave Interface Data path parity protection) flipped. Hardware will clear this bit once respective parity bit is flipped.
11	0h RW	**IPERD DWC_ETHER_QOS (IPERD):** Insert Parity error in Rx write-back Descriptor parity generator When set to 1, parity bit of first valid data generated by the DMA Rx write-back descriptor parity generator(or at PG8 as shown in Fig.Receive data path parity protection) is flipped.
10	0h RW	**IPETD DWC_ETHER_QOS (IPETD):** Insert Parity error in Tx write-back Descriptor parity generator When set to 1, parity bit of first valid data generated by the DMA Tx write-back descriptor parity generator(or at PG4 as shown in Fig.Transmit data path parity protection) is flipped. Hardware will clear this bit once respective parity bit is flipped.
9	0h RW	**IPETSO DWC_ETHER_QOS (IPETSO):** Insert Parity Error in DMA TSO parity generator When set to 1, parity bit of first valid data generated by the DMA TSO parity generator is (or at PG3 as shown in Fig.Transmit data path parity protection) flipped. Hardware will clear this bit once respective parity bit is flipped.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**IPEDDC DWC_ETHER_QOS (IPEDDC):** Insert Parity Error in DMA DTX Control word parity generator When set to 1, parity bit of first valid data generated by the DMA DTX Control word parity generator (or at PG2 as shown in Fig.Transmit data path parity protection) is flipped. Hardware will clear this bit once respective parity bit is flipped.
7	0h RW	**IPEMRF DWC_ETHER_QOS (IPEMRF):** Insert Parity Error in MTL Rx FIFO read control parity generator When set to 1, parity bit of first valid data generated by the MTL Rx FIFO read control parity generator (or at PG7 as shown in Fig.Receive data path parity protection) is flipped. Hardware will clear this bit once respective parity bit is flipped.
6	0h RW	**IPEMTS DWC_ETHER_QOS (IPEMTS):** Insert Parity Error in MTL Tx Status parity generator When set to 1, parity bit of first valid data generated by the MTL Tx Status parity generator (or at PG6 as shown in Fig.Transmit data path parity protection) is flipped. Hardware will clear this bit once respective parity bit is flipped.
5	0h RW	**IPEMC DWC_ETHER_QOS (IPEMC):** Insert Parity Error in MTL checksum parity generator When set to 1, parity bit of first valid data generated by the MTL checksum parity generator (or at PG5 as shown in Fig.Transmit data path parity protection) is flipped. Hardware will clear this bit once the respective parity bit is flipped.
4:3	0h RO	**Reserved**
2	0h RW	**EPSI DWC_ETHER_QOS (EPSI):** Enable Parity on Slave Interface port When set to 1, enables the parity check for the slave interface ports and disables the internal generation of parity for the input slave data port. When set to 0, disables the parity check for the slave interface ports and enables the internal parity generation for the input slave data port.
1	0h RW	**OPE DWC_ETHER_QOS (OPE):** Odd Parity Enable When set to 1, enables odd parity protection on all the external interfaces and when set to 0, enables even parity protection on all the external interfaces.
0	0h RW	**EDPP DWC_ETHER_QOS (EDPP):** Enable Data path Parity Protection When set to 1, enables the parity protection for EQOS datapath by generating and checking the parity on EQOS datapath. When set to 0, disables the parity protection for EQOS datapath.

21.2.358 MTL_TXQ0_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ0_OPERATION_MODE) — Offset D00h

The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D00h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:16	00h RW	**TQS DWC_ETHER_QOS (TQS):** Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
15:7	0h RO	**Reserved**
6:4	0h RW	**TTC DWC_ETHER_QOS (TTC):** Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset.
3:2	0h RW	**TXQEN DWC_ETHER_QOS (TXQEN):** Transmit Queue Enable This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Reserved - 2'b10: Enabled - 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field.
1	0h RW	**TSF DWC_ETHER_QOS (TSF):** Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped.
0	0h RW	**FTQ DWC_ETHER_QOS (FTQ):** Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.359 MTL_TXQ0_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ0_UNDERFLOW) — Offset D04h

The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Type	Size	Offset	Default
MMIO	32 bit	BAR + D04h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11	0h RO/V	**UFCNTOVF DWC_ETHER_QOS (UFCNTOVF):** Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event.
10:0	000h RO/V	**UFFRMCNT DWC_ETHER_QOS (UFFRMCNT):** Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

21.2.360 MTL_TXQ0_DEBUG DWC_ETHER_QOS (MTL_TXQ0_DEBUG) — Offset D08h

The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D08h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RO/V	**STXSTSF DWC_ETHER_QOS (STXSTSF):** Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
18:16	0h RO/V	**PTXQ DWC_ETHER_QOS (PTXQ):** Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	0h RO	**Reserved**
5	0h RO/V	**TXSTSFSTS DWC_ETHER_QOS (TXSTSFSTS):** MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission.
4	0h RO/V	**TXQSTS DWC_ETHER_QOS (TXQSTS):** MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission.
3	0h RO/V	**TWCSTS DWC_ETHER_QOS (TWCSTS):** MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue.
2:1	0h RO/V	**TRCSTS DWC_ETHER_QOS (TRCSTS):** MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller:
0	0h RO/V	**TXQPAUSED DWC_ETHER_QOS (TXQPAUSED):** Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: - Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled - Reception of 802.3x Pause packet when PFC is disabled

21.2.361 MTL_TXQ0_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ0_ETS_STATUS) — Offset D14h

The Queue 0 ETS Status register provides the average traffic transmitted in Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D14h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:0	000000h RO/V	**ABS DWC_ETHER_QOS (ABS_DWC_ETHER_QOS):** Average Bits per Slot This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

21.2.362 MTL_TXQ0_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ0_QUANTUM_WEIGHT) — Offset D18h

The Queue 0 Quantum or Weights register contains the quantum value for Deficit Weighted Round Robin (DWRR), weights for the Weighted Round Robin (WRR), and Weighted Fair Queuing (WFQ) for Queue 0.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D18h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW DWC_ETHER_QOS (ISCQW):** Quantum or Weights When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.

21.2.363 MTL_Q0_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q0_INTERRUPT_CONTROL_STATUS) — Offset D2Ch

This register contains the interrupt enable and status bits for the queue 0 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**RXOIE DWC_ETHER_QOS (RXOIE):** Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled.

Bit Range	Default & Access	Field Name (ID): Description
23:17	0h RO	**Reserved**
16	0h RW	**RXOVFIS DWC_ETHER_QOS (RXOVFIS):** Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
15:10	0h RO	**Reserved**
9	0h RW	**ABPSIE DWC_ETHER_QOS (ABPSIE):** Average Bits Per Slot Interrupt Enable When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event.
8	0h RW	**TXUIE DWC_ETHER_QOS (TXUIE):** Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled.
7:2	0h RO	**Reserved**
1	0h RW	**ABPSIS DWC_ETHER_QOS (ABPSIS):** Average Bits Per Slot Interrupt Status When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
0	0h RW	**TXUNFIS DWC_ETHER_QOS (TXUNFIS):** Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

21.2.364 MTL_RXQ0_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ0_OPERATION_MODE) — Offset D30h

The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Type	Size	Offset	Default
MMIO	32 bit	BAR + D30h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
26:20	00h RW	**RQS DWC_ETHER_QOS (RQS):** Receive Queue Size This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
19:14	00h RW	**RFD DWC_ETHER_QOS (RFD):** Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: - 0: Full minus 1kB, that is, FULL 1kB - 1: Full minus 1.5kB, that is, FULL 1.5 kB - 2: Full minus 2 kB, that is, FULL 2 kB - 3: Full minus 2.5 kB, that is, FULL 2.5kB - ... - 62: Full minus 32kB, that is, FULL 32kB - 63: Full minus 32.5kB, that is, FULL 32.5 kB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4kB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5kB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:8	00h RW	**RFA DWC_ETHER_QOS (RFA):** Threshold for Activating Flow Control (in half-duplex and full-duplex These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD.
7	0h RW	**EHFC DWC_ETHER_QOS (EHFC):** Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled.
6	0h RW	**DIS_TCP_EF DWC_ETHER_QOS (DIS_TCP_EF):** Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset.
5	0h RW	**RSF DWC_ETHER_QOS (RSF):** Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register.
4	0h RW	**FEP DWC_ETHER_QOS (FEP):** Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA.
3	0h RW	**FUP DWC_ETHER_QOS (FUP):** Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01.
2	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
1:0	0h RW	**RTC DWC_ETHER_QOS (RTC):** Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.

21.2.365 MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT) — Offset D34h

The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D34h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	**Reserved**
27	0h RO/V	**MISCNTOVF DWC_ETHER_QOS (MISCNTOVF):** Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event.
26:16	000h RO/V	**MISPKTCNT DWC_ETHER_QOS (MISPKTCNT):** Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	0h RO	**Reserved**
11	0h RO/V	**OVFCNTOVF DWC_ETHER_QOS (OVFCNTOVF):** Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event.
10:0	000h RO/V	**OVFPKTCNT DWC_ETHER_QOS (OVFPKTCNT):** Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

21.2.366 MTL_RXQ0_DEBUG DWC_ETHER_QOS (MTL_RXQ0_DEBUG) — Offset D38h

The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D38h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:16	0000h RO/V	**PRXQ DWC_ETHER_QOS (PRXQ):** Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256kB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	0h RO	**Reserved**
5:4	0h RO/V	**RXQSTS DWC_ETHER_QOS (RXQSTS):** MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue:
3	0h RO	**Reserved**
2:1	0h RO/V	**RRCSTS DWC_ETHER_QOS (RRCSTS):** MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller:
0	0h RO/V	**RWCSTS DWC_ETHER_QOS (RWCSTS):** MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue.

21.2.367 MTL_RXQ0_CONTROL DWC_ETHER_QOS (MTL_RXQ0_CONTROL) — Offset D3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D3Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3	0h RW	**RXQ_FRM_ARBIT DWC_ETHER_QOS (RXQ_FRM_ARBIT):** Receive Queue Packet Arbitration When this bit is set, the DWC_ether_qos drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the DWC_ether_qos drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: - PBL amount of data (indicated by ari_qN_pbl_i[]) or - Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the DWC_ether_qos drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode).
2:0	0h RW	**RXQ_WEGT DWC_ETHER_QOS (RXQ_WEGT):** Receive Queue Weight This field indicates the weight assigned to the Rx Queue 0. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle.

21.2.368 MTL_TXQ1_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ1_OPERATION_MODE) — Offset D40h

The Queue 1 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D40h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:16	00h RW	**TQS DWC_ETHER_QOS (TQS):** Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6:4	0h RW	**TTC DWC_ETHER_QOS (TTC):** Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset.
3:2	0h RW	**TXQEN DWC_ETHER_QOS (TXQEN):** Transmit Queue Enable This field is used to enable/disable the transmit queue 0. - 2'b00: Not enabled - 2'b01: Enable in AV mode - 2'b10: Enabled - 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field.
1	0h RW	**TSF DWC_ETHER_QOS (TSF):** Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped.
0	0h RW	**FTQ DWC_ETHER_QOS (FTQ):** Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.369 MTL_TXQ1_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ1_UNDERFLOW) — Offset D44h

The Queue 1 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset D04h.

21.2.370 MTL_TXQ1_DEBUG DWC_ETHER_QOS (MTL_TXQ1_DEBUG) — Offset D48h

The Queue 1 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset D08h.

21.2.371 MTL_TXQ1_ETS_CONTROL DWC_ETHER_QOS (MTL_TXQ1_ETS_CONTROL) — Offset D50h

The Queue ETS Control register controls the enhanced transmission selection operation.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D50h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RW	**SLC DWC_ETHER_QOS (SLC):** Slot Count If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH[n]_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ[n]_ETS_Status register, need to be computed for Queue. The encoding is as follows:
3	0h RW	**CC DWC_ETHER_QOS (CC):** Credit Control When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated.
2	0h RW	**AVALG DWC_ETHER_QOS (AVALG):** AV Algorithm When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected.
1:0	0h RO	**Reserved**

21.2.372 MTL_TXQ1_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ1_ETS_STATUS) — Offset D54h

The Queue 1 ETS Status register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D54h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
23:0	000000h RO/V	**ABS DWC_ETHER_QOS (ABS_DWC_ETHER_QOS):** Average Bits per Slot This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ[n]_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680.

21.2.373 MTL_TXQ1_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ1_QUANTUM_WEIGHT) — Offset D58h

The Queue 1 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 1.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D58h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20:0	000000h RW	**ISCQW DWC_ETHER_QOS (ISCQW):** idleSlopeCredit, Quantum or Weights - idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. - Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. - Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. - Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. - Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) - Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.

21.2.374 MTL_TXQ1_SENDSLOPECREDIT DWC_ETHER_QOS (MTL_TXQ1_SENDSLOPECREDIT) — Offset D5Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D5Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:0	0000h RW	**SSC DWC_ETHER_QOS (SSC):** sendSlopeCredit Value When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission.

21.2.375 MTL_TXQ1_HICREDIT DWC_ETHER_QOS (MTL_TXQ1_HICREDIT) — Offset D60h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D60h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**HC DWC_ETHER_QOS (HC):** hiCredit Value When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000.

21.2.376 MTL_TXQ1_LOCREDIT DWC_ETHER_QOS (MTL_TXQ1_LOCREDIT) — Offset D64h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Type	Size	Offset	Default
MMIO	32 bit	BAR + D64h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28:0	00000000h RW	**LC DWC_ETHER_QOS (LC):** loCredit Value When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000.

21.2.377 MTL_Q1_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q1_INTERRUPT_CONTROL_STATUS) — Offset D6Ch

This register contains the interrupt enable and status bits for the queue 1 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset D2Ch.

21.2.378 MTL_RXQ1_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ1_OPERATION_MODE) — Offset D70h

The Queue 1 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset D30h.

21.2.379 MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ1_MISSED_PACKET_OVERFLOW_CNT) — Offset D74h

The Queue 1 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset D34h.

21.2.380 MTL_RXQ1_DEBUG DWC_ETHER_QOS (MTL_RXQ1_DEBUG) — Offset D78h

The Queue 1 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset D38h.

21.2.381 MTL_RXQ1_CONTROL DWC_ETHER_QOS (MTL_RXQ1_CONTROL) — Offset D7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset D3Ch.

21.2.382 MTL_TXQ2_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ2_OPERATION_MODE) — Offset D80h

The Queue 2 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset D40h.

21.2.383 MTL_TXQ2_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ2_UNDERFLOW) — Offset D84h

The Queue 2 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset D04h.

21.2.384 MTL_TXQ2_DEBUG DWC_ETHER_QOS (MTL_TXQ2_DEBUG) — Offset D88h

The Queue 2 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset D08h.

21.2.385 MTL_TXQ2_ETS_CONTROL DWC_ETHER_QOS (MTL_TXQ2_ETS_CONTROL) — Offset D90h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset D50h.

21.2.386 MTL_TXQ2_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ2_ETS_STATUS) — Offset D94h

The Queue 2 ETS Status register provides the average traffic transmitted in Queue 2.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset D54h.

21.2.387 MTL_TXQ2_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ2_QUANTUM_WEIGHT) — Offset D98h

The Queue 2 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 2.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset D58h.

21.2.388 MTL_TXQ2_SENDSLOPECREDIT DWC_ETHER_QOS (MTL_TXQ2_SENDSLOPECREDIT) — Offset D9Ch

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset D5Ch.

21.2.389 MTL_TXQ2_HICREDIT DWC_ETHER_QOS (MTL_TXQ2_HICREDIT) — Offset DA0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset D60h.

21.2.390 MTL_TXQ2_LOCREDIT DWC_ETHER_QOS (MTL_TXQ2_LOCREDIT) — Offset DA4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset D64h.

21.2.391 MTL_Q2_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q2_INTERRUPT_CONTROL_STATUS) — Offset DACh

This register contains the interrupt enable and status bits for the queue 2 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset D2Ch.

21.2.392 MTL_RXQ2_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ2_OPERATION_MODE) — Offset DB0h

The Queue 2 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset D30h.

21.2.393 MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ2_MISSED_PACKET_OVERFLOW_CNT) — Offset DB4h

The Queue 2 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset D34h.

21.2.394 MTL_RXQ2_DEBUG DWC_ETHER_QOS (MTL_RXQ2_DEBUG) — Offset DB8h

The Queue 2 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset D38h.

21.2.395 MTL_RXQ2_CONTROL DWC_ETHER_QOS (MTL_RXQ2_CONTROL) — Offset DBCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset D3Ch.

21.2.396 MTL_TXQ3_OPERATION_MODE DWC_ETHER_QOS (MTL_TXQ3_OPERATION_MODE) — Offset DC0h

The Queue 3 Transmit Operation Mode register establishes the Transmit queue operating modes and commands.

Note: Bit definitions are the same as MTL_TXQ1_OPERATION_MODE, offset D40h.

21.2.397 MTL_TXQ3_UNDERFLOW DWC_ETHER_QOS (MTL_TXQ3_UNDERFLOW) — Offset DC4h

The Queue 3 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

Note: Bit definitions are the same as MTL_TXQ0_UNDERFLOW, offset D04h.

21.2.398 MTL_TXQ3_DEBUG DWC_ETHER_QOS (MTL_TXQ3_DEBUG) — Offset DC8h

The Queue 3 Transmit Debug register gives the debug status of various blocks related to the Transmit queue.

Note: Bit definitions are the same as MTL_TXQ0_DEBUG, offset D08h.

21.2.399 MTL_TXQ3_ETS_CONTROL DWC_ETHER_QOS (MTL_TXQ3_ETS_CONTROL) — Offset DD0h

The Queue ETS Control register controls the enhanced transmission selection operation.

Note: Bit definitions are the same as MTL_TXQ1_ETS_CONTROL, offset D50h.

21.2.400 MTL_TXQ3_ETS_STATUS DWC_ETHER_QOS (MTL_TXQ3_ETS_STATUS) — Offset DD4h

The Queue 3 ETS Status register provides the average traffic transmitted in Queue 3.

Note: Bit definitions are the same as MTL_TXQ1_ETS_STATUS, offset D54h.

21.2.401 MTL_TXQ3_QUANTUM_WEIGHT DWC_ETHER_QOS (MTL_TXQ3_QUANTUM_WEIGHT) — Offset DD8h

The Queue 3 idleSlopeCredit, Quantum or Weights register provides the average traffic transmitted in Queue 3.

Note: Bit definitions are the same as MTL_TXQ1_QUANTUM_WEIGHT, offset D58h.

21.2.402 MTL_TXQ3_SENDSLOPECREDIT DWC_ETHER_QOS (MTL_TXQ3_SENDSLOPECREDIT) — Offset DDCh

The sendSlopeCredit register contains the sendSlope credit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_SENDSLOPECREDIT, offset D5Ch.

21.2.403 MTL_TXQ3_HICREDIT DWC_ETHER_QOS (MTL_TXQ3_HICREDIT) — Offset DE0h

The hiCredit register contains the hiCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_HICREDIT, offset D60h.

21.2.404 MTL_TXQ3_LOCREDIT DWC_ETHER_QOS (MTL_TXQ3_LOCREDIT) — Offset DE4h

The loCredit register contains the loCredit value required for the credit-based shaper algorithm for the Queue.

Note: Bit definitions are the same as MTL_TXQ1_LOCREDIT, offset D64h.

21.2.405 MTL_Q3_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q3_INTERRUPT_CONTROL_STATUS) — Offset DECh

This register contains the interrupt enable and status bits for the queue 3 interrupts.

Note: Bit definitions are the same as MTL_Q0_INTERRUPT_CONTROL_STATUS, offset D2Ch.

21.2.406 MTL_RXQ3_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ3_OPERATION_MODE) — Offset DF0h

The Queue 3 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset D30h.

21.2.407 MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ3_MISSED_PACKET_OVERFLOW_CNT) — Offset DF4h

The Queue 3 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset D34h.

21.2.408 MTL_RXQ3_DEBUG DWC_ETHER_QOS (MTL_RXQ3_DEBUG) — Offset DF8h

The Queue 3 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset D38h.

21.2.409 MTL_RXQ3_CONTROL DWC_ETHER_QOS (MTL_RXQ3_CONTROL) — Offset DFCh

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset D3Ch.

21.2.410 MTL_Q4_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q4_INTERRUPT_CONTROL_STATUS) — Offset E2Ch

This register contains the interrupt enable and status bits for the queue 4 interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + E2Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**RXOIE DWC_ETHER_QOS (RXOIE):** Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled.
23:17	0h RO	**Reserved**
16	0h RW	**RXOVFIS DWC_ETHER_QOS (RXOVFIS):** Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
15:0	0h RO	**Reserved**

21.2.411 MTL_RXQ4_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ4_OPERATION_MODE) — Offset E30h

The Queue 4 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset D30h.

21.2.412 MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ4_MISSED_PACKET_OVERFLOW_CNT) — Offset E34h

The Queue 4 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset D34h.

21.2.413 MTL_RXQ4_DEBUG DWC_ETHER_QOS (MTL_RXQ4_DEBUG) — Offset E38h

The Queue 4 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset D38h.

21.2.414 MTL_RXQ4_CONTROL DWC_ETHER_QOS (MTL_RXQ4_CONTROL) — Offset E3Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset D3Ch.

21.2.415 MTL_Q5_INTERRUPT_CONTROL_STATUS DWC_ETHER_QOS (MTL_Q5_INTERRUPT_CONTROL_STATUS) — Offset E6Ch

This register contains the interrupt enable and status bits for the queue 5 interrupts.

Note: Bit definitions are the same as MTL_Q4_INTERRUPT_CONTROL_STATUS, offset E2Ch.

21.2.416 MTL_RXQ5_OPERATION_MODE DWC_ETHER_QOS (MTL_RXQ5_OPERATION_MODE) — Offset E70h

The Queue 5 Receive Operation Mode register establishes the Receive queue operating modes and command. The RFA and RFD fields are not backward compatible with the RFA and RFD fields of 4.00a release

Note: Bit definitions are the same as MTL_RXQ0_OPERATION_MODE, offset D30h.

21.2.417 MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT DWC_ETHER_QOS (MTL_RXQ5_MISSED_PACKET_OVERFLOW_CNT) — Offset E74h

The Queue 5 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow.

Note: Bit definitions are the same as MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT, offset D34h.

21.2.418 MTL_RXQ5_DEBUG DWC_ETHER_QOS (MTL_RXQ5_DEBUG) — Offset E78h

The Queue 5 Receive Debug register gives the debug status of various blocks related to the Receive queue.

Note: Bit definitions are the same as MTL_RXQ0_DEBUG, offset D38h.

21.2.419 MTL_RXQ5_CONTROL DWC_ETHER_QOS (MTL_RXQ5_CONTROL) — Offset E7Ch

The Queue Receive Control register controls the receive arbitration and passing of received packets to the application.

Note: Bit definitions are the same as MTL_RXQ0_CONTROL, offset D3Ch.

21.2.420 DMA_MODE DWC_ETHER_QOS (DMA_MODE) — Offset 1000h

The Bus Mode register establishes the bus operating modes for the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1000h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**INTM DWC_ETHER_QOS (INTM):** Interrupt Mode This field defines the interrupt mode of DWC_ether_qos. The behavior of the following outputs changes depending on the following settings: - sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) - sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) - sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. - 00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. - 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. - 11: Reserved For more details refer to the Table "DWC_ether_qos Transfer Complete Interrupt Behavior".
15:11	0h RO	**Reserved**
10	0h RW	**Reserved**
9	0h RO	**Reserved**
8	0h RW	**DSPW DWC_ETHER_QOS (DSPW):** Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted.
7:1	0h RO	**Reserved**
0	0h RW	**SWR DWC_ETHER_QOS (SWR):** Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

21.2.421 DMA_SYSBUS_MODE DWC_ETHER_QOS (DMA_SYSBUS_MODE) — Offset 1004h

The System Bus mode register controls the behavior of the AHB or AXI master. It mainly controls burst splitting and number of outstanding requests.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1004h	01010000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**EN_LPI DWC_ETHER_QOS (EN_LPI):** Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller.
30	0h RW	**LPI_XIT_PKT DWC_ETHER_QOS (LPI_XIT_PKT):** Unlock on Magic Packet or Remote Wake-Up Packet When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received.
29:28	0h RO	**Reserved**
27:24	1h RW	**WR_OSR_LMT DWC_ETHER_QOS (WR_OSR_LMT):** AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note: - Bit 26 is reserved if DWC_ETHER_QOS_AXI_MAX_WR_REQ = 4 - Bit 27 is reserved if DWC_ETHER_QOS_AXI_MAX_WR_REQ!= 16
23:20	0h RO	**Reserved**
19:16	1h RW	**RD_OSR_LMT DWC_ETHER_QOS (RD_OSR_LMT):** AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Note: - Bit 18 is reserved if parameter DWC_ETHER_QOS_AXI_MAX_RD_REQ = 4 - Bit 19 is reserved if parameter DWC_ETHER_QOS_AXI_MAX_RD_REQ!= 16
15:14	0h RO	**Reserved**
13	0h RW	**ONEkBBE DWC_ETHER_QOS (ONEkBBE):** 1 kB Boundary Crossing Enable for the EQOS-AXI Master When set, the burst transfers performed by the EQOS-AXI master do not cross 1 kB boundary. When reset, the burst transfers performed by the EQOS-AXI master do not cross 4 kB boundary.
12	0h RW	**AAL DWC_ETHER_QOS (AAL):** Address-Aligned Beats When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels.
11	0h RW	**EAME DWC_ETHER_QOS (EAME):** Enhanced Address Mode Enable. When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**AALE DWC_ETHER_QOS (AALE):** Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the DWC_ether_qos for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register.
9:8	0h RO	**Reserved**
7	0h RW	**BLEN256 DWC_ETHER_QOS (BLEN256):** AXI Burst Length 256 When this bit is set to 1, the EQOS-AXI master can select a burst length of 256 on the AXI interface.
6	0h RW	**BLEN128 DWC_ETHER_QOS (BLEN128):** AXI Burst Length 128 When this bit is set to 1, the EQOS-AXI master can select a burst length of 128 on the AXI interface.
5	0h RW	**BLEN64 DWC_ETHER_QOS (BLEN64):** AXI Burst Length 64 When this bit is set to 1, the EQOS-AXI master can select a burst length of 64 on the AXI interface.
4	0h RW	**BLEN32 DWC_ETHER_QOS (BLEN32):** AXI Burst Length 32 When this bit is set to 1, the EQOS-AXI master can select a burst length of 32 on the AXI interface.
3	0h RW	**BLEN16 DWC_ETHER_QOS (BLEN16):** AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.
2	0h RW	**BLEN8 DWC_ETHER_QOS (BLEN8):** AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.
1	0h RW	**BLEN4 DWC_ETHER_QOS (BLEN4):** AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.
0	0h RW	**FB DWC_ETHER_QOS (FB):** Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. - Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field - Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1].

21.2.422 DMA_INTERRUPT_STATUS DWC_ETHER_QOS (DMA_INTERRUPT_STATUS) — Offset 1008h

The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1008h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17	0h RO/V	**MACIS DWC_ETHER_QOS (MACIS):** MAC Interrupt Status This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source.
16	0h RO/V	**MTLIS DWC_ETHER_QOS (MTLIS):** MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source.
15:6	0h RO	**Reserved**
5	0h RO/V	**DC5IS DWC_ETHER_QOS (DC5IS):** DMA Channel 5 Interrupt Status This bit indicates an interrupt event in DMA Channel 5. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 5 to get the exact cause of the interrupt and clear its source.
4	0h RO/V	**DC4IS DWC_ETHER_QOS (DC4IS):** DMA Channel 4 Interrupt Status This bit indicates an interrupt event in DMA Channel 4. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 4 to get the exact cause of the interrupt and clear its source.
3	0h RO/V	**DC3IS DWC_ETHER_QOS (DC3IS):** DMA Channel 3 Interrupt Status This bit indicates an interrupt event in DMA Channel 3. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 3 to get the exact cause of the interrupt and clear its source.
2	0h RO/V	**DC2IS DWC_ETHER_QOS (DC2IS):** DMA Channel 2 Interrupt Status This bit indicates an interrupt event in DMA Channel 2. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 2 to get the exact cause of the interrupt and clear its source.
1	0h RO/V	**DC1IS DWC_ETHER_QOS (DC1IS):** DMA Channel 1 Interrupt Status This bit indicates an interrupt event in DMA Channel 1. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 1 to get the exact cause of the interrupt and clear its source.
0	0h RO/V	**DC0IS DWC_ETHER_QOS (DC0IS):** DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source.

21.2.423 DMA_DEBUG_STATUS0 DWC_ETHER_QOS (DMA_DEBUG_STATUS0) — Offset 100Ch

The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 100Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	**TPS2 DWC_ETHER_QOS (TPS2):** DMA Channel 2 Transmit Process State This field indicates the Tx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt.
27:24	0h RO/V	**RPS2 DWC_ETHER_QOS (RPS2):** DMA Channel 2 Receive Process State This field indicates the Rx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt.
23:20	0h RO/V	**TPS1 DWC_ETHER_QOS (TPS1):** DMA Channel 1 Transmit Process State This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt.
19:16	0h RO/V	**RPS1 DWC_ETHER_QOS (RPS1):** DMA Channel 1 Receive Process State This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt.
15:12	0h RO/V	**TPS0 DWC_ETHER_QOS (TPS0):** DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt.
11:8	0h RO/V	**RPS0 DWC_ETHER_QOS (RPS0):** DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt.
7:2	0h RO	**Reserved**
1	0h RO/V	**AXRHSTS DWC_ETHER_QOS (AXRHSTS):** AXI Master Read Channel Status When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data.
0	0h RO/V	**AXWHSTS DWC_ETHER_QOS (AXWHSTS):** AXI Master Write Channel When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data.

21.2.424 DMA_DEBUG_STATUS1 DWC_ETHER_QOS (DMA_DEBUG_STATUS1) — Offset 1010h

The Debug Status1 register gives the Receive and Transmit process status for DMA Channel 3-Channel 6.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1010h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO/V	**RPS5 DWC_ETHER_QOS (RPS5):** DMA Channel 5 Receive Process State This field indicates the Rx DMA FSM state for Channel 5. The MSB of this field always returns 0. This field does not generate an interrupt.
15:12	0h RO	**Reserved**
11:8	0h RO/V	**RPS4 DWC_ETHER_QOS (RPS4):** DMA Channel 4 Receive Process State This field indicates the Rx DMA FSM state for Channel 4. The MSB of this field always returns 0. This field does not generate an interrupt.
7:4	0h RO/V	**TPS3 DWC_ETHER_QOS (TPS3):** DMA Channel 3 Transmit Process State This field indicates the Tx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt.
3:0	0h RO/V	**RPS3 DWC_ETHER_QOS (RPS3):** DMA Channel 3 Receive Process State This field indicates the Rx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt.

21.2.425 AXI4_TX_AR_ACE_CONTROL DWC_ETHER_QOS (AXI4_TX_AR_ACE_CONTROL) — Offset 1020h

This register is used to control the AXI4 Cache Coherency Signals for read transactions by all the Transmit DMA channels. The following signals of the AXI4 interface are driven with different values as programmed for corresponding type (descriptor, buffer1, buffer2) of access. - arcache_m_o[3:0] - ardomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1020h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**THD DWC_ETHER_QOS (THD):** Transmit DMA First Packet Buffer or TSO Header Domain Control When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO Header data.
19:16	0h RW	**THC DWC_ETHER_QOS (THC):** Transmit DMA First Packet Buffer or TSO Header Cache Control When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).. When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO Header data.
15:14	0h RO	**Reserved**
13:12	0h RW	**TED DWC_ETHER_QOS (TED):** Transmit DMA Extended Packet Buffer or TSO Payload Domain Control When TSO is NOT enabled, This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive ardomain_o[1:0] signal when the Transmit DMA is accessing the TSO payload data.
11:8	0h RW	**TEC DWC_ETHER_QOS (TEC):** Transmit DMA Extended Packet Buffer or TSO Payload Cache Control When TSO is NOT enabled, This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). When TSO is enabled, This field is used to drive arcache_o[3:0] signal when the Transmit DMA is accessing the TSO payload data.
7:6	0h RO	**Reserved**
5:4	0h RW	**TDRD DWC_ETHER_QOS (TDRD):** Transmit DMA Read Descriptor Domain Control This field is used to drive ardomain_o[1:0] signal when Transmit DMA engines access the Descriptor.
3:0	0h RW	**TDRC DWC_ETHER_QOS (TDRC):** Transmit DMA Read Descriptor Cache Control This field is used to drive arcache_o[3:0] signal when Transmit DMA engines access the Descriptor.

21.2.426 AXI4_RX_AW_ACE_CONTROL DWC_ETHER_QOS (AXI4_RX_AW_ACE_CONTROL) — Offset 1024h

This register is used to control the AXI4 Cache Coherency Signals for write transactions by all the Receive DMA channels. The following signals of the AXI4 interface are driven with different values as programmed for corresponding type (descriptor, buffer1, buffer2) of access. - awcache_m_o[3:0] - awdomain_m_o[1:0]

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1024h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:28	0h RW	**RDD DWC_ETHER_QOS (RDD):** Receive DMA Buffer Domain Control This field is used to drive the awdomain_o[1:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
27:24	0h RW	**RDC DWC_ETHER_QOS (RDC):** Receive DMA Buffer Cache Control This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated.
23:22	0h RO	**Reserved**
21:20	0h RW	**RHD DWC_ETHER_QOS (RHD):** Receive DMA Header Domain Control This field is used to drive awdomain_o[1:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
19:16	0h RW	**RHC DWC_ETHER_QOS (RHC):** Receive DMA Header Cache Control This field is used to drive awcache_o[3:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated.
15:14	0h RO	**Reserved**
13:12	0h RW	**RPD DWC_ETHER_QOS (RPD):** Receive DMA Payload Domain Control This field is used to drive awdomain_o[1:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
11:8	0h RW	**RPC DWC_ETHER_QOS (RPC):** Receive DMA Payload Cache Control This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated.
7:6	0h RO	**Reserved**
5:4	0h RW	**RDWD DWC_ETHER_QOS (RDWD):** Receive DMA Write Descriptor Domain Control This field is used to drive awdomain_o[1:0] signal when Receive DMA accesses the Descriptor.
3:0	0h RW	**RDWC DWC_ETHER_QOS (RDWC):** Receive DMA Write Descriptor Cache Control This field is used to drive awcache_o[3:0] signal when Receive DMA accesses the Descriptor.

21.2.427 AXI4_TXRX_AWAR_ACE_CONTROL DWC_ETHER_QOS (AXI4_TXRX_AWAR_ACE_CONTROL) — Offset 1028h

This register is used to control the AXI4 Cache Coherency Signals for Descriptor write transactions by all the TxDMA channels and Descriptor read transactions by all the RxDMA channels. It also controls the values to be driven on awprot_m_o and arprot_m_o.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1028h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22:20	0h RW	**WRP DWC_ETHER_QOS (WRP):** DMA Write Protection control This field is used to drive awprot_m_o[2:0] signal on the AXI Write Channel.
19	0h RO	**Reserved**
18:16	0h RW	**RDP DWC_ETHER_QOS (RDP):** DMA Read Protection control This field is used to drive arprot_m_o[2:0] signal during all read requests.
15:14	0h RO	**Reserved**
13:12	0h RW	**RDRD DWC_ETHER_QOS (RDRD):** Receive DMA Read Descriptor Domain control This field is used to drive ardomain_o[1:0] signal when Receive DMA engines read the Descriptor.
11:8	0h RW	**RDRC DWC_ETHER_QOS (RDRC):** Receive DMA Read Descriptor Cache control This field is used to drive arcache_o[3:0] signal when Receive DMA engines read the Descriptor.
7:6	0h RO	**Reserved**
5:4	0h RW	**TDWD DWC_ETHER_QOS (TDWD):** Transmit DMA Write Descriptor Domain control This field is used to drive awdomain_o[1:0] signal when Transmit DMA write to the Descriptor.
3:0	0h RW	**TDWC DWC_ETHER_QOS (TDWC):** Transmit DMA Write Descriptor Cache control This field is used to drive awcache_o[3:0] signal when Transmit DMA writes to the Descriptor.

21.2.428 AXI_LPI_ENTRY_INTERVAL DWC_ETHER_QOS (AXI_LPI_ENTRY_INTERVAL) — Offset 1040h

This register is used to control the AXI LPI entry interval.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1040h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**Reserved**
3:0	0h RW	**LPIEI DWC_ETHER_QOS (LPIEI):** LPI Entry Interval Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the DWC_ether_qos to enter into the AXI low power state 0 indicates 64 clock cycles

21.2.429 DMA_TBS_CTRL DWC_ETHER_QOS (DMA_TBS_CTRL) — Offset 1050h

This register is used to control the TBS attributes.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1050h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	000000h RW	**FTOS DWC_ETHER_QOS (FTOS):** Fetch Time Offset The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value.
7	0h RO	**Reserved**
6:4	0h RW	**FGOS DWC_ETHER_QOS (FGOS):** Fetch GSN Offset The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set.
3:1	0h RO	**Reserved**
0	0h RW	**FTOV DWC_ETHER_QOS (FTOV):** Fetch Time Offset Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the DMA engine can fetch the frames from host memory without any time restrictions.

21.2.430 DMA_SAFETY_INTERRUPT_STATUS DWC_ETHER_QOS (DMA_SAFETY_INTERRUPT_STATUS) — Offset 1080h

This register indicates summary (whether error occured in DMA/MTL/MAC and correctable/uncorrectable) of the Automotive Safety related error interrupts.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1080h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**MCSIS DWC_ETHER_QOS (MCSIS):** MAC Safety Uncorrectable Interrupt Status Indicates a uncorrectable Safety related Interrupt is set in the MAC module. MAC_DPP_FSM_Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC.
30	0h RO	**Reserved**
29	0h RO/V	**MSUIS DWC_ETHER_QOS (MSUIS):** MTL Safety Uncorrectable error Interrupt Status This bit indicates an uncorrectable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register.
28	0h RO/V	**MSCIS DWC_ETHER_QOS (MSCIS):** MTL Safety Correctable error Interrupt Status This bit indicates a correctable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register.
27:2	0h RO	**Reserved**
1	0h RO/V	**DEUIS DWC_ETHER_QOS (DEUIS):** DMA ECC Uncorrectable error Interrupt Status This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register.
0	0h RO/V	**DECIS DWC_ETHER_QOS (DECIS):** DMA ECC Correctable error Interrupt Status This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register.

21.2.431 DMA_ECC_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_ECC_INTERRUPT_ENABLE) — Offset 1084h

This register is used to enable the Automotive Safety related TSO memory ECC error interrupt.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1084h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**TCEIE DWC_ETHER_QOS (TCEIE):** TSO memory Correctable Error Interrupt Enable When set, generates an interrupt when a correctable error is detected at the DMA TSO memory interface. It is indicated in the TCES bit of DMA_ECC_Interrupt_Status register. When reset this event does not generates an interrupt.

21.2.432 DMA_ECC_INTERRUPT_STATUS DWC_ETHER_QOS (DMA_ECC_INTERRUPT_STATUS) — Offset 1088h

This register indicates the Automotive Safety related TSO memory ECC error interrupt status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1088h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	**Reserved**
2	0h RW	**TUES DWC_ETHER_QOS (TUES):** DMA TSO memory Uncorrectable Error status When set, indicates that an uncorrectable error is detected at DMA TSO memory interface.
1	0h RW	**TAMS DWC_ETHER_QOS (TAMS):** DMA TSO memory Address Mismatch status This bit when set indicates that address mismatch is found for address bus of DMA TSO memory.
0	0h RW	**TCES DWC_ETHER_QOS (TCES):** DMA TSO memory Correctable Error status This bit when set indicates that correctable error is detected at DMA TSO memory interface.

21.2.433 DMA_CH0_CONTROL DWC_ETHER_QOS (DMA_CH0_CONTROL) — Offset 1100h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1100h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved** Platform firmware & software shall not set this field to 0x1
23:21	0h RO	**Reserved**
20:18	0h RW	**DSL DWC_ETHER_QOS (DSL):** Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**PBLX8 DWC_ETHER_QOS (PBLX8):** 8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.
15:14	0h RO	**Reserved**
13:0	0000h RW	**MSS DWC_ETHER_QOS (MSS):** Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

21.2.434 DMA_CH0_TX_CONTROL DWC_ETHER_QOS (DMA_CH0_TX_CONTROL) — Offset 1104h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1104h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW	**EDSE DWC_ETHER_QOS (EDSE):** Enhanced Descriptor Enable When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes.
27:24	0h RW	**TQOS DWC_ETHER_QOS (TQOS):** Transmit QOS. This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0.
23:22	0h RO	**Reserved**
21:16	00h RW	**TXPBL DWC_ETHER_QOS (TXPBL):** Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RW	**IPBL DWC_ETHER_QOS (IPBL):** Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer.
14:13	0h RW	**TSE_MODE DWC_ETHER_QOS (TSE_MODE):** TSE Mode - 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. - 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. - 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. - 11: Reserved
12	0h RW	**TSE DWC_ETHER_QOS (TSE):** TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4.
11:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**OSF DWC_ETHER_QOS (OSF):** Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained.
3:1	0h RO	**Reserved**
0	0h RW	**ST DWC_ETHER_QOS (ST):** Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. - The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state.

21.2.435 DMA_CH0_RX_CONTROL DWC_ETHER_QOS (DMA_CH0_RX_CONTROL) — Offset 1108h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1108h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RPF DWC_ETHER_QOS (RPF):** Rx Packet Flush. When this bit is set to 1, then DWC_ether_qos automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the DWC_ether_qos not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the corresponding RxQueue.
30:28	0h RO	**Reserved**
27:24	0h RW	**RQOS DWC_ETHER_QOS (RQOS):** Rx AXI4 QOS. This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0.

Bit Range	Default & Access	Field Name (ID): Description
23:22	0h RO	**Reserved**
21:16	00h RW	**RXPBL DWC_ETHER_QOS (RXPBL):** Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	0h RO	**Reserved**
14:4	000h RW	**RBSZ_13_Y DWC_ETHER_QOS (RBSZ_13_Y):** Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).
3:1	0h RO/V	**RBSZ_X_0 DWC_ETHER_QOS (RBSZ_X_0):** Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO).
0	0h RW	**SR DWC_ETHER_QOS (SR):** Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions: - The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. - The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state.

21.2.436 DMA_CH0_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH0_TXDESC_LIST_HADDRESS) — Offset 1110h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1110h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**TDESHA DWC_ETHER_QOS (TDESHA):** Start of Transmit List This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

21.2.437 DMA_CH0_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH0_TXDESC_LIST_ADDRESS) — Offset 1114h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1114h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**TDESLA DWC_ETHER_QOS (TDESLA):** Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

21.2.438 DMA_CH0_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH0_RXDESC_LIST_HADDRESS) — Offset 1118h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1118h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RW	**RDESHA DWC_ETHER_QOS (RDESHA):** Start of Receive List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

21.2.439 DMA_CH0_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH0_RXDESC_LIST_ADDRESS) — Offset 111Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 111Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**RDESLA DWC_ETHER_QOS (RDESLA):** Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

21.2.440 DMA_CH0_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH0_TXDESC_TAIL_POINTER) — Offset 1120h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1120h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**TDTP DWC_ETHER_QOS (TDTP):** Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

21.2.441 DMA_CH0_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH0_RXDESC_TAIL_POINTER) — Offset 1128h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1128h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:3	00000000h RW	**RDTP DWC_ETHER_QOS (RDTP):** Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: - 31:2 for 32-bit configuration - 31:3 for 64-bit configuration - 31:4 for 128-bit configuration
2:0	0h RO	**Reserved**

21.2.442 DMA_CH0_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH0_TXDESC_RING_LENGTH) — Offset 112Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 112Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**TDRL DWC_ETHER_QOS (TDRL):** Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Intel recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

21.2.443 DMA_CH0_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH0_RXDESC_RING_LENGTH) — Offset 1130h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1130h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	000h RW	**RDRL DWC_ETHER_QOS (RDRL):** Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

21.2.444 DMA_CH0_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH0_INTERRUPT_ENABLE) — Offset 1134h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1134h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**NIE DWC_ETHER_QOS (NIE):** Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled.
14	0h RW	**AIE DWC_ETHER_QOS (AIE):** Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled.
13	0h RW	**CDEE DWC_ETHER_QOS (CDEE):** Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**FBEE DWC_ETHER_QOS (FBEE):** Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled.
11	0h RW	**ERIE DWC_ETHER_QOS (ERIE):** Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled.
10	0h RO	**Reserved**
9	0h RW	**RWTE DWC_ETHER_QOS (RWTE):** Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled.
8	0h RW	**RSE DWC_ETHER_QOS (RSE):** Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.
7	0h RW	**RBUE DWC_ETHER_QOS (RBUE):** Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled.
6	0h RW	**RIE DWC_ETHER_QOS (RIE):** Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.
5:3	0h RO	**Reserved**
2	0h RW	**TBUE DWC_ETHER_QOS (TBUE):** Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled.
1	0h RW	**TXSE DWC_ETHER_QOS (TXSE):** Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled.
0	0h RW	**TIE DWC_ETHER_QOS (TIE):** Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.

21.2.445 DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER) — Offset 1138h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1138h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**RWTU DWC_ETHER_QOS (RWTU):** Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. - 2'b00: 256 - 2'b01: 512 - 2'b10: 1024 - 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	0h RO	**Reserved**
7:0	00h RW	**RWT DWC_ETHER_QOS (RWT):** Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

21.2.446 DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS) — Offset 113Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 113Ch	000007C0h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:16	0h RO/V	**RSN DWC_ETHER_QOS (RSN):** Reference Slot Number This field gives the current value of the reference slot number in the DMA. It is used for slot comparison.

Bit Range	Default & Access	Field Name (ID): Description
15:4	07Ch RW	**SIV DWC_ETHER_QOS (SIV):** Slot Interval Value This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us
3:2	0h RO	**Reserved**
1	0h RW	**ASC DWC_ETHER_QOS (ASC):** Advance Slot Check When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is - equal to the reference slot number given in the RSN field or - ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set.
0	0h RW	**ESC DWC_ETHER_QOS (ESC):** Enable Slot Comparison When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is - equal to the reference slot number or - ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets.

21.2.447 DMA_CH0_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_TXDESC) — Offset 1144h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1144h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CURTDESAPTR DWC_ETHER_QOS (CURTDESAPTR):** Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

21.2.448 DMA_CH0_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_RXDESC) — Offset 114Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 114Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CURRDESAPTR DWC_ETHER_QOS (CURRDESAPTR):** Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

21.2.449 DMA_CH0_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_TXBUFFER_H) — Offset 1150h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1150h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**CURTBUFAPTRH DWC_ETHER_QOS (CURTBUFAPTRH):** Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

21.2.450 DMA_CH0_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_TXBUFFER) — Offset 1154h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1154h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CURTBUFAPTR DWC_ETHER_QOS (CURTBUFAPTR):** Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

21.2.451 DMA_CH0_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_RXBUFFER_H) — Offset 1158h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1158h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	00h RO/V	**CURRBUFAPTRH DWC_ETHER_QOS (CURRBUFAPTRH):** Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

21.2.452 DMA_CH0_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH0_CURRENT_APP_RXBUFFER) — Offset 115Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 115Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h RO/V	**CURRBUFAPTR DWC_ETHER_QOS (CURRBUFAPTR):** Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

21.2.453 DMA_CH0_STATUS DWC_ETHER_QOS (DMA_CH0_STATUS) — Offset 1160h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH[n]_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1160h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	**Reserved**
21:19	0h RO/V	**REB DWC_ETHER_QOS (REB):** Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 21 -- 1'b1: Error during data transfer by Rx DMA -- 1'b0: No Error during data transfer by Rx DMA - Bit 20 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 19 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	0h RO/V	**TEB DWC_ETHER_QOS (TEB):** Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. - Bit 18 -- 1'b1: Error during data transfer by Tx DMA -- 1'b0: No Error during data transfer by Tx DMA - Bit 17 -- 1'b1: Error during descriptor access -- 1'b0: Error during data buffer access - Bit 16 -- 1'b1: Error during read transfer -- 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**NIS DWC_ETHER_QOS (NIS):** Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
14	0h RW	**AIS DWC_ETHER_QOS (AIS):** Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit 1: Transmit Process Stopped - Bit 7: Receive Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
13	0h RW	**CDE DWC_ETHER_QOS (CDE):** Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
12	0h RW	**FBE DWC_ETHER_QOS (FBE):** Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
11	0h RW	**ERI DWC_ETHER_QOS (ERI):** Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
10	0h RO	**Reserved**
9	0h RW	**RWT DWC_ETHER_QOS (RWT):** Receive Watchdog Timeout This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received.
8	0h RW	**RPS DWC_ETHER_QOS (RPS):** Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
7	0h RW	**RBU DWC_ETHER_QOS (RBU):** Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**RI DWC_ETHER_QOS (RI):** Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
5:3	0h RO	**Reserved**
2	0h RW	**TBU DWC_ETHER_QOS (TBU):** Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
1	0h RW	**TPS DWC_ETHER_QOS (TPS):** Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.
0	0h RW	**TI DWC_ETHER_QOS (TI):** Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.

21.2.454 DMA_CH0_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH0_MISS_FRAME_CNT) — Offset 1164h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1164h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RO/V	**MFCO DWC_ETHER_QOS (MFCO):** Overflow status of the MFC Counter When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.
14:11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:0	000h RO/V	**MFC DWC_ETHER_QOS (MFC):** Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

21.2.455 DMA_CH0_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH0_RX_ERI_CNT) — Offset 116Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 116Ch	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	000h RO/V	**ECNT DWC_ETHER_QOS (ECNT):** ERI Counter When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet.

21.2.456 DMA_CH1_CONTROL DWC_ETHER_QOS (DMA_CH1_CONTROL) — Offset 1180h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 1100h.

21.2.457 DMA_CH1_TX_CONTROL DWC_ETHER_QOS (DMA_CH1_TX_CONTROL) — Offset 1184h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 1104h.

21.2.458 DMA_CH1_RX_CONTROL DWC_ETHER_QOS (DMA_CH1_RX_CONTROL) — Offset 1188h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 1108h.

21.2.459 DMA_CH1_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH1_TXDESC_LIST_HADDRESS) — Offset 1190h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 1110h.

21.2.460 DMA_CH1_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH1_TXDESC_LIST_ADDRESS) — Offset 1194h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 1114h.

21.2.461 DMA_CH1_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH1_RXDESC_LIST_HADDRESS) — Offset 1198h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 1118h.

21.2.462 DMA_CH1_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH1_RXDESC_LIST_ADDRESS) — Offset 119Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 111Ch.

21.2.463 DMA_CH1_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH1_TXDESC_TAIL_POINTER) — Offset 11A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 1120h.

21.2.464 DMA_CH1_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH1_RXDESC_TAIL_POINTER) — Offset 11A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 1128h.

21.2.465 DMA_CH1_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH1_TXDESC_RING_LENGTH) — Offset 11ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 112Ch.

21.2.466 DMA_CH1_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH1_RXDESC_RING_LENGTH) — Offset 11B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 1130h.

21.2.467 DMA_CH1_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH1_INTERRUPT_ENABLE) — Offset 11B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 1134h.

21.2.468 DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH1_RX_INTERRUPT_WATCHDOG_TIMER) — Offset 11B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 1138h.

21.2.469 DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH1_SLOT_FUNCTION_CONTROL_STATUS) — Offset 11BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 113Ch.

21.2.470 DMA_CH1_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_TXDESC) — Offset 11C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 1144h.

21.2.471 DMA_CH1_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_RXDESC) — Offset 11CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 114Ch.

21.2.472 DMA_CH1_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_TXBUFFER_H) — Offset 11D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 1150h.

21.2.473 DMA_CH1_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_TXBUFFER) — Offset 11D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 1154h.

21.2.474 DMA_CH1_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_RXBUFFER_H) — Offset 11D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 1158h.

21.2.475 DMA_CH1_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH1_CURRENT_APP_RXBUFFER) — Offset 11DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 115Ch.

21.2.476 DMA_CH1_STATUS DWC_ETHER_QOS (DMA_CH1_STATUS) — Offset 11E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH[n]_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 1160h.

21.2.477 DMA_CH1_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH1_MISS_FRAME_CNT) — Offset 11E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 1164h.

21.2.478 DMA_CH1_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH1_RX_ERI_CNT) — Offset 11ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 116Ch.

21.2.479 DMA_CH2_CONTROL DWC_ETHER_QOS (DMA_CH2_CONTROL) — Offset 1200h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 1100h.

21.2.480 DMA_CH2_TX_CONTROL DWC_ETHER_QOS (DMA_CH2_TX_CONTROL) — Offset 1204h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 1104h.

21.2.481 DMA_CH2_RX_CONTROL DWC_ETHER_QOS (DMA_CH2_RX_CONTROL) — Offset 1208h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 1108h.

21.2.482 DMA_CH2_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH2_TXDESC_LIST_HADDRESS) — Offset 1210h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 1110h.

21.2.483 DMA_CH2_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH2_TXDESC_LIST_ADDRESS) — Offset 1214h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 1114h.

21.2.484 DMA_CH2_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH2_RXDESC_LIST_HADDRESS) — Offset 1218h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 1118h.

21.2.485 DMA_CH2_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH2_RXDESC_LIST_ADDRESS) — Offset 121Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 111Ch.

21.2.486 DMA_CH2_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH2_TXDESC_TAIL_POINTER) — Offset 1220h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 1120h.

21.2.487 DMA_CH2_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH2_RXDESC_TAIL_POINTER) — Offset 1228h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 1128h.

21.2.488 DMA_CH2_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH2_TXDESC_RING_LENGTH) — Offset 122Ch

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 112Ch.

21.2.489 DMA_CH2_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH2_RXDESC_RING_LENGTH) — Offset 1230h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 1130h.

21.2.490 DMA_CH2_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH2_INTERRUPT_ENABLE) — Offset 1234h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 1134h.

21.2.491 DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH2_RX_INTERRUPT_WATCHDOG_TIMER) — Offset 1238h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 1138h.

21.2.492 DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH2_SLOT_FUNCTION_CONTROL_STATUS) — Offset 123Ch

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 113Ch.

21.2.493 DMA_CH2_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_TXDESC) — Offset 1244h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 1144h.

21.2.494 DMA_CH2_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_RXDESC) — Offset 124Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 114Ch.

21.2.495 DMA_CH2_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_TXBUFFER_H) — Offset 1250h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 1150h.

21.2.496 DMA_CH2_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_TXBUFFER) — Offset 1254h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 1154h.

21.2.497 DMA_CH2_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_RXBUFFER_H) — Offset 1258h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 1158h.

21.2.498 DMA_CH2_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH2_CURRENT_APP_RXBUFFER) — Offset 125Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 115Ch.

21.2.499 DMA_CH2_STATUS DWC_ETHER_QOS (DMA_CH2_STATUS) — Offset 1260h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH[n]_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 1160h.

21.2.500 DMA_CH2_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH2_MISS_FRAME_CNT) — Offset 1264h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 1164h.

21.2.501 DMA_CH2_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH2_RX_ERI_CNT) — Offset 126Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 116Ch.

21.2.502 DMA_CH3_CONTROL DWC_ETHER_QOS (DMA_CH3_CONTROL) — Offset 1280h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH0_CONTROL, offset 1100h.

21.2.503 DMA_CH3_TX_CONTROL DWC_ETHER_QOS (DMA_CH3_TX_CONTROL) — Offset 1284h

The DMA Channeli Transmit Control register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights.

Note: Bit definitions are the same as DMA_CH0_TX_CONTROL, offset 1104h.

21.2.504 DMA_CH3_RX_CONTROL DWC_ETHER_QOS (DMA_CH3_RX_CONTROL) — Offset 1288h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 1108h.

21.2.505 DMA_CH3_TXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH3_TXDESC_LIST_HADDRESS) — Offset 1290h

The Channeli Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CHi_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier. This register must be programmed with desired the higher address before programming the DMA_CHi_TxDesc_List_Address register.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_HADDRESS, offset 1110h.

21.2.506 DMA_CH3_TXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH3_TXDESC_LIST_ADDRESS) — Offset 1294h

The Channeli Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LSB to low. You can write to this register only when the Tx DMA has stopped, that is, the ST bit is set to zero in DMA_CH0_Tx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the ST bit to 1, the DMA takes the newly-programmed descriptor base address. If this register is not changed when the ST bit is set to 0, the DMA takes the descriptor address where it was stopped earlier.

Note: Bit definitions are the same as DMA_CH0_TXDESC_LIST_ADDRESS, offset 1114h.

21.2.507 DMA_CH3_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH3_RXDESC_LIST_HADDRESS) — Offset 1298h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 1118h.

21.2.508 DMA_CH3_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH3_RXDESC_LIST_ADDRESS) — Offset 129Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 111Ch.

21.2.509 DMA_CH3_TXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH3_TXDESC_TAIL_POINTER) — Offset 12A0h

The Channeli Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_TXDESC_TAIL_POINTER, offset 1120h.

21.2.510 DMA_CH3_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH3_RXDESC_TAIL_POINTER) — Offset 12A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 1128h.

21.2.511 DMA_CH3_TXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH3_TXDESC_RING_LENGTH) — Offset 12ACh

The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring.

Note: Bit definitions are the same as DMA_CH0_TXDESC_RING_LENGTH, offset 112Ch.

21.2.512 DMA_CH3_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH3_RXDESC_RING_LENGTH) — Offset 12B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 1130h.

21.2.513 DMA_CH3_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH3_INTERRUPT_ENABLE) — Offset 12B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH0_INTERRUPT_ENABLE, offset 1134h.

21.2.514 DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH3_RX_INTERRUPT_WATCHDOG_TIMER) — Offset 12B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 1138h.

21.2.515 DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS DWC_ETHER_QOS (DMA_CH3_SLOT_FUNCTION_CONTROL_STATUS) — Offset 12BCh

The Slot Function Control and Status register contains the control bits for slot function and the status for Transmit path.

Note: Bit definitions are the same as DMA_CH0_SLOT_FUNCTION_CONTROL_STATUS, offset 113Ch.

21.2.516 DMA_CH3_CURRENT_APP_TXDESC DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_TXDESC) — Offset 12C4h

The Channeli Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXDESC, offset 1144h.

21.2.517 DMA_CH3_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_RXDESC) — Offset 12CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 114Ch.

21.2.518 DMA_CH3_CURRENT_APP_TXBUFFER_H DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_TXBUFFER_H) — Offset 12D0h

The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER_H, offset 1150h.

21.2.519 DMA_CH3_CURRENT_APP_TXBUFFER DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_TXBUFFER) — Offset 12D4h

The Channeli Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_TXBUFFER, offset 1154h.

21.2.520 DMA_CH3_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_RXBUFFER_H) — Offset 12D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 1158h.

21.2.521 DMA_CH3_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH3_CURRENT_APP_RXBUFFER) — Offset 12DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 115Ch.

21.2.522 DMA_CH3_STATUS DWC_ETHER_QOS (DMA_CH3_STATUS) — Offset 12E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH[n]_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 1160h.

21.2.523 DMA_CH3_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH3_MISS_FRAME_CNT) — Offset 12E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 1164h.

21.2.524 DMA_CH3_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH3_RX_ERI_CNT) — Offset 12ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 116Ch.

21.2.525 DMA_CH4_CONTROL DWC_ETHER_QOS (DMA_CH4_CONTROL) — Offset 1300h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1300h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RO	**Reserved** Platform firmware & software shall not set this field to 0x1
23:21	0h RO	**Reserved**
20:18	0h RW	**DSL DWC_ETHER_QOS (DSL):** Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	0h RO	**Reserved**
16	0h RW	**PBLX8 DWC_ETHER_QOS (PBLX8):** 8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.
15:0	0h RO	**Reserved**

21.2.526 DMA_CH4_RX_CONTROL DWC_ETHER_QOS (DMA_CH4_RX_CONTROL) — Offset 1308h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 1108h.

21.2.527 DMA_CH4_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH4_RXDESC_LIST_HADDRESS) — Offset 1318h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 1118h.

21.2.528 DMA_CH4_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH4_RXDESC_LIST_ADDRESS) — Offset 131Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 111Ch.

21.2.529 DMA_CH4_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH4_RXDESC_TAIL_POINTER) — Offset 1328h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 1128h.

21.2.530 DMA_CH4_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH4_RXDESC_RING_LENGTH) — Offset 1330h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 1130h.

21.2.531 DMA_CH4_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH4_INTERRUPT_ENABLE) — Offset 1334h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Type	Size	Offset	Default
MMIO	32 bit	BAR + 1334h	00000000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	0h RW	**NIE DWC_ETHER_QOS (NIE):** Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 0: Transmit Interrupt - Bit 2: Transmit Buffer Unavailable - Bit 6: Receive Interrupt - Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled.
14	0h RW	**AIE DWC_ETHER_QOS (AIE):** Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: - Bit 1: Transmit Process Stopped - Bit 7: Rx Buffer Unavailable - Bit 8: Receive Process Stopped - Bit 9: Receive Watchdog Timeout - Bit 10: Early Transmit Interrupt - Bit 12: Fatal Bus Error - Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled.
13	0h RW	**CDEE DWC_ETHER_QOS (CDEE):** Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled.
12	0h RW	**FBEE DWC_ETHER_QOS (FBEE):** Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled.
11	0h RW	**ERIE DWC_ETHER_QOS (ERIE):** Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled.
10	0h RO	**Reserved**
9	0h RW	**RWTE DWC_ETHER_QOS (RWTE):** Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled.
8	0h RW	**RSE DWC_ETHER_QOS (RSE):** Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.
7	0h RW	**RBUE DWC_ETHER_QOS (RBUE):** Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled.
6	0h RW	**RIE DWC_ETHER_QOS (RIE):** Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.
5:0	0h RO	**Reserved**

21.2.532 DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH4_RX_INTERRUPT_WATCHDOG_TIMER) — Offset 1338h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 1138h.

21.2.533 DMA_CH4_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH4_CURRENT_APP_RXDESC) — Offset 134Ch

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 114Ch.

21.2.534 DMA_CH4_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH4_CURRENT_APP_RXBUFFER_H) — Offset 1358h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 1158h.

21.2.535 DMA_CH4_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH4_CURRENT_APP_RXBUFFER) — Offset 135Ch

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 115Ch.

21.2.536 DMA_CH4_STATUS DWC_ETHER_QOS (DMA_CH4_STATUS) — Offset 1360h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH[n]_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 1160h.

21.2.537 DMA_CH4_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH4_MISS_FRAME_CNT) — Offset 1364h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 1164h.

21.2.538 DMA_CH4_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH4_RX_ERI_CNT) — Offset 136Ch

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 116Ch.

21.2.539 DMA_CH5_CONTROL DWC_ETHER_QOS (DMA_CH5_CONTROL) — Offset 1380h

The DMA Channeli Control register specifies the MSS value for segmentation, length to skip between two descriptors, and also the features such as header splitting and 8xPBL mode.

Note: Bit definitions are the same as DMA_CH4_CONTROL, offset 1300h.

21.2.540 DMA_CH5_RX_CONTROL DWC_ETHER_QOS (DMA_CH5_RX_CONTROL) — Offset 1388h

The DMA Channeli Receive Control register controls the Rx features such as PBL, buffer size, and extended status.

Note: Bit definitions are the same as DMA_CH0_RX_CONTROL, offset 1108h.

21.2.541 DMA_CH5_RXDESC_LIST_HADDRESS DWC_ETHER_QOS (DMA_CH5_RXDESC_LIST_HADDRESS) — Offset 1398h

The Channeli Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in the DMA_CHi_RxDesc_List_Address register When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_HADDRESS, offset 1118h.

21.2.542 DMA_CH5_RXDESC_LIST_ADDRESS DWC_ETHER_QOS (DMA_CH5_RXDESC_LIST_ADDRESS) — Offset 139Ch

The Channeli Rx Descriptor List Address register points the DMA to the start of Receive descriptor list. This register points to the start of the Receive Descriptor List. The descriptor lists reside in the physical memory space of the application and must be Word, Dword, or Lword-aligned (for 32-bit, 64-bit, or 128-bit data bus). The DMA internally converts it to bus width aligned address by making the corresponding LS bits low. Writing to this register is permitted only when reception is stopped. When stopped, this register must be written to before the receive Start command is given. You can write to this register only when Rx DMA has stopped, that is, SR bit is set to zero in DMA_CH0_Rx_Control register. When stopped, this register can be written with a new descriptor list address. When you set the SR bit to 1, the DMA takes the newly programmed descriptor base address.

Note: Bit definitions are the same as DMA_CH0_RXDESC_LIST_ADDRESS, offset 111Ch.

21.2.543 DMA_CH5_RXDESC_TAIL_POINTER DWC_ETHER_QOS (DMA_CH5_RXDESC_TAIL_POINTER) — Offset 13A8h

The Channeli Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor.

Note: Bit definitions are the same as DMA_CH0_RXDESC_TAIL_POINTER, offset 1128h.

21.2.544 DMA_CH5_RXDESC_RING_LENGTH DWC_ETHER_QOS (DMA_CH5_RXDESC_RING_LENGTH) — Offset 13B0h

The Channeli Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring.

Note: Bit definitions are the same as DMA_CH0_RXDESC_RING_LENGTH, offset 1130h.

21.2.545 DMA_CH5_INTERRUPT_ENABLE DWC_ETHER_QOS (DMA_CH5_INTERRUPT_ENABLE) — Offset 13B4h

The Channeli Interrupt Enable register enables the interrupts reported by the Status register.

Note: Bit definitions are the same as DMA_CH4_INTERRUPT_ENABLE, offset 1334h.

21.2.546 DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER DWC_ETHER_QOS (DMA_CH5_RX_INTERRUPT_WATCHDOG_TIMER) — Offset 13B8h

The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA. When this register is written with a non-zero value, it enables the watchdog timer for the RI bit of the DMA_CHi_Status register.

Note: Bit definitions are the same as DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER, offset 1138h.

21.2.547 DMA_CH5_CURRENT_APP_RXDESC DWC_ETHER_QOS (DMA_CH5_CURRENT_APP_RXDESC) — Offset 13CCh

The Channeli Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXDESC, offset 114Ch.

21.2.548 DMA_CH5_CURRENT_APP_RXBUFFER_H DWC_ETHER_QOS (DMA_CH5_CURRENT_APP_RXBUFFER_H) — Offset 13D8h

The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER_H, offset 1158h.

21.2.549 DMA_CH5_CURRENT_APP_RXBUFFER DWC_ETHER_QOS (DMA_CH5_CURRENT_APP_RXBUFFER) — Offset 13DCh

The Channel 0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA.

Note: Bit definitions are the same as DMA_CH0_CURRENT_APP_RXBUFFER, offset 115Ch.

21.2.550 DMA_CH5_STATUS DWC_ETHER_QOS (DMA_CH5_STATUS) — Offset 13E0h

The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA. Note: The number of DMA_CH[n]_Status register in the configuration is the higher of number of Rx DMA Channels and Tx DMA Channels.

Note: Bit definitions are the same as DMA_CH0_STATUS, offset 1160h.

21.2.551 DMA_CH5_MISS_FRAME_CNT DWC_ETHER_QOS (DMA_CH5_MISS_FRAME_CNT) — Offset 13E4h

This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH${i}_Rx_Control register.

Note: Bit definitions are the same as DMA_CH0_MISS_FRAME_CNT, offset 1164h.

21.2.552 DMA_CH5_RX_ERI_CNT DWC_ETHER_QOS (DMA_CH5_RX_ERI_CNT) — Offset 13ECh

The DMA_CH(#i)_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted.

Note: Bit definitions are the same as DMA_CH0_RX_ERI_CNT, offset 116Ch.

21.3 PHY Sublayer Registers Accessible via the MDIO Interface Controller

Note: These registers are only applicable for the Intel Atom® x7000 processor series.

The Management Data Input/Output (MDIO) Interface is defined in IEEE Standard 802.3-2018:

Clause 22 – Chapter 22.2.4 of the IEEE standard specifies the MDIO interface and registers. The MAC device controlling the MDIO is called the Station Management (STA) entity. The STA issues MDIO frames that have the 2-bit, start-of-frame Symbol Time (ST) code of 01 to access registers. See Table below for the Clause 22 frame format and terminology.

Clause 45 – See Chapter 45 of the IEEE standard. This MDIO interface and register format are extensions to the two-signal MDIO Interface specified in Clause 22. For Clause 45, additional registers are added to the address space by defining MDIO frames that use a start-of-frame Symbol Time (ST) code of 00. See Table below for the Clause 45 frame format and terminology.

The TSN-GbE Controller supports both formats. The C45E bit (bit 1) of the MAC_MDIO_Address register at MMIO offset 200h can be programmed to select the Clause 22 or Clause 45 mode of operation of the STA for the particular MDIO frame. The C45E bit must be programmed to support the capability of the PHY that is connected to MDIO.

The PHY sublayer, or grouping of sublayers, is an individually manageable entity referred to as an MDIO Manageable Device (MMD).

Table 45. MDIO Clause 22 Management Frame Format

Operation	32-Bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	PHY Address (PHYAD)	PHY Register Address (REGAD)	2-Bit Turn-around (TA) Time	Data (16 Bits)	High-Z (Idle)
Write	1111... 1	01	01	AAAAA	RRRRR	10	16-Bit Data to be written to the register	z
Read	1111...1	01	10	AAAAA	RRRRR	Z0	16-Bit Data read from the register	z

For the Clause 22 frame, the PHY Address (PHYAD) selects one of 32 PHYs attached to the MDIO interface. The PHY Register Address (REGAD) selects one of 32 16-bit registers within each MMD.

Table 46. MDIO Clause 45 Management Frame Format

Operation	32-Bit Preamble (1's)	Start of Frame (ST)	Operation Code (OP)	Port Address (PRTAD)	Device Address (DEVAD)	2-Bit Turn-around (TA) Time	Address /Data (16 Bits)	High-Z (Idle)
Address	1111...1	00	00	ppppp	EEEEE	Z0	16-Bit Address of the register to be accessed on the next cycle	z
Write	1111... 1	00	01	ppppp	EEEEE	Z0	16-Bit Data to be written to the register	z
Post-Read-Increment Address	1111...1	00	10	ppppp	EEEEE	Z0	16-Bit Data read from the register	z
Read	1111...1	00	11	ppppp	EEEEE	Z0	16-Bit Data read from the register	z

For the Clause 45 frame, the Port Address (PRTAD) selects one of 32 Ports attached to the MDIO interface. The Device Address (DEVAD) selects one of 32 unique MDDs per Port. Notice that the register address and register data are separate MDIO frames.

21.3.1 MDIO - PCS PHY Sublayer Registers - PHY Port Address 16h

The MAC uses the GMII as the data interface to the PHY sublayers of the Ethernet LAN Controller including the Physical Coding Sublayer (PCS). The MAC uses the MDIO as the configuration and management interface to the PHY sublayers. This section describes the PCS MDIO registers which follow the IEEE 802.3 standard register sets for the different MMIO Management Devices (MMD).

The PCS PHY sublayer is an IEEE Std 802.3 Clause-45-capable MDIO entity with the following IEEE 802.3 MDIO frame fields:

- Start-of-Frame Symbol Time (ST) 2-bit code: 00b – Indicates a Clause 45 MDIO frame.
- Port Address (PRTAD) 5-bit ID: 10110b (16h) – This Port contains two MMDs:
    - MMD (DEVAD) 5-bit ID: 11110b (1Eh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h though 000Fh. This MMD is named Vendor-Specific 1 (Control MMD). The registers are used to control the other MMDs of the LAN Controller.
    - MMD (DEVAD) 5-bit ID: 11111b (1Fh) – Vendor-Specific MMD with 65,535 addressable 16-bit registers. The valid register addresses range from 0000h though 0E2h. This MMD is named Vendor-Specific MII MMD (VR MII MMD).

Table 47. Summary of PCS MMIO Registers, PRTAD = 16h, DEVAD = 1Eh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1E0000 0000h	2	SR_VSMMD_PMA_ID1 DWC_XPCS (SR_VSMMD_PMA_ID1)	0000h
1E0000 0002h	2	SR_VSMMD_PMA_ID2 DWC_XPCS (SR_VSMMD_PMA_ID2)	0000h
1E0000 0004h	2	SR_VSMMD_DEV_ID1 DWC_XPCS (SR_VSMMD_DEV_ID1)	0000h
1E0000 0006h	2	SR_VSMMD_DEV_ID2 DWC_XPCS (SR_VSMMD_DEV_ID2)	0000h
1E0000 0008h	2	SR_VSMMD_PCS_ID1 DWC_XPCS (SR_VSMMD_PCS_ID1)	0000h
1E0000 000Ah	2	SR_VSMMD_PCS_ID2 DWC_XPCS (SR_VSMMD_PCS_ID2)	0000h
1E0000 000Ch	2	SR_VSMMD_AN_ID1 DWC_XPCS (SR_VSMMD_AN_ID1)	0000h
1E0000 000Eh	2	SR_VSMMD_AN_ID2 DWC_XPCS (SR_VSMMD_AN_ID2)	0000h
1E0000 0010h	2	SR_VSMMD_STS DWC_XPCS (SR_VSMMD_STS)	0000h
1E0000 0012h	2	SR_VSMMD_CTRL DWC_XPCS (SR_VSMMD_CTRL)	0000h
1E0000 001Ch	2	SR_VSMMD_PKGID1 DWC_XPCS (SR_VSMMD_PKGID1)	0000h
1E0000 001Eh	2	SR_VSMMD_PKGID2 DWC_XPCS (SR_VSMMD_PKGID2)	0000h

21.3.1.1 SR_VSMMD_PMA_ID1 DWC_XPCS (SR_VSMMD_PMA_ID1) — Offset 1E00000000h

SR Control MMD PMA Device Identifier Register 1

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1E00000000h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Reserved**

21.3.1.2 SR_VSMMD_PMA_ID2 DWC_XPCS (SR_VSMMD_PMA_ID2) — Offset 1E00000002h

SR Control MMD PMA Device Identifier Register 2

Note: Bit definitions are the same as SR_VSMMD_PMA_ID1, offset 1E00000000h.

21.3.1.3 SR_VSMMD_DEV_ID1 DWC_XPCS (SR_VSMMD_DEV_ID1) — Offset 1E00000004h

SR Control MMD Device Identifier Register 1

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1E00000004h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**VSDOUI_3_18 DWC_XPCS (VSDOUI_3_18):** Organizationally Unique Identifier[3:18] for Vendor-Specific MMD1 This field contains Bits[18:3] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer.

21.3.1.4 SR_VSMMD_DEV_ID2 DWC_XPCS (SR_VSMMD_DEV_ID2) — Offset 1E00000006h

SR Control MMD Device Identifier Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1E00000006h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RW	**VSDOUI_19_24 DWC_XPCS (VSDOUI_19_24):** Organizationally Unique Identifier[19:24] for Vendor-Specific MMD1 This field contains Bits[24:19] of the device manufacturer's 24- bit OUI. The DWC_xpcs offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer.
9:4	00h RW	**VSDMMN_5_0 DWC_XPCS (VSDMMN_5_0):** Model Number for Vendor-Specific MMD1 This field contains the 6-bit Model number of the vendor-specific MMD1.
3:0	0h RW	**VSDRN_3_0 DWC_XPCS (VSDRN_3_0):** Revision Number for Vendor-Specific MMD1 This field contains the 4-bit Revision number of the vendor-specific MMD1.

21.3.1.5 SR_VSMMD_PCS_ID1 DWC_XPCS (SR_VSMMD_PCS_ID1) — Offset 1E00000008h

SR Control MMD PCS Device Identifier Register 1

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1E00000008h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**PCSDOUI_3_18 DWC_XPCS (PCSDOUI_3_18):** Organizationally Unique Identifier[3:18] for PCS MMD This field contains Bits[18:3] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. The default value of this register is similar to the default value of SR XS or PCS MMD Device Identifier Register 1. The value written in this register is reflected in SR XS or PCS MMD Device Identifier Register 1. Access Type: - RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. - RO: For all other configurations.

21.3.1.6 SR_VSMMD_PCS_ID2 DWC_XPCS (SR_VSMMD_PCS_ID2) — Offset 1E0000000Ah

SR Control MMD PCS Device Identifier Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1E0000000Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RW	**PCSDOUI_19_24 DWC_XPCS (PCSDOUI_19_24):** Organizationally Unique Identifier[19:24] for PCS MMD This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable bits [24:1], known as OUI, for identifying the device manufacturer. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2. Access Type: - RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled. - RO: For all other configurations.
9:4	00h RW	**PCSDMMN_5_0 DWC_XPCS (PCSDMMN_5_0):** Model Number for XS or PCS MMD This field contains the 6-bit Model number of vendor-specific XS or PCS MMD. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2. Access Type: - RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled - RO: For all other configurations

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RW	**PCSDRN_3_0 DWC_XPCS (PCSDRN_3_0):** Revision Number for XS or PCS MMD This field contains the 4-bit Revision number of vendor-specific XS or PCS MMD. The default value of this field is similar to the default value of the corresponding field in SR XS or PCS MMD Device Identifier Register 2. The value written in this field is reflected in the corresponding field of SR XS or PCS MMD Device Identifier Register 2. Access Type: - RW: For configurations with IEEE_REG_WR_SUPPORT = Enabled - RO: For all other configurations

21.3.1.7 SR_VSMMD_AN_ID1 DWC_XPCS (SR_VSMMD_AN_ID1) — Offset 1E0000000Ch

SR Control MMD AN Device Identifier Register 1

Note: Bit definitions are the same as SR_VSMMD_PMA_ID1, offset 1E00000000h.

21.3.1.8 SR_VSMMD_AN_ID2 DWC_XPCS (SR_VSMMD_AN_ID2) — Offset 1E0000000Eh

SR Control MMD AN Device Identifier Register 2

Note: Bit definitions are the same as SR_VSMMD_PMA_ID1, offset 1E00000000h.

21.3.1.9 SR_VSMMD_STS DWC_XPCS (SR_VSMMD_STS) — Offset 1E00000010h

SR Control MMD Status Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1E00000010h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO/V	**VSDP DWC_XPCS (VSDP):** Control MMD Device Present This field indicates if the control MMD device is present and responding to this address: - 10: Device responding at this address - 11, 01, or 00: No device responding at this address
13:0	0h RO	**Reserved**

21.3.1.10 SR_VSMMD_CTRL DWC_XPCS (SR_VSMMD_CTRL) — Offset 1E00000012h

SR Control MMD Control Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1E00000012h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RW	**PD_CTRL DWC_XPCS (PD_CTRL):** Power Down Control This bit is used to control the output port 'xpcs_pdown_o'. If this bit is set, xpcs_pdown_o port will NOT be asserted when LPM (Low Power Enable) bit is programmed to 1. If this bit is low, xpcs_down_o port will be asserted when LPM (Low Power Enable) bit is programmed to 1.
4	0h RW	**FASTSIM DWC_XPCS (FASTSIM):** Fast Simulation Enable When set, this bit indicates that the Fast simulation is enabled. When this bit is set to 1, all IEEE Std 802.3 defined long timers, implemented in the DWC_xpcs are reduced to shorter time period to reduce the simulation time. The long timers are implemented in Clause 73 and Clause 37 auto-negotiation modules and also EEE Tx and Rx modules.
3	0h RO	**Reserved**
2	0h RW	**MII_MMD_EN DWC_XPCS (MII_MMD_EN):** VS MMD Enable When set, this bit indicates that the vendor-specific MMD1 device is accessible. When reset, this bit indicates that the vendor-specific MMD2 (MII MMD) device is not accessible. Default Value: If CL37_AN = Enabled, this bit returns 1. Otherwise, this bit returns 0. Access Type: If CL37_AN = Enabled, this bit is RW. Otherwise, this bit is RO.
1:0	0h RO	**Reserved**

21.3.1.11 SR_VSMMD_PKGID1 DWC_XPCS (SR_VSMMD_PKGID1) — Offset 1E0000001Ch

SR Control MMD Package Identifier Register 1

Note: Bit definitions are the same as SR_VSMMD_PMA_ID1, offset 1E00000000h.

21.3.1.12 SR_VSMMD_PKGID2 DWC_XPCS (SR_VSMMD_PKGID2) — Offset 1E0000001Eh

SR Control MMD Package Identifier Register 2 Note: The values written in the fields of this register are reflected in the corresponding fields of the following registers: - SR PMA MMD Package Identifier Register 2 - SR XS or PCS MMD Package Identifier Register 2 - SR AN MMD Package Identifier Register 2

Note: Bit definitions are the same as SR_VSMMD_PMA_ID1, offset 1E00000000h.

Table 48. Summary of PCS MMIO Registers, PRTAD = 16h, DEVAD = 1Fh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F0000 0000h	2	SR_MII_CTRL DWC_XPCS (SR_MII_CTRL)	0000h
1F0000 0002h	2	SR_MII_STS DWC_XPCS (SR_MII_STS)	0000h
1F0000 0004h	2	SR_MII_DEV_ID1 DWC_XPCS (SR_MII_DEV_ID1)	0000h
1F0000 0006h	2	SR_MII_DEV_ID2 DWC_XPCS (SR_MII_DEV_ID2)	0000h
1F0000 0008h	2	SR_MII_AN_ADV DWC_XPCS (SR_MII_AN_ADV)	0000h
1F0000 000Ah	2	SR_MII_LP_BABL DWC_XPCS (SR_MII_LP_BABL)	0000h
1F0000 000Ch	2	SR_MII_EXPN DWC_XPCS (SR_MII_EXPN)	0000h
1F0000 001Eh	2	SR_MII_EXT_STS DWC_XPCS (SR_MII_EXT_STS)	0000h
1F0000 0E10h	2	SR_MII_TIME_SYNC_ABL DWC_XPCS (SR_MII_TIME_SYNC_ABL)	0000h
1F0000 0E12h	2	SR_MII_TIME_SYNC_TX_MAX_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR)	0000h
1F0000 0E14h	2	SR_MII_TIME_SYNC_TX_MAX_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR)	0000h
1F0000 0E16h	2	SR_MII_TIME_SYNC_TX_MIN_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR)	0000h
1F0000 0E18h	2	SR_MII_TIME_SYNC_TX_MIN_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR)	0000h
1F0000 0E1Ah	2	SR_MII_TIME_SYNC_RX_MAX_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR)	0000h
1F0000 0E1Ch	2	SR_MII_TIME_SYNC_RX_MAX_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR)	0000h
1F0000 0E1Eh	2	SR_MII_TIME_SYNC_RX_MIN_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR)	0000h
1F0000 0E20h	2	SR_MII_TIME_SYNC_RX_MIN_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR)	0000h
1F0001 0000h	2	VR_MII_DIG_CTRL1 DWC_XPCS (VR_MII_DIG_CTRL1)	0000h
1F0001 0002h	2	VR_MII_AN_CTRL DWC_XPCS (VR_MII_AN_CTRL)	0000h
1F0001 0004h	2	VR_MII_AN_INTR_STS DWC_XPCS (VR_MII_AN_INTR_STS)	0000h
1F0001 0006h	2	VR_MII_TC DWC_XPCS (VR_MII_TC)	0000h
1F0001 000Ah	2	VR_MII_DBG_CTRL DWC_XPCS (VR_MII_DBG_CTRL)	0000h
1F0001 000Ch	2	VR_MII_EEE_MCTRL0 DWC_XPCS (VR_MII_EEE_MCTRL0)	0000h
1F0001 0010h	2	VR_MII_EEE_TXTIMER DWC_XPCS (VR_MII_EEE_TXTIMER)	0000h
1F0001 0012h	2	VR_MII_EEE_RXTIMER DWC_XPCS (VR_MII_EEE_RXTIMER)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1F0001 0014h	2	VR_MII_LINK_TIMER_CTRL DWC_XPCS (VR_MII_LINK_TIMER_CTRL)	0000h
1F0001 0016h	2	VR_MII_EEE_MCTRL1 DWC_XPCS (VR_MII_EEE_MCTRL1)	0000h
1F0001 0020h	2	VR_MII_DIG_STS DWC_XPCS (VR_MII_DIG_STS)	0000h
1F0001 0022h	2	VR_MII_ICG_ERRCNT1 DWC_XPCS (VR_MII_ICG_ERRCNT1)	0000h
1F0001 0030h	2	VR_MII_MISC_STS DWC_XPCS (VR_MII_MISC_STS)	0000h
1F0001 0040h	2	VR_MII_RX_LSTS DWC_XPCS (VR_MII_RX_LSTS)	0000h
1F0001 01C2h	2	VR_MII_DIG_CTRL2 DWC_XPCS (VR_MII_DIG_CTRL2)	0000h
1F0001 01C4h	2	VR_MII_DIG_ERRCNT_SEL DWC_XPCS (VR_MII_DIG_ERRCNT_SEL)	0000h

21.3.1.13 SR_MII_CTRL DWC_XPCS (SR_MII_CTRL) — Offset 1F00000000h

SR MII MMD Control Register The host can use this register to control (enable or disable) some of the features supported by the DWC_xpcs with 1G (1000BASE-X) or USXGMII support) and Clause 37 auto-negotiation support.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000000h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**RST DWC_XPCS (RST):** Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the software reset process in which all internal blocks are reset, except the Management Interface block. The registers are reset to their default values. When this bit is set, it also resets the PHY. This bit is self-cleared after the following: - 32 clk_csr_i clocks for the MCI interface - 1 MDC clock period for the MDIO interface.
14	0h RW	**LBE DWC_XPCS (LBE):** Loopback Enable When set, this bit loops the PHY Tx lanes back to the PHY Rx lanes. 0: The DWC_xpcs de-asserts xpcs_loopback_en_o signal. - 1: The DWC_xpcs asserts xpcs_loopback_en_o signal.
13	0h RW	**SS13 DWC_XPCS (SS13):** Speed Selection (LSB) This bit, along with the SS6 bit and SS5 bit of this register, indicates the speed. For USXGMII configurations: - When SS5=1, SS6=0 and SS13=1, speed is 5 Gbps - When SS5=1, SS6=0 and SS13=0, speed is 2.5 Gbps - When SS5=0, SS6=1 and SS13=1, speed is 10 Gbps - When SS5=0, SS6=1 and SS13=0, speed is 1000 Mbps - When SS5=0, SS6=0 and SS13=1, speed is 100 Mbps - When SS5=0, SS6=0 and SS13=0, speed is 10 Mbps For SGMII configurations: - When SS6=1 and SS13=0, speed is 1000 Mbps - When SS6=0 and SS13=1, speed is 100 Mbps - When SS6=0 and SS13=0, speed is 10 Mbps This bit is reserved when SGMII_EN = Disabled and QSGMII_EN=Disabled and USXGMII_EN = Disabled.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**AN_ENABLE DWC_XPCS (AN_ENABLE):** Enable Auto-Negotiation When set to 1, this bit enables the Clause 37 auto-negotiation process. Default Value: If MAIN_MODE = Backplane Ethernet PCS or if USXGMII_EN=Enabled, this bit returns 0. Otherwise, this bit returns 1.
11	0h RW	**LPM DWC_XPCS (LPM):** Power-Down Mode This bit controls the power-down mode of the DWC_xpcs. - 0: Normal operation - 1: The DWC_xpcs goes to the power-down mode along with the PHY; the xpcs_pdown_o port is asserted.
10	0h RO	**Reserved**
9	0h RW	**RESTART_AN DWC_XPCS (RESTART_AN):** Restart Auto-Negotiation (RW,SC Type) When the host writes this bit, the DWC_xpcs initiates the auto-negotiation process. This bit is used to restart the auto-negotiation which is already initiated by setting Bit 12. The DWC_xpcs clears this bit after restarting the autonegotiation.
8	0h RW	**DUPLEX_MODE DWC_XPCS (DUPLEX_MODE):** Duplex Mode This bit specifies the duplex mode of the DWC_xpcs. - 0: Half duplex - 1: Full duplex If Bit 12 is set to 0, this bit determines the PHY link duplex mode. If Bit 12 is set to 1, then the PHY link duplex mode is independent of this bit (although the host can write any value) and is determined by the outcome of the Clause 37 auto-negotiation process. Note: USXGMII mode supports only FULL duplex mode, irrespective of the value programmed to this bit.
7	0h RO	**Reserved**
6	0h RW	**SS6 DWC_XPCS (SS6):** Speed Selection This bit, along with the SS13 bit (and SS5 bit, in case of USXGMII configuration) of this register indicates the speed. For more information, see description of the SS13 bit. This bit is reserved when SGMII_EN = Disabled and QSGMII_EN =Disabled and USXGMII_EN=Disabled.
5:0	0h RO	**Reserved**

21.3.1.14 SR_MII_STS DWC_XPCS (SR_MII_STS) — Offset 1F00000002h

SR MII MMD Status Register The host uses this register to know the features supported by the DWC_xpcs in the 1000BASE-X mode. Note:This register is present if the selected configuration has 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000002h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	**ABL100T4 DWC_XPCS (ABL100T4):** 100BASE-T4 Ability The DWC_xpcs always returns 0 because it does not support this functionality.

Bit Range	Default & Access	Field Name (ID): Description
14	0h RO/V	**FD100ABL DWC_XPCS (FD100ABL):** 100BASE-X Full-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
13	0h RO/V	**HD100ABL DWC_XPCS (HD100ABL):** 100BASE-X Half-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
12	0h RO/V	**FD10ABL DWC_XPCS (FD10ABL):** 10 Mbps Full-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
11	0h RO/V	**HD10ABL DWC_XPCS (HD10ABL):** 10 Mbps Half-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
10	0h RO/V	**FD100T DWC_XPCS (FD100T):** 100BASE-T2 Full-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
9	0h RO/V	**HD100T DWC_XPCS (HD100T):** 100BASE-T2 Half-Duplex Ability The DWC_xpcs always returns 0 because it does not support this functionality.
8	0h RO/V	**EXT_STS_ABL DWC_XPCS (EXT_STS_ABL):** Extended Status Information - 0: No Extended Status information is present at register address 16'h000F of this MMD device. - 1: Extended Status information is present at register address 16'h000F of this MMD device. DWC_xpcs returns this bit as 1.
7	0h RO/V	**UN_DIR_ABL DWC_XPCS (UN_DIR_ABL):** Unidirectional Ability - 1: The DWC_xpcs is able to transmit GMII irrespective of whether device has determined the valid link or not. - 0: The DWC_xpcs is able to transmit GMII only when the device has determined the valid link. The DWC_xpcs always returns this bit as 1.
6	0h RO/V	**MF_PRE_SUP DWC_XPCS (MF_PRE_SUP):** MF Preamble Suppression - 1: The DWC_xpcs accepts the MDIO frames with preamble suppressed. - 0: The DWC_xpcs does not accept the MDIO frames with preamble suppressed. This bit is always set to 0.
5	0h RO/V	**AN_CMPL DWC_XPCS (AN_CMPL):** Auto-negotiation Complete - 1: The AN process is complete - 0: The AN process is not complete When this bit is set to 1, the contents of the AN MMD Advertizement, AN MMD Link partner Ability, and AN MMD Expansion registers are valid. This bit returns 0 if AN_ENABLE is set to 0.
4	0h RO/V	**RF DWC_XPCS (RF):** Remote Fault (RO,LH Type) When set to 1, this bit indicates that the receive link of the link partner is down. This bit is set based on the auto-negotiated (1000BASE-X auto-negotiation) information from the link partner. - 1: The DWC_xpcs detected a remote fault. - 0: The DWC_xpcs did not detect a remote fault.
3	0h RO/V	**AN_ABL DWC_XPCS (AN_ABL):** Auto-negotiation Ability The DWC_xpcs always returns this bit as 1. - 1: The DWC_xpcs is able to perform auto-negotiation. - 0: The DWC_xpcs is not able to perform auto-negotiation.
2	0h RO/V	**LINK_STS DWC_XPCS (LINK_STS):** Link Status (RO,LL Type) When the DWC_xpcs sets this bit to 1, it indicates that the Rx link is up. If the link goes down, it is latched until the host perform the read operation to this register. - 1: Link Up - 0: Link Down
1	0h RO	**Reserved**
0	0h RO/V	**EXT_REG_CAP DWC_XPCS (EXT_REG_CAP):** Extended Register Capability - 1: Extended Register capability exists. This bit is always set to 1. - 0: Extended Register capability does not exist.

21.3.1.15 SR_MII_DEV_ID1 DWC_XPCS (SR_MII_DEV_ID1) — Offset 1F00000004h

SR MII MMD Device Identifier Register 1 This register returns the configurable Organizationally Unique Identifier (OUI) to the host.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000004h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**VS_MII_DEV_OUI_3_18 DWC_XPCS (VS_MII_DEV_OUI_3_18):** Organizationally Unique Identifier[3:18] This field contains Bits [18:3] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable Bits[24:1] for identifying the device manufacturer. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 1. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[15:0] of SR XS or PCS MMD Device Identifier Register 1 modifies the content of this register.

21.3.1.16 SR_MII_DEV_ID2 DWC_XPCS (SR_MII_DEV_ID2) — Offset 1F00000006h

SR MII MMD Device Identifier Register 2 This register returns the configurable Organizationally Unique Identifier (OUI), Model Number, and Revision Number of the device to the host.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000006h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:10	00h RO/V	**VS_MMD_DEV_OUI_19_24 DWC_XPCS (VS_MMD_DEV_OUI_19_24):** Organizationally Unique Identifier [19:24] This field contains Bits[24:19] of 24-bit OUI of device manufacturer. The DWC_xpcs offers 24 configurable Bits[24:1] for identifying the device manufacturer. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 2. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[15:10] of SR XS or PCS MMD Device Identifier Register 2 modifies the content of this register.
9:4	00h RO/V	**VS_MMD_DEV_MMN_5_0 DWC_XPCS (VS_MMD_DEV_MMN_5_0):** Model Number This field contains the 5-bit Model Number of the device. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 2. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[9:4] of SR XS or PCS MMD Device Identifier Register 2 modifies the content of this register.

Bit Range	Default & Access	Field Name (ID): Description
3:0	0h RO/V	**VS_MMD_DEV_RN_3_0 DWC_XPCS (VS_MMD_DEV_RN_3_0):** Revision Number This field contains the 4-bit Revision Number of the device. The default value of this register is similar to the value of SR XS or PCS MMD Device Identifier Register 2. If IEEE_REG_WR_SUPPORT = Enabled, writing to Bits[3:0] of SR XS or PCS MMD Device Identifier Register 2 modifies the content of this register.

21.3.1.17 SR_MII_AN_ADV DWC_XPCS (SR_MII_AN_ADV) — Offset 1F00000008h

SR MII MMD AN Advertisement Register The host uses this register to advertise the abilities and status of the local device to its link partner through Clause 37 auto-negotiation protocol. Note:This register is present only for configurations with 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000008h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	**NP DWC_XPCS (NP):** Next Page The DWC_xpcs always returns this bit as 0 because it does not support the Next Page feature.
14	0h RO	**Reserved**
13:12	0h RW	**RF DWC_XPCS (RF):** Remote Fault This field indicates the fault signaling of the local device to be communicated to the link partner. - 00: No Error - 01: Offline - 10: Link Failure - 11: Auto-negotiation Error
11:9	0h RO	**Reserved**
8:7	0h RW	**PAUSE DWC_XPCS (PAUSE):** Pause Ability This field indicates the Pause ability of the device: - 00: No Pause - 01: Asymmetric Pause towards the link partner - 10: Symmetric Pause - 11: Symmetric Pause and Asymmetric Pause towards the local device. Software can program suitable values based on the capability of the MAC.
6	0h RW	**HD DWC_XPCS (HD):** Half Duplex When this bit is set, it indicates that the device can operate in the half-duplex mode.
5	0h RW	**FD DWC_XPCS (FD):** Full Duplex When this bit is set, it indicates that the device can operate in the full-duplex mode.
4:0	0h RO	**Reserved**

21.3.1.18 SR_MII_LP_BABL DWC_XPCS (SR_MII_LP_BABL) — Offset 1F0000000Ah

SR MII MMD AN Link Partner Base Ability Register The host uses this page to know the link partner's ability when the base page is received through Clause 37 auto-negotiation. The content of this register is valid only for 1000BASE-X autonegotiation. It is not valid in SGMII auto-negotiation. Note:This register is present only for configurations with 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F0000000Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	**LP_NP DWC_XPCS (LP_NP):** Next Page This bit indicates that the link partner can handle Next Page. Note: To exchange information through Next Page, both devices (local and remote) should have the capability to handle Next Page. The DWC_xpcs does not support Next Page. Therefore, the Next Page exchange does not happen.
14	0h RO/V	**LP_ACK DWC_XPCS (LP_ACK):** ACK bit from the Link Partner This bit indicates that the link partner has successfully received the page sent by the local device.
13:12	0h RO/V	**LP_RF DWC_XPCS (LP_RF):** Remote Fault This field indicates the fault signaling of the link partner: - 00: No Error - 01: Offline - 10: Link Failure - 11: Auto-negotiation Error
11:9	0h RO	**Reserved**
8:7	0h RO/V	**LP_PAUSE DWC_XPCS (LP_PAUSE):** Pause Ability This field indicates the Pause ability of the link partner: - 00: No Pause - 01: Asymmetric Pause towards the link partner - 10: Symmetric Pause - 11: Both Symmetric Pause and Asymmetric Pause towards the local device
6	0h RO/V	**LP_HD DWC_XPCS (LP_HD):** Half Duplex When this bit is set, it indicates that the link partner is capable of operating in the half-duplex mode.
5	0h RO/V	**LP_FD DWC_XPCS (LP_FD):** Full Duplex When this bit is set, it indicates that the link partner is capable of operating in the full-duplex mode.
4:0	0h RO	**Reserved**

21.3.1.19 SR_MII_EXPN DWC_XPCS (SR_MII_EXPN) — Offset 1F0000000Ch

SR MII MMD AN Expansion Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F0000000Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2	0h RO/V	**LD_NP_ABL DWC_XPCS (LD_NP_ABL):** Local Device NP Able - 1: The local device has the next page ability - 0: The local device does not have the next page ability The DWC_xpcs always returns this bit as 0 because it does not support Next Page.
1	0h RO/V	**PG_RCVD DWC_XPCS (PG_RCVD):** Page Received (RO,LH Type) This bit indicates that the local device received a page from the link partner. - 1: The local device received a new page - 0: The local device did not receive a new page
0	0h RO	**Reserved**

21.3.1.20 SR_MII_EXT_STS DWC_XPCS (SR_MII_EXT_STS) — Offset 1F0000001Eh

SR MII MMD Extended Status Register This register is present only for configurations with 1G/KX support.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F0000001Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO/V	**CAP_1G_X_FD DWC_XPCS (CAP_1G_X_FD):** 1000BASE-X Full-Duplex Capable - 1: 1000BASE-X full-duplex capable - 0: Not 1000BASE-X full-duplex capable The DWC_xpcs always returns 1 because it supports this feature.
14	0h RO/V	**CAP_1G_X_HD DWC_XPCS (CAP_1G_X_HD):** 1000BASE-X Half-Duplex Capable - 1: 1000BASE-X half-duplex capable - 0: Not 1000BASE-X half-duplex capable The DWC_xpcs always returns 1 because it supports this feature.
13	0h RO/V	**CAP_1G_T_FD DWC_XPCS (CAP_1G_T_FD):** 1000BASE-T Full-Duplex Capable - 1: 1000BASE-T full-duplex capable - 0: Not 1000BASE-T full-duplex capable The DWC_xpcs always returns 0 because it does not support this feature.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RO/V	**CAP_1G_T_HD DWC_XPCS (CAP_1G_T_HD):** 1000BASE-T Half-Duplex Capable - 1: 1000BASE-T half-duplex capable - 0: Not 1000BASE-T half-duplex capable The DWC_xpcs always returns 0 because it does not support this feature.
11:0	0h RO	**Reserved**

21.3.1.21 SR_MII_TIME_SYNC_ABL DWC_XPCS (SR_MII_TIME_SYNC_ABL) — Offset 1F00000E10h

SR MII MMD Time Sync Capability Register. This register is present only in 1000BaseX-Only PCS configurations

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E10h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO/V	**MII_TX_DLY_ABL DWC_XPCS (MII_TX_DLY_ABL):** XPCS Transmit Path Data Delay Information Available. If this bit is set, it indicates that the information regarding the maximum and minimum transmit data delay of XPCS is available in MII MMD Tx Time Delay Registers
0	0h RO/V	**MII_RX_DLY_ABL DWC_XPCS (MII_RX_DLY_ABL):** XPCS Receive Path Data Delay Information Available. If this bit is set, it indicates that the information regarding the maximum and minimum receive data delay of XPCS is available in MII MMD Rx Time Delay Registers

21.3.1.22 SR_MII_TIME_SYNC_TX_MAX_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_TX_MAX_DLY_LWR) — Offset 1F00000E12h

SR MII MMD Time Sync Tx Max Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E12h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_TX_MAX_DLY_LWR DWC_XPCS (MII_TX_MAX_DLY_LWR):** This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path (in nano-seconds) of XPCS.

21.3.1.23 SR_MII_TIME_SYNC_TX_MAX_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_TX_MAX_DLY_UPR) — Offset 1F00000E14h

SR MII MMD Time Sync Tx Max Delay Upper Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E14h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_TX_MAX_DLY_UPR DWC_XPCS (MII_TX_MAX_DLY_UPR):** This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Transmit Path (in nano-seconds) of XPCS.

21.3.1.24 SR_MII_TIME_SYNC_TX_MIN_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_TX_MIN_DLY_LWR) — Offset 1F00000E16h

SR MII MMD Time Sync Tx Min Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E16h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_TX_MIN_DLY_LWR DWC_XPCS (MII_TX_MIN_DLY_LWR):** This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path (in nano-seconds) of XPCS.

21.3.1.25 SR_MII_TIME_SYNC_TX_MIN_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_TX_MIN_DLY_UPR) — Offset 1F00000E18h

SR MII MMD Time Sync Tx Min Delay Upper Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E18h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_TX_MIN_DLY_UPR DWC_XPCS (MII_TX_MIN_DLY_UPR):** This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Transmit Path (in nano-seconds) of XPCS.

21.3.1.26 SR_MII_TIME_SYNC_RX_MAX_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_RX_MAX_DLY_LWR) — Offset 1F00000E1Ah

SR MII MMD Time Sync Rx Max Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E1Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_RX_MAX_DLY_LWR DWC_XPCS (MII_RX_MAX_DLY_LWR):** This field indicates the lower 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path (in nano-seconds) of XPCS.

21.3.1.27 SR_MII_TIME_SYNC_RX_MAX_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_RX_MAX_DLY_UPR) — Offset 1F00000E1Ch

SR MII MMD Time Sync Rx Max Delay Upper Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E1Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_RX_MAX_DLY_UPR DWC_XPCS (MII_RX_MAX_DLY_UPR):** This field indicates the upper 16-bit of the 32-bit value which indicates the Maximum Data Delay in the Receive Path (in nano-seconds) of XPCS

21.3.1.28 SR_MII_TIME_SYNC_RX_MIN_DLY_LWR DWC_XPCS (SR_MII_TIME_SYNC_RX_MIN_DLY_LWR) — Offset 1F00000E1Eh

SR MII MMD Time Sync Rx Min Delay Lower Register. This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E1Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_RX_MIN_DLY_LWR DWC_XPCS (MII_RX_MIN_DLY_LWR):** This field indicates the lower 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path (in nano-seconds) of PCS.

21.3.1.29 SR_MII_TIME_SYNC_RX_MIN_DLY_UPR DWC_XPCS (SR_MII_TIME_SYNC_RX_MIN_DLY_UPR) — Offset 1F00000E20h

SR MII MMD Time Sync Rx Min Delay Upper Register This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00000E20h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MII_RX_MIN_DLY_UPR DWC_XPCS (MII_RX_MIN_DLY_UPR):** This field indicates the upper 16-bit of the 32-bit value which indicates the Minimum Data Delay in the Receive Path (in nano-seconds) of PCS

21.3.1.30 VR_MII_DIG_CTRL1 DWC_XPCS (VR_MII_DIG_CTRL1) — Offset 1F00010000h

VR MII MMD Digital Control1 Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010000h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**VR_RST DWC_XPCS (VR_RST):** Vendor-Specific Soft Reset (RW,SC Type) When the host sets this bit, the CSR block triggers the vendor-specific software reset process in which all internal blocks, except the Management Interface block and CSR block, are reset. When this bit is set, it also resets the PHY. This bit is self cleared under the following conditions: This bit is self cleared after the following: - 32 clk_csr_i clocks for the MCI interface - 1 MDC clock period for the MDIO interface.
14	0h RW	**R2TLBE DWC_XPCS (R2TLBE):** Rx to Tx Loopback Enable This bit controls the loopback path from the GMII Rx to the GMII Tx at the GMII interface. * 0: Loopback path is disabled * 1: Loopback path is enabled Access Type: * In 1000BaseX-Only PCS configuration: RW * In configurations with CL37_AN=Enabled and MAIN_MODE!=1000BaseX-Only PCS, this bit is RO. But it reflects the value programmed to R2TLBE bit of VR XS or PCS MMD Digital Control 1 Register, as it is a shared bit.
13	0h RW	**EN_VSMMD1 DWC_XPCS (EN_VSMMD1):** Enable Vendor-Specific MMD1 When this bit is set to 1, the vendor-specific MMD1 (VSMMD1) is enabled. When this bit is set to zero, VSMMD1 is disabled. Access Type: * In 1000BaseX-Only PCS configuration: RW * In configurations with CL37_AN=Enabled and MAIN_MODE!=1000BaseX-Only PCS, this bit is RO. But it reflects the value programmed to R2TLBE bit of VR XS or PCS MMD Digital Control 1 Register, as it is a shared bit.
12	0h RO/V	**CL37_BP DWC_XPCS (CL37_BP):** Enable Clause 37 AN in Backplane Configuration This bit is present when MAIN_MODE = Backplane Ethernet PCS and CL37_AN = Enabled. This is a read-only bit and it reflects the value programmed to CL37_BP bit of VR PCS MMD Digital Control 1 Register.
11	0h RO	**Reserved**
10	0h RW	**CS_EN DWC_XPCS (CS_EN):** Clock Stop Enable - 1: The PHY may stop the clock during LPI mode - 0: The clock cannot be stopped during LPI mode You should program this bit based on the capability of the MAC during Rx LPI mode. Access Type: - For configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled, this bit is RW. - For all other configurations, this bit is reserved and RO. Default Value: - 1'b1: For configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled - 1'b0: For all other configurations

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**MAC_AUTO_SW DWC_XPCS (MAC_AUTO_SW):** Automatic Speed Mode Change after CL37 AN When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXGMII_EN=Enabled: It this field is set to 1, DWC_xpcs automatically switches to the negotiated SGMII/USXGMII/QSGMII(port0) speed, after the completion of Clause 37 auto-negotiation. This mode is valid only when DWC_xpcs is configured as MAC-side SGMII/USXGMII/QSGMII and should be set only when Auto-negotiation is enabled (AN_ENABLE bit is set to 1). If this bit is set to 0, DWC_xpcs will operate at the speed/duplex mode as per the values programmed to SR MII MMD Control Register. In that case, after the completion of CL37 AN, application has to read the negotiated Speed/Duplex Mode from VR MII MMD AN Interrupt and Status Register and then program SR MII MMD Control Register appropriately. If this bit is set to 1 in SGMII mode, xpcs_sgmii_link_sts_o, xpcs_link_speed_o and xpcs_sgmii_full_duplex_o outputs will reflect the auto-negotiated values i.e., values from CL37_ANSGM_STS field of VR MII MMD AN Interrupt and Status Register. For USXGMII mode, if clk_xgmii_tx_i and clk_xgmii_rx_i do not stabilize at the new operating frequency (based on the selected speed) immediately after the completion of auto-negotiation, then software might need to program 'USRA_RST' bit prior to starting packet transfer in the new speed mode. Note: This bit should be set only when XPCS is configured as SGMII/USXGMII/QSGMII MAC i.e., TX_CONFIG=0 For other configurations: This is a read-only reserved field and returns 0.
8	0h RW	**INIT DWC_XPCS (INIT):** Datapath Initialization Control This bit can be set to flush/initialize the various FIFOs implemented inside DWC_xpcs. This is Self-Clear bit. After writing 1 to this bit, soft-ware should poll this bit continuously.Software should proceed to any other operation, only after reading this bit as 0. When this bit is programmed to 1, RXFIFO_OVF/ RXFIFO_UNF bits of VR MII MMD Digital Status Register might get set incorrectly. Hence,read these register bits (RXFIFO_OVF and RXFIFO_UNF) so that they get cleared. Thereafter, RXFIOF_UNF and RXFIFO_UNF bits would be reliable
7	0h RO/V	**MSK_RD_ERR DWC_XPCS (MSK_RD_ERR):** Mask Running Disparity Error. In QSGMII mode of operation, an error in data received from a particular port of a far-end device can result in unprecedent running disparity errors for other ports (even if data is received correctly). In order to resolve this issue, XPCS provides an option to mask the running disparity errors. If this register bit is set, then running disparity errors are ignored by XPCS receiver in evaluating the validity of received code-groups.
6	0h RW	**PRE_EMP DWC_XPCS (PRE_EMP):** Pre-emption Packet Enable. This bit should be set to 1 to allow the DWC_xpcs to properly receive/transmit pre-emption packets in SGMII 10M/100M Modes.
5	0h RO	**Reserved**
4	0h RW	**DTXLANED_0 DWC_XPCS (DTXLANED_0):** Tx Lane 0 Disable When this bit is set, the DWC_xpcs disables the Tx Lane 0 of the PHY. When reset, the DWC_xpcs enables the Tx Lane 0 of the PHY. This bit is Read-Write only when MAIN_MODE= 1000BASEX-Only PCS. Notes: This bit is shared with the following bits: - Bit 4 of VR XS or PCS MMD Digital Control1 Register and VR MII MMD Digital Control1 Register - Bit 1 of SR PMA MMD Transmit Disable Register - Bit 0 of SR PMA or PMD KX Control Register
3	0h RW	**CL37_TMR_OVR_RIDE DWC_XPCS (CL37_TMR_OVR_RIDE):** Over-Ride Control for CL37 Link Timer. This bit can be set to over-ride the default value of Clause 37 link_timer used by DWC_xpcs for auto-negotiation. If this bit is set, the value programmed to VR MII MMD Link Timer Control Register will be used to compute the duration of Link Timer. This bit should be set, only after programming the appropriate value to VR MII MMD Link Timer Control Register.
2	0h RW	**EN_2_5G_MODE DWC_XPCS (EN_2_5G_MODE):** Enable 2.5G GMII Mode. This bit should be set to 1 to enable 2.5G GMII Mode of operation.This bit drives the output port 'xpcs_2pt5g_mode_o'. This bit is shared with bit[2] of VR XS or PCS MMD Digital Control 1 Register.
1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**SGMII_PHY_MODE_CTRL DWC_XPCS (SGMII_PHY_MODE_CTRL):** When SGMII_PHY_AN_AUTO_RESTART=Enabled or QSGMII_PHY_AN_AUTO_RESTART=Enabled: PHY mode control This bit controls the CL37_AN when operating in SGMII/QSGMII (Port 0) PHY mode. When this bit is set to 1, DWC_xpcs advertises the values of input ports xpcs_sgmii_link_sts_i, xpcs_sgmii_link_speed_i and xpcs_sgmii_full_duplex_i during SGMII/(Port0)QSGMII autonegotiation. When this bit is set to 0, SGMII/QSGMII(Port0) autonegotiation will advertise the values programmed to: - bit 4 (SGMII_LINK_STS) of VR MII MMD AN Control Register - bit 13 (ss13) and 6 (ss6) of SR MII MMD Control Register and - bit 5 (FD) of SR MII MMD AN Advertisement Register Note: This bit should be set only when XPCS is configured as SGMII/QSGMII PHY i.e., TX_CONFIG=1 In other configurations, this field is reserved and read-only.

21.3.1.31 VR_MII_AN_CTRL DWC_XPCS (VR_MII_AN_CTRL) — Offset 1F00010002h

VR MII MMD AN Control Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010002h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RW	**MII_CTRL DWC_XPCS (MII_CTRL):** MII Control When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXGMII_EN=Enabled: This bit controls the width of the MAC interface when operating at SGMII/QSGMII/USXGMII speed modes of 10 Mbps or 100 Mbps - 0: 4-bit MII - 1: 8-bit MII This bit also controls the xpcs_mii_ctrl_o signal which is used for external clock multiplexing of the clk_mii_tx_i and clk_mii_rx_i signals. For other configurations: This is a read-only reserved field and returns 0.
7:5	0h RO	**Reserved**
4	0h RW	**SGMII_LINK_STS DWC_XPCS (SGMII_LINK_STS):** When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXGMII Link Status: SGMII Link Status/ USXGMII Link Status /QSGMII Port0 Link Status This bit is used in Bit 15 of the Config_Reg during Clause 37 auto-negotiation when the TX_CONFIG bit of this register is set to 1 in the SGMII/QSGMII/USXGMII mode and when SGMII_PHY_MODE_CTRL bit of VR MII MMD Digital Control 1 Register is 0. - 0: Link Down - 1: Link Up For other configurations: This is a read-only reserved field and returns 0.
3	0h RW	**TX_CONFIG DWC_XPCS (TX_CONFIG):** When SGMII_EN=Enabled or QSGMII_EN=Enabled or USXMII_EN=Enabled: Transmit Configuration This bit controls the Config_Reg value to be used during the Clause 37 auto-negotiation in the SGMII/QSGMII/USXGMII mode. - 1: Configures the DWC_xpcs as the PHY side SGMII/QSGMII/USXGMII. - 0: Configures the DWC_xpcs as the MAC side SGMII/QSGMII/USXGMII. For other configurations: This is a read-only reserved field and returns 0.

Bit Range	Default & Access	Field Name (ID): Description
2:1	0h RW	**PCS_MODE DWC_XPCS (PCS_MODE):** When SGMII_EN=Enabled or QSGMII_EN=Enabled: PCS Mode This field controls the auto-negotiation (and operating) mode. - 00: 1000BASE-X mode (clause 37 auto-negotiation is as per 1000BaseX). - 10: SGMII mode (clause 37 auto-negotiation is as per SGMII). - 11: QSGMII mode (clause 37 auto-negotiation conforms to QSGMII) If this field is set as 2'b11, then XPCS asserts the 'xgxs_qsgmii_mode_o' port. For other configurations: This is a read-only reserved field and returns 0.
0	0h RW	**MII_AN_INTR_EN DWC_XPCS (MII_AN_INTR_EN):** Clause 37 AN Complete Interrupt Enable When set to 1, this bit enables the generation of Clause 37 auto-negotiation complete interrupt output. When set to 0, it disables the generation of Clause 37 auto-negotiation complete interrupt.

21.3.1.32 VR_MII_AN_INTR_STS DWC_XPCS (VR_MII_AN_INTR_STS) — Offset 1F00010004h

VR MII MMD AN Interrupt and Status Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010004h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	0h RO/V	**LP_CK_STP DWC_XPCS (LP_CK_STP):** Link Partner EEE Clock Stop Capability This field indicates the EEE clock stop capability (or clock-stop enabe - in case far-end is acting as QSGMII MAC) advertised by the far-end device. This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 0. Note:This field is present only in configurations with QSGMII_EN=Enabled
5	0h RO/V	**LP_EEE_CAP DWC_XPCS (LP_EEE_CAP):** Link Partner EEE Capability This field indicates the EEE capability advertised by the far-end device (Port 0 QSGMII PHY). This field is valid only when PCS_MODE[1:0] is set to the QSGMII mode and the auto-negotiation is complete along port 0. Note:This field is present only in configurations with QSGMII_EN=Enabled
4:1	0h RO/V	**CL37_ANSGM_STS DWC_XPCS (CL37_ANSGM_STS):** When SGMII_EN=Enabled or QSGMII_EN=Enabled: Clause 37 AN SGMII Status/ QSGMII Port 0 Status This field is valid only when the PCS_MODE[1:0] is set to the SGMII/QSGMII mode and the auto-negotiation is complete. It indicates the status received from remote link after the SGMII/QSGMII (Port 0) autonegotiation is complete. CL37_ANSGM_STS[0] - 0: Half Duplex - 1: Full Duplex CL37_ANSGM_STS[2:1] - 00: 10 Mbps speed link - 01: 100 Mbps speed link - 10: 1000 Mbps speed link CL37_ANSGM_STS[3] - 0: Link is Down - 1: Link is Up For other configurations: This is a read-only reserved field and returns 0.
0	0h RW	**CL37_ANCMPLT_INTR DWC_XPCS (CL37_ANCMPLT_INTR):** Clause 37 AN Complete Interrupt (SS,WC Type) The DWC_xpcs sets this bit when Clause 37 auto-negotiation is complete. The host must clear this bit by writing 0 to it.

21.3.1.33 VR_MII_TC DWC_XPCS (VR_MII_TC) — Offset 1F00010006h

VR MII MMD Test Control Register. Note: This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010006h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2	0h RW	**TPE DWC_XPCS (TPE):** Test Pattern Enable Lanes This bit indicates that a test pattern can be enabled in the Tx path after the current normal frame transmission is complete. - 0: Test pattern disabled - 1: Test pattern enabled Dependencies: The specific test pattern that is generated is based on Bits[1:0] of this register.
1:0	0h RW	**TP DWC_XPCS (TP):** Test Pattern Select This field indicates the pattern type that is enabled with Bit 2 of this register. The following are the supported test patterns: - 2'b00: High Frequency Test Pattern - 2'b01: Low Frequency Test Pattern - 2'b10: Mixed Frequency Test Pattern - 2'b11: Reserved The definition of these test patterns is specified in IEEE Std 802.3ae, Annex 48A.

21.3.1.34 VR_MII_DBG_CTRL DWC_XPCS (VR_MII_DBG_CTRL) — Offset 1F0001000Ah

VR MII MMD Debug Control Register Note: This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F0001000Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**TX_PMBL_CTL DWC_XPCS (TX_PMBL_CTL):** Transmit Preamble Control This bit can be set to 1 to prevent possible preamble truncation in the DWC_xpcs transmitter when operating in 1000BASE-X (or 2.5G Mode over GMII) Mode. As per IEEE spec, it is permissible for a compliant 1000BASE-X PCS transmit process to truncate the first byte of preamble in order to align the start of the packet on the EVEN boundary. If this bit is set to 1, DWC_xpcs does not delete any preamble bytes (received from GMII Tx interface) and passes on the same number of preamble bytes to its output. DWC_xpcs carries out this operation by adjusting the IPG. This mode is a deviation from Clause 36 of IEEE802.3 specification. But it can prove useful when operating at 2.5G Mode (over clocked 1000BASE-X Mode) and the far-end device is compliant to IEEE802.3bz/cb specification.
7:6	0h RO	**Reserved**
5	0h RW	**SUPRESS_EEE_LOS_DET DWC_XPCS (SUPRESS_EEE_LOS_DET):** Suppress EEE Loss of Signal Detection. When this field is set to 1, Loss of Signal indicated by the PHY (based on input port xpcs_los_i. Receive link will be purely evaluated based the on data received by DWC_xpcs from PHY. When this field is set to 0, Loss of signal indicated by the PHY will be considered by the DWC_xpcs while evaluating the Receive link status in EEE mode.
4	0h RW	**SUPRESS_LOS_DET DWC_XPCS (SUPRESS_LOS_DET):** Suppress Loss of Signal Detection When this field is set to 1, Loss of Signal indicated by the PHY (based on input port xpcs_los_i. When this field is set to 0, Loss of signal indicated by the PHY will be considered by the DWC_xpcs while evaluating the Receive link status. Note: This register bit has an impact on the EEE Rx behaviour of DWC_xpcs when operating in QSGMII Mode for Enterprise Gen5 12G PHY configurations. if this register bit is set to 1, then entry to RX_QUIET state is based on 'code_sync_status' (genereated by PCS Synchronization State Diagram) instead of 'signal_detect'.
3:1	0h RO	**Reserved**
0	0h RW	**RESTAR_SYNC_0 DWC_XPCS (RESTAR_SYNC_0):** Restart Synchronization When set to 1, this bit restarts the Rx Synchronization State machine on Lane 0. The host must clear this bit to 0 before setting it to 1 next time.

21.3.1.35 VR_MII_EEE_MCTRL0 DWC_XPCS (VR_MII_EEE_MCTRL0) — Offset 1F0001000Ch

VR MII MMD EEE Mode Control Register This register enables or disables the Energy Efficient Ethernet (EEE) support. This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F0001000Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**CLKSTOP DWC_XPCS (CLKSTOP):** Clock Stop This field holds the count value after which the Rx clock to the MAC can be stopped. The default value is 8. The host should program this value depending on the capability of the MAC. This field is used to control the assertion of the xpcs_lrx_clk_gat_o signal (to gate the Rx clock of the MAC) By default, the xpcs_lrx_clk_gat_o signal is asserted after the PCS Rx module detects the LPI pattern followed by the following: Number of clk_xgxs_rx0_i or clk_rpcs_rx_i clocks (specified in this field) + clk_eee_i synchronization delay + FIFO initialization delay
11:8	0h RW	**MULT_FACT_100NS DWC_XPCS (MULT_FACT_100NS):** 100 ns Clock Tic Multiplying Factor This bit is the multiplying factor to the clk_eee_i clock time period to make it closer to 100 ns. For example, if the clk_eee_i clock time period (clk_eee_i_time_period) is 10 ns, the value of this field is 9, that is, 1 less than 10. This value should be programmed such that the clk_eee_i_time_period * (MULT_FACT_100NS + 1) should be within 80 ns to 120 ns. The default value of this register is 9, assuming that the default clk_eee_i time period to be 10 ns.
7	0h RW	**RX_EN_CTRL DWC_XPCS (RX_EN_CTRL):** Rx Control Enable This bit controls the generation of the xpcs_rx_en_o{lane} signal. When this bit is set to 1, the xpcs_rx_en_o{lane} signal is de-asserted when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_rx_en_o{lane} signal is not de-asserted when the EEE transmit controller reaches the Quiet state.
6	0h RW	**SIGN_BIT DWC_XPCS (SIGN_BIT):** Effective 100 ns Tic Value The host should use this bit to fine tune the EEE timing requirement. The host should set this bit to 0 when the clk_eee_i_time_period * (MULT_FACT_100NS + 1) value is more than 100 ns. The host should set this bit to 1 when the clk_eee_i clock period * (MULT_FACT_100NS + 1) value is less than or equal to 100 ns.
5	0h RO	**Reserved**
4	0h RW	**TX_EN_CTRL DWC_XPCS (TX_EN_CTRL):** Tx Control Enable This bit controls the generation of the following signals: - xpcs_tx_en_o{lane}.When this bit is set to 1, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is de-asserted when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xgxs_tx{lane}_en_o or xpcs_tx_en_o{lane} signal is not de-asserted when the EEE transmit controller reaches the Quiet state.
3	0h RW	**RX_QUIET_EN DWC_XPCS (RX_QUIET_EN):** Rx Quiet Enable This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE receive controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
2	0h RW	**TX_QUIET_EN DWC_XPCS (TX_QUIET_EN):** Tx Quiet Enable This bit controls the generation of the xpcs_lpitx_quiet_o output. When this bit is set to 1, the xpcs_lpitx_quiet_o output is set to 1 when the EEE transmit controller reaches the Quiet state. When this bit set to 0, the xpcs_lpitx_quiet_o output is not set to 1.
1	0h RW	**LRX_EN DWC_XPCS (LRX_EN):** LPI Rx Enable When set to 1, this bit enables the Energy Efficient Ethernet support in the DWC_xpcs receive path. When set to 0, it disables the support for Energy Efficient Ethernet in the DWC_xpcs receive path.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**LTX_EN DWC_XPCS (LTX_EN):** LPI Tx Enable When set to 1, this bit enables the Energy Efficient Ethernet support in the DWC_xpcs Transmit path. When set to 0, it disables the support for Energy Efficient Ethernet in the DWC_xpcs Transmit path.

21.3.1.36 VR_MII_EEE_TXTIMER DWC_XPCS (VR_MII_EEE_TXTIMER) — Offset 1F00010010h

VR MII MMD EEE Tx Timer Register This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010010h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5:0	00h RW	**TSL_RES DWC_XPCS (TSL_RES):** TSL Resolution This field stores the resolution value for the TSL timer. When the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TSL timer. The DWC_xpcs maintains the default value of the TSL timer as 199, assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100 ns to produce 19900 ns (19.9 us) as per the TSL requirement in the IEEE standard. If clk_eee_i_time_period * (MULT_FACT_100NS + 1) is 90, the default TSL timer produces 17910 ns (17.91 us) which is lesser than the standard 19.9 us. To make it 19.9 us, you should program this register such that (199 +/- TSL_RES) * ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) is greater than 19.9 us and less than 20.1 us (max limit), that is, (199 + TSL_RES)*90 = 19.9 us. TWL_RES = 23 meets the requirement which produces 19.98 us. The SIGN_BIT should be programmed as 1.

21.3.1.37 VR_MII_EEE_RXTIMER DWC_XPCS (VR_MII_EEE_RXTIMER) — Offset 1F00010012h

VR MII MMD EEE Rx Timer Register This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010012h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:8	00h RW	**TWR_RES DWC_XPCS (TWR_RES):** TWR Resolution This field stores the resolution value for the TWR timer. When the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the TWR timer. Default Value: The default value is 11 us for 1000BASEX-Only PCS mode. This value is as per the requirements specified in the standard assuming that clk_eee_i_time_period * (MULT_FACT_100NS + 1) produces 100 ns tick. Example: For KX mode, the time requirement is 11 us. The DWC_xpcs maintains the default value of the TWR timer as 110, assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100 ns to produce 11000 ns (11 us). If clk_eee_i_time_period * (MULT_FACT_100NS + 1) is 110, the default TWR timer produces 12100 ns (12.1 us) which is more than 11 us. To make it 11 us, you must program this register such that (110 +/- TWR_RES) * ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) = 11 us. Therefore, use the following equation: (110 - TWR_RES) * 110 = 11000 ns TWL_RES = 10 meets the requirement which produces 11 us. The SIGN_BIT should be programmed as 0.
7:0	00h RW	**RES_100U DWC_XPCS (RES_100U):** 100 us Resolution This field stores the resolution value for the 100 us timer. If the generated 100 ns tic timer is not exactly 100 ns, this field is programmed with the required value. The programmed value is equivalent to the number of more (SIGN_BIT is low) or less (SIGN_BIT is high) counts than the ideal count to meet the range of the 100 us timer. This field is used to control the generation of 100 us time tick using the clk_eee_i clock and MULT_FACT_100NS field. By default, the 100 us timer is generated assuming clk_eee_i_time_period * (MULT_FACT_100NS + 1) is equal to 100 ns. Therefore, the DWC_xpcs maintains the default value of the 100 us timer as 1000 to achieve 100000 ns (100 us). You should use this field if clk_eee_i_time_period * (MULT_FACT_100NS + 1) is not equal to 100 ns. To program this field, use the following equation: (1000 +/- RES_100US)* ((MULT_FACT_100NS + 1) * clk_eee_i_time_period) = 100 us The SIGN_BIT should be programmed as 1 for (+) and 0 for (-).

21.3.1.38 VR_MII_LINK_TIMER_CTRL DWC_XPCS (VR_MII_LINK_TIMER_CTRL) — Offset 1F00010014h

VR MII MMD Link Timer Control Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010014h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**CL37_LINK_TIME DWC_XPCS (CL37_LINK_TIME):** Programmable Link Timer Value for Clause 37 autonegotiation. This field can be programmed to any desired value if application wishes to over-ride the standard specified values for Link Timer used during Clause 37 Auto negotiation. Link timer is implemented in XPCS using a 24-bit timer.When operating in USXGMII mode, link timer runs at 156.25 MHz. When operating in 1000BaseX/SGMII mode, this timer operates at 125 MHz. For USXGMII configurations: This field forms the upper 16-bit of the 24-bit value that gets loaded to the link timer.The lower 8-bits are hard-coded as zero. For example, if CL37_LINK_TIME = 1, the value that is loaded to the timer is 24'h100, which corresponds to a duration of 1638 ns (256*6.4ns) in USXGMII mode or 2048 ns (256*8ns) in 1000BaseX/SGMII mode. For configurations without USXGMII: This field forms the upper 16-bit of the 24-bit value that gets loaded to the link timer.The lower 8-bits are hardcoded as 8'h7D. For example, if CL37_LINK_TIME = 1, the value that is loaded to the timer is 24'h17D, which corresponds to a duration of 3048 ns (381*8ns). After programming this register, application should perform either of the following steps, so that the new values takes effect: - Set CL37_TMR_OVR_RIDE bit (bit[3]) of VR MII MMD Digital Control 1 Register to 1 - FAST_SIM bit of SR Control MMD Control Register should be cleared (if already set) and then set back to 1.

21.3.1.39 VR_MII_EEE_MCTRL1 DWC_XPCS (VR_MII_EEE_MCTRL1) — Offset 1F00010016h

VR MII MMD EEE Mode Control 1 Register This register also controls the Energy Efficient Ethernet (EEE) related settings of DWC_xpcs.This register is present only for configurations with MAIN_MODE = 1000BASEX-Only PCS and EEE_EN = Enabled.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010016h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**TRN_LPI DWC_XPCS (TRN_LPI):** Transparent Tx LPI Mode Enable. When set to 1 (along with LTX_EN=1), transparent LPI mode gets activated in the DWC_xpcs Transmit path. In this mode,the transmit LPI state-machine doesn't move to TX_QUIET state. On detecting Lower-Power Idle on GMII Tx interface, DWC_xpcs goes to the TX_SLEEP state and remains in this state till MAC stops sending LPI. In this mode,DWC_xpcs merely sends the encoded LPI pattern to the serdes. This mode does not involve gating-off of any clocks to DWC_xpcs. In addition, the serdes transmitter is not disabled (xpcs_tx_data_en_o signal remains high). MAC should ensure that it does not gate-off XGMII/GMII Tx clock to DWC_xpcs during this mode of operation.

21.3.1.40 VR_MII_DIG_STS DWC_XPCS (VR_MII_DIG_STS) — Offset 1F00010020h

VR MII MMD Digital Status Register. Note: This register is present only in 1000BaseX-Only PCS configurations.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010020h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**LTX_STATE DWC_XPCS (LTX_STATE):** LPI Transmit State. This field indicates the current state of the LPI Transmit state Machine. This is a 2-bit field if the selected configuration does not have RPCS.Otherwise, it is a 3-bit field. - 000: LTX_ACTIVE - 001: LTX_SLEEP - 010: LTX_QUIET - 011: LTX_REF_WAKE - 100: LTX_ALERT (valid only if RPCS is present) - 101: LTX_SCR_BYP (valid only if RPCS is present)
12:10	0h RO/V	**LRX_STATE DWC_XPCS (LRX_STATE):** LPI Receive State This field indicates the current state of the LPI Receive State Machine: - 000: LRX_ACTIVE - 001: LRX_SLEEP - 010: LRX_QUIET - 011: LRX_WAKE - 100: LRX_WTF - 101: LRX_LINK_FAIL - 110: LRX_LPI_K
9:7	0h RO	**Reserved**
6	0h RO/V	**RXFIFO_OVF DWC_XPCS (RXFIFO_OVF):** Rx FIFO Overflow (RO,LH Type) This bit indicates the clock rate compensation FIFO overflow. - 0: Normal operation - 1: FIFO overflow
5	0h RO/V	**RXFIFO_UNDF DWC_XPCS (RXFIFO_UNDF):** Rx FIFO Underflow (RO,LH Type) This bit indicates the clock rate compensation FIFO underflow. - 0: Normal operation - 1: FIFO underflow
4:0	0h RO	**Reserved**

21.3.1.41 VR_MII_ICG_ERRCNT1 DWC_XPCS (VR_MII_ICG_ERRCNT1) — Offset 1F00010022h

VR MII MMD Invalid Code Group Error Count1 Register. Note: This register is present only for 1000BaseX-Only PCS configurations

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010022h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7:0	00h RO/V	**EC0 DWC_XPCS (EC0):** Invalid Code Group Count Lane 0 (RO,LH Type) This field gives the invalid code group count in Lane 0 when Bit 4 of VR MII MMD Digital Error Count Select Register is set to 1.

21.3.1.42 VR_MII_MISC_STS DWC_XPCS (VR_MII_MISC_STS) — Offset 1F00010030h

VR MII MMD Miscellaneous Status Register. This register is present only when the DWC_xpcs is configured in 1000BASEX-Only PCS mode.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010030h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**
3:0	0h RO/V	**BIT_SFT DWC_XPCS (BIT_SFT):** Bit Shift This field indicates the number of bit-shifts carried-out by comma-detect logic so as to align the incoming 10-bit XGXS Rx data Default Value: The default value of this field can be any value, depending on the status of comma-detect logic.

21.3.1.43 VR_MII_RX_LSTS DWC_XPCS (VR_MII_RX_LSTS) — Offset 1F00010040h

VR MII PHY Rx Lane Status Register In KX_Only, KR_Only, KR_KX, 10GBASE-R PCS, and 1000BASEX-Only PCS configurations, only Lane 0 control and status information is present. In configurations with both 1G (KX) and 10G (XGXS PCS, 10GBASE-X PCS, or KX4) modes, only Lane 0 control and status information is used when the DWC_xpcs is operating in the 1G mode.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F00010040h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO/V	**RX_VALID_3_1 DWC_XPCS (RX_VALID_3_1):** DPLL Lock Status for Lanes[3:1] This field indicates that the DPLL in the PHY is locked on the serial data in the corresponding lane. - 3'b**1: Lane 1 DPLL bit locked - 3'b*1*: Lane 2 DPLL bit locked - 3'b1**: Lane 3 DPLL bit locked Dependency: This field is present only the following configurations: Backplane Ethernet PCS configurations.
12	0h RO/V	**RX_VALID_0 DWC_XPCS (RX_VALID_0):** DPLL Lock Status for Lane 0 This field indicates that the DPLL in the PHY is locked on the serial data in Lane 0. The value 1'b1 indicates that Lane 0 DPLL bit is locked. Dependency: This field is present only the following configurations: Backplane Ethernet PCS configurations.
11:5	0h RO	**Reserved**
4	0h RO/V	**SIG_DET_0 DWC_XPCS (SIG_DET_0):** Rx Signal Detect for Lane 0 This bit indicates that the Rx detected the signal on Lane 0. This bit is the complement value of the signals input from PHY (xgxs_los_i[0]) on Lane 0. The value 1'b1 indicates that Lane 0 signal is detected. This field is unreliable for a short duration around the transition of any field in the VR MII Consumer Gen1 PHY Rx Loss-of-Signal Control Register.
3:0	0h RO	**Reserved**

21.3.1.44 VR_MII_DIG_CTRL2 DWC_XPCS (VR_MII_DIG_CTRL2) — Offset 1F000101C2h

VR MII MMD Digital Control2 Register This register is present only when the DWC_xpcs is configured in 1000BASEX-Only PCS mode.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F000101C2h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	**Reserved**
4	0h RW	**TX_POL_INV_0 DWC_XPCS (TX_POL_INV_0):** Tx Polarity Invert on Lane 0 When set to 1, this bit reverses the data polarity on the Tx differential lines of Lane 0.
3:1	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**RX_POL_INV_0 DWC_XPCS (RX_POL_INV_0):** Rx Polarity Invert on Lane 0 When set, the bits within this field indicate that the data received on Rx serial line is inverted on Lane 0. This reverses the polarity on the data received from the PHY core. The value 1 indicates that Rx data on Lane 0 is inverted.

21.3.1.45 VR_MII_DIG_ERRCNT_SEL DWC_XPCS (VR_MII_DIG_ERRCNT_SEL) — Offset 1F000101C4h

VR MII MMD Digital Error Count Select Register This register is present only when the DWC_xpcs is configured in 1000BASEX-Only PCS mode.

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1F000101C4h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	**Reserved**
4	0h RW	**INV_EC_EN DWC_XPCS (INV_EC_EN):** Invalid Code Group Error Counter Enable When this bit is set, the counting of invalid code group errors is enabled. - 0: The counting of errors is disabled - 1: The counting of errors is enabled For information about the fields containing the number of errors counted, see VR MII MMD Invalid Code Group Error Count1 Register.
3:1	0h RO	**Reserved**
0	0h RW	**COR DWC_XPCS (COR):** Clear on Read When this bit is set and the host reads any error counter, that counter is cleared after the read cycle. - 0: Normal operation - 1: Clear any error counter that is read

21.3.2 MDIO - Adhoc PHY Sublayer Registers - PHY Address 15h

The Adhoc Registers are accessible as an IEEE Std 802.3 Clause 22 capable PHY MDIO Manageable Device (MMD). Its 5-bit PHY Address (PHYAD) is 15h. Its 32 16-bit data registers are accessible using the 5-bit PHY Register Address (REGAD).

The Adhoc Registers consist of a PHY Global Configuration Register (GCR), one captured 64-bit Always Running Timer (ART) Time Stamp, one six-byte, unique MAC Address provided by the Intel product customer via the system Flash Device, and various status registers and configuration registers related to the PCH internal PHY sublayer circuitry and debug circuity.

Table 21-49. Summary of BAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1500000000h	2	GCR mgbe_mdio (GCR)	0826h
1500000002h	2	PMC_ART0 mgbe_mdio (PMC_ART0)	0000h
1500000004h	2	PMC_ART1 mgbe_mdio (PMC_ART1)	0000h
1500000006h	2	PMC_ART2 mgbe_mdio (PMC_ART2)	0000h
1500000008h	2	PMC_ART3 mgbe_mdio (PMC_ART3)	0000h
150000000Ah	2	GPSR0 mgbe_mdio (GPSR0)	0000h
150000000Ch	2	GPSR1 mgbe_mdio (GPSR1)	0000h
150000000Eh	2	GPSR2 mgbe_mdio (GPSR2)	0000h
1500000010h	2	GPSR3 mgbe_mdio (GPSR3)	0000h
1500000012h	2	GPSR4 mgbe_mdio (GPSR4)	0000h
1500000014h	2	GPSR5 mgbe_mdio (GPSR5)	0000h
1500000016h	2	GPCR0 mgbe_mdio (GPCR0)	0000h
1500000018h	2	GPCR1 mgbe_mdio (GPCR1)	0000h
150000001Ah	2	GPCR2 mgbe_mdio (GPCR2)	0000h
150000001Ch	2	GPCR3 mgbe_mdio (GPCR3)	0000h
150000001Eh	2	GPCR4 mgbe_mdio (GPCR4)	0000h
1500000020h	2	GPCR5 mgbe_mdio (GPCR5)	0000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1500000022h	2	GPCR6 mgbe_mdio (GPCR6)	0000h
1500000024h	2	GPCR7 mgbe_mdio (GPCR7)	0000h
1500000026h	2	MACADDR0 mgbe_mdio (MACADDR0)	0000h
1500000028h	2	MACADDR1 mgbe_mdio (MACADDR1)	0000h
150000002Ah	2	MACADDR2 mgbe_mdio (MACADDR2)	0000h
150000002Ch	2	MGBE_HH_STATUS mgbe_mdio (MGBE_HH_STATUS)	0000h
150000002Eh	2	MGBE_STATUS1 mgbe_mdio (MGBE_STATUS1)	0000h
1500000030h	2	MGBE_STATUS2 mgbe_mdio (MGBE_STATUS2)	0000h
1500000032h	2	MGBE_STATUS3 mgbe_mdio (MGBE_STATUS3)	0000h
1500000034h	2	MGBE CONFIG1 mgbe_mdio (MGBE_CONFIG1)	0000h
1500000036h	2	MGBE CONFIG2 mgbe_mdio (MGBE_CONFIG2)	0000h
1500000038h	2	MGBE CONFIG3 mgbe_mdio (MGBE_CONFIG3)	0000h
150000003Ah	2	MGBE CONFIG4 mgbe_mdio (MGBE_CONFIG4)	0000h
150000003Ch	2	MGBE CONFIG5 mgbe_mdio (MGBE_CONFIG5)	0000h
150000003Eh	2	MGBE CONFIG6 mgbe_mdio (MGBE_CONFIG6)	0000h

21.3.2.1 GCR mgbe_mdio (GCR) — Offset 1500000000h

Global Control Register

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000000h	0826h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	8h RW	**ART_SKEW mgBE_mdio (ART_SKEW):** ART timer capture skew

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Reserved**
6	0h RW	**PHY2MAC_INTR_POL mgBE_mdio (PHY2MAC_INTR_POL):** Disable Auto negotiation
5	1h RW	**FLR_ENABLE:** 1'b0: FLR is disabled 1'b1: FLR is enabled
4	0h RW	**PHYIF_STRAPOVR mgBE_mdio (PHYIF_STRAPOVR):** PHY interface strap override
3	0h RW	**PHYIF_MODE mgBE_mdio (PHYIF_MODE):** Phy interface mode
2:1	3h RW	**LINK_MODE mgBE_mdio (LINK_MODE):** mgbe Link speed selection
0	0h RW	**AUTONEG_DISABLE mgBE_mdio (AUTONEG_DISABLE):** Disable Auto negotiation

21.3.2.2 PMC_ART0 mgbe_mdio (PMC_ART0) — Offset 1500000002h

PMC ART Time capture Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000002h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**PMC_ART0_FLD mgBE_mdio (PMC_ART0_FLD):** Read pmc art timer value

21.3.2.3 PMC_ART1 mgbe_mdio (PMC_ART1) — Offset 1500000004h

PMC ART Time capture Register 1

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000004h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**PMC_ART1_FLD mgBE_mdio (PMC_ART1_FLD):** Read pmc art timer value

21.3.2.4 PMC_ART2 mgbe_mdio (PMC_ART2) — Offset 1500000006h

PMC ART Time capture Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000006h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**PMC_ART2_FLD mgBE_mdio (PMC_ART2_FLD):** Read pmc art timer value

21.3.2.5 PMC_ART3 mgbe_mdio (PMC_ART3) — Offset 1500000008h

PMC ART Time capture Register 3

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000008h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**PMC_ART3_FLD mgBE_mdio (PMC_ART3_FLD):** Read pmc art timer value

21.3.2.6 GPSR0 mgbe_mdio (GPSR0) — Offset 150000000Ah

General purpose status Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000000Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**GPSR0_FLD mgBE_mdio (GPSR0_FLD):** Read pmc art timer value

21.3.2.7 GPSR1 mgbe_mdio (GPSR1) — Offset 150000000Ch

General purpose status Register 1

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000000Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**GPSR1_FLD mgBE_mdio (GPSR1_FLD):** Read pmc art timer value

21.3.2.8 GPSR2 mgbe_mdio (GPSR2) — Offset 150000000Eh

General purpose status Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000000Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**GPSR2_FLD mgBE_mdio (GPSR2_FLD):** Read pmc art timer value

21.3.2.9 GPSR3 mgbe_mdio (GPSR3) — Offset 1500000010h

General purpose status Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000010h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**GPSR3_FLD mgBE_mdio (GPSR3_FLD):** Read pmc art timer value

21.3.2.10 GPSR4 mgbe_mdio (GPSR4) — Offset 1500000012h

General purpose status Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000012h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**GPSR4_FLD mgBE_mdio (GPSR4_FLD):** Read pmc art timer value

21.3.2.11 GPSR5 mgbe_mdio (GPSR5) — Offset 1500000014h

General purpose status Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000014h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**GPSR5_FLD mgBE_mdio (GPSR5_FLD):** Read pmc art timer value

21.3.2.12 GPCR0 mgbe_mdio (GPCR0) — Offset 1500000016h

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000016h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR0_FLD mgBE_mdio (GPCR0_FLD):** Read pmc art timer value

21.3.2.13 GPCR1 mgbe_mdio (GPCR1) — Offset 1500000018h

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000018h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR1_FLD mgBE_mdio (GPCR1_FLD):** Read pmc art timer value

21.3.2.14 GPCR2 mgbe_mdio (GPCR2) — Offset 150000001Ah

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000001Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR2_FLD mgBE_mdio (GPCR2_FLD):** Read pmc art timer value

21.3.2.15 GPCR3 mgbe_mdio (GPCR3) — Offset 150000001Ch

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000001Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR3_FLD mgBE_mdio (GPCR3_FLD):** Read pmc art timer value

21.3.2.16 GPCR4 mgbe_mdio (GPCR4) — Offset 150000001Eh

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000001Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR4_FLD mgBE_mdio (GPCR4_FLD):** Read pmc art timer value

21.3.2.17 GPCR5 mgbe_mdio (GPCR5) — Offset 1500000020h

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000020h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR5_FLD mgBE_mdio (GPCR5_FLD):** Read pmc art timer value

21.3.2.18 GPCR6 mgbe_mdio (GPCR6) — Offset 1500000022h

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000022h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR6_FLD mgBE_mdio (GPCR6_FLD):** Read pmc art timer value

21.3.2.19 GPCR7 mgbe_mdio (GPCR7) — Offset 1500000024h

General purpose config Register 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000024h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**GPCR7_FLD mgBE_mdio (GPCR7_FLD):** Read pmc art timer value

21.3.2.20 MACADDR0 mgbe_mdio (MACADDR0) — Offset 1500000026h

Mac address strap value 0

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000026h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MAC_ADDR_STRAP0_FLD mgBE_mdio (MAC_ADDR_STRAP0_FLD):** Mac address strap value

21.3.2.21 MACADDR1 mgbe_mdio (MACADDR1) — Offset 1500000028h

Mac address strap value 1

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000028h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MAC_ADDR_STRAP1_FLD mgBE_mdio (MAC_ADDR_STRAP1_FLD):** Mac address strap value

21.3.2.22 MACADDR2 mgbe_mdio (MACADDR2) — Offset 150000002Ah

Mac address strap value 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000002Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RO/V	**MAC_ADDR_STRAP2_FLD mgBE_mdio (MAC_ADDR_STRAP2_FLD):** Mac address strap value

21.3.2.23 MGBE_HH_STATUS mgbe_mdio (MGBE_HH_STATUS) — Offset 150000002Ch

Hammock harbour status

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000002Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:2	0000h RO/V	**MGBE_RSVD_FLD mgBE_mdio (MGBE_RSVD_FLD):** Reserved
1	0h RO/V	**MGBE_TSW_ERR mgBE_mdio (MGBE_TSW_ERR):** Timestamp error status
0	0h RO/V	**MGBE_SNAPSHOT_DONE mgBE_mdio (MGBE_SNAPSHOT_DONE):** Snapshot done bit

21.3.2.24 MGBE_STATUS1 mgbe_mdio (MGBE_STATUS1) — Offset 150000002Eh

mgbe status

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000002Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RO	**Reserved**

21.3.2.25 MGBE_STATUS2 mgbe_mdio (MGBE_STATUS2) — Offset 1500000030h

mgbe status

Note: Bit definitions are the same as MGBE_STATUS1, offset 150000002Eh.

21.3.2.26 MGBE_STATUS3 mgbe_mdio (MGBE_STATUS3) — Offset 1500000032h

mgbe status

Note: Bit definitions are the same as MGBE_STATUS1, offset 150000002Eh.

21.3.2.27 MGBE CONFIG1 mgbe_mdio (MGBE_CONFIG1) — Offset 1500000034h

MGBE config Register 1

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000034h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**MGBE_CONFIG1_FLD mgBE_mdio (MGBE_CONFIG1_FLD):** Reserved

21.3.2.28 MGBE CONFIG2 mgbe_mdio (MGBE_CONFIG2) — Offset 1500000036h

MGBE config Register 2

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000036h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**MGBE_CONFIG2_FLD mgBE_mdio (MGBE_CONFIG2_FLD):** Reserved

21.3.2.29 MGBE CONFIG3 mgbe_mdio (MGBE_CONFIG3) — Offset 1500000038h

MGBE config Register 3

Type	Size	Offset	Default
MMIO	16 bit	BAR + 1500000038h	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**MGBE_CONFIG3_FLD mgBE_mdio (MGBE_CONFIG3_FLD):** Reserved

21.3.2.30 MGBE CONFIG4 mgbe_mdio (MGBE_CONFIG4) — Offset 150000003Ah

MGBE config Register 4

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000003Ah	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**MGBE_CONFIG4_FLD mgBE_mdio (MGBE_CONFIG4_FLD):** Reserved

21.3.2.31 MGBE CONFIG5 mgbe_mdio (MGBE_CONFIG5) — Offset 150000003Ch

MGBE config Register 5

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000003Ch	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**MGBE_CONFIG5_FLD mgBE_mdio (MGBE_CONFIG5_FLD):** Reserved

21.3.2.32 MGBE CONFIG6 mgbe_mdio (MGBE_CONFIG6) — Offset 150000003Eh

MGBE config Register 6

Type	Size	Offset	Default
MMIO	16 bit	BAR + 150000003Eh	0000h

Register Level Access:

BIOS Access	SMM Access	OS Access
None	None	None

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW	**MGBE_CONFIG6_FLD mgBE_mdio (MGBE_CONFIG6_FLD):** Reserved

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