Intel® 700 Series Chipset Family On-Package Platform Controller Hub (PCH)

Specification Update

Supporting Raptor Lake – PX Platforms

Revision 002

June 2023

Document Number: 766712

Contents

Revision History

Document Number	Revision Number	Description	Revision Date
766712	001	• Initial release	January 2023
	002	• Added Errata: 014	June 2023

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. This document is a compilation of device and document errata and specification clarifications and changes. It is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into the specification update and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® 700 Series Chipset Family On-Package Platform Controller Hub (PCH), Datasheet, Volume 1 of 2	765585
Intel® 700 Series Chipset Family On-Package Platform Controller Hub Datasheet, Volume 2 of 2	765764

1.2 Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

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2 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

2.1 Codes Used in Summary Table

Stepping	Description
X	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank Box)	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

2.2 Errata Summary Table

Erratum ID	Intel® 700 Series Chipset On-Package Stepping	Errata
	B1	
001	No Fix	USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State
002	No Fix	xHCI Power Management Link Timer
003	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
004	No Fix	SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used
005	No Fix	Intel Trace Hub Pipe Line Empty

Erratum ID	Intel® 700 Series Chipset On-Package Stepping	Errata
	B1	
006	No Fix	xHCI Short Packet Event Using Non-Event Data TRB
007	No Fix	eSPI SBLCL Register Bit Not Cleared by PLTRST#
008	No Fix	USB Audio Offload Traffic with Full-Speed Device Behind Hub
009	No Fix	Integrated GbE Controller Reset on D3 Exit
010	No Fix	USB VTIO Device Capabilities Field Length
011	No Fix	SLP_A# Minimum Assertion Width Timer During G3 Exit
012	No Fix	xHCI Force Header Command Incorrect Return Code
013	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
014	Fixed	USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug

2.3 Specification Changes

No.	Specification Changes
	No specification changes for this revision of the specification update.

2.4 Specification Clarifications

No.	Specification Clarifications
	No specification clarifications for this revision of the specification update.

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3 Errata Details

001	USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State
Problem	If a PCH USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2. 2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance Mode is disabled. 3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.
Implication	PCH USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

002	xHCI Power Management Link Timer
Problem	The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.
Implication	USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21. Note: No functional issues are expected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

003	xHCI USB 2.0 ISOCH Device Missed Service Interval
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets. Note: This issue has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

004	SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used
Problem	For flash device suspend / resume opcodes, the SPI controller does not use JEDEC SFDP's 13th DWORD bits [15:0], Program Suspend Instruction and Program Resume Instruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend / resume opcodes.

Implication	If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend / resume feature is not functional. In this case, system behavior varies depending on what the suspend / resume instruction is and when it is generated. Note: major flash vendors have been using the same value for bits [31:16] and bits [15:0].
Workaround	None identified. If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.
Status	For the steppings affected, refer to the Summary Table of Changes.

005	**Intel Trace Hub Pipe Line Empty**
Problem	The Intel Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset 0xD4) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset 0xD8) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).
Implication	There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).
Workaround	None identified. CaptureDone should be cleared or de-asserted after the pipe line is empty.
Status	For the steppings affected, refer to the Summary Table of Changes.

006	**xHCI Short Packet Event Using Non-Event Data TRB**
Problem	The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.
Implication	Transfer may fail due to the packet size error. **NOTE:** This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.
Workaround	None identified. Intel recommends software to use Data Event TRBs for short packet completion.
Status	For the steppings affected, refer to the Summary Table of Changes.

007	**eSPI SBLCL Register Bit Not Cleared by PLTRST#**
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to the Summary Table of Changes.

008	USB Audio Offload Traffic with Full-Speed Device Behind Hub
Problem	If USB audio offload is enabled for a USB Full-Speed Isochronous audio device connected behind a USB 2.0 or later hub and there is an active concurrent bulk transfer to another device on any port of the xHCI controller or behind the hub, the controller may stall the offloaded audio traffic and a split transaction error may occur.
Implication	The USB audio offload playback may stop. Audio may be recovered if the audio stream is paused and restarted, the audio device is removed and reconnected, or the audio application is restarted.
Workaround	None identified. A mitigation for this erratum is available with Intel® Smart Sound Technology version 10.29.00.5574 or later for systems with Microsoft Windows* 11 OS Release or Intel Smart Sound Technology version 10.29.00.7767 or later for systems with Microsoft Windows 10 OS Release. This mitigation will disable audio offload functionality for USB audio devices connected behind a hub.
Status	For the steppings affected, refer to the Summary Table of Changes.

009	Integrated GbE Controller Reset on D3 Exit
Problem	Upon GbE controller D3 exit, the GbE host driver performs a controller reset. During this reset, software accesses to the GbE MMIO registers may not complete.
Implication	The system may hang. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

010	USB VTIO Device Capabilities Field Length
Problem	The xHCI spec version 1.2 defines the PCI Express Capability structure offset 04h Device Capabilities (DVSEC) field to be 8 bytes. The USB Virtualization Based Trusted IO (VTIO) Management controller implements the DVSEC field as 12 bytes.
Implication	An USB controller driver may not be able to enable the USB VTIO controller.
Workaround	None identified. To mitigate this erratum, an Independent Software Vendor could account for the field length in the USB controller driver.
Status	For the steppings affected, refer to the Summary Table of Changes.

011	SLP_A# Minimum Assertion Width Timer During G3 Exit
Problem	Setting the Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) bit (offset 1020h, bit 12 in PMC_MMIO space) to 1 does not disable the SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH) timer (offset 1020h, bit 17 and 16 in PMC_MMIO space).
Implication	G3 exit duration may be extended by the value programmed in the SLP_A_MIN_ASST_WDTH register.
Workaround	None identified. To mitigate the issue for platforms that do not require SLP_A# stretching, BIOS should program SLP_A_MIN_ASST_WDTH to 0.
Status	For the steppings affected, refer to the Summary Table of Changes.

012	xHCI Force Header Command Incorrect Return Code
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification Rev 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

013	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

014	USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug
Problem	During the hot-plug of a USB 2.0 hub with Low-Speed or Full-Speed device connected behind the hub, a split transaction error may occur during the enumeration of the USB Low-Speed or Full-Speed device.
Implication	Due to this erratum, the USB Low-Speed or Full-Speed device may fail to enumerate when connected to the USB 2.0 hub. This condition is recovered after the xHCI controller has been reset (for example, software setting the xHCI Host Controller Reset (HCRST) bit or by performing a power button override).
Workaround	A fix for this erratum is available in BIOS. Please see BIOS version 3342_00 release or later.
Status	For the steppings affected, refer to the Summary Table of Changes.

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4 Specification Changes

There are no specification changes in this revision of the Specification Update.

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5 Specification Clarification

There are no specification clarifications in this revision of the Specification Update.

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