



Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series

Specification Update

Formerly known as Alder Lake-N and Twin Lake

Revision 004

January 2025



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Revision History

Document Number	Revision Number	Description	Revision Date
764616	001	Initial release	January 2023
764616	002	- Added USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug CPU May Not Load The Most Recent Data	August 2023
764616	003	- Added I2S Audio Channels Swapped With High Frame Polarity in Device Mode USB 3.2 DbC Sublink Speed Attribute ID (SSID) Value	June 2024
764616	004	Added Intel® Core™ 3 N-Series Processor	January 2025

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1 Preface

This document is an update to the specifications contained in the documents listed in the Affected Documents. It is a compilation of device and document errata and specification clarifications and changes and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools. Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet, Volume 1 of 2	759603
Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series Datasheet, Volume 2 of 2	759604

1.2 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor’s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes are incorporated in the next release of the specifications.

Specification Clarifications – This describes the specification in greater detail or further highlight a specifications impact to a complex design situation. These clarifications are incorporated in the next release of the specifications.

Documentation Changes – This includes typos, errors, or omissions from the current published specifications. These changes are incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product’s lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



2 Identification Information

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 2-1. Processor Lines Component Identification

Samples	CPUID	Reserved	Extended Family ¹	Extended Model ²	Reserved	SoC Type ³	Family Code ⁴	Model Number ⁵	Stepping ID ⁶
		31:28	27:20	19:16	15:14	13:12	11:8	7:4	3:0
Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-series	0xB06E0	Reserved	0000000b	1011b	Reserved	00b	0110b	1110b	0000b

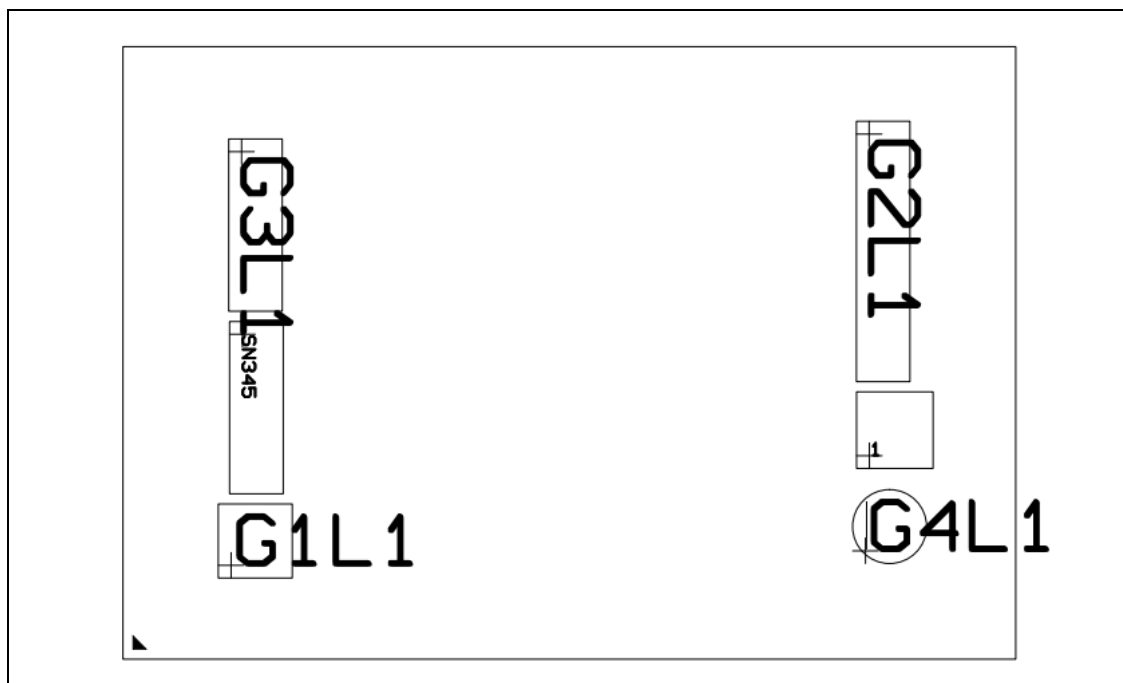
NOTES:

1. The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the SoC belongs to Intel® Core™ SoC family.
2. The Extended Model, bits [19:16] in conjunction with the model number, specified in bits [7:4], are used to identify the model of the SoC within the SoC family.
3. The SoC Type, specified in bits [13:12] indicates whether the SoC is an original OEM SoC, an OverDrive SoC, or a dual SoC (capable of being used in a dual SoC system).
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. Refer to above table for the SoC stepping ID number in the CPUID information.

2.2 Component Marking Information

Intel® Processor and Intel® Core™ i3 and Intel® Core™ 3 N-Series SoC is identified by the following component markings:

Figure 2-1. SoC Markings



Pin count:1264

Package Size: 35 mm x 24 mm

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3 Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Table 3-1. Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

Table 3-2. Errata Summary Table

Erratum ID	Stepping NO	Title
001	No Fix	USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State
002	No Fix	xHCI Power Management Link Timer
003	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
004	No Fix	SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used
005	No Fix	Intel® Trace Hub Pipe Line Empty
006	No Fix	xHCI Short Packet Event Using Non-Event Data TRB
007	No Fix	eSPI SBLCL Register Bit Not Cleared By PLTRST#
008	No Fix	USB Audio Offload Traffic with Full-Speed Device Behind Hub
009	No Fix	USB VTIO Device Capabilities Field Length
010	No Fix	Processor C-States with USB Full-speed or Low-speed Device Hotplug

Erratum ID	Stepping NO	Title
011	No Fix	xHCI Force Header Command Incorrect Return Code
012	No Fix	Leakage Current from VCCPRIM 1P8 Power Rail
013	No Fix	#UD May be Delivered Instead of Other Exceptions
014	No Fix	Type-C Host Controller Does Not Support Certain Qword Accesses
015	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
016	Fixed	Microcode Update May Cause a System Hang
017	Fixed	USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug
018	Fixed	CPU May Not Load The Most Recent Data
019	No Fix	I2S Audio Channels Swapped With High Frame Polarity in Device Mode
020	No Fix	USB 3.2 DbC Sublink Speed Attribute ID (SSID) Value

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4 Errata

001	USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State
Problem	If a PCH USB Type-C port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1. PCH resumes from S3, S4, or S5 state, the port may remain in U2. 2. Port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled. 3. Port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.
Implication	PCH USB Type C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

002	xHCI Power Management Link Timer
Problem	The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.
Implication	USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21. NOTE: No functional issues are expected.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

003	xHCI USB 2.0 ISOCH Device Missed Service Interval
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets. NOTE: This issue has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

004	SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used
Problem	For flash device suspend/resume opcodes, the SPI controller does not use JEDEC SFDPs 13th DWORD bits [15:0], Program Suspend Instruction and Program ResumeInstruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend/resume opcodes.
Implication	If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend /resume feature is not functional. In this case, system behavior varies depending on what the suspend/resume instruction is and when it is generated. NOTE: Major flash vendors have been using the same value for bits [31:16] and bits [15:0].
Workaround	None identified. If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.
Status	For the steppings affected, refer to Summary Tables of Changes .

005	Intel® Trace Hub Pipe Line Empty
Problem	The Intel® Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset 0xD4) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the capture Done signal is de-asserted by clearing the Force Capture Done bit (CSR_MTB_BAR, Offset 0xD8) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).
Implication	There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).
Workaround	None identified. Capture Done should be cleared or de-asserted after the pipe line is empty.
Status	For the steppings affected, refer to Summary Tables of Changes .

006	xHCI Short Packet Event Using Non-Event Data TRB
Problem	The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.
Implication	Transfer may fail due to the packet size error. NOTE: This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.
Workaround	None identified. Intel recommends software to use Data Event TRBs for short packet completion.
Status	For the steppings affected, refer to Summary Tables of Changes .

007	eSPI SBLCL Register Bit Not Cleared by PLTRST#
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to Summary Tables of Changes .

008	USB Audio Offload Traffic with Full-Speed Device Behind Hub
Problem	If USB audio offload is enabled for a USB Full-Speed Isochronous audio device connected behind a USB 2.0 or later hub and there is an active concurrent bulk transfer to another device on any port of the xHCI controller or behind the hub, the controller may stall the offloaded audio traffic and a split transaction error may occur.
Implication	The USB audio offload playback may stop. Audio may be recovered if the audio stream is paused and restarted, the audio device is removed and reconnected, or the audio application is restarted.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

009	USB VTIO Device Capabilities Field Length
Problem	The xHCI spec version 1.2 defines the PCI Express Capability structure offset 04h Device Capabilities (DVSEC) field to be 8 bytes. The USB Virtualization Based Trusted IO (VTIO) Management controller implements the DVSEC field as 12 bytes.
Implication	An USB controller driver may not be able to enable the USB VTIO controller.
Workaround	None identified. To mitigate this erratum, an Independent Software Vendor could account for the field length in the USB controller driver.
Status	For the steppings affected, refer to Summary Tables of Changes .

010	Processor C-States with USB Full-speed or Low-speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller
Implication	The processor may fail to enter C3 or deeper package C-States. NOTE: This erratum has only been observed in a synthetic environment
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to Summary Tables of Changes .

011	xHCI Force Header Command Incorrect Return Code
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification Rev 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

012	Leakage Current from VCCPRIM_1P8 Power Rail
Problem	When the VCCPRIM_1P8 is off and the VCCPRIM_3P3 is powered on during G3 to S5, there may be a leakage current from the VCCPRIM_3P3 power rail to VCCPRIM_1P8 power rail.
Implication	The leakage voltage may be observed on VCCPRIM_1P8 power rail. There is no known functional or reliability impact.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

013	#UD May be Delivered Instead of Other Exceptions
Problem	An invalid instruction opcode that runs into another exception before fetching all instruction bytes (example: A #GP due to the instruction being longer than 15 bytes or a CS limit violation) may signal a #UD despite not fetching all instruction bytes under some microarchitectural conditions.
Implication	Due to this erratum, a #UD exception may be serviced before other exceptions. This does not occur for valid instructions. Intel has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

014	Type-C Host Controller Does Not Support Certain Qword Accesses
Problem	The Type-C controller does not properly support Qword accesses to its MSI-X interrupt table which may lead to unexpected behavior.
Implication	When this erratum occurs, Qword reads do not return Unsupported Request and may not return correct data and Qword writes may lead to unexpected behavior. Intel has not observed this erratum to affect any commercially available software.
Workaround	Software should not utilize Qword access for the Type-C MSI-X table.
Status	For the steppings affected, refer to Summary Tables of Changes .

015	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified
Status	For the steppings affected, refer to Summary Tables of Changes .

016	Microcode Update May Cause a System Hang
Problem	A microcode update initiated by writing to MSR IA32_BIOS_UPDT_TRIG (MSR 79h) may cause the system to hang.
Implication	Due to this erratum, the microcode update will not complete and a system may hang with machine check exception (MSCOD = 045CH, MCACOD = 0402H)
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to Summary Tables of Changes .

017	USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug
Problem	A microcode update initiated by writing to MSR IA32_BIOS_UPDT_TRIG (MSR 79h) may cause the system to hang.
Implication	Due to this erratum, the USB Low-Speed or Full-Speed device may fail to enumerate when connected to the USB 2.0 hub. This condition is recovered after the xHCI controller has been reset (for example, software setting the xHCI Host Controller Reset (HCRST) bit or by performing a power button override).
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum
Status	For the steppings affected, refer to Summary Tables of Changes .

018	CPU May Not Load The Most Recent Data
Problem	Under complex microarchitectural conditions, a read on one logical processor may not receive the most recently stored data by another logical processor.
Implication	Due to this erratum, unpredictable system behavior or a system hang may occur. Intel has only observed this behavior in a synthetic test environment. Intel has not observed this erratum with any commercially available system.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to Summary Tables of Changes .

019	I2S Audio Channels Swapped With High Frame Polarity in Device Mode
Problem	When the I2S interface is in device mode, the audio controller may not be correctly configured if the audio codec requires high frame polarity.
Implication	Due to this erratum, the left and right audio channels may swap when frame polarity is set to high.
Workaround	None identified.
Status	For the steppings affected, refer to Summary Tables of Changes .

020	USB 3.2 DbC Sublink Speed Attribute ID (SSID) Value
Problem	The USB 3.2 Debug Class Device (DbC) reports an incorrect Sublink Speed Attribute ID (SSID) value in the SuperSpeedPlus USB Device Capability field.
Implication	Due to this erratum, the PCH USB 3.2.DbC (Debug Capability) device may fail to enumerate when connected to a USB 3.2 Gen 2x1 port.
Workaround	None identified
Status	For the steppings affected, refer to Summary Tables of Changes .

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5 ***Specification Changes***

There are no specification changes in this revision of the Specification Update.

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6 ***Specification Clarification***

There are no specification clarifications in this revision of the Specification Update.

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