Technology Brief

FPGAs and SoCs

Nios® V Processors for Agilex™ 5 FPGAs

Next generation soft processor based on the RISC-V architecture with improved performance over previous generations and access to a diverse ecosystem

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Embedded applications in markets like industrial and military that run complex workloads need the ability to have multiple soft processors with higher performance and easy to use tools accelerating software development. Additionally, it is critical to support the functional safety needs of these embedded markets. Furthermore, as designs are getting dramatically more complex, often consisting of a combination of large subsystems, intellectual property blocks (IP) and operating systems, there is a need for a unified solution to debug these complex heterogeneous environments. The Agilex™ 5 FPGA offers key benefits for these industrial applications at the edge such as improved performance, lower power consumption and the ability to instantiate RISC-V based Nios V soft cores within the fabric. While not always as efficient as hard processors, soft processors are useful because of their reconfigurability, flexibility and low cost. Soft processor IP removes the instance count limit by allowing users the ability to use portions of their programmable logic for routine compute and enables application code reusability. By leveraging Nios V processor and the Ashling* RiscFree* IDE for Altera® FPGAs, the Agilex 5 FPGA meets the requirements of these embedded markets along with a path to consistent IP upgrades, functional safety capabilities, access to industry-leading tools, broad software compatibility, better tool and compiler support, standard unified debug environment for the soft and hard processors and a growing ecosystem.

Nios V Processor Overview

The Nios V processor is Altera's next generation soft processor based on the RISC-V instruction set architecture. It is designed for Altera® FPGAs including the Agilex 5 FPGAs and SoCs to provide optimal performance for a wide range of edge applications. The roadmap for Nios V processor consists of 32-bit and 64-bit processors. The Nios V processor delivers improved features and capabilities over previous generations and provides access to the growing RISC-V ecosystem that gives you the ability to choose from a wide range of open source and commercial compilers, operating systems and debuggers that are readily available for RISC-V processors.

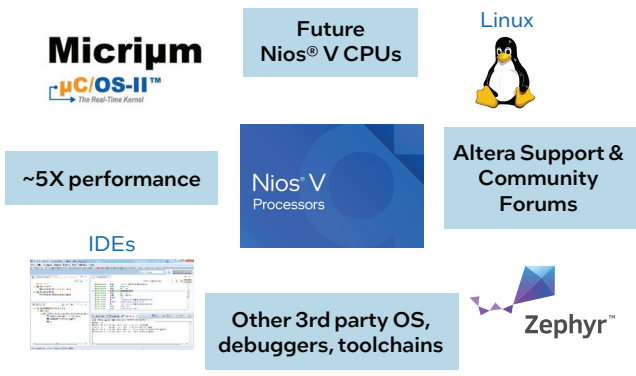

Figure 1. Nios V Processor Ecosystem

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32-bit Nios V Processors

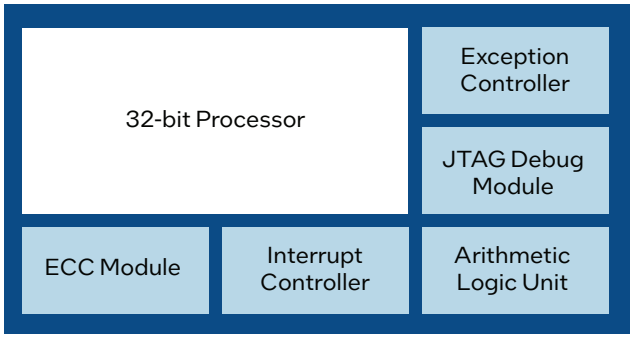


Figure 2. Microcontroller

Microcontroller (0.572 DMIPS/MHz)

- 32-bit based on RISC-V RV32I
- Error Correction Code (ECC)
- JTAG debug module
- Interrupt controller
- Exception controller
- Control and Status registers (CSRs)
- Machine mode

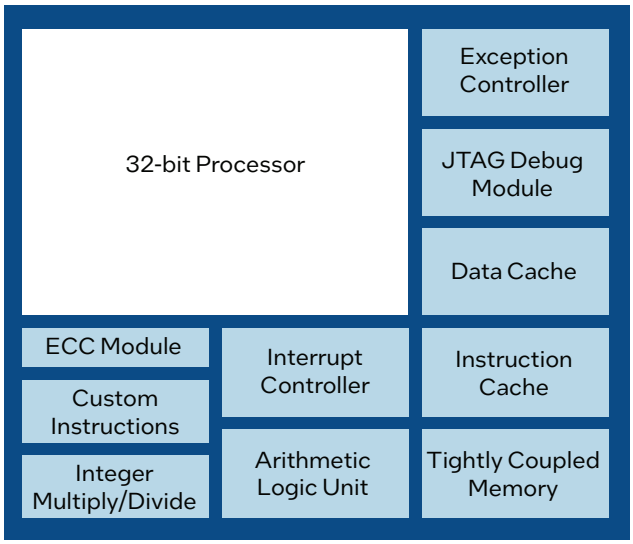


Figure 3. General-Purpose Processor

General-Purpose Processor

- 32-bit based on RISC-V RV32IM(F)ZicBom
- ECC module
- JTAG debug module
- Control and Status registers (CSRs)
- Interrupt controller
- Exception controller
- Custom instructions
- Integer multiply/divide hardware
- Tightly coupled memory
- Instruction and data caches
- Error correction code
- Machine mode

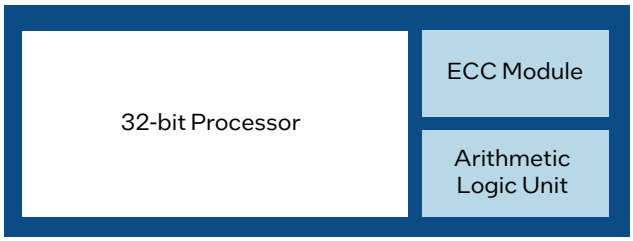
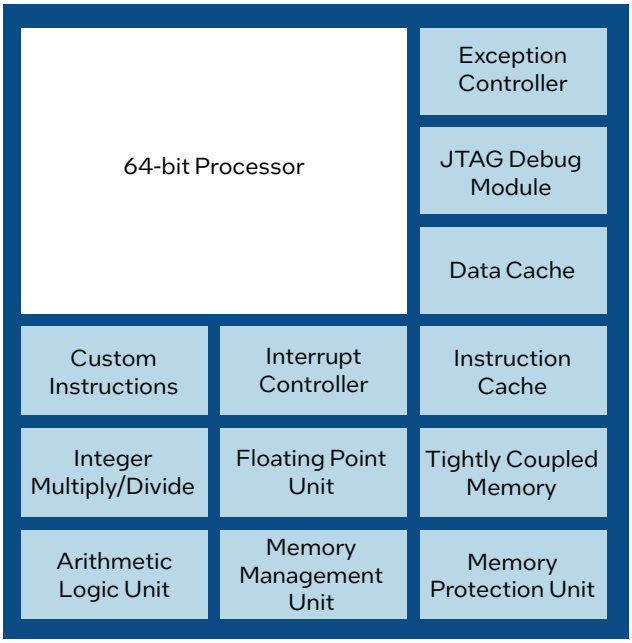


Figure 4. Size-Optimized Processor

Future Size-Optimized Core

- 32-bit based on RISC-V RV32I
- Timer module
- Error correction code
- Machine mode

Future 64-bit Nios V Features



- 64-bit - based on RISC-V RV64IMAF
- Timer module
- JTAG debug module
- Interrupt controller
- Exception controller
- Custom Instructions
- Integer multiply/divide hardware
- Tightly coupled memory
- Instruction and data caches
- ECC
- On-chip trace
- Branch prediction
- Memory Protection Unit (MPU)
- 32-bit Floating Point Unit (FPU)
- Memory Management Unit (MMU)
- Machine, Supervisor and User modes

Figure 5. 64-bit Nios V Features

Design Using Traditional Tools and Familiar Flows

Quartus® Prime Software and Platform Designer allow hardware teams to create a processor and peripheral solution based on the RISC-V architecture using traditional hardware tool flows as needed for your production solution.

Designs using the Nios V processor can be created or existing Nios® II/e designs can be ported to the Nios® V/m processor using traditional hardware development tools. The Nios V/m processor IP is available under embedded processors in the IP catalog making it easy to quickly configure and integrate your Nios V processor system using the platform designer system integration tool. Platform Designer is a system integration tool that allows you to stitch IP together to create a system. You can create the processor subsystem, pick from a range of IP for easy integration or add custom IP from your own library or design.

A board support package (BSP) provides a software runtime environment for embedded systems, such as Nios V/m processor systems. The BSP Editor is a GUI tool that you can launch from Platform Designer to generate and configure BSP contents. BSP generation can be performed using Platform Designer BSP Editor or using the Command Line Utility.

You can enable BSP creation for the most up-to-date design configuration using the Platform Designer System file and the Quartus Project File. The Platform Designer also supports Nios V Integrated BSP Editor Mode, which enables side-by-side viewing of loaded Platform Designer system and BSP settings. You can dynamically update available BSP settings based on hardware changes in loaded Platform Designer system.

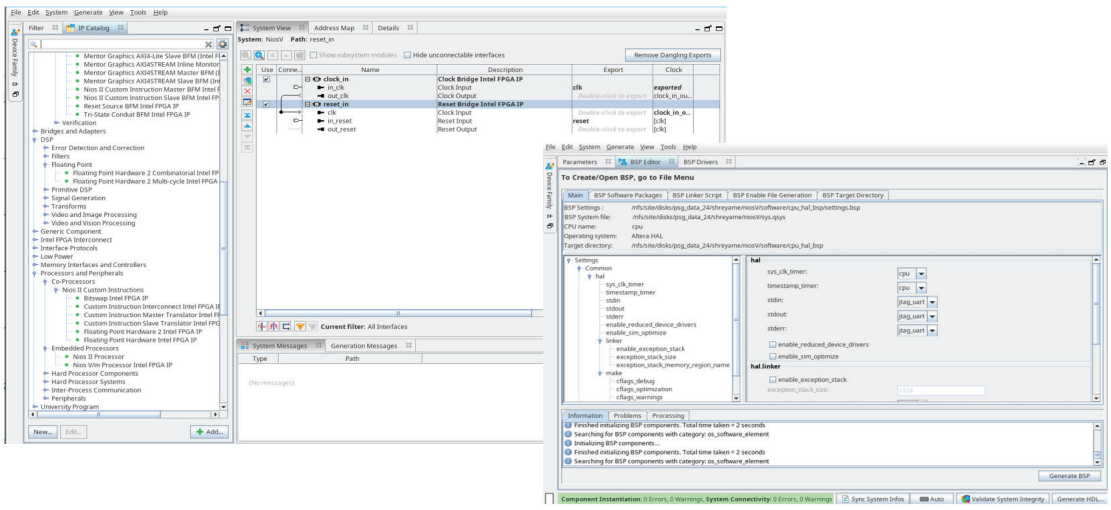


Figure 6. Nios V processor in the Platform Designer

Easy Migration from Nios® II Processor with Continued Intel HAL Support

The Hardware Abstraction Layer serves as a device driver package, providing a consistent interface to the peripherals in your system. Like Nios II processor system, the baremetal HAL drivers are also supported in the Nios V processor system making it easy to migrate designs using Nios II processors to Nios V processors.

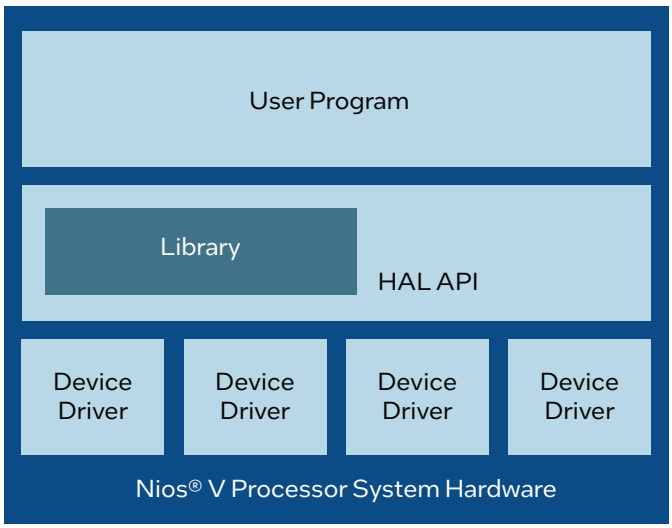


Figure 7. Hardware Abstraction Layer

Ease of Debug with a Unified Development Environment for Soft and Hard Processors

The Ashling RiscFree IDE for Altera® FPGAs is the Integrated unified development environment for creating embedded applications on Altera's Arm* based hard processor system and Nios V soft processors. This IDE delivers homogeneous and heterogeneous multi-processor design, and debug capabilities. Key features include:

- Included with the Quartus Prime Software at no additional cost or available as a standalone free download for embedded software developers
- Full tool-chain including Ashling RiscFree for Altera FPGAs IDE, Compiler, Debugger and Trace for Nios V processors
- Eclipse-CDT based IDE with full source and project creation, editing, build and debug support
- Run-time Debug with support for the FPGA Download Cable II (USB Blaster II)
- Register Visualization for Nios V processors and Arm cores
- Heterogeneous and homogeneous simultaneous multi-core debug support for Arm cores and Nios V processors
- Zephyr debug awareness for Nios V and Arm processors, FreeRTOS and µC/OS-II RTOS debug awareness for Nios V processor
- Full target Linux OS (multi-core/multi-hart) kernel, device driver and application debug support
- Real-time trace (on-chip and off-chip) support for both Nios V processors and Arm cores

It's All About the Ecosystem

A very important RISC-V benefit has been a rapid emergence of a broad, open-source ecosystem. The open-source nature of RISC-V is enabling a new era of processor innovation through open standard collaboration. Multiple participants are fostering implementation innovation, resulting in the rapid emergence of a broad, open-source ecosystem that includes sophisticated hardware design and verification tools, a rich suite of software development tools, operating system (OS) and real-time OS (RTOS) ports.

From the bare metal Intel HAL and uC/OS-II operating system to FreeRTOS, Zephyr and more in the future, Nios V processor provides access to the latest and up-to-date open source and commercial debuggers, IDEs and Operating systems from the ecosystem that are readily available for RISC-V processors.

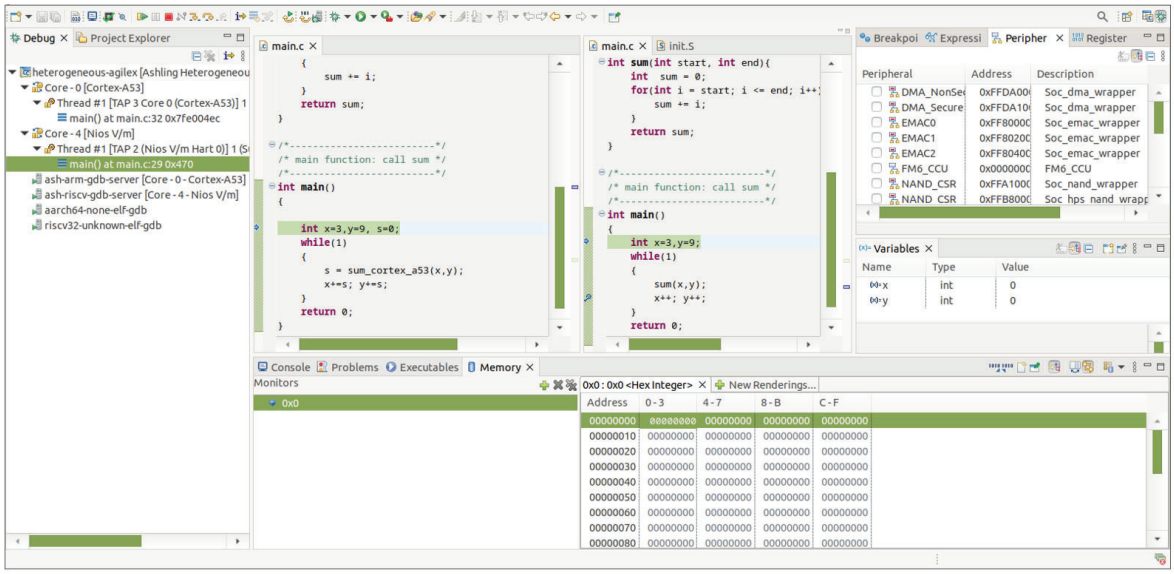


Figure 8. Different Cores, One Solution – Ashling RiscFree IDE for Altera FPGAs

Conclusion

Nios V processors in Agilex 5 FPGAs and SoCs address the real time application needs for embedded markets. With familiar development tools and flows, it is easy to create the processor and peripheral subsystem in Agilex 5 FPGAs thereby increasing productivity. Using the unified development and debugging tools such as the Ashling RiscFree IDE for Altera FPGAs, it is easy to debug complex heterogeneous embedded applications involving the soft RISC-V and hard Arm cores in Agilex 5 FPGAs, thus reducing the overall time to market.

Learn More

- Visit the Nios V processor web page to learn more about Nios V processor and the Ashling RiscFree IDE
- Read the Nios V processor documentation to get started
- Get the Nios V processor IP license from the Self-Service Licensing Center at no cost.
- Download the latest Quartus Prime Pro Edition Software and get started today.

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