Architecture Brief

FPGA and SoC

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Agilex™ 5 FPGAs: Hard Processor Subsystem and Embedded Software

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Introduction

The new Agilex™ 5 device family offers SoC FPGAs with improved performance and reduced power consumption to address the range of embedded and edge-of-the-network applications across many markets including industrial, automation, wireline/wireless, test and medical.

Agilex 5 SoC FPGAs provide higher performance and lower total power consumption by leveraging key innovations and techniques include:

- Intel® 7 process technology
- Second generation Hyperflex® FPGA architecture
- High level of system integration
- Selective power reduction techniques

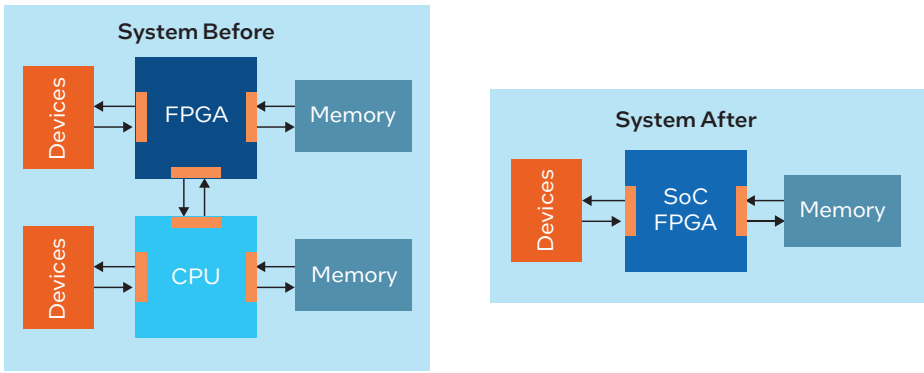


Figure 1. SoC FPGA Value

As shown in Figure 1, SoC FPGAs integrate both processor and FPGA architectures into a single device. Consequently, they provide higher integration, lower power, smaller board size, and higher bandwidth communication between the processor and FPGA. They further include a rich set of peripherals, on-chip memory, an FPGA-style logic array, and high-speed transceivers.

With the Agilex 5 device family, Altera drives power, cost, and performance to the next level, establishing a leadership position in the embedded marketplace.

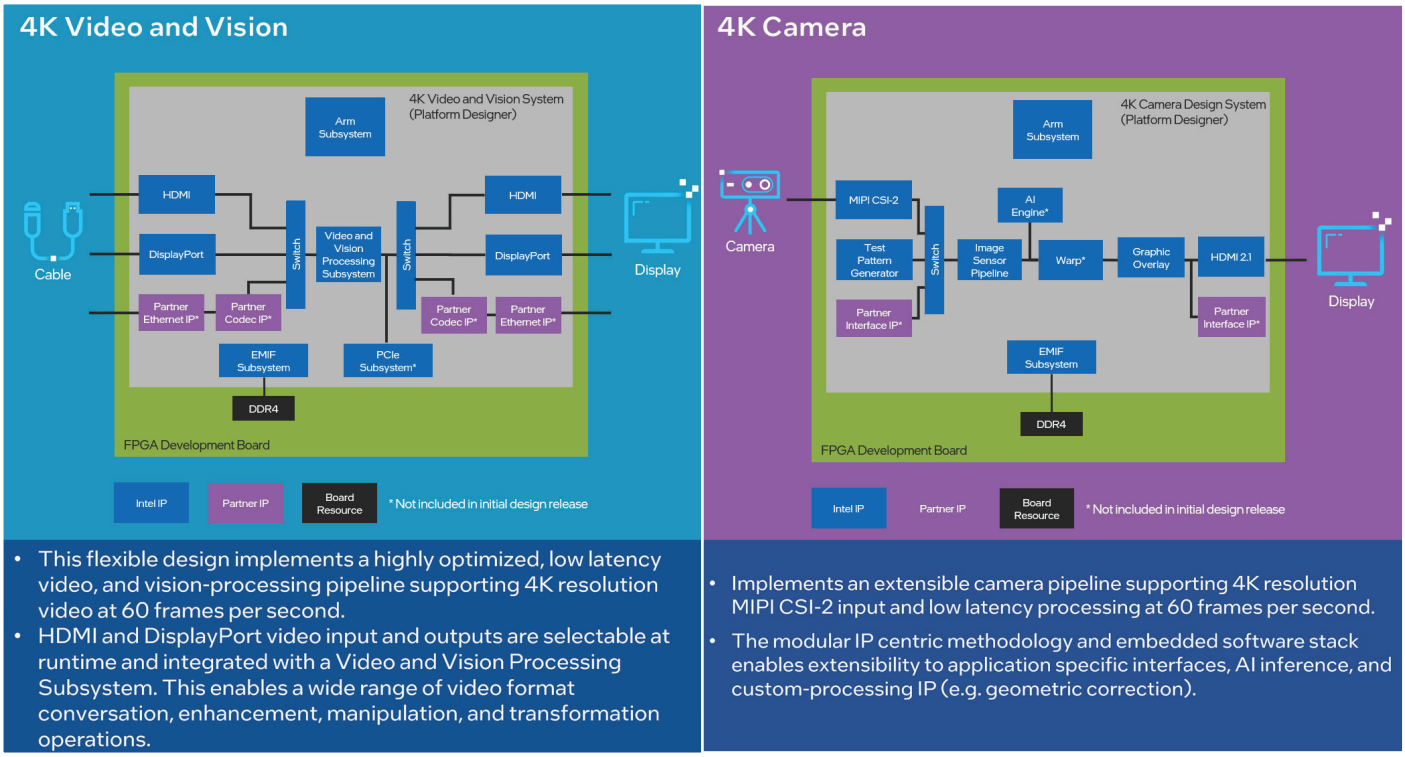
This product family is uniquely suited to fit in to edge-of-the-network applications in various vertical markets through features including lower power and higher performance. The Agilex 5 device family includes a multicore Arm* offering, along with a wide density range (up to 650 KLEs) offered to suit different applications.

Advanced security features will be enabled through the Secure Device Manager (SDM). In addition, the Agilex 5 device family is the first edge-optimized FPGA that includes enhanced digital signal processing (DSP) with AI Tensor Block.

Altera offers two major variants in the Agilex 5 FPGA E-Series product family: E-Series Device Group A FPGAs and E-Series Device Group B FPGAs. The E-Series Device Group B FPGAs offer up to 50% reduction in power compared with Cyclone® V FPGAs using the same fmax. Optionally you can have up to 2.5X performance increase while maintaining the same power budget or up to 2.5X the fabric performance than of Cyclone V FPGAs. E-Series Device Group A FPGAs will offer up to 39% lower total power or up to 1.3X fabric performance when compared to Arria® 10 FPGAs.

The Agilex 5 device fabric performance enables higher fmax and fabric speed enables higher rate video processing with resource-optimized intellectual property (IP). High-performance Arm CPUs allow for extended processing and/or control aspects.

Figure 2 and Figure 3 show the Agilex 5 device-based use cases for Video & Vision and Industrial applications.



- This flexible design implements a highly optimized, low latency video, and vision-processing pipeline supporting 4K resolution video at 60 frames per second.
- HDMI and DisplayPort video input and outputs are selectable at runtime and integrated with a Video and Vision Processing Subsystem. This enables a wide range of video format conversation, enhancement, manipulation, and transformation operations.

- Implements an extensible camera pipeline supporting 4K resolution MIPI CSI-2 input and low latency processing at 60 frames per second.
- The modular IP centric methodology and embedded software stack enables extensibility to application specific interfaces, AI inference, and custom-processing IP (e.g. geometric correction).

Figure 2. Agilex 5 Device Vision Solutions

The Agilex 5 device family targets excel in both video and vision applications. Altera's IP and design examples allow you to develop a very broad range of designs across many markets.

Key features to highlight in Figure 2 include:

- Connectivity IP
- HDMI v2.1
- DisplayPort v1.4 and v2.0
- Integrated MIPI (new in Agilex 5 device)
- Video processing IP, including ACI-based IP Suite with image scaler, warp engine, color space conversion, 2D FIR filter, and Clipper

Altera has long demonstrated the value of FPGA in high-performance, deterministic drive control, industrial functional safety, and higher-level Programmable Logic Controllers (PLCs). With the higher performance Agilex 5 SoC FPGAs, Altera builds on these foundational value propositions starting from Drive-on-Chip to encompass static and mobile Robot-on-Chip solutions.

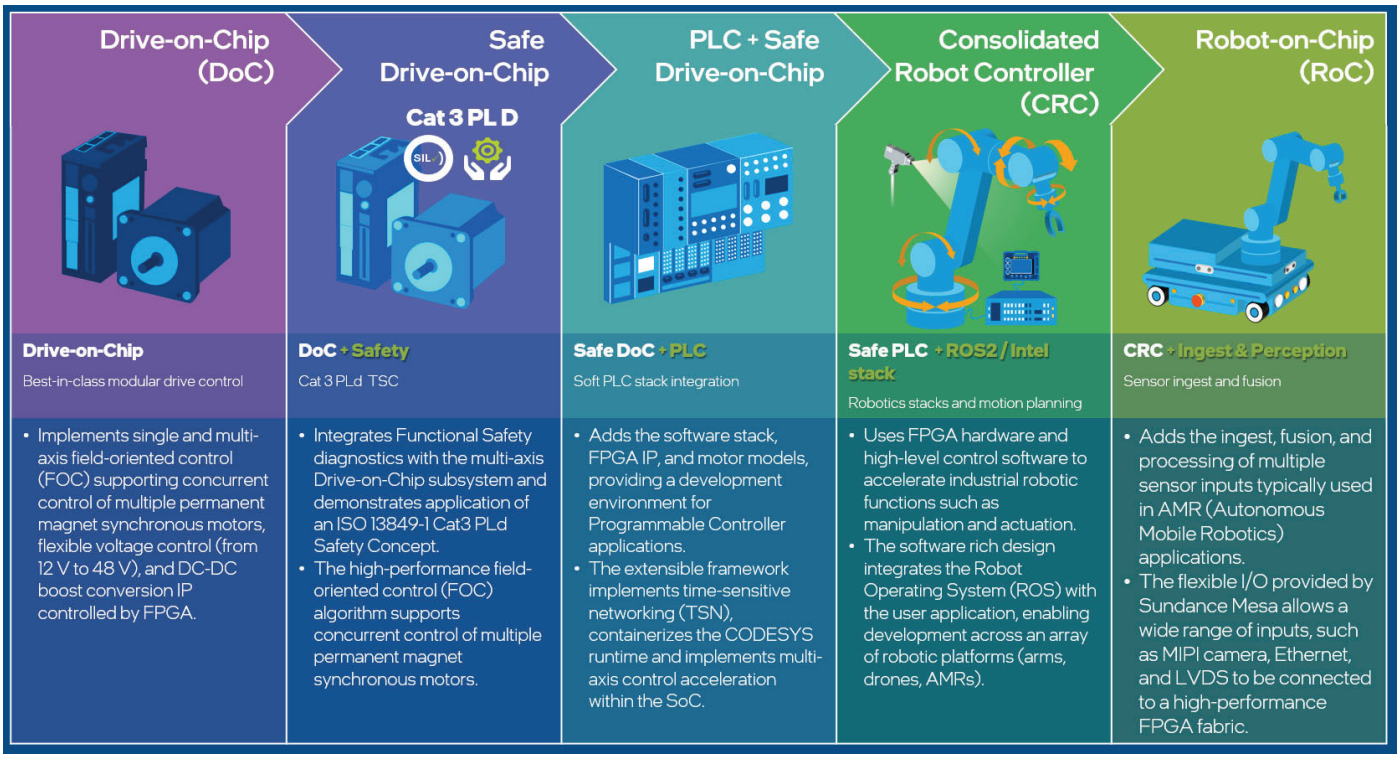


Figure 3. Agilex 5 Device Industrial Solutions

Agilex 5 FPGA Hard Processor Subsystem

The Agilex 5 FPGA Hard Processor Subsystem (HPS) gets significant uplift versus the prior architectures of the Stratix® 10 and Agilex device series. Agilex 5 FPGA upgrades from the Arm Cortex-A53 Quad-core processor to an Arm v8.2-A architecture, including both Arm Cortex-A76 core and Arm Cortex-A55 core CPUs, providing a modernization from the current Arm v8-A architecture. This approach allows for a mix and match of core types using Arm's DynamIQ technology. These CPUs operate with the DynamIQ Shared Unit (DSU) to create a four-core cluster that allows the CPUs to run asynchronously to each other, giving a wider range of performance options. The microprocessor unit (MPU) complex leverages a Network-on-Chip (NoC) to allow sharing of peripheral components and external DRAM interfaces. The Secure Device Manager interfaces to the HPS system using existing interfaces such as the Agilex SoC FPGA products.

The choice of the Arm Cortex-A76 core and Arm Cortex-A55 core combination provides the broadest spectrum of enabling customer choice between power efficiency and performance, along with enabling core isolation to a software thread, partitioning different tasks allocated to independent cores. An upgrade, all cores have dedicated L2 cache and unified L3 cache. Half or all the L3 cache can be powered down. For example, >1MB L3 cache may not have significant impact when using two Arm Cortex-A55 cores, so 1MB could be powered off.

Arm Cortex-A76 core is a major upgrade compared with the Arm Cortex-A72 core with more pipelining stages, private L2, and shared L3 cache. Each Arm Cortex-A76 core has its own set of power connections.

You have the option to choose. If only the Arm Cortex-A55 core is required, you can tie the power connections to the same one, the microprocessor unit and peripheral subsystem all together, and tie the Arm Cortex-A76 core to ground so that they will not operate at all. This method saves both dynamic and static power.

For other customers that need more performance, an Arm Cortex-A76 core could be tied to a power connection and leave the other core tied to ground, giving them the performance at the desired power consumption.

Figure 4 shows the Agilex 5 FPGA HPS and dual IO96B Multi-Ported Front End (MPFE). It consists of the following blocks:

- MPU: Microprocessor Unit contains the Arm Cortex processors and the DynamIQ Shared Unit
- APS: The Application Processor System contains the Cache Coherency Unit (CCU), I/O Coherent Fabric Bridge,Generic Interrupt Controller, System MMU-TCU, and OCRAM.
- PSS: The Peripheral Subsystem contains the PSI interface to the SDM, the H2F Bridge, the Light Weight H2F Bridge, the PSS NoC, and all the peripherals.
- MPFE: The Multi-Ported Front End provides an interface to SDRAM from both the fabric and the HPS.

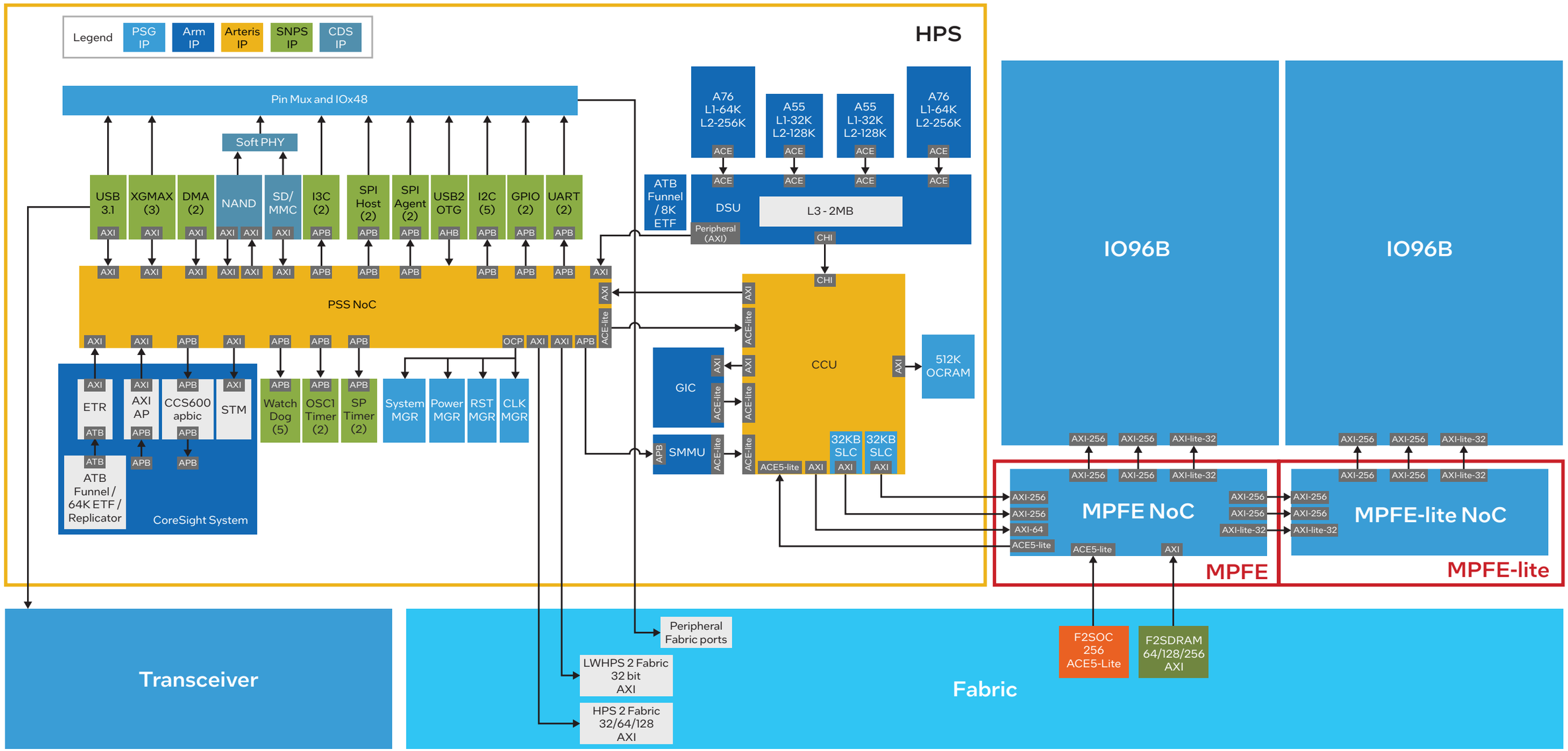


Figure 4. Agilex 5 FPGA HPS Architecture

Upgraded Microprocessor Unit (MPU)

The MPU implements the following features:

Dual Arm Cortex-A76

- Targeted for up to 1.8 GHz operation
- 64K L1 I-Cache and 64K private L1 D-Cache per core
- 256K Shared L2-Cache per core

Dual Arm Cortex-A55

- Targeted for up to 1.5 GHz operation
- 32K L1 I-Cache and 32K L1 D-Cache per core
- 128K Shared L2-Cache per core

Arm DynamIQ Shared Unit (DSU)

- Snoop Control Unit (SCU) for full coherency among cores
- CoreSight debug and trace
- One CHI-B Memory Interface Port
  - Supports stashing into L1, L2, and L3 caches
- Peripheral port for lower latency access to peripheral subsystem (PSS)
- 2 MB L3 cache

Upgraded Application Processor Subsystem (APS)

Cache Coherent Unit

- Manages I/O coherency with fabric accesses to SDRAM
- 2x 32 KB System Level Cache (SLC)
- Used to support atomic CHI commands
- ACE5-lite port from fabric and CHI.B port to DSU supports direct allocation from fabric into L1, L2, and L3 caches using new command types

Arm Cortex GIC-600 for Interrupt Support

- Supports upgraded GIC V3 architecture
- Placed in APS to reduce latency to memory
- ACE-lite host port to support Interrupt Translation Service (ITS)

Arm Cortex MMU-600 for System MMU Support

- Supports SMMU architecture V3.1
- Distributed microarchitecture for flexible implementation options
- Two-stage translation process to support multiple virtual machines
- ACE-lite host port for page table walks and distributed virtual memory

512 KB of On-chip RAM (OCRAM)

- A mini-FlexNoc has been added between the NoC and OCRAM to support the exclusive monitors and firewalls
- 512 KB OCRAM is upgrade from 256 KB OCRAM on Stratix 10 FPGA or Agilex FPGA

Upgraded Peripheral Subsystem (PSS)

Agilex 5 FPGA HPS supports new features such as Time Sensitive Networking (TSN), USB 3.1, and I3C. The NAND and SD/MMC controllers are upgraded to support newer versions of the associated protocol specifications. System-level IP such as the GIC, System MMU, and direct memory access (DMA) controller are also upgraded to the latest versions, as well as MIPI I3C controllers. The MPFE is upgraded to support either a single IO96B or dual IO96Bs.

USB 3.1 Gen1 Controller

- Supports both Device and Host controller modes
- USB 3.1 and USB2.0 interfaces must both be configured as either device or host, mixing modes is not supported
- Supports up to 5Gbps when configured for USB 3.1 gen1 and interfaced with transceiver
- Supports up to 480Mbps when configured for USB2.0

Three Gigabit Ethernet Media Access Controller (xGMAC) Controllers

- Supports TSN endpoint functionality compliant to IEEE 802.1Qav, Qbv, Qbu, Qbr, and IEEE 802.1AS
- Supports 2.5G interface when used with transceiver macro
- Supports 1G/100M/10M when used with HPS or fabric I/O pads

Two I3C Controllers

- One configured as primary host
- One configured as a secondary host
- Hardware-assisted device role switching

Two DMA Controllers

- Four channels each
- Each DMA controller can be configured for secure or non-secure access to HPS resources.

One NAND Controller

- Compatible with the ONFI 1.x, 2.x, 3.x, and 4.1 specifications
- Compatible with toggle 1.x and 2.x specification
- HPS I/O supports SDR, NV-DDR, and NV-DDR2 protocols up to 200 MT/s

One SD/eMMC Controller

- Supports SD devices up to V6.1
- Supports SDIO devices up to V4.1
- Supports SD/eMMC devices up to V5.1

Upgraded CoreSight Debug and Trace System

The Arm CoreSight debug and trace system is built on top of the debug and trace system that was developed for the Stratix 10 FPGA or Agilex FPGA HPS. However, there are a few key changes made to support the higher speed cores and to refresh the debug and trace IP.

CoreSight IP Upgrade

CoreSight SoC-600 Debug and Trace IP replaces the older CoreSight SoC-400 Debug and Trace IP used on the HPS for Stratix 10 FPGA and Agilex FPGA. The newer SoC-600 release includes feature upgrades, fixes, and improvements.

Debug APB

The CoreSight debug APB bus connects to CoreSight debug IP via APB interconnects and includes ROM tables for auto topology detection.

The debug APB also connects to the FPGA fabric to allow soft debug IP connections from the CoreSight debug system.

Trace

A core-specific Embedded Trace FIFO (ETF) is added with 8 KB of RAM within the MPU running at DSU clock frequency. This FIFO will buffer trace messages generated at the MPU clock frequency and hold them as they are transferred to the centralized FIFO.

Increased the centralized ETF size to 64 KB of RAM (from 32KB in Stratix 10 FPGA or Agilex FPGA HPS).

A CoreSight trace AMBA Trace Bus from the fabric is provided for soft trace IP connection to the CoreSight trace system. This allows soft IP trace from the fabric to be routed to the HPS to take advantage of the CoreSight trace IP.

Triggers

The same basic cross triggers on the Stratix 10 FPGA or Agilex FPGA HPS is connected to the same Cross Trigger Interface. Minor changes will be made to support the new CoreSight SoC-600 Cross Trigger IP.

Hardware events from within the fabric can connect to the System Trace Module to allow fabric soft logic signals to trigger System Trace Module trace messages.

ATB SYNCREQ was added to allow a fabric trigger event to cause trace synchronization event.

Upgraded Multi-ported Front End (MPFE and MPFE-lite)

To facilitate sharing access between user soft fabric logic and Hard Processor Subsystem to a common hard memory controller, Agilex 5 FPGA integrates a Multi-Port Front End (MPFE). The MPFE block allows the HPS and user FPGA logic to share access to external SDRAM. It is made up of the MPFE NoC, the FPGA Initiator bridge, and the Translation Buffer Unit and fabric bypass wires. Note that there is no more HMC adapter, error correction code (ECC) is handled by the IO96B. The MPFE NoC arbitrates memory access from multiple ports. The Agilex 5 FPGA MPFE communicates to IO96B using AXI protocol.

- MPFE supports 1 or 2 IO96B
- Configurable 256/128/64-bit AXI4 interface from fabric host for non-shared SDRAM accesses
- A 256-bit I/O ACE5-lite interface from fabric host for shared (both coherent and non-coherent) SDRAM and HPS peripheral accesses

Upgraded Time Sensitive Networking (TSN)

TSN is an enhancement to Ethernet to enable reliable and deterministic delivery of data. This is something that standard Ethernet was not previously able to achieve and allows it to be used for time-sensitive applications.

The key features supported by TSN are time synchronization between network elements, traffic shaping enabling the timely delivery of packets, and mechanisms for reliability and system configuration. TSN allows all types of traffic to exist on the same network.

Altera works with a range of partners, consortia, and standards bodies to ensure interoperability and industry best practice in implementation for each market. Some of the critical ones include IEEE, IEC, OPC foundation, AVNU and IETF, defining standards, profiles and use-cases, higher-level protocols and conformance testing standards and programs.

Key Interfaces

The following key interfaces are supported for fabric to MPFE, HPS to MPFE, and MPFE to HPS.

FPGA-to-SDRAM Bridge (F2SDRAM)

256/128/64-bit AXI4 port providing direct access from fabric to SDRAM. Provides fabric access to all SDRAM channels with lower latency than F2SOC but does not support coherency with the HPS. This port supports the isolation of TSN related data flows from other fabric data flows to prevent latency increases in TSN data flows due to high traffic.

FPGA-to-HPS Bridge (F2H)

A 256-bit ACE5-lite port provides access from fabric to HPS peripherals, OCRAM or both coherent and non-coherent accesses to SDRAM. The F2H supports direct allocation into the core's L1 and L2 caches as well as the DSU's L3 cache. The F2H also provides a pathway for the PCIe interrupt translation service (ITS) provided by the GIC-600.

HPS-to-FPGA Bridge (H2F)

A 128/64/32-bit AXI4 port from HPS to fabric for high-bandwidth access. Intended to be used for large data movement to/from the fabric that is initiated by the HPS. Supports up to 256 GB address space at up to 6.4 GB/s. Ready latency is implemented as part of the AXI pipeline block.

Lightweight HPS-to-FPGA Bridge (LWH2F)

A 32-bit AXI4 port from HPS to fabric for low bandwidth access to soft IP control and status registers. Supports up to 512 MB address space at up to 1.6 GB/s.

Power Management

The HPS implements the following power management techniques.

Clock Gating

Static Clock Gating

- The HPS Clock Manager implements clock gates on many of the branches of the clock tree so that clocks to IP can be disabled. These clock gates disable clocks by default, requiring the user software to enable clocks to any IP needed by their application.
- Clock gates are opened before releasing reset to a peripheral so that proper reset of the peripheral is achieved.

Dynamic Clock Gating

The Arm Cortex-A76 and Cortex-A55 cores offer dynamic clock gating. The Wait for Interrupt (WFI) and Wait for Event (WFE) are features of Arm 8A architecture that put the core in a low-power standby mode by architecturally disabling the clock at the top of the clock tree. The cores are fully powered and retain state during WFI and WFE.

Power Islands and Power Gating

Static Power Gating

The HPS supports five statically controllable power domains in the MPU.

- Two A55
- One A76
- The other A76
- One-half of the L3 cache
- Other half of L3 cache

These cores have individual power bumps, which can either be tied to HPS supply voltage or to ground, thus enabling the customer to tradeoff between power and performance.

Agilex 5 FPGA Software Development

Altera's Arm-based SoC FPGAs inherit the rich software development ecosystem, available for the Arm Cortex-A55 and -A76 processors employed in Agilex 5 FPGA device, including software development tools and operating systems. This ecosystem compatibility ensures that software developers can remain productive using familiar tools and reuse legacy software to shorten the development cycle. The software development process for Altera SoC FPGAs follows the same steps as other SoCs. Altera and its ecosystem partners provide tool choices for each step of the process, from board bring-up, to building Linux kernels, to debugging application software.

Altera has developed comprehensive operating system (OS) support including Linux and real-time operating systems. Using Intel Yocto Project reference Linux kernel or board support packages for other operating systems, like Zephyr RTOS, software engineers can start OS-based application development immediately.

Accelerating Software Development - Concurrent Software and Hardware Development

Device-specific firmware and software development can begin on the Agilex 5 FPGA Simics Virtual Platform. The Simics Virtual Platform is a fast, host-based functional simulation of a target development system. It functions like a complete development board that runs on a workstation. The Agilex 5 FPGA Virtual Platform (SM VP) enables a "shift-left" for software development on Agilex 5 FPGA, months before Agilex 5 FPGA hardware is available ensuring high quality software availability as hardware becomes available.

Binary-compatible and register-compatible with the real hardware that it simulates, the Agilex 5 FPGA Virtual Platform enables the development of device-specific production software, which can run unmodified on real hardware. Virtual platforms provide an unparalleled level of full-system visibility and control for software development. With the use of a virtual platform, software development can begin well in advance of hardware availability and continue to make software teams more productive even after SoC FPGAs are available.

Embedded Software Leadership

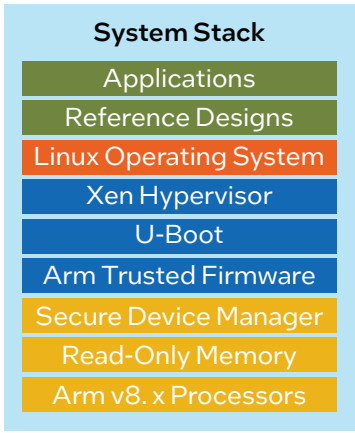


Figure 5. Typical Embedded System stack

From a hardware perspective, the Agilex 5 FPGAhas a cluster of Arm Cortex v8.2-A processors for application processing. ROM code built into the device is responsible for the initial bootup. Serving as the central command center for the Agilex 5 FPGA, the Secure Device Manager (SDM) controls key operations, such as configuration, device security, single event upset responses, and power management.

From a software perspective, Arm Trusted Firmware (ATF) implements the secure monitor firmware layer. Second Stage Bootloader for open-source software. This is typically the U-Boot. The second stage bootloader will boot Linux operating system. Xen, a type-1 hypervisor, provides services that allow multiple operating systems to execute on the same hardware concurrently. Regarding the Linux operating system, Altera supports and maintains the latest versions of both Long-Term Support (LTS) and Mainline Linux kernels. On top of the operating system, customer can access supported and maintained reference designs comprising of both software and hardware to accelerate their product development process.

Embedded Software Benefits

Today the main enablement for all Altera SoC FPGAs is open-source software. Open-source software includes Linux Kernels, Bootloaders, Yocto Project to build custom Linux distributions, and Zephyr RTOS.

An important element of Altera's open-source software strategy is "Upstream First". Upstreaming ensures that Altera's open-source software is in kernel.org and denx.de even before silicon availability. In addition, it ensures that Altera's embedded software is on the latest version, enabling our customers with up-to-date features, bug fixes, and security patches. Another benefit of upstreaming is that all our code that is upstreamed is maintained and supported by the open-source project developers.

Altera has a unique, differentiated solution. First, Altera keeps up with the Linux community's latest stable kernel release. The mainline kernel is upgraded every 2 to 3 months against every new kernel.org release. As Altera is the maintainer for the SoC FPGA architecture, and upstreams code to kernel.org, moving the SoC FPGAs to the latest stable kernel is accomplished in a few days.

Second, Altera maintains the LTS kernel for the SoC FPGA portfolio. The customer benefits of a Linux LTS kernel for the SoC FPGAs include a stable code base for more than 24 months. Bug fixes, security patches, and new features backported from latest stable kernel. One additional benefit of the LTS kernel for Altera's SoCs is the seamless transition to commercial Linux vendors. Wind River Linux employs the LTS kernel in Wind River's commercial Linux products.

Third, Linux drivers for SoC FPGAs are very high quality. SoC FPGA hard IP, acquired from EDA vendors like Synopsis and Cadence, employ community Linux drivers. These Linux drivers are used by many SoC vendors. Consequently, these drivers have more support, more developers refining and maintaining these drivers, and are therefore higher quality than Altera's competition that employs proprietary hard IP and associated Linux drivers.

In addition to a choice of Linux kernels and distributions, Altera offers customers more software component choices. Choice of Bootloaders; U-Boot, Arm Trusted Firmware. Choice of Reference Designs, to accelerate customer's product development, some examples include Golden Hardware Design and Partial Reconfiguration.

In addition to Linux, Altera and the open-source community support and maintain the Zephyr Real Time Operating System (RTOS) port for Agilex 5 FPGA. Like Linux, Zephyr RTOS is a Linux Foundation open-source project that strives to deliver RTOS for connected, resource-constrained devices, built to be secure and safe. Zephyr is available through the Apache 2.0 open-source license. Zephyr has a highly modular software structure; all device drivers are enabled via device tree and all features are configurable via DEFCONFIG file.

Standard Software Development and debugging via Arm Development Studio for SoC FPGA, an industry standard tool at a "value" price point. In addition, Ashling* RiscFree* IDE for FPGAs, a free IDE that offers heterogeneous debug on Arm and Nios® V processors.

Altera also invests in advanced Crypto Services, like Vendor Authorized Boot and Secure Device Object Services built on the Secure Device Manager. In addition, Altera offers a comprehensive ecosystem covering operating systems, tools, and hardware.

With embedded software and tools, Altera builds robust, scalable, and quality platforms based on open source and industry-standard technologies.

Agilex 5 FPGA Embedded Software Scope

Agilex 5 FPGA HPS embedded software scope supports:

1. Boot Linux operating system in symmetric multi-processor mode
   - Using U-Boot as bootloader
   - Using ATF (ATF BL31) as secure runtime
2. Boot Linux operating system in symmetric multi-processor mode
   - Using ATF (ATF BL2 as FBSL) as bootloader
   - Using ATF (ATF BL31) as secure runtime
3. Boot Zephyr real-time operating system in symmetric multi-processor mode
   - Using ATF (ATF BL2 as FSBL) as bootloader
   - Using ATF (ATF BL31) as secure runtime
4. Boot Hypervisor on main CPU core and launch Linux/Zephyr Guest OS on secondary CPU core.
   - Using U-Boot as bootloader
   - Using ATF (ATF BL31) as secure runtime
   - Virtualization is achieved via Xen hypervisor

Reset and Boot Flow

Agilex 5 SoC boot flow is separated to multiple stages:

- Power-on reset
- SoC FPGA configuration and HPS first stage boot
- HPS second stage boot
- HPS operating system boot
- FPGA core configuration (HPS boot first only)

There are two booting methods for SoC FPGA configuration:

- FPGA boot first
- HPS boot first

Altera provides U-Boot and ATF, (BL2 and BL31) as HPS bootloader to boot to the operating system. Altera provides both Linux and Zephyr RTOS support for Agilex 5 FPGA. ATF BL31, a part of secondary stage bootloader, is also the secure monitor firmware running at Arm EL3 level to control the access from the operating system to privilege access. For example, the SDM mailbox and secure register.

Agilex 5 FPGA Boot Flow: FPGA Boot First

As demonstrated in Figure 6, in the FPGA boot first method, the SDM fully configures the FPGA, then configures the HPS SDRAM pins, loads the HPS first-stage bootloader (FSBL) into HPS OCRAM and takes the HPS boot core out of reset. The FPGA and all the I/Os are fully configured before the HPS is released from reset. Thus, when the HPS boots, the FPGA is in user mode and is ready to interact with the HPS.

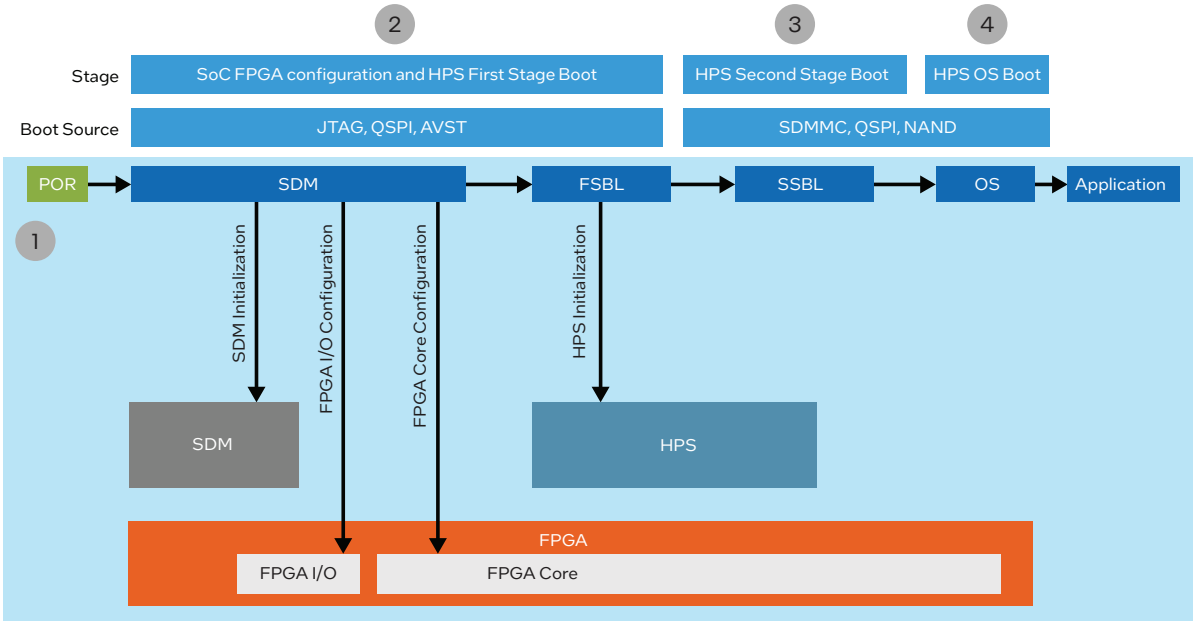


Figure 6. FPGA Boot First

Agilex 5 FPGA Boot Flow: HPS Boot First

In the HPS Boot First method (Figure 7), the SDM first configures the HPS SDRAM pins, loads the HPS FSBL into HPS OCRAM, and takes the HPS boot core out of reset. Then the HPS configures the FPGA I/O and FPGA fabric later. This mode is also referred to as Early I/O Release Mode or Early I/O Configuration. After power-on, the device configures a minimal amount of I/O required by the HPS before releasing the HPS from reset. This mode allows the HPS to boot quickly without having to wait for the full configuration to complete. Subsequently, the HPS may trigger an FPGA configuration request during the Second Stage Bootloader or OS stage.

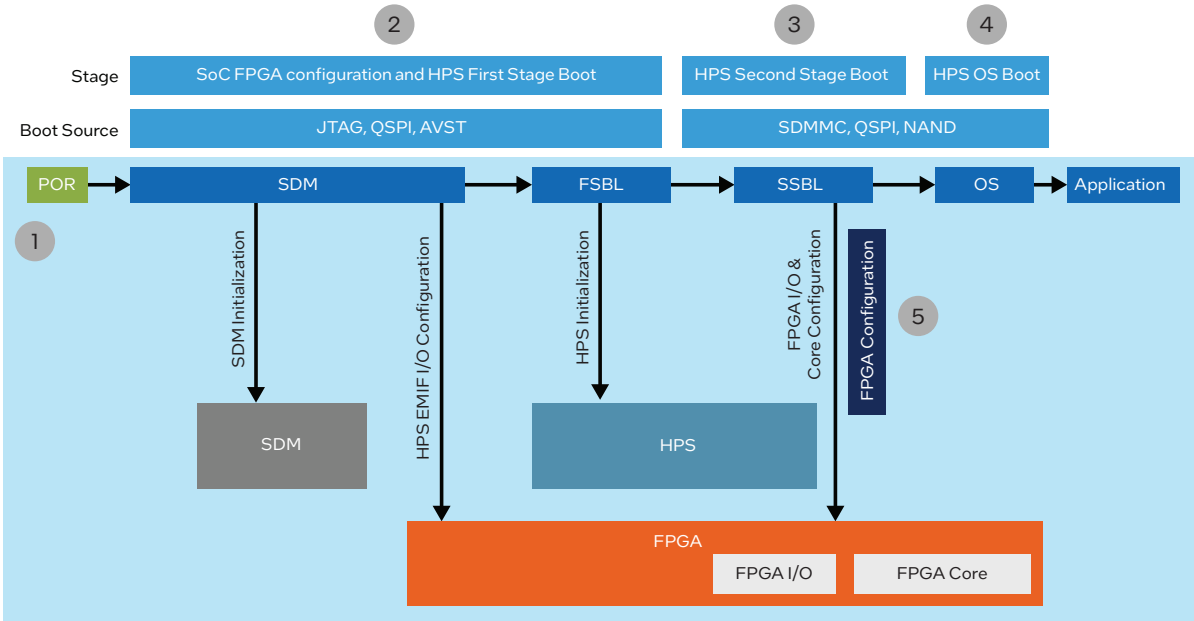


Figure 7. HPS Boot First

Table 1 describes the bootloader boot to OS flow within HPS. The HPS boot flow is the same in both FPGA boot first and HPS boot first SoC FPGA configuration boot flow.

Use Case / Boot Flow	Agilex™ 7 FPGA	Agilex™ 5 FPGA
U-Boot SPL -> U-Boot -> Linux	YES	NO
U-Boot SPL -> ATF BL31 -> U-Boot -> Linux	YES	YES
U-Boot SPL -> ATF BL31 -> U-Boot -> Linux (U-Boot VAB enabled)	YES	YES
ATF BL2 -> ATF BL31 -> UEFI -> Linux	YES	NO
ATF BL2 -> ATF BL31 -> Linux	NO	YES
ATF BL2 -> ATF BL31 -> Zephyr	NO	YES
ATF BL2 VAB enabled	NO	YES

Table 1. Boot to Operating System

Agilex 5 FPGA U-Boot, ATF Linux Boot

Figure 8 shows the high-level Agilex 5 FPGA HPS OS boot flow using U-Boot as HPS bootloader to boot to Linux. This is the typical flow used by most users. The flow is like the Stratix 10 and Agilex SoC user flow:

1. Configuration management firmware (CMF) running on SDM will load the FSBL, which is the U-Boot SPL into HPS OCRAM then bring HPS boot core out from reset.

2. U-Boot SPL load SSBL, which is ATF BL31 and U-Boot proper (SSBL) into DDR.

3. U-Boot SPL jump to ATF BL31.

4. ATF BL31 set up EL3 environment and initialize PSCI services.

5. ATF BL31 jump to U-Boot proper.

6. U-Boot proper load Linux into DDR.

7. U-Boot jump to Linux.

8. U-Boot proper and Linux can access SDM FPGA features via ATF BL31 through Arm Secure Monitor Call (SMC).

Agilex 5 FPGA ATF Linux Boot

Figure 9 shows the high-level boot flow that directly boots from ATF to Linux. This is the solution for the customer looking for a non-GPL licensed bootloader to boot Linux. This solution replaces the legacy UEFI bootloader supported in Agilex FPGA and previous device families.

1. CMF running on SDM will load the FSBL, which is ATF BL2 into HPS OCRAM then bring HPS boot core out from reset.

2. ATF BL2 load SSBL and OS, which is ATF BL31 and Linux into DDR.

3. ATF BL2 jump to ATF BL31.

4. ATF BL31 set up EL3 environment and initialize Power State Coordination Interface services.

5. ATF BL31 jump to Linux.

6. Linux can access SDM FPGA features via ATF BL31 through Arm Secure Monitor Call (SMC).

This is also the same boot flow for ATF to Zephyr boot.

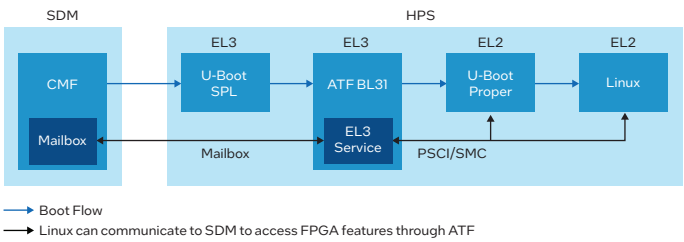


Figure 8. Agilex 5 FPGA U-Boot, ATF Linux Boot Flow

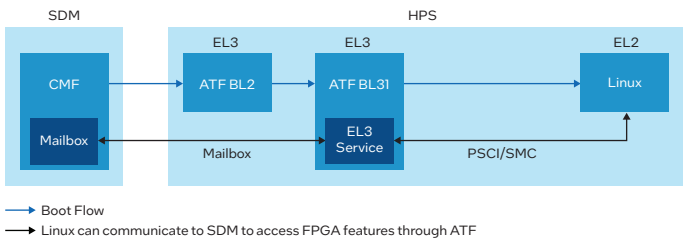


Figure 9. Agilex 5 FPGA ATF Linux Boot Flow

FPGA Partial Reconfiguration

Partial Reconfiguration (PR) allows you to reconfigure a portion of the FPGA dynamically while the remaining FPGA design continues to function. HPS and SDM mailbox handshake are the same for FPGA configuration and PR. The only difference is the bitstream content. FPGA manager is used to send the bitstream to SDM for both FPGA configuration and PR. Table 2 shows the differences between FPGA Configuration and Partial Reconfiguration.

FPGA Configuration	Partial Reconfiguration
Configures entire FPGA fabric	Reconfigures a PR region
Disable and enable bridge before and after sending bitstream.	Freeze and unfreeze PR region before and after sending bitstream.

Table 2. Configuration versus Partial Configuration

FPGA Remote System Update

The Remote System Update (RSU) is a feature available on all Secure Device Manager based FPGAs, which allows you to safely update the configuration bitstreams stored in QSPI flash on deployed target systems.

Industry-Leading Ecosystem Support

Commercial Operating Systems

In addition to Linux and Zephyr RTOS, Altera is planning numerous commercial operating systems ported to Agilex 5 FPGAs.

Commercial Software Development Tools

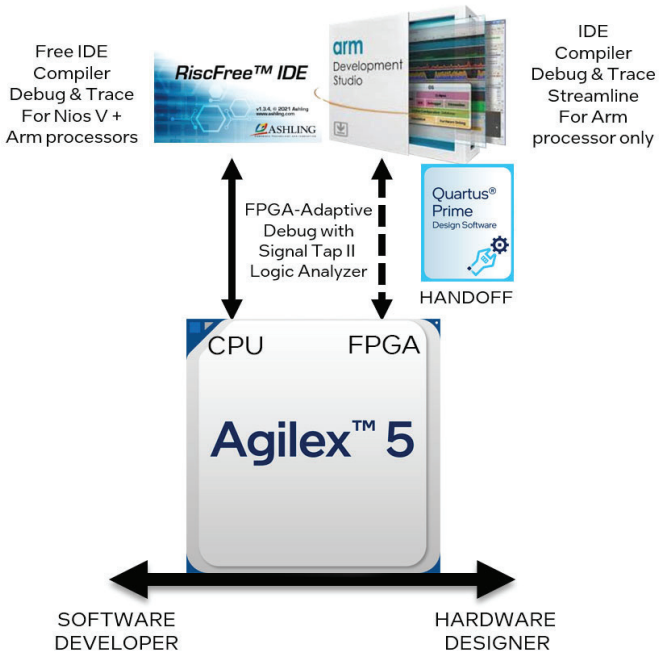


Figure 10. Altera-provided Integrated Development Environments

For software development, Altera provides the Arm Development Studio for SoC FPGAs and the Ashling* RiscFree* IDE for FPGAs (see Figure 10)

RiscFree* IDE for FPGAs

- Compiler, Debug, and Trace for Nios V and Arm processors
- Heterogeneous debug on Nios V and Arm processors
- Free IDE

Arm Development Studio for SoC FPGA

- Continue enabling premium Arm Development Studio for SoC FPGA tools
- Arm industry standard
- Value price point

RocketBoards.org

RocketBoards.org is your first and best resource for open-source software, like U-Boot, ATF, Zephyr, and Linux* operating system used by most customers. RocketBoards.org delivers comprehensive Agilex 5 FPGA documentation on subjects, such as Agilex 5 FPGA SoC Golden System Reference Design, boot flow, development kit, and much more. In addition, information and step by step instructions can be found on supported and maintained Agilex 5 FPGA reference designs, such as the Golden Hardware Reference Design and Partial Reconfiguration reference design.

There is Agilex 5 FPGAs support via the following resources:

- Google searchable >7-year FAQ database on SoC FPGAs
- Community Forum where you can post questions on embedded software
- RocketBoards.org that enables a step-by-step, stress-free, easy-to-navigate workflow
- News blog that is frequently updated with the latest information on our embedded software

Conclusion

The Agilex 5 device family is a powerful class of programmable devices that are applicable to a wide range of embedded applications. Commercially available devices integrate standard Arm processors, either a Cortex-A55 or the more powerful Cortex-A76 processor with a rich set of peripherals, on-chip memory, high-speed internal interconnect architecture, a hierarchy of on-chip memory, and leading-edge FPGA fabric. This brief discusses several criteria to enable you to select Agilex 5 device for your application including system performance, design reliability and flexibility, system cost, power consumption, future product road maps, and the important role that development tools will play in the success of Agilex 5 devices.

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