

Product Marking Information for Intel[®] MAX[®] Series Devices

MAX[®] II, MAX[®] V

Version: **1.0**

Last updated: **April, 2022**



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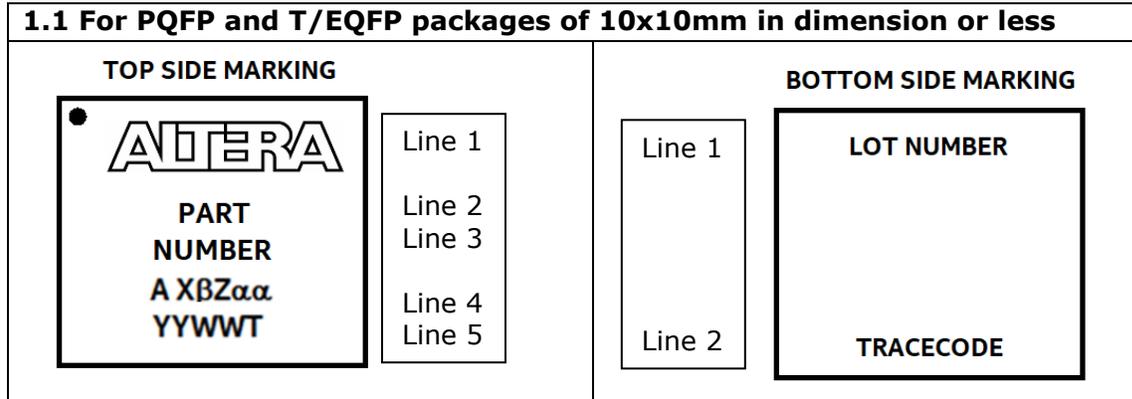
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1.0 Top Mark Layout for Intel MAX II & MAX V Devices

1.1 For PQFP and T/EQFP packages of 10x10mm in dimension or less



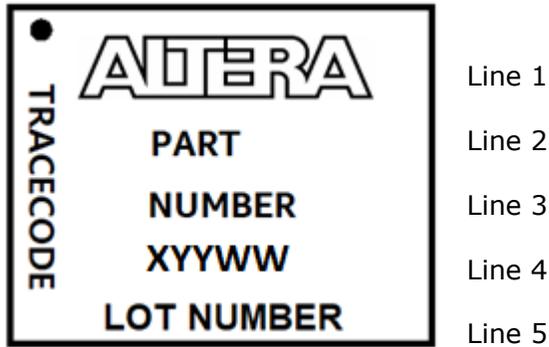
Line 1	Company logo (ALTERA®)
Line 2	Part Number
Line 3	Part Number (continued)
Line 4	Date Code
Line 5	Date Code (continued)
Bottom side marking Line 1	Lot Number
Bottom side marking line 2	Tracecode

Date Code: A Xβ Z αα YYWWT	
A, X, β, Z, αα, T	Manufacturing Identifiers
YYWW	YY = Year, WW = Workweek in a 6-week date code window

Work Week	Date Code
1 - 6	YY01
7 - 12	YY07
13 - 18	YY13
19 - 24	YY19
25 - 30	YY25
31 - 36	YY31
37 - 42	YY37
43 - 48	YY43
49 - 53	YY49



1.2 For MBGA 64,68 and 100 pin count



Line 1	Company logo (ALTERA®)
Line 2	Part Number
Line 3	Part Number (continued)
Line 4	Date Code
Line 5	Lot Number
Left side vertical mark	Tracecode

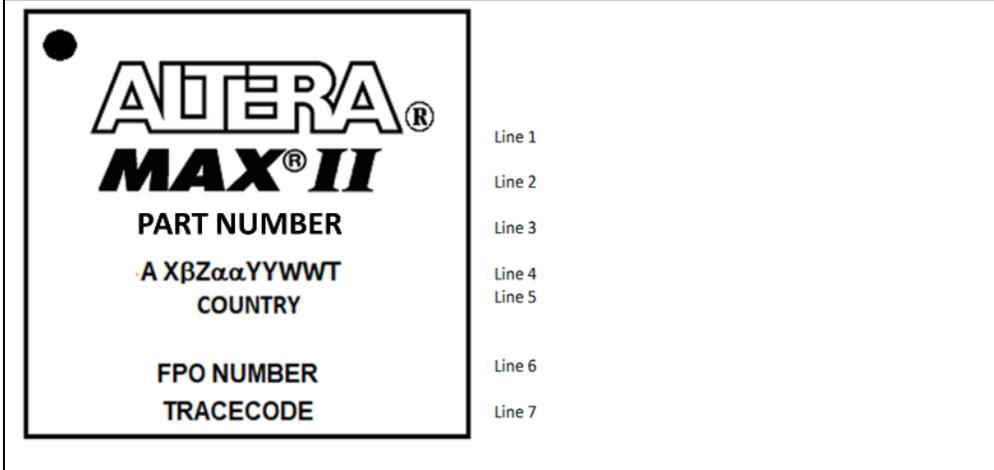
Date Code: CWWYY

X	Manufacturing Identifiers
YYWW	YY = Year, WW = Workweek in a 6-week date code window

Work Week	Date Code
1 - 6	YY01
7 - 12	YY07
13 - 18	YY13
19 - 24	YY19
25 - 30	YY25
31 - 36	YY31
37 - 42	YY37
43 - 48	YY43
49 - 53	YY49



1.3 All other MAX II and MAX V packages and pin count



Line 1	Company logo (ALTERA®)
Line 2	Device Family logo (MAX® II or MAX® V)
Line 3	Part Number
Line 4	Date Code
Line 5	Country of Origin (COO)
Line 6	Top ID* (FPO/Lot#)
Line 7	Top ID* (Tracecode)
*Certain packages (RQFP, EQUAD) will have the Top ID marked in a single line	

Date Code: A Xβ Z αα YYWWT	
A, X, β, Z, αα, T	Manufacturing Identifiers
YYWW	YY = Year, WW = Workweek in a 6-week date code window

Work Week	Date Code
1 - 6	YY01
7 - 12	YY07
13 - 18	YY13
19 - 24	YY19
25 - 30	YY25
31 - 36	YY31
37 - 42	YY37
43 - 48	YY43
49 - 53	YY49



2.0 Document Revision History

Date	Version	Changes
April 2022	1.0	Initial release.