12th Generation Intel® Core™ Desktop Processor and Intel® 600 Series Chipset Family Platform Controller Hub for IoT Platforms

Datasheet Addendum

January 2024

Document Number: 710371-003

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or visit www.intel.com/design/literature.htm.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No product or component can be absolutely secure. Check with your system manufacturer or retailer or learn more at intel.com.

No product or component can be absolutely secure.

Your costs and results may vary.

© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others.

Revision History

Date	Revision	Description
January 2024	003	Chapter 1 “Introduction” - Updated Table 6 “HSIO Details”
March 2022	002	Chapter 2 “Thermal Management” - Updated Table 7 “12th Gen Intel® Core™ Desktop Processor Line and Intel® 600 Series PCH SKU Summary” Chapter 3 “Graphics and Display” - Added Table 12 “PLL Reference Clock (DISP_UTILS_2)” - Added Table 13 “PLL Reference Clock (DISP_UTILS_2)” Chapter 4 “High Speed Input/Output (I/O)” - Added Section 4.3 “Thunderbolt™”
January 2022	001	Initial release.

§ §

<This page is intentionally left blank.>

Contents

List of Figures

List of Tables

1.0 Introduction

This 12th Generation Intel® Core™ Desktop Processor Datasheet Addendum is to be used as supplement documentation that covers IoT-specific features and complements the 12th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2 (RDC#655258) and Intel® 600 Series Chipset Family Platform Controller Hub Datasheet, Volume 1 of 2 (RDC#648364).

12th Generation Intel® Core™ Desktop Processor Datasheet processor is a 64-bit, multi-core processor built on Intel® 7 process technology.

The S-Processor Line offered in a 2-Chip Platform that includes the Processor Die and Platform Controller Hub (Intel® 600 Series Chipset Family Platform Controller Hub) die.

Throughout this document, **12th Gen Processor Datasheet** is used as a general term to refer to the *12th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2 (RDC#655258)* and refers to all SKUs, unless specifically noted otherwise.

Throughout this document, **Intel® 600 Series PCH Datasheet** is used as a general term to refer to the *Intel® 600 Series Chipset Family Platform Controller Hub Datasheet*, *Volume 1 of 2 (RDC#648364)* and refers to all SKUs, unless specifically noted otherwise.

Note: This document serves as a supplementary documentation, please ensure all required specifications from the **12th Gen Processor Datasheet** and **Intel® 600 Series PCH Datasheet** are met prior to using this document, unless specifically noted otherwise.

1.1 Terminology

Table 1. Terminology

Term	Description
AHCI	Advanced Host Controller Interface
ALT	Alternate (DP ALT Mode)
AMT	Active Management Technology
ART	Always Running Timer
AVB	Audio Video Bridging
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BL	Baseline
CAT	Cache Allocation Technology
CLK	Clock
CML	Current-Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DDR	Double Date Rate
DP	DisplayPort
GbE	Gigabit Ethernet
GGTT	Global Graphics Translation Table
GMII	Gigabit Media Independent Interface
GOP	Graphics Output Protocol
GPA	Graphics Performance Analyzers
gPTP	generalized Precision Time Protocol
GT	Graphic Technology
GTT	Graphics Translation Table
GTTMMADR	Graphics Translation Table Memory Mapped Range Address
GuC	Graphic Microcontroller
HBM	High Bandwidth Memory
HDMI	High-Definition Multimedia Interface
HSIO	High Speed Input Output
HW	Hardware
I/O	Input / Output
IEEE	Institute of Electrical and Electronic Engineers
IET	Interspersed Express Traffic
Intel® RDT	Intel® Resource Director Technology
Intel® TCC	Intel® Time Coordinated Computing
KMD	Kernel Mode Driver
LAN	Local Area Network
LGA	Land Grid Array
LLC	Last Level Cache
LMGAW	Local Memory Guest Address Width
LMHAW	Local Memory Host Address Width

Table 1. Terminology

Term	Description
LMTT	Local Memory Translation Table
LRR	Low Refresh Rate
LRR2	Low Refresh Rate 2
MAC	Media-Access Control
MMC	MAC Management Counters
MMIO	Memory-mapped Input/Output
OA	Observation Architecture
PASID	Process Address Space Identifier
PCH-S	Platform Controller Hub-Desktop
PCI	Peripheral Component Interconnect
PCIe*	Peripheral Component Interconnect Express
PCS	Physical Coding Sublayer
PF	Physical Function
PLL	Phase-locked Loop
PWM	Pulse Width Modulation
RCiEP	Root Complex Integrated Endpoint
SATA	Serial Advanced Technology Attachment
SDC	Secondary Data Cache
SGMII	Serial Gigabit Media-Independent Interface
SIOV	Scalable I/O Virtualization
SoC	System on Chip
SRIOV	Single Root I/O Virtualization
STA	Station Management
SW	Software
TBI	Ten-Bit Interface
TDP	Processor Base Power (a.k.a Thermal Design Power)
TGPIO	Time-Aware General Purpose Input Output
TSN	Time-Sensitive Networking
UI	User Interface
UMA	Unified Memory Architecture
USB	Universal Serial Bus
VF	Virtual Functions
VM	Virtual Memory
VMM	Virtual Machine Monitor
VSYNC	Vertical Reference Synchronization
WCET	Worst-Case Execution Time
xHCI	eXtensible Host Controller Interface

1.2 Reference Documents

Table 2. Reference Document

Document	Document No./Location
12th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2	655258
12th Generation Intel® Core™ Processor Datasheet, Volume 2 of 2	655259
Intel® 600 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 1 of 2	648364
Intel® 600 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 2 of 2	680836
Intel® TCC Tools Product Page	https://software.intel.com/content/www/us/en/develop/tools/time-coordinated-computing-tools.html
Intel® 64 and IA-32 Architectures Software Developer's Manual	https://software.intel.com/en-us/articles/intel-sdm

1.3 Supported Package and Die Plan

Table 3. Processor Lines Package and Die Plan

Processor Line Segment	Die Type	Package Type (mm)	TDP	PCH
S (LGA 8+8)	8P + 8E + 1	45 x 37.5	35W	Intel® 600 Series PCH-S
			65W	
S (LGA 8+4)			35W	
			65W	
S (LGA 6+0)	6P + 0E + 1		35W	
			65W	
S (LGA4+0)			35W	
			60W	
S (LGA 2+0)			35W	
			46W	

1.4 Pin List for Ethernet TSN, Time-Aware GPIO and Genlock

Table 4. Pin List Mapping Details

Reference Platform Signal Name/Interface	Package Name	GPIO Native Function	GPIO Native Direction	Package	Pin Map
Ethernet TSN					
SGMII0_TX_DP	PCIE9_TXP	N/A	N/A	PCH	BF30
SGMII0_TX_DN	PCIE9_TXN	N/A	N/A	PCH	BG30
SGMII0_RX_DP	PCIE9_RXP	N/A	N/A	PCH	AT29
SGMII0_RX_DN	PCIE9_RXN	N/A	N/A	PCH	AR29
SGMII1_TX_DP	PCIE10_TXP	N/A	N/A	PCH	BH32
SGMII1_TX_DN	PCIE10_TXN	N/A	N/A	PCH	BJ31

SGMII1_RX_DP	PCIE10_RXP	N/A	N/A	PCH	AW29
SGMII1_RX_DN	PCIE10_RXN	N/A	N/A	PCH	BA29
SGMII_MDC_0	GPP_G3	1	Out	PCH	R53
SGMII_MDIO_0	GPP_G4	1	InOut	PCH	N51
SGMII_MDC_1	GPP_E11/USB_OC2#	2	Out	PCH	BG51
SGMII_MDIO_1	GPP_E12/USB_OC3#	2	InOut	PCH	BC47
SGMII_AUXTS_0	GPP_S0/SNDW1_CLK	3	InOut	PCH	BJ45
SGMII_AUXTS_1	GPP_S4/SNDW3_CLK/DMIC_CLKA1	3	InOut	PCH	BE46
SGMII_INT_0	GPP_S1/SNDW1_DATA	3	In	PCH	BH45
SGMII_INT_1	GPP_S5/SNDW3_DATA/ DMIC_DATA1	3	In	PCH	BG47
SGMII_RESET_N_0	GPP_S2/SNDW2_CLK/DMIC_CLKB0	3	Out	PCH	BG45
SGMII_RESET_N_1	GPP_S6/SNDW4_CLK/DMIC_CLKA0	3	Out	PCH	BF47
SGMII_PPS_0	GPP_S3/SNDW2_DATA/ DMIC_CLKB1	3	InOut	PCH	BF46
SGMII_PPS_1	GPP_S7/SNDW4_DATA/ DMIC_DATA0	3	InOut	PCH	BF48
Time-Aware GPIO					
TIME_SYNC_0	GPP_H23/TIME_SYNC0	1	InOut	PCH	M51
TIME_SYNC_1	GPP_I10/GSPI1_CS1#/ TIME_SYNC1	2	InOut	PCH	BF14
Display Genlock					
Vertical Reference [Frame Sync]	DISP_UTILS_1	N/A	N/A	CPU	K17
PLL Reference Clock	DISP_UTILS_2	N/A	N/A	CPU	H16
Genlock Direction Enable	GPP_F20/EDP_BKLTEN	N/A	N/A	PCH	AT48
Genlock Direction Select	GPP_F21/EDP_BKLTCTL	N/A	N/A	PCH	AP52

Notes:
1. For more details on signal description refer to Chapter 3.0, “Graphics and Display”, Chapter 5.0, “Ethernet & Time-Sensitive Networking (TSN),” and Chapter 6.0, “Intel® Time Coordinated Computing (Intel® TCC).”

1.5 R680E PCH SKU

Table 5. Features for R680E

Features	R680E
DMI	x8
Maximum SATA 6 Gb/s Ports	8
Maximum PCIe Gen3 Lanes	16
Maximum PCIe Gen4 Lanes	12
Total USB 2.0 Ports	14
Maximum USB 3.2 Gen 1x1 (5 Gb/s)	10
Maximum USB 3.2 Gen 2x1 (10 Gb/s)	10
Maximum USB 3.2 Gen 2x2 (20 Gb/s)	4
Intel® Smart Sound Technology	YES
Intel® CSME Firmware	Intel® CSME 16 Corporate
Intel® Rapid Storage Technology 19.x	YES
PCIe RAID 0,1,5 Support	YES
SATA RAID 0, 1, 5, 10 Support	YES
eSPI Chip Select	4

Table 6. HSIO Details

Flex I/O Lane	R680E
0	USB 3.2 Gen 2x1
1	USB 3.2 Gen 2x1
2	USB 3.2 Gen 2x1
3	USB 3.2 Gen 2x1
4	USB 3.2 Gen 2x1
5	USB 3.2 Gen 2x1
6	USB 3.2 Gen 2x1
7	USB 3.2 Gen 2x1
8	USB 3.2 Gen 2x1
9	USB 3.2 Gen 2x1
10	PCIe 3.0
11	PCIe 3.0
12	PCIe 3.0 / GbE
13	PCIe 3.0
14	PCIe 3.0
15	PCIe 3.0
16	PCIe 3.0 / GbE
17	PCIe 3.0
18	PCIe 3.0 / GbE-TSN
19	PCIe 3.0 / GbE-TSN
20[1]	PCIe 3.0
21[1]	PCIe 3.0

Table 6. HSIO Details

22	PCIe 4.0 / SATA
23	PCIe 4.0 / SATA
24	PCIe 4.0 / SATA / GbE
25	PCIe 4.0 / SATA
26	PCIe 3.0 / SATA
27	PCIe 3.0 / SATA
28	PCIe 3.0 / SATA
29	PCIe 3.0 / SATA
30	PCIe 4.0
31	PCIe 4.0
32	PCIe 4.0
33	PCIe 4.0
34	PCIe 4.0
35	PCIe 4.0
36	PCIe 4.0
37	PCIe 4.0

Note:

1. Lane 20 and Lane 21 are unusable when enabling either or both of the GbE-TSN lanes.

§ §

2.0 Thermal Management

2.1 Thermal Management Introduction

The 12th Generation Intel® Core™ Desktop Processor is a 64-bit, multi-core processor built on a Intel® 7 process technology. The S-processor line is offered in a 2-Chip Platform and connected to a discrete Intel® 600 Series PCH chipset on the motherboard.

Table 7. 12th Gen Intel® Core™ Desktop Processor Line and Intel® 600 Series PCH SKU Summary

Segment	Package	SKU Series	Base TDP	Processor IA P-Cores	Processor IA E-Cores	Graphics Configuration
S (LGA 8+8)	LGA1700	Embedded	35W	8	8	32EU
		Embedded	65W	8	8	32EU
S (LGA 8+4)		Embedded	35W	8	4	32EU
		Embedded	65W	8	4	32EU
S (LGA 6+0)		Embedded	35W	6	0	32EU
		Embedded	65W	6	0	32EU
		Embedded	65W	6	0	24EU
S (LGA 4+0)		Embedded	35W	4	0	24EU
		Embedded	60W	4	0	24EU
S (LGA 2+0)		Embedded	35W	2	0	16EU
		Embedded	46W	2	0	16EU
Intel® 600 Series (PCH-S)	BGA1045	R680E	≤ 6W	N/A	N/A	N/A
		Q670E	≤ 6W			
		H610E	≤ 6W			

Notes:
1. Processor lines offer may change.
2. For more details refer to Table 2, *12th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2 (document number 655258).*
3. The TDP is the average power dissipation in junction temperature operating condition limit, for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.
4. TDP workload may consist of a combination of processor IA core intensive and graphics core intensive applications.
5. P-Cores refers to Performance-cores and E-Cores refers to Efficient-cores.

2.2 S Processor Line Thermal and Power Specifications

Additional note for Thermal and Power Specifications. This note is an addition to the other notes mentioned in *Thermal Management* in the *12th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2*.

Table 8. Processor Temperature Specifications

Segment	SKU Series	Symbol	Description	Temperature Range		TDP Specification Temperature Range		Notes
				Min	Max	Min	Max	
S-Processor Line LGA	Embedded	Tj	Junction Temperature Limit	0°C	100°C	35°C	100°C	1,2
Intel 600 Series (PCH-S)	R680E	Tj	Junction Temperature Limit	0°C	108°C	35°C	100°C	1,2
	Q670E							
	H610E							

Notes:

1. The processor supports commercial ambient temperature range, and memory devices should operate in the same condition.
2. For other junction temperature specification refer to the note mentioned in *S-Processor Line Thermal and Power Specifications* under *Thermal Management* in the *12th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2 (document number 655258).*

§ §

3.0 Graphics and Display

3.1 Graphics SRIOV

3.1.1 Overview

SRIOV(64) extends the SRIOV architecture to provide support for 64 functions: 1 Physical Function (PF) plus 63 Virtual Functions (VF).

3.1.2 Feature Summary

- Schedule-enabled GT engines can run on behalf of any of the 64 Functions. VF# is specified in the context image (LRCA).
- LRCA memory is allocated and managed by PF driver.
- GT Engines running on behalf of VFs (Render, Compute, Blitter, Video Decoder, Video Enhancement) report interrupt status in memory.
- GT Global engines (GuC, KCR, GPM) will report interrupts through PF MMIO registers.
- Doorbells is 256.
- Display planes can be assigned to VFs, but Display events get reported through the PF MMIO interrupt registers.
- When enabled, SRIOV Virtual Functions are identified by PCI Requestor IDs that increment sequentially from the Requestor ID of the Physical Function. In this case, there is no distinction between “Device” and “Function” fields.
- Layout of Per-VF MMIO Registers within PF MMIO space supports more VFs with less space per VF. Specifically, VF# is encoded in MMIO Register Address bits [15:10] supporting 1KB of MMIO space for up to 63 VF.

3.1.3 Local Memory 2nd-level Translation Table (LMTT)

Local Memory 2nd-Level Translation Table (LMTT) is implemented in GT HW and SW in order to flexibly allocate a limited amount of memory that is local to the GPU device and isolate that allocation from other Virtual Machines. The key characteristics of the Local Memory Translation Tables (LMTT) are:

- A separate LMTT is allocated for each Guest VM or Assignable Interface that receives HBM resources.
- The LMTT are managed by the Host KMD, in coordination with the VMM or Host OS.
- LMTT is a two-level structure, residing entirely in Local Memory.
- 2nd-level is the LMTT, that translates a 2MB page of Local Memory in Guest address space to physical Local Memory
  - — The size of each 2nd-level LMTT depends on the Local Memory address space supported for each Guest.

    - The parameter Local Memory Guest Address Width (LMGAW) defines the number of address bits available for Guest view of Local Memory
    - The parameter Local Memory Host Address Width (LMHAW) defines the number of address bits available for the final Host view of Local Memory
    - Each LMTT Entry is 32-bits wide, including a Valid bit (0), and maps a Guest Local Memory 2MB page into the final Host Local Memory Page (address bits LMHAW-1:21).
    - As an example for a Local Memory size of 32GB, LMGAW = LMHAW = 35 bits, and LMTT will be 64KB per VM/VF instance
- 1st-level is a Directory, with an entry for each Guest VM/VF, indexed by the VF# (or PASID with future SRIOV support)
    - Each Directory Entry is 32-bit and stores:
        - Offset of the 2nd-level LMTT for the specified VM, in multiples of 64KB (LMHAW-16 bits)
        - Valid bit
    - Size of table is 256 Bytes assuming 63 VF + PF, aligned on a 64KB boundary
    - With future SIOV support, this expands up to 4MB (20-bit PASID = 1M Entries), and must be naturally aligned.
- The location of the LMTT Directory is stored in two MMIO registers accessible only by the Host KMD: one in Gunit, and one in GT (GAM)

3.1.4 Global Memory Space

Global Address space, and the associated Global GTT, are shared for all Global allocations for all Guest VMs or AIs, as is already defined for SRIOV in monolithic configurations with UMA memory. In the current SRIOV definition, the Global GTT is managed by the Host KMD, which determines which global address can be accessed by which Guests. The Host KMD programs the GGTT via the GTTMMADR MMIO range of the Physical Function, and the Guests are prevented from directly accessing the GGTT. The Global GTT Entry includes the Function Number of the guest (or Host) to which that global page has been allocated.

When GAM receives a request from a global agent, such as GuC or OA, or from an Engine that is operating on behalf of the Host, that targets Global Memory, GAM will use the Function Number from the GGTT for 2nd-level translation, instead of the Host's Function Number of 0. This allows the Host to share global space with all Guests.

Note: New bit is required to distinguish Local vs System Memory because the GGTT Entry may contain either a GPA pointing to DDR, or an HPA pointing to Local Memory, and nothing prevents the DDR GPA from overlapping the LMEM_BAR range.

Because the global address space is shared by all contexts and all Guest VMs, and is limited to 4GB total, the GGTT page size granularity remains 4KB. When allocating global surfaces larger than 4KB, the Host KMD should attempt to choose contiguous 4KB pages up to at least 64KB, which is the minimum page size for which HBM accesses are optimized.

3.2 Genlock Design Guidelines

3.2.1 Overview

Multichip Genlock is a feature which helps in synchronizing frames across displays connected to multiple systems. This feature ensures that all the monitors that are part of the Genlock configuration displays the same scan line of the same frame within +/- Δ pixels.

Figure 1. High Level Block Diagram - Multichip Genlock Configuration

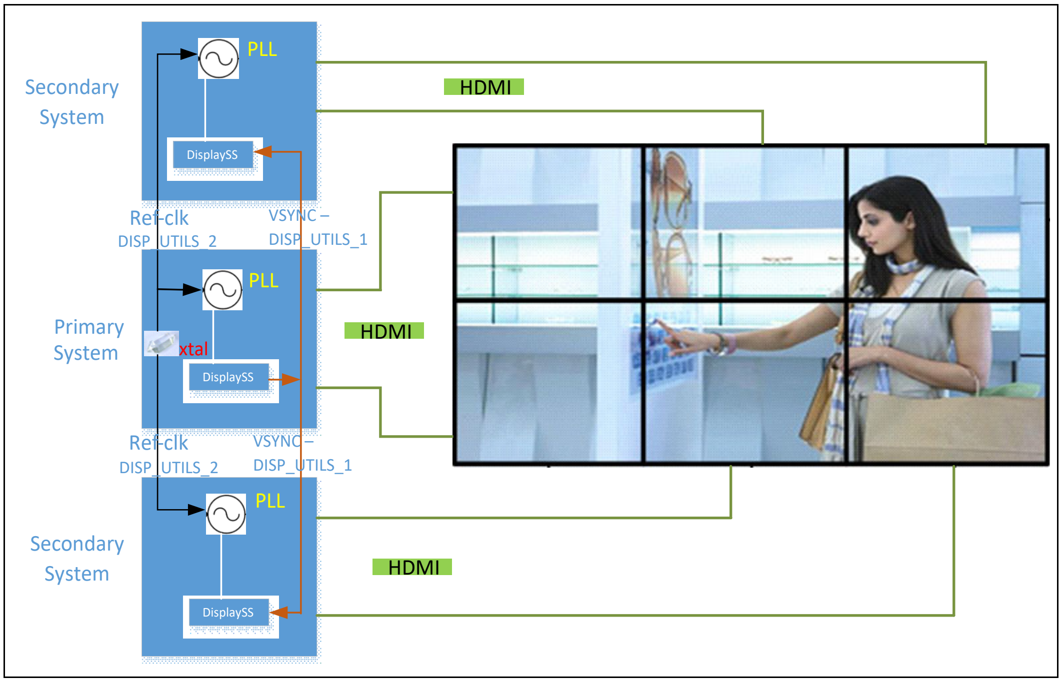


Figure 1 above illustrates a wall of 2x3 displays connected to three 12th Generation Intel® Core™ Desktop Processor systems in a Multichip Genlock configuration, where one system acts as a genlock primary generating the clock and two other systems, as genlock secondary receiving the clock.

Each Genlock configuration allows:

- All display PLLs are running off of the same reference clock
- All displays receive their vertical reference at the same time (via a separate wire or combined with the reference clock).

Note: Having the frame start at the same time is the responsibility of this feature. Flipping the right frame across displays is the responsibility of the application software.

3.2.2 Functional Details

Genlock requires a primary-secondary topology to operate. One of the systems runs as a primary, providing the clock and vertical sync to other systems (secondary) in the configuration so that Genlock can be achieved (refer to Figure 1).

3.2.2.1 Functional Considerations: Generic

1. Genlock functionality is not supported in the pre-boot environment (GOP does not support this feature).
2. All displays in a Multichip Genlock system must have the exact same timing requirements and support the same transport protocol (i.e. two panels with different 1080p timings are not allowed).

3. Multichip Genlock is supported by both HDMI and DP protocols, but not both in the same configuration. Displays in a Genlock topology will either be all DP displays or all HDMI displays.
4. Genlock selection is not persistent across reboots.
5. After reboot, the system always comes back in default mode.
6. App or UI will select primary, secondary(ies) after system boots
7. Genlock Hardware shares pins with other mutually exclusive features as follows:

Table 9. Genlock Functional Pin List Muxing

Pin	Genlock Function	Pin Functionality Shared With
Utility Pin 1	Vertical Reference [Frame Sync	DSI_DE_TE (TE1)
Utility Pin 2	PLL Reference Clock	DSI_DE_TE (TE2)
BL PWM/Genlock En	Genlock Direction Enable	Backlight PWM
BL Enable/Genlock Sel	Genlock Direction Select	Backlight Enable

3.2.2.1.1 Genlock Direction

Genlock sends syncing signals between multiple graphics capable chips to align their display outputs for usages like video walls. Each chip can be programmed as either a transmitter (primary) or receiver (secondary) of sync signals (secondary). The motherboard components control the routing of the syncs (direction in or out). The north display and PLLs are consuming and driving the sync signals. The south display is driving direction controls to the motherboard components.

There is a genlock direction enable signal to enable the motherboard components and a genlock direction select signal to specify the direction of the genlock signals. These are controlled by register fields.

To save pins, the genlock direction signals are muxed with the backlight signals since internal panel and genlock are mutually exclusive at the platform level.

- Backlight PWM is muxed with Genlock direction enable
- Backlight Enable is muxed with Genlock direction select

Table 10. SBLC_PWM_CTL1 Register Control Setting

SBLC_PWM_CTL1 Register Field	Setting for Genlock Secondary Device	Setting for Genlock Primary Device	Setting for No Genlock
PWM Enable	0	0	As Needed for Backlight
Backlight Polarity	0	0	As Needed for Backlight
Genlock Direction IO Select	Genlock	Genlock	Backlight
Genlock Direction Enable Pin Value	1	1	0
Genlock Direction Select Pin Value	1	0	0

3.2.2.2 Functional Considerations: Driver Specific

Each Genlock system contains a single SoC and runs in either primary, secondary or default mode.

Table 11. Genlock System Mode

Mode	Description
Genlock Primary	System provides the clock and vertical sync reference to other systems
Genlock Secondary	System receives the clock and vertical sync reference from a primary and synchronizes to it
Default	Neither primary nor secondary (i.e., doesn't send or receive a clock)

Each display output of a given system can be independently selected for Genlock. Genlock is enabled on a port by port basis. HW is capable of supporting one pipe using an external clock and another pipe using an internal clock. This enables the software to make multiple mode set calls across the individual displays connected to a single system.

A Genlock secondary will not generate VBI (vertical blanking interval) until after Genlock sync is achieved. Multichip Genlock cannot be enabled at the same time port sync is enabled. Spread Spectrum,VRR (variable refresh rate) and Joint Displays is/are not supported in Genlock configuration.

Multichip Genlock is not supported with software-programmable Vtotal and pixel clock based refresh rate switching (LRR/LRR2). Active Dongles (Protocol converters) are not allowed to be part of a Genlock configuration. DP ALT mode on USB-C connectors concurrent USB Super-speed operation on genlocked connectors is not supported.

There is no scaling support enabled for Genlock displays. Only those target modes that are common across all the displays in a Genlock topology within a system will be supported.

All Genlock displays must train their links identically. By default, and after each reboot, the system will come up in "default mode".

Once Genlock selection is made, the graphics driver reconfigures the hardware through a mode set triggered by the application software (OS aware).

If the system is a primary device: All transcoders in the display engine will continue using the internal reference clock. The primary transcoder will be configured to provide the vertical sync to all local secondary. Local secondary transcoders will be configured to receive the vertical sync from the primary transcoder.

If the system is a secondary device: The display engine will move from an internal reference clock to an external clock. All remote secondary will receive their frame sync from the Primary Genlock system.

Runtime selection of primary or secondary requires a mode set. (OS aware)

3.2.2.3 Primary Configuration (Output)

Table 12. PLL Reference Clock (DISP_UTILS_2)

Parameter	Minimum	Maximum	Unit	Figure
Pull Up		50	ohm	
Pull Down		50	ohm	
Rising Edge Rate	1.45	3.45	V/ns	Figure 2
Falling Edge Rate	1.45	3.45	V/ns	Figure 2

Table 13. PLL Reference Clock (DISP_UTILS_2)

Parameter	Minimum	Maximum	Unit	Figure
Operating Frequency		38.4	MHz	Figure 2

3.2.2.4 Functional Considerations: Application Software Specific

The application should ensure that every Genlock system has the same SoC, it is a requirement for the feature to work.

The driver cannot ensure that there is only one primary or there is a primary in a Genlock configuration. This is the responsibility of the application software.

If a system is configured as a secondary and it is not connected to a primary, the secondary system displays won't come up. This may cause a system hang since there will be no VBI until the synchronization happens.

If more than one system is configured as a primary or if the Genlock wiring is not correct, the system or the attached displays are not expected to function properly. This represents a bug in the application configuration.

All displays in a Multichip Genlock system must have the exact same timing supported and should support the same transport protocol. The application must configure the timing to be identical across all elements of the array of displays.

The driver knows timings of displays within a system but does not know configurations across the systems and therefore cannot prevent programming issues.

An application must ensure that all the displays within a Genlock configuration across devices should be of the same type (either all HDMIs or all DPs).

Any runtime selection of a Genlock primary or secondary requires a full mode set to be triggered by the application through the OS.

For Genlock to function properly, the application software MUST:

Ensure that it always triggers the mode set for the primary display(s) first prior to the mode set of any secondary display(s), across the Genlock topology.

Ensure that it triggers the destroy mode set of all secondary displays first prior to triggering the destroy mode set of the primary display(s).

There is no scaling support enabled for Genlock displays. The application must ensure that the OS selects the appropriate target mode that is common across all Genlock displays during a mode set.

The application can ensure the desired target mode selection by triggering an SDC with both the Source Mode timing AND the right Target Mode timing sent to the OS or by letting the OS know that there is no scaling supported for the selected Source Mode.

If the application fails to ensure the right Target Mode is selected, the OS can pin a different target mode for the chosen Source Mode. This can lead to issues in Genlock synchronizations.

Post-Genlock configuration enabling: The application is expected to query all the displays for their trained link parameters (link rate and lane count) and ensure that all displays are trained identically. If there are any discrepancies, it is up to the application software to disable the Genlock topology.

Flipping the right frame across displays is the responsibility of the application software.

3.2.3 Sequence to Achieve Genlock

The term Genlock refers to locking the timing and the pixel clock together. This is typically done by providing a common clock reference to all the devices along with a vertical frame sync reference. Once locked, the video output streams will have their vertical periods aligned and should remain so unless disabled.

The pipe attached to the Primary transcoder sends its Vertical Blank signal to the pin to be used as a reference. All secondary ports will use this pin as an input to start their respective timing generators.

1. Primary transcoder outputs the frame sync to be used by local and remote secondary.
2. Local secondary (secondary transcoders within the primary device) receive frame sync from the primary transcoder in the same device and use the local PLL reference.
3. Remote secondary (secondary transcoders within a secondary device) receive frame sync from the primary transcoder in the primary device and use the primary device PLL reference.

Primary transcoder outputs the frame sync to be used by local and remote secondary.

Local secondary (secondary transcoders within the primary device) receive frame sync from the primary transcoder in the same device and use the local PLL reference.

Remote secondary (secondary transcoders within a secondary device) receive frame sync from the primary transcoder in the primary device and use the primary device PLL reference.

3.2.3.1 Entering Genlock Mode

1. The system identified as the primary system should enter Genlock primary mode first prior to any other systems entering secondary mode. This ensures that the external clock source is active before any secondary(ies) can use it. This crucial step is the responsibility of the application software.
2. Other systems can then enter from default mode into secondary mode.

3.2.3.2 Exiting Genlock Mode

1. Secondary transcoders (local and remote) should exit from secondary mode to default mode.
2. The primary transcoder should exit from primary mode to default mode last and only after all secondary transcoders have exited to default mode.

3.2.4 Restrictions

1. Multichip Genlock cannot be enabled at the same time port sync is enabled.
2. Spread Spectrum is not supported in a Genlock configuration.

3. VRR is not supported in a Genlock configuration.
4. Active Dongles (Protocol converters) are not allowed to be part of the Genlock configuration.
5. DP ALT mode on USB-C connectors: concurrent USB Super-speed operation on genlocked connectors is not supported.
6. Genlock is supported by both HDMI and DP protocols, but not both in the same configuration. Displays in a Genlock configuration will either be all DP or all HDMI displays.
7. The Primary display should enter primary mode first before any secondary displays enter secondary mode from default mode.
8. The Primary display should exit primary mode only after all secondary displays have exited to default mode.
9. All displays in a Multichip Genlock system must have the exact same timings.
10. There is no scaling support enabled for Genlock displays.
11. All Genlock displays must train their links identically.
12. Genlock selection is not persistent across reboots.
13. All displays must be same resolution.

§ §

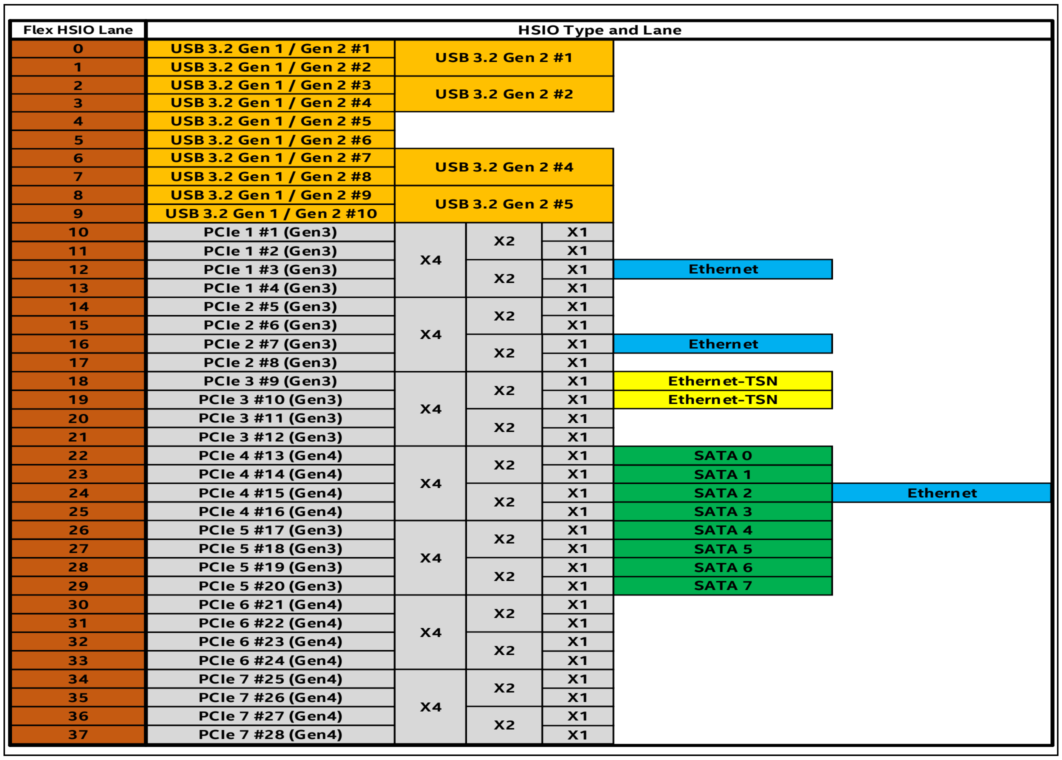
4.0 High Speed Input/Output (I/O)

4.1 Flexible High Speed Input/Output (HSIO) Introduction

The flexible Input/Output (I/O) is a technology that allows some of the PCH High Speed I/O (HSIO) lanes to be configured for connection to a Ethernet Controller, a PCIe* Controller, an eXtensible Host Controller Interface (xHCI) USB 3.2 Controller, an Advanced Host Controller Interface (AHCI) SATA Controller or Ethernet TSN Controller. Flexible I/O enables customers to optimize the allocation of the PCH HSIO interfaces to better meet the I/O needs of their system.

4.2 Flexible HSIO Lane Multiplexing

Figure 2. Flexible HSIO Lane Multiplexing in Intel® 600 Series PCH-S



Flex HSIO Lane	HSIO Type and Lane					
0	USB 3.2 Gen 1 / Gen 2 #1	USB 3.2 Gen 2 #1				
1	USB 3.2 Gen 1 / Gen 2 #2					
2	USB 3.2 Gen 1 / Gen 2 #3	USB 3.2 Gen 2 #2				
3	USB 3.2 Gen 1 / Gen 2 #4					
4	USB 3.2 Gen 1 / Gen 2 #5					
5	USB 3.2 Gen 1 / Gen 2 #6					
6	USB 3.2 Gen 1 / Gen 2 #7	USB 3.2 Gen 2 #4				
7	USB 3.2 Gen 1 / Gen 2 #8					
8	USB 3.2 Gen 1 / Gen 2 #9	USB 3.2 Gen 2 #5				
9	USB 3.2 Gen 1 / Gen 2 #10					
10	PCIe 1 #1 (Gen3)	X4	X2	X1		
11	PCIe 1 #2 (Gen3)			X1		
12	PCIe 1 #3 (Gen3)		X2	X1	Ethernet	
13	PCIe 1 #4 (Gen3)			X1		
14	PCIe 2 #5 (Gen3)	X4	X2	X1		
15	PCIe 2 #6 (Gen3)			X1		
16	PCIe 2 #7 (Gen3)		X2	X1	Ethernet	
17	PCIe 2 #8 (Gen3)			X1		
18	PCIe 3 #9 (Gen3)	X4	X2	X1	Ethernet-TSN	
19	PCIe 3 #10 (Gen3)			X1	Ethernet-TSN	
20	PCIe 3 #11 (Gen3)		X2	X1		
21	PCIe 3 #12 (Gen3)			X1		
22	PCIe 4 #13 (Gen4)	X4	X2	X1	SATA 0	
23	PCIe 4 #14 (Gen4)			X1	SATA 1	
24	PCIe 4 #15 (Gen4)		X2	X1	SATA 2	Ethernet
25	PCIe 4 #16 (Gen4)			X1	SATA 3	
26	PCIe 5 #17 (Gen3)	X4	X2	X1	SATA 4	
27	PCIe 5 #18 (Gen3)			X1	SATA 5	
28	PCIe 5 #19 (Gen3)		X2	X1	SATA 6	
29	PCIe 5 #20 (Gen3)			X1	SATA 7	
30	PCIe 6 #21 (Gen4)	X4	X2	X1		
31	PCIe 6 #22 (Gen4)			X1		
32	PCIe 6 #23 (Gen4)		X2	X1		
33	PCIe 6 #24 (Gen4)			X1		
34	PCIe 7 #25 (Gen4)	X4	X2	X1		
35	PCIe 7 #26 (Gen4)			X1		
36	PCIe 7 #27 (Gen4)		X2	X1		
37	PCIe 7 #28 (Gen4)			X1		

The 38 HSIO lanes on Intel® 600 Series PCH-S support Ethernet-TSN in the following configurations:

1. Up to 2 Ethernet-TSN Ports
    - — A maximum of 2 Ethernet-TSN port (or device) can be enabled.

- — Intel® 600 Series PCH-S Ethernet-TSN supports is SKU dependent and support on R680E PCH pairing only. Others PCH pairing is not supported.
- — Intel® 600 Series PCH-S supports concurrent Ethernet and Ethernet-TSN port. This makes 1 port of Ethernet 1Gb/Intel vPro® Technology capable Ethernet and 2 ports of 2.5Gb/TSN capable Ethernet. In total, three Ethernet ports can be enabled at the same time.
- — A maximum of sixteen PCIe* Root Ports (or devices) can be enabled. When a Ethernet/Ethernet-TSN Port is enabled, the maximum number of PCIe* Root Ports (or devices) that can be enabled reduces based off the following:
  - Max PCIe* Root Ports (or devices) = 16 - Ethernet (0 or 1) - Ethernet TSN (0, 1, or 2).
- — Enabling Ethernet-TSN configuration and type is statically selected by soft straps, which are managed through the Platform Flash Image Tool (FIT), available as part of Intel® CSME releases. Refer to the SPI Programming Guide documentation for details on how to configure the Ethernet-TSN lanes via soft straps.
  - To enable Ethernet-TSN, either one or both of PCIe 3 #9 and/or PCIe 3 #10 lanes must be strap enabled in FIT to TSN.
  - If only one Ethernet-TSN port is enabled, the other Ethernet-TSN port (PCIe 3 #9 or PCIe 3 #10 lane) must be strap disabled in FIT.
  - PCIe 3 #11 and PCIe 3 #12 are unusable and must be strap disabled in FIT when enabling either or both of the Ethernet-TSN lanes.

4.3 Thunderbolt™

To be granted access to all Thunderbolt™ documentation available on RDC and the Developer's Area of the community, customers must first register following this link: Create new account | Thunderbolt Technology Community

Once a customer has registered and has been approved, they will have access to a wealth of substantive Thunderbolt information enabling them to proceed with their design.

§ §

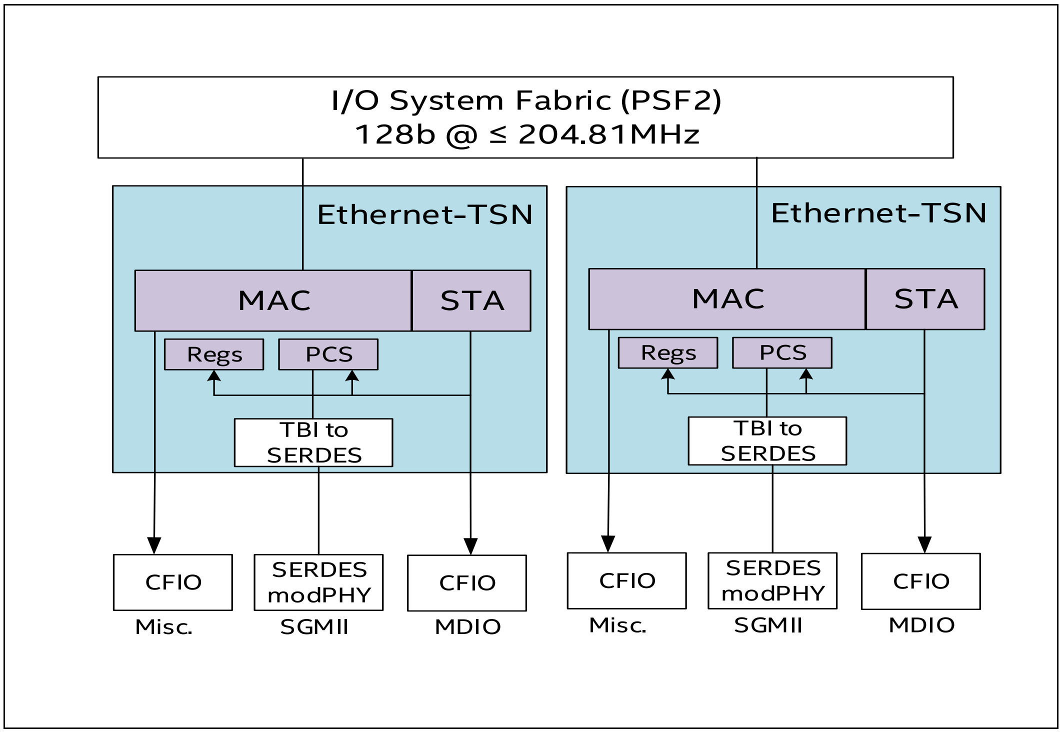
5.0 Ethernet & Time-Sensitive Networking (TSN)

5.1 Ethernet & Time-Sensitive Networking (TSN) Introduction

The Intel® 600 Series PCH-S contains one Ethernet controller and two Ethernet-TSN controllers. The Ethernet and Ethernet-TSN controllers are physically isolated from each other and are designed to run concurrently. This make 1 port of Ethernet 1Gb/Intel vPro® Technology capable Ethernet and 2 ports of 2.5 Gb/TSN capable Ethernet. Each Ethernet-TSN controller has a Media-Access Control (MAC). Total of three Ethernet ports can be enabled simultaneously.

This chapter describes the behavior of the Ethernet-TSN controllers. Time-Sensitive Networking (TSN) is a set of IEEE standards that are intended to ensure quality transmission of the time-sensitive data over Ethernet networks. These Ethernet-TSN controllers is Time-Sensitive Networking (TSN) capable. Besides that, it supports Audio Video Bridging (AVB). It doesn't support Intel Active Management Technology (Intel® AMT) or Modern Standby (S0ix) power management. Ethernet-TSN controllers can operate at multiple speeds, 10Mbps, 100Mbps, 1Gbps, and 2.5Gbps (SGMII) and in either full duplex or half duplex mode. Figure 3 shows two Ethernet-TSN MAC placement in Intel® 600 Series PCH-S.

Figure 3. Ethernet-TSN MAC Placement

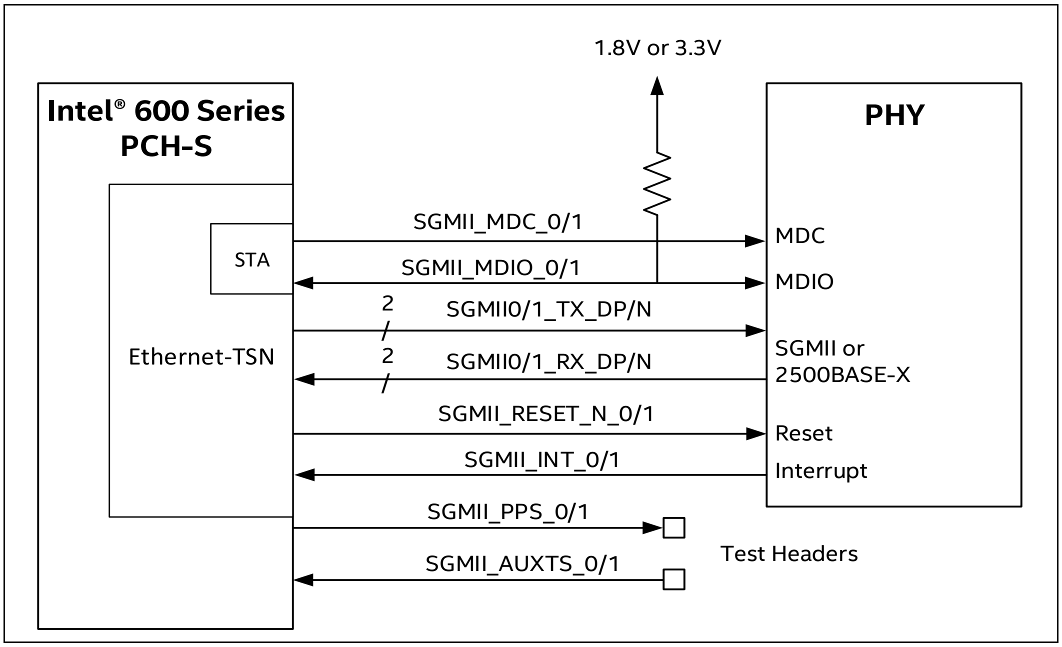


The Ethernet-TSN MAC is accessed by the 12th Generation Intel® Core™ Desktop Processor cores through system software as a PCI Express Root Complex Integrated Endpoint (RCiEP) via PCH IO Fabric (PSF2) and only supports the SGMII interface.

This MAC has a Station Management (STA) Entity that is accessible to software via the Memory Map IO (MMIO) registers to control the associated MDIO interface. Refer to the IEEE Standard 802.3, Clause 22, and Clause 45. The Physical Coding Sublayer (PCS) module provides the sublayer circuitry between the GMII of the MAC and Ten-Bit Interface (TBI) of the Serial Gigabit Media-Independent Interface (SGMII) circuitry. See IEEE Standard 802.3 Clause 35 for GMII and Clause 36 for TBI.

Figure 4 shows a typical Ethernet-TSN interface to an External PHY. The figure does not show the additional board components required for AC-Coupling and signal voltage-level converters if needed.

Figure 4. **Intel® 600 Series PCH-S Ethernet-TSN Platform Design**



5.2 External Interfaces Description

The Ethernet-TSN MAC module provides an SGMII interface to its external PHY component. The PCH does not use any of the Precision Time Protocol (PTP) capture capabilities that may exist in the external PHY component. All the PTP events and timestamps are triggered in the MAC portion of the subsystem.

SGMII is a de-facto industry standard for achieving Ethernet LAN speeds of 10Mbps, 100Mbps, 1Gbps, and 2.5Gbps. It consists of two sets of Current-Mode Logic (CML) differential signal using one of the multiplexed PCH ModPHY lanes (see Chapter 4.0, "High Speed Input/Output (I/O)" for further details). The design embeds the SGMII transmit clock in the transmit data and expects the SGMII receive clock to be embedded in the receive data. This eliminates four of the standard SGMII interface pins. For the controller's IEEE Std 802.3 Physical Sublayer configuration and management, it also provides two CMOS Management Data Input/Output (MDIO) interface signals. SGMII provides a reduced-pin implementation of GMII (IEEE Std 802.3, Clause 35) which would require 25 single-ended signals plus the two MDIO interface signals.

5.2.1 SGMII Signal Description

Table 14. SGMII Ethernet-TSN Signals

Signal Name[1,2]	Package Name	Type (Voltage Domain)	Direction	Description
SGMII0_TX_DP	PCIE9_TXP	CML Differential Signal (1.05V)	Output	Transmit P&N of the serial differential output
SGMII0_TX_DN	PCIE9_TXN			
SGMII1_TX_DP	PCIE10_TXP			
SGMII1_TX_DN	PCIE10_TXN			
SGMII0_RX_DP	PCIE9_RXP	CML Differential Signal (1.05V)	Input	Receive P&N of the serial differential input
SGMII0_RX_DN	PCIE9_RXN			
SGMII1_RX_DP	PCIE10_RXP			
SGMII1_RX_DN	PCIE10_RXN			

Notes:
1. Refer Chapter 4.0, "High Speed Input/Output (I/O)" in this document for a description of how these signals are routed to and selected by the FIA/MODPHY.
2. 0 and 1 can be used for two Ethernet-TSN ports.

5.2.2 MDIO Signal Description

External PHY can be accessed through MDC/MDIO where the external MDIO/MDC interface is implemented over GPIO and is used by the SW/HW/BIOS to configure external PHY. The IEEE Standard 802.3 defines the MDIO Management Interface, which serves to access the Management register of 802.3 compliant devices. This is a two-line interface including MDC (clock) and MDIO (bidirectional data). I2C is not supported in the PCH for management. Only the IEEE Std 802.3 Station Management (STA) interface is made available (MDIO, MDC). STA interface characteristics are different than I2C. For the MDIO signal timing relationship to the MDC signal, see IEEE Std 802.3-2008, Section 45.4.2.

Table 15. MDIO Ethernet-TSN Signals

Signal Name[1,2]	Package Name	Type (Voltage Domain)	Direction	Description
SGMII_MDC_0	GPP_G3	CMOS (1.8V or 3.3V)	Output	**Management Data Clock** This clock signal is driven by the Ethernet-TSN controllers to clock the serial MDIO data. The clock period is programmable.
SGMII_MDC_1	GPP_E11 / USB_OC2#			
SGMII_MDIO_0	GPP_G4	Open-Drain (1.8V or 3.3V)	Input/ Output	**Management Data Input Output** This signal is driven by either the Ethernet-TSN controllers or the External PHY during MDIO transaction.
SGMII_MDIO_1	GPP_E12 / USB_OC3#			

Notes:
1. 0 and 1 can be used for two Ethernet-TSN ports.
2. The signals should be configured to 1.8V or 3.3V using the multiplexed GPIO's Individual Voltage Select soft strap.

5.2.3 Other Signals Associated with Ethernet-TSN Subsystem Description

Table 16. Other Signals Associated with Ethernet-TSN Subsystem Description

Signal Name[1]	Package Name	Type (Voltage Domain)	Direction	Description
SGMII_AUXTS_0	GPP_S0 / SNDW1_CLK	CMOS (1.8V)	Input	**Auxiliary Time Stamp Trigger** This edge-sensitive input signal triggers the storing of the time stamp into a 4x64 deep FIFO on its rising edge. If it is not used, this signal must be tied to GND through 20kOhm internal resistor.
SGMII_AUXTS_1	GPP_S4 / SNDW3_CLK / DMIC_CLKA1			
SGMII_INT_0	GPP_S1 / SNDW1_DATA	CMOS (1.8V)	Input	**Interrupt** This configurable input signal is driven by the External SGMII PHY device. If it is not used, this signal must be tied to GND through 20kOhm internal resistor.
SGMII_INT_1	GPP_S5 / SNDW3_DATA / DMIC_DATA1			
SGMII_RESET_N_0	GPP_S2 / SNDW2_CLK / DMIC_CLKB0	CMOS (1.8V)	Output	**PHY Reset** This output signal is used to reset the External SGMII device. If it is not used, should be left as a No Connect.
SGMII_RESET_N_1	GPP_S6 / SNDW4_CLK / DMIC_CLKA0			
SGMII_PPS_0	GPP_S3 / SNDW2_DATA / DMIC_CLKB1	CMOS (1.8V)	Output	**Pulse-Per-Second (PPS)** This output signal is generated as a pulse by Ethernet-TSN Controller each time its system timer indicates a new “seconds” value. If it is not used, should be left as a No Connect.
SGMII_PPS_1	GPP_S7 / SNDW4_DATA / DMIC_DATA0			

Note:
1. 0 and 1 can be used for two Ethernet-TSN ports.

5.2.4 MDIO Signal During Reset

Table 17. MDIO Signal During Reset

Signal Name	Direction	Power / Voltage	Resistor	S0	Sx	DSx
				CRST#=0	PLTRST#=0	PLTRST#=0
SGMII_MDC_0	Output	Primary / 1.8V or 3.3V	None	Driven Low	Driven Low	Powered OFF
SGMII_MDC_1						
SGMII_MDIO_0	Input / Output	Primary / 1.8V or 3.3V	None	Input, Pull Down-On	Input, Pull Down-On	Powered OFF
SGMII_MDC_1						

5.2.5 Other Signals Associated with Ethernet-TSN Subsystem During Reset

Table 18. Other Signals Associated with Ethernet-TSN Subsystem During Reset

Signal Name	Direction	Power / Voltage	Resistor	S0	Sx	DSx
				CRST#=0	PLTRST#=0	PLTRST#=0
SGMII_AUXTS_0	Input	Primary / 1.8V	None	Driven Low	Driven Low	Powered OFF
SGMII_AUXTS_1						
SGMII_INT_0	Input	Primary / 1.8V	None	Input, Pull Down-On	Input, Pull Down-On	Powered OFF
SGMII_INT_1						
SGMII_RESET_0	Output	Primary / 1.8V	None	Input, Pull Down-On	Input, Pull Down-On	Powered OFF
SGMII_RESET_1						
SGMII_PPS_0	Output	Primary / 1.8V	None	Input, Pull Down-On	Input, Pull Down-On	Powered OFF
SGMII_PPS_1						

5.3 Ethernet and Ethernet-TSN Features Description

5.3.1 Ethernet Features Description

Ethernet-TSN instance supports the following Ethernet features.

- 10Mbps/100Mbps/1Gbps/2.5Gbps SGMII mode through SERDES interface
- Ethernet-TSN MAC enabled with SGMII modes
- MDIO (station management) interface
- GPIO-based output pin to reset SGMII PHY on the platform
- 4 TX queues and 6 RX queues with separate DMA channels and interrupts. Each TX/RX queue is 4KB for storing at least two normal packets with total of 40KB memory (TX+RX). Buffer sizes are programmable with TX FIFO not to exceed 16KB and RX FIFO not to exceed 24KB.
- Priority scheme for DMA channels - Fixed, Weighted Strict, and Weighted Round Robin.
- Support for Jumbo packets (9018 bytes) in cut-through mode
- Support for TCP/IP Offloading
  - Checksum Offload Engine (COE) that does Checksum insertion (on TX path) and detection (on RX path) for TCP/UDP/ICMP segments encapsulated in IPv4/ IPv6 datagrams
  - TCP Segmentation Offload (TSO) Engine where large TCP packets are split into multiple small packets to save application bus cycles. 4 TX DMA Channels with separate 1KB memory (256 bytes per channel)
- Double VLAN support:
  - Insertion, replacement, or deletion of up to two VLAN tags on TX path
  - Packet filtering (layer-2) and stripping based on any one of two VLAN tags on RX path
- MAC Management Counters (MMC) for gathering statistics on the received and transmitted packets. Interrupts are generated for various events.
  - On TX: Jabber Timeout, No Carrier or Loss of Carrier, Late Collision, Packet Underflow, Excessive Deferral and Excessive Collision
  - On RX: CRC error, Runt packet (shorter than 64 bytes), Alignment error (in 10/100Mbps only), Length error (non-Type packet only), Out of Range (non-Type packet only, longer than 1518 bytes), GMII_RXER Input error
- Low-power management:
  - IEEE Std 802.3az-2010 Energy-Efficient Ethernet (EEE) with automatic entry/exit when link is Idle - Low Power Idle mode. Only TX clock gating is supported
- RX Filtering:
  - 64 Address (SA/DA) based layer-2 perfect and Hash table filtering
  - 4 VLAN tag layer-2 filters
  - 2 Layer-3 and Layer-4 frame filters
- Only non-spread spectrum clocking is supported with the SGMII interface. It is not possible to enable spread spectrum clocking

5.3.2 Ethernet-TSN Features Description

TSN is a set of standards that are intended to ensure quality transmission of the time-sensitive data over Ethernet networks. TSN standards are governed by an IEEE* 802.1 task group are driven by, in part, Avnu Alliance*, which is a consortium of organizations involved and invested in deterministic Ethernet Technology.

The Ethernet-TSN has Ethernet MAC IP, which enables a host to Transmit and Receive data over Ethernet, and in compliance with IEEE Std 802.3-2002/2008 specification. Table 19 shows IEEE Standard and TSN features.

Table 19. IEEE Standard and TSN Features

IEEE Standard	Description
IEEE Std 1588-2008 v2	Precision Clock Synchronization Protocol for Networked Measurement and Control Systems
IEEE Std 802.1AS-2011	A specific profile of IEEE Standard 1588-2008. IEEE Standard 802.1AS specifies the generalized Precision Time Protocol (gPTP). It provides a Layer 2 time synchronizing service
IEEE Std 802.1Qav 2009	Forwarding and Queueing Enhancements for Time-Sensitive Stream, which specifies the Credit-Based Shaper
IEEE Std 802.1Qbu 2016	Frame Preemption. It allows a Bridge Port to suspend the transmission of non-time critical frames while one or more time critical frames are transmitted
IEEE Std 802.3br 2015	Interspersed Express Traffic (IET)
IEEE Std 802.1Qbv 2015	Enhancements for Scheduled Traffic. It specifies time aware queue draining to schedule the transmission of frames relative to a known time scale

In addition to IEEE standards above, Ethernet-TSN instance supports the following TSN features.

- Time-Based Scheduling (TBS)
  - — Time deterministic transmission of the packet according to per packet transmit time specified by users
- IEEE Std 1588-2002/2008 timestamp support for PTP packets
  - — 80-bit internal system timer that runs at 204.8MHz for high-precision one-step time stamping
  - — 64-bit ART timer that runs at 19.2MHz for local and system timer correlation
  - — The ART timer and PTP clock values are captured with accuracy less than 5ns for timing correlation
  - — PTP offloading (Automatic generation of SYNC, Delay_Resp, Pdelay_Req and Pdelay_Resp PTP packets) in the TX path
- GPIO Auxiliary Timestamp Trigger (AUXTS) input (IEEE Std 802.1AS)
- GPIO-based Pulse Per Second (PPS) output with programmable pulse width
- Each Control List of 1K entries for all TX queues. 32x128(x8) memory for Control List to support IEEE Std 802.1Qbv
- Provides Express Media Access Control (eMAC) and Preemptable Media Access Control (pMAC) each with TX and RX queues. The eMAC transfers have higher priority than the pMAC transfers

5.4 Ethernet-TSN Time Stamping Logic

The Precision Time Protocol (PTP) over Ethernet is described in the IEEE Std 1588-2002 and 2008 versions. The subsystem provides the following features:

- IEEE Std 1588-2002 and 2008 formats
- Provides an option to take snapshot of all packets or only PTP type packets
- Provides an option to take snapshot of only event messages
- Provides an option to take the snapshot based on the clock type: ordinary boundary, end-to-end transparent, and peer-to-peer transparent
- Provides an option to select the node to be a primary clock or secondary clock for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in the packets sent directly over Ethernet and sends the status
- Provides an option to measure sub-second time in digital or binary format
- Two time stamp sources
    a. External timestamp
    b. Internal timestamp, which is selected by software

5.5 Ethernet-TSN Cross-Timestamp Logic

Additional logic is included in the Ethernet design to provide time synchronization between the 64-bit timer Always Running Timer (ART) and the 80-bit system timer in Ethernet-TSN controllers.

When system software sets the cross-timestamp enable bit in the Ethernet-TSN ART MDIO register, it captures simultaneous snapshots of the values of the Ethernet-TSN System Timer and the ART. System software can then read the captured time values to establish a relationship between ART and Ethernet-TSN system timer; When the Ethernet-TSN system timer value is X, the ART value is Y.

5.6 BIOS Sub-Region Capsule Update

The 12th Generation Intel® Core™ Desktop Processor BIOS has the following Ethernet TSN sub-region configuration support for the Intel® 600 Series PCH-S port.

- MAC address region

Firmware and BIOS Utilities (FBU) is the configuration tool for provisioning data into the BIOS sub-regions. The latest open-source FBU release package can be downloaded from iotg-fbu page at the GitHub* software development platform.

The Capsule Update process on the target are available through OS, in EFI Shell and in Yocto.

For EFI shell, use CapsuleApp.efi to update the capsule. The CapsuleApp.efi is available in GitHub* page.

For Yocto Project*-based Linux* platform, use fwupdate tool to update the capsule. The fwupdate tool is available in 12th Generation Intel® Core™ Desktop Processor Yocto* BSP image.

The following table lists the configuration line format definition settings and definitions across Javascript* Object Notation (JSON).

Table 20. Configuration Line Format Definition Setting and Definition Across JSON

Variable name (in String)	Variable Format (Decimal or Hexadecimal)	Variable size (Always 4 bytes)	Variable Value (Decimal Value without Quotes or Hexadecimal Value with quotes)
“Version”	“DECIMAL”	4	1
“Version”	“HEXADECIMAL”	4	“00000001”

5.6.1 Common Configuration Setting and Definition Across JSON

Total number of ports for configuring the JSON file (‘X’ - minimum: 0; maximum: 4):

["NumPorts", "DECIMAL", 4, X],

To configure the subsequent JSON setting for Intel® 600 Series PCH-S Ethernet TSN port:

["BDF", "HEXADECIMAL", 4, "000F4000"],

To enable port configuration from the sub-region JSON file:

["PortValid", "DECIMAL", 4, 1],

To disable port configuration from the sub-region JSON file:

["PortValid", "DECIMAL", 4, 0],

5.6.2 MAC Address Sub-Region Configuration

This region configuration applies to the Intel® 600 Series PCH-S Ethernet TSN port.

Configure the MAC address for the specific port (e.g. c6:70:09:b1:54:a9):

["MacAddressLow", "HEXADECIMAL", 4, "B10970C6"],

["MacAddressHigh", "HEXADECIMAL", 4, "0000A954"],

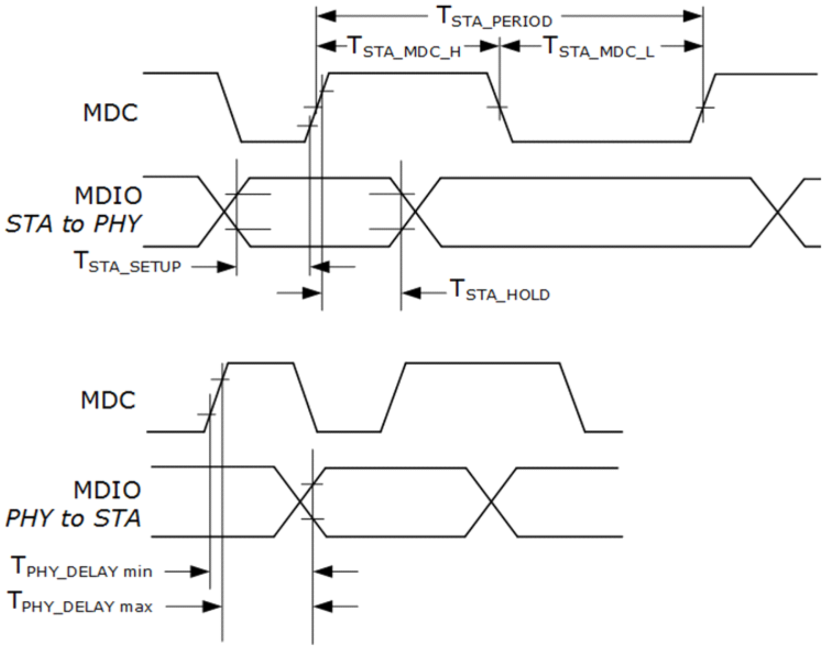
5.7 Gigabit Ethernet Controller AC Specification

5.7.1 GbE AC Specification [MDC/MDIO]

Table 21. GbE AC Specification [MDC/MDIO]

Symbol	Parameter	Minimum	Maximum	Units
TSTA_PERIOD	MDC period	400	-	ns
TSTA_MDC_H	STA MDC high	160	-	ns
TSTA_MDC_L	STA MDC low	160	-	ns
TSTA_SETUP	STA MDC to STA MDIO setup time	10	-	ns
TSTA_HOLD	STA MDC to STA MDIO hold time	10	-	ns
TPHY_DELAY	PHY MDIO delay from STA MDC	0	300	ns

Figure 5. Timing Waveforms - MDC and MDIO Signals



5.7.2 GbE AC Specification [SGMII-XAUI Driver Characteristic]

Table 22. GbE AC Specification [SGMII-XAUI Driver Characteristic]

Parameter[1]	Minimum	Maximum	Units	Notes
Bit Rate	1.25Gb ± 100 ppm	3.125Gb ± 100 ppm	Gb/ppm	
Nominal Unit Interval	320	800	ps	
Differential Amplitude Minimum and Maximum	800	1200	mVp-p	
Absolute Output Voltage Limits	-400	1800	mV	

Parameter[1]	Minimum	Maximum	Units	Notes
Differential Output return loss minimum	-	-	dB	2
Output Total Jitter (near end maximum)	-	±0.175 peak from the mean	UI	
Output Deterministic Jitter (near end maximum)	-	±0.085 peak from the mean	UI	
Output Total Jitter (far end maximum)	-	±0.275 peak from the mean	UI	
Output Deterministic Jitter (far end maximum)	-	±0.185 peak from the mean	UI	

Notes:
1. The load is 100 Ω ± 5% differential to 2.5 GHz for these measurements, unless otherwise noted.
2. For frequencies from 312.5 MHz to 3.125 GHz, the differential return loss of the driver shall exceed equation:-
   S_{11} = -10dB for 312.5 MHz < Freq (f) < 625 MHz, and
   -10 + 10log(f/625) dB for 625 MHz < Freq (f) < 3.125 GHz
   (f = frequency in MHz)

Differential transitions time between 60 ps and 130 ps are recommended, measured between 20% to 80%.

The driver shall satisfy either the near-end eye template and jitter requirements, of the far-end eye template and jitter requirements.

Figure 6. Driver Template

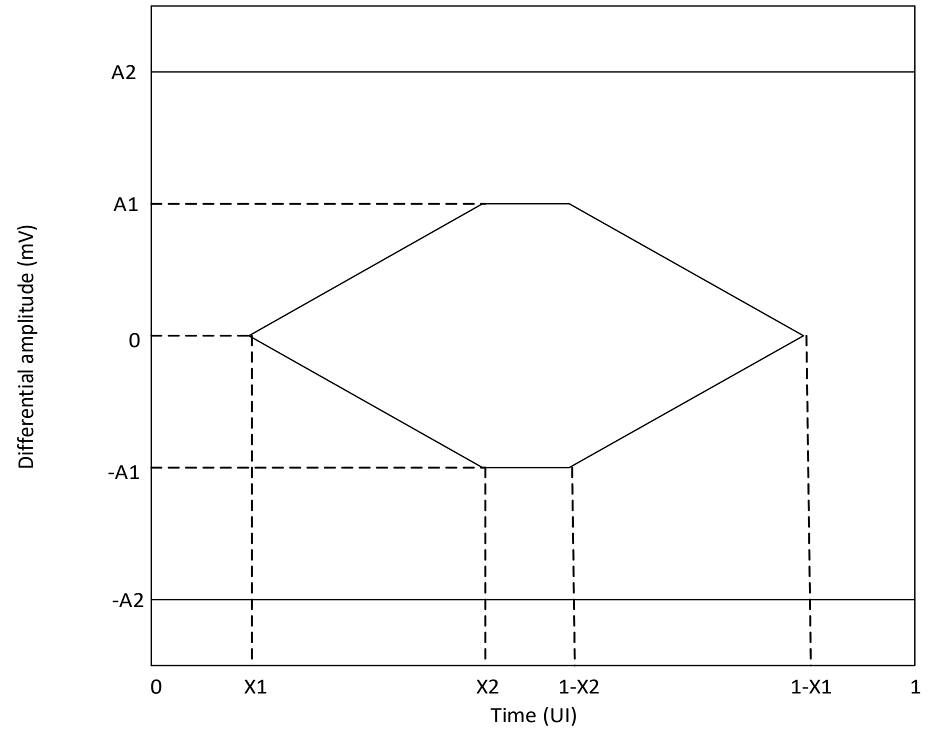


Table 23. Driver Template Intervals

Symbol	Near-End Value	Far-End Value	Units
X1	0.175	0.275	UI
X2	0.390	0.400	UI
A1	400	100	mV
A2	800	800	mV

5.7.3 GbE AC Specification [SGMII-XAUI Receiver Characteristic]

The receiver shall operate with a BER of better than 10^{-12} in the presence of reference input signal as defined in the Driver Characteristic section, Section 5.7.2.

Table 24. GbE AC Specification [SGMII-XAUI Receiver Characteristic]

Parameter	Minimum	Maximum	Units
Bit Rate	1.25 Gb ± 100 ppm	3.125 Gb ± 100 ppm	Gb/ppm
Nominal Unit Interval	320	800	ps
Receiver Coupling	AC Coupled		
EEE Signal Detect deactivation time (TSD) from active to LPI quiet	-	750	ns
EEE Signal Detect activation time (TSA) from LPI quiet to active	-	750	ns
Return Loss Differential	-	10	dB
Return Loss Common-Mode	-	6	dB
Jitter Amplitude Tolerance	-	0.65	UIp-p

Notes:

1. The reference impedance for Return Loss measurements is 100 Ω for Return Loss Differential and 25 Ω for Return Loss Common-Mode.
2. The total jitter is composed of deterministic jitter, random jitter and sinusoidal jitter.
3. Deterministic jitter tolerance shall be at least 0.37UIp-p. Tolerance to the sum of deterministic and random jitter shall be at least 0.55UIp-p. The receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of the Figure 7.

Figure 7. Single-Tone Sinusoidal Jitter Mask

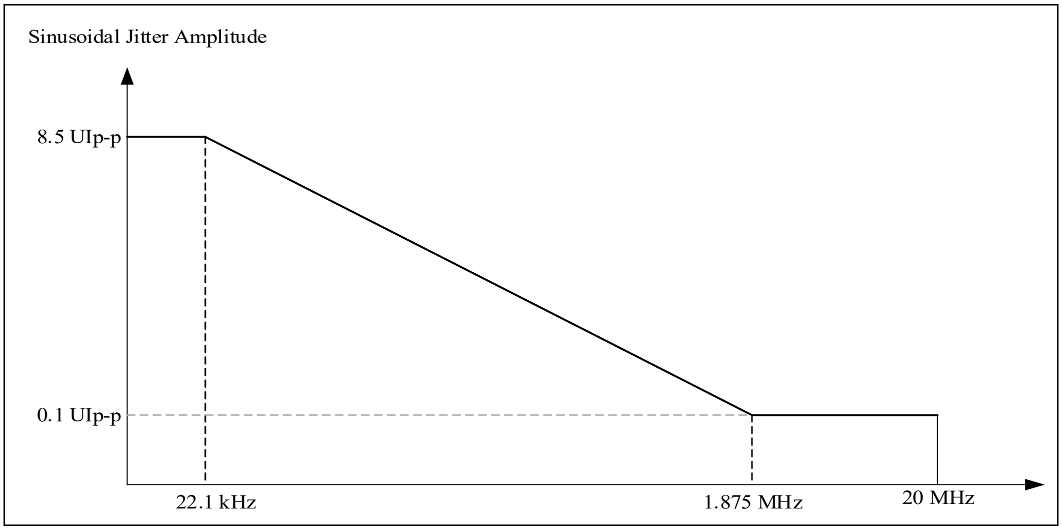


Table 25. XAUI Loss, Skew and Jitter Budge

	Loss (dB)[1]	Differential Skew (ps_{p-p})	Total Jitter (UI_{p-p})[3]	Deterministic Jitter (UI_{p-p})[3]
Driver	0	15	0.35	0.17
Interconnect	7.50	60	0.20	0.20
Other[2]	4.50		0.10	0.10
Total	12.10	75	0.65	0.47

Notes:
1. Budgetary loss in height of eye opening.
2. Includes such effects as crosstalk noise and interaction between jitter and eye height.
3. Jitter specifications include all but 10-12 of the jitter population.

§ §

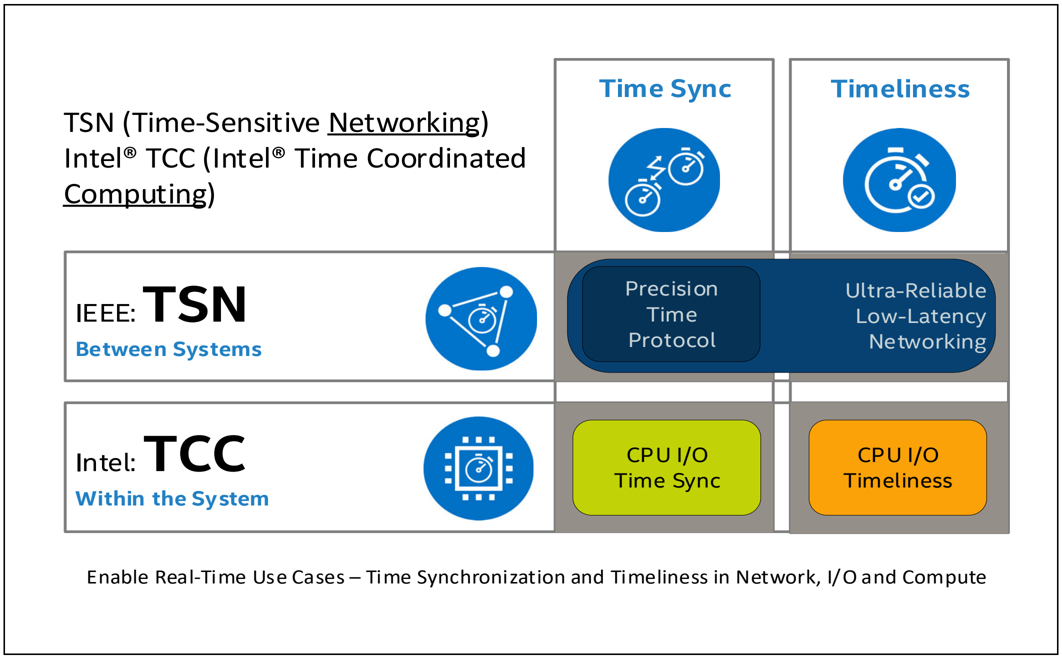
6.0 Intel® Time Coordinated Computing (Intel® TCC)

6.1 Intel® Time Coordinated Computing Introduction

Intel® Time Coordinated Computing (Intel® TCC) is ushering in a new era of coordination of computation scheduling to reduce jitter and improve performance of time-sensitive applications. Intel® TCC is not an IP block but a set of capabilities available across multiple IP blocks of the processor. Intel® TCC enhances performance along two vectors: Time Synchronization and Timeliness. Timeliness is traditionally referred to as “Real-Time” systems that are focused on the optimization. Time Synchronization provides a hardware mechanism to precisely determine how various IP specific clocks are related. Real-Time provides a hardware mechanism to minimize the latency of data packets from one IP block to another IP block.

This chapter describes the key features and requirements that compose Intel® TCC, split into the respective performance vectors. For each feature, the motivation, description, software interface (if any), hardware dependencies (if any) and formal requirements are listed.

Figure 8. Intel® TCC Features within System and TSN between Systems



6.2 Intel® Time Coordinated Computing Features

Intel® TCC helps real-time applications meet performance metrics, such as worst-case execution time (WCET). In addition, it keeps all software and hardware time-synchronized.

Intel® TCC performance is measured by the temporal determinism afforded to the critical tasks. The following section outlines the platform capabilities that enable temporal determinism.

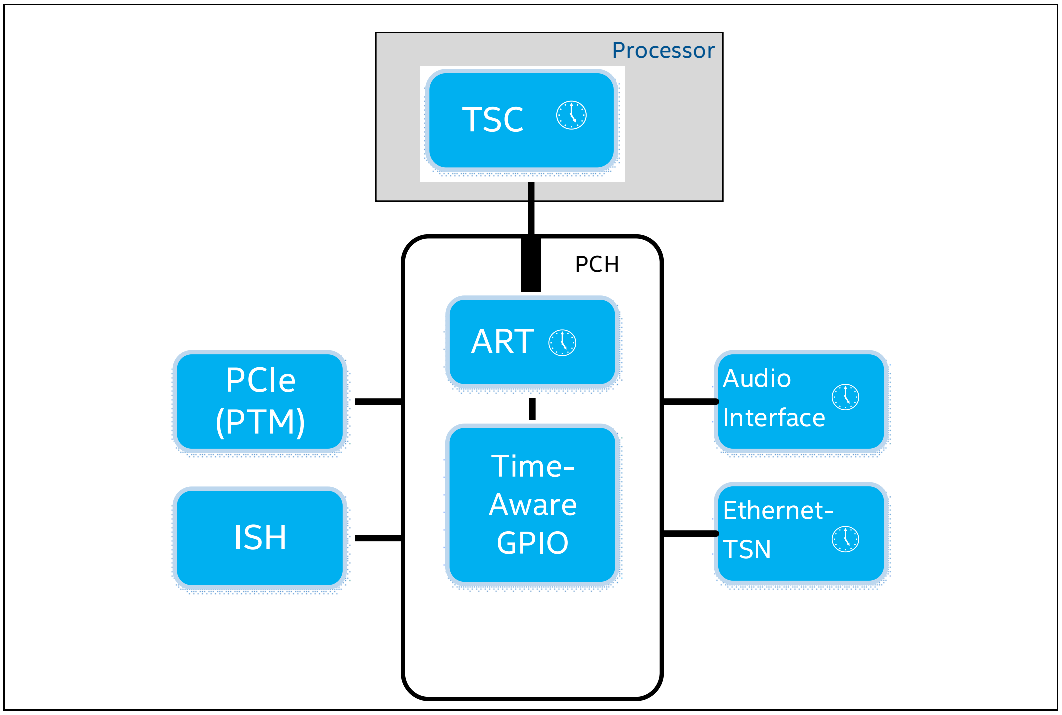
6.2.1 Time-Synchronization Support Features

The processor provides a common timekeeping framework, based on the Always Running Timer (ART) defined in Intel® 64 and IA-32 Architectures Software Developer's Manual. ART runs at the core crystal clock frequency. The ART clock is at 19.2MHz. This makes it possible for software to calculate the precise time relationship between numerous subsystems, including the CPU's time-stamp counter (TSC), the network device, Time-Aware GPIOs, and other various IPs. This processor support makes deep sub-microsecond time-correlation / synchronization possible, which is a requirement of coordinated computing, sensing, and actuation.

Processor Time-Synchronization Support provides the following:

- Global time reference based on Always Running Timer (ART)
- IEEE Std 802.1AS, the TSN standard for time synchronization across wired Ethernet network
- Global time synchronization for the following local time bases with respect to ART:
  - Ethernet Time-Sensitive Networking (TSN)
  - High Definition Audio
  - PCI Express Root-ports Precision Time Measurement (PCIe* PTM)
  - Integrated Sensor Hub (ISH)
  - Time-Aware GPIO

Figure 9. Platform Time-Synchronization Support



6.2.1.1 CPU Time Stamp Counter to I/O Time-Synchronization Support

The CPU Time Stamp Counter (TSC) Root in the Power Management Controller (PMC) is the global referenced time in the Time Synchronization architecture. The software can access the CPU TSC through the Read Time Stamp Counter (RDTSC) assembly instruction. RDTSC is based on the ART counter, which is the root of time in the system. The CPU TSC is derived from ART. ART is discoverable in the CPUID leaf 15H, and the ART relationship to all other clock domains is maintained in software.

The relation between the network device timestamp clock and ART (also TSC) is determined using cross-timestamp hardware. Using TSN the ART clock is extended outside of the platform. Refer to Section 6.2.1.3 for more information about IEEE Std 802.1AS network time synchronization.

The relation between Audio hardware clock and ART (also TSC) is determined using cross-timestamp hardware. Refer to Section 6.2.1.4 for more information about audio cross-timestamping.

The Time-Aware GPIO interface logic is driven by ART. Edge events (one shot and pulse train) can be sampled or driven with respect to the ART clock. Refer to Section 6.2.1.5 for details on Time-Aware GPIO.

6.2.1.2 Off-Chip Time-Synchronization Support via PCIe* PTM

Besides supporting known hardware, ART also extends to PCIe peripherals using Precision Time Measurement (PTM). PTM provides a hardware mechanism for PCIe devices to correlate clock domains between an end point and the root complex.

6.2.1.3 IEEE Std 802.1AS Network Time-Synchronization Support

The IEEE Std 802.1AS TSN standard extends time synchronization across multiple platforms for time-sensitive applications such as audio and video when these platforms are Ethernet connected. The integrated Ethernet MAC supports the IEEE Std 802.1AS generalized Precision Time Protocol (gPTP) event messages for network path delay measurement between two time-aware systems.

Time Synchronization utilizes the standard IEEE Std 802.1AS capability as the base feature to enable cross-platform time synchronization. At the high level, the IEEE Std 802.1AS implements the following:

- Select the best clock source on the network using the algorithm specified in IEEE Standard 802.1AS.
- Determine the propagation delay through the network
- Calculate the offset between the selected clock source and the local clock

The IEEE Std 802.1AS timer runs on its Local Time base. It supports a 19.2MHz crystal oscillator clock determined by a pin-strap based on platform configurations where it does not require any PLL to be running. The crystal oscillator continues running when Std IEEE Std 802.1AS time synchronization is enabled such that a valid time stamp is always available when gPTP event messages are transmitted or received.

6.2.1.4 Audio Cross-Timestamp

For Time Synchronization, the audio software stack handles the scheduled audio cross-timestamp such that an audio stream plays in-sync with multiple audio/video components in a network distributed system. Using audio hardware-assisted time synchronization, software can determine the relation between the best clock source and the local audio clock by determining the appropriate start time across the network on the network using the algorithm specified in IEEE

Standard 802.1AS. Any error is corrected using audio sample rate conversion by performing linear regression approximation to calculate variance. Software may utilize other information available to achieve the best audio cross-timestamp accuracy.

Before the scheduled start of the stream is carried out, software is expected to trigger a time synchronization request such that offset tracking between the Local Time base and the ART is intact and does not roll over.

6.2.1.5 Time-Aware GPIO

The PCH has two Time-Aware GPIO (TGPIO) controllers. Each controller can be independently configured to generate or capture timestamped events. TGPIO events are timestamped using the Always Running Timer (ART) clock. TGPIOs provide the following functions:

- Generate an edge or pulse at a future ART clock value
- Generate periodic pulse or square wave output with a software programmed interval
- Capture the current ART value when an edge (rising or falling) is detected
- Modulate the periodic output interval to generate an average interval that is an arbitrary fraction of the ART period and aligned with the system clock

Refer to Section 7.4 “Time-Aware GPIO Registers” for Time-Aware GPIO Registers for the registers information. The I/O from the TGPIO controllers is routed on the board via the TIME_SYNC0 and TIME_SYNC1 signals which are connected to pins M51 and BF14, respectively.

Table 26. Time-Aware GPIO Signals Description

Signal Name	Type (Voltage Domain)	Direction	Description
TIME_SYNC0	CMOS (1.8V)	Input	Time-Aware GPIO Input Signal
TIME_SYNC1	CMOS (1.8V)	Output	Time-Aware GPIO Output Signal

Notes:
1. The usage of pin groups and usage of SRCCLKREQ in the grouping requiring entire group to be 3.3V.
2. With reference to 12th Generation Intel® Core™ Processor-S RVP, the 1.8V TGPIO0 cannot be enabled due to platform limitation. The RVP design of the TGPIO is intended for 3.3V operation. Enabling TGPIO at 1.8V will cause functionality issue for the pin that intended for 3.3V design. There is no issue with 1.8V TGPIO1 and 3.3V TGPIO0/TGPIO1.

6.2.2 Real-Time Features for I/O

The processor provides hardware mechanisms to improve the worst-case, which aims to put an upper bound on the latency for data coming into the system. The following features are required to provide a bounded latency for incoming transactions.

6.2.2.1 Upstream Virtual Channels

The processor provides support for upstream virtual channels through the PCIe* and processor fabric. I/O devices are expected to make use of the PCIe base specification definition around quality of service mechanisms for data movement, specifically those related to Traffic Class. Upstream transactions that are differentiated by Traffic Class have the ability to be mapped to a separate virtual channel in an attempt to provide a low latency path to the coherent domain.

The processor PCIe* controller supports 1 virtual channel on PEG60 controller (PCIe* Gen 4).

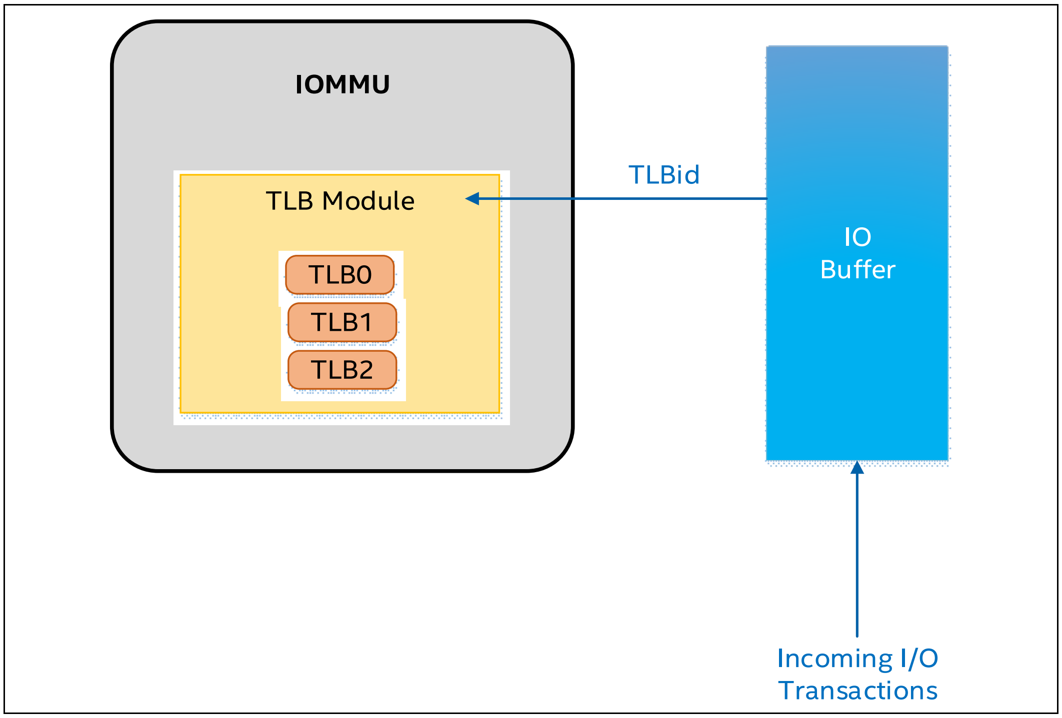
The PCH PCIe* controller supports 1 virtual channel on Ethernet-TSN controller.
Note: No virtual channel on any other controllers from PCH.

6.2.2.2 Dedicated IOTLB

The processor provides support for a dedicated I/O Translation Lookaside Buffer (IOTLB) to cache critical address translations for real-time I/O traffic.

When workload consolidation is implemented with virtualization, the I/O transactions of real-time workloads running in a virtual machine are subject to increased jitter as a result of a page walk by the I/O Memory Management Unit (IOMMU). To avoid additional page walk latency on all I/O transactions, an IOTLB is implemented in the IOMMU to cache the guest physical address to host physical address translation. There are no Quality of Service (QoS) mechanisms available on this cache, and therefore translations for time-critical addresses are subject to eviction as a result of concurrent best effort traffic.

Figure 10. IOTLB Usage



By providing a dedicated IOTLB for time-critical transactions, it is possible to minimize the additional latency and jitter previously introduced by the IOMMU. The processor specifies a TLBid based on the PCIe traffic class used, avoiding contention on the cache resources from concurrent best effort traffic.

6.2.3 Real-Time Features for Processor

The processor provides mechanisms to promote the reduction of execution jitter, leading to a more deterministic computing environment.

6.2.3.1 Multiple Outstanding MMIO

The processor provides support for tracking multiple downstream non-posted transactions simultaneously targeting the Memory Mapped I/O subsystem.

6.2.3.2 Alignment Check Exception on Split Lock

The processor provides support to generate an Alignment Check Exception (#AC) when an application attempts to issue a split lock.

When the LOCK prefix is used on an unaligned operand, there is the potential for the operand to span multiple cache lines. In the case where an atomic operation is necessary across two cache lines, a bus lock is executed. A bus lock stops all cores and I/Os from initiating transactions, resulting in an increase in latency. This increased latency can be significant, and many real-time applications cannot tolerate the jitter that a split lock introduces.

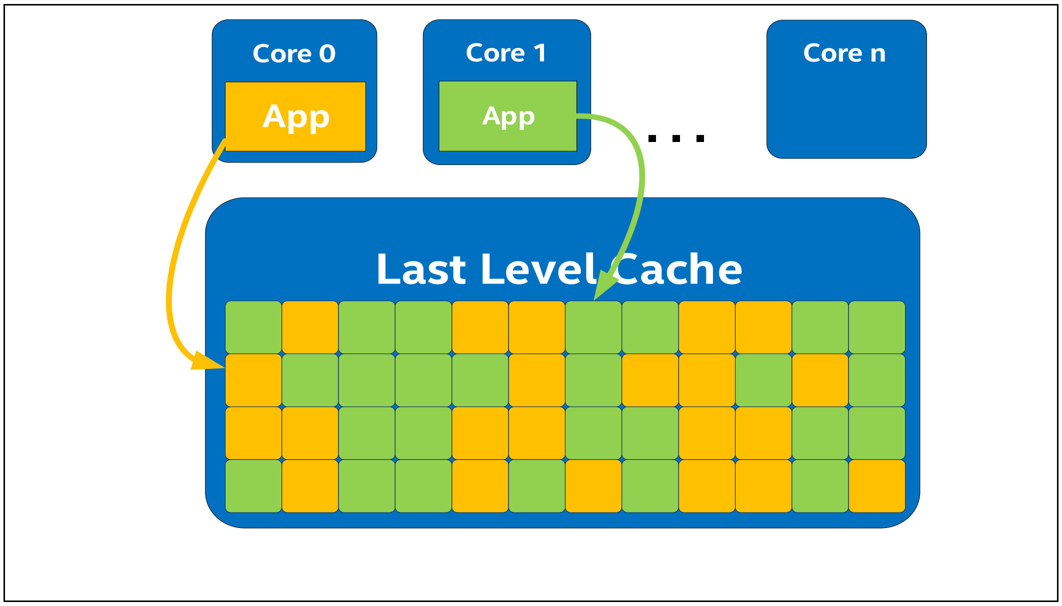
6.2.3.3 L2 and L3 Cache QoS

The processor provides support for Cache Allocation Technology (CAT), a Quality of Service (QoS) feature under the Intel® Resource Director Technology (Intel® RDT) portfolio.

On 12th Generation Intel® Core™ Processor-S that support Intel Time Coordinated Computing (Intel TCC), a model-specific, non-architectural version of L3 CAT is supported. Support for this feature will not be enumerated via CPUID leafs as indicated in the Intel Software Developers Manual. For details on how to use L3 CAT, including information on the number of classes of service, selecting the active class of service, and more, please consult the Cache Allocation Technology chapter in the Real-Time Tuning Guide for 12th Generation Intel® Core™ Processor-S.

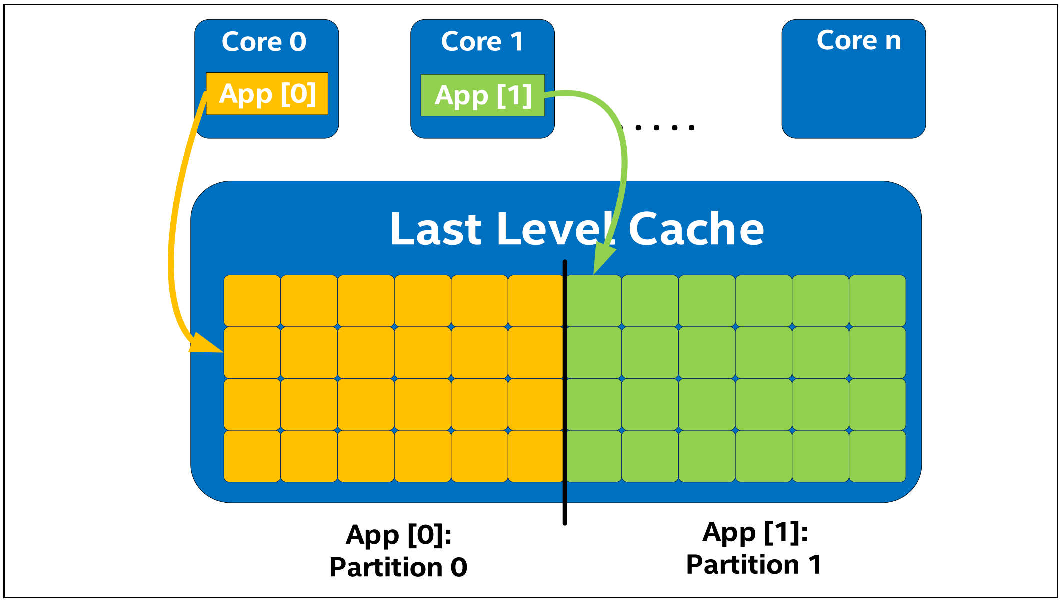
CAT helps address shared cache resource contention by providing software control of where data is allocated into the Level 2 (L2) cache and L3 cache, enabling isolation and prioritization of key applications. Without CAT, cache resources are shared between applications.

Figure 11. LLC without Cache QoS



With CAT, cache resources can be partitioned. This partitioning leads to improved performance determinism.

Figure 12. LLC with Cache QoS



6.3 Intel® Time Coordinated Computing Tools

Intel® TCC Tools provide application and middleware support, including APIs, tools, and sample applications that enable developers to access certain Intel® TCC features. Intel® TCC Tools also enable developers to analyze the behavior of real-time applications. For more information about Intel® TCC Tools beyond the scope of this document, see the Intel® TCC Tools product page listed in Section 1.2“Reference Documents”.

§ §

<This page is intentionally left blank.>