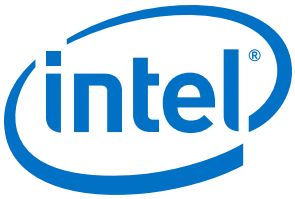

Intel® FPGA Power and Thermal Calculator User Guide

Updated for Intel® Quartus® Prime Design Suite: **20.3**


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Contents

1. Overview of the Intel® FPGA Power and Thermal Calculator

This user guide describes the Intel® FPGA Power and Thermal Calculator (PTC). The current version of the Intel FPGA PTC supports Intel Agilex™ and Intel Stratix® 10 devices.

This tool does not support older devices such as the Intel Arria® 10 and Intel Cyclone® 10 families; use the corresponding Early Power Estimator if you are working with those devices.

This user guide provides guidelines for using the Intel FPGA PTC, and details about thermal parameters and the factors contributing to FPGA power consumption.

You can calculate FPGA power consumption using the Intel FPGA PTC, and for more accurate power estimation, use the Power Analyzer in the Intel Quartus® Prime software. Intel recommends that you switch from the Intel FPGA PTC to the Power Analyzer once your design is available. The Power Analyzer produces more accurate results because it has more detailed information about your design, including routing and configuration information about each of the resources in your design.

You should treat the Intel FPGA PTC results as an estimate of power, not as a specification. You must verify the actual power consumption during device operation, because the information is sensitive to the actual device and design input signals. See the appendix *Measuring Static Power* for information on how to measure device static power in a way that correlates with the way that Intel FPGA PTC reports static power.

The features of the Intel FPGA PTC include:

- The ability to estimate the power consumption of your design before creating the design or during the design process.
- The ability to import device resource information from the Intel Quartus Prime software using the **.qptc** file generated with the Intel Quartus Prime software.
- The ability to determine preliminary thermal assessments of your design.

1.1. Intel FPGA PTC Power Model Status

The Main page of the Intel FPGA Power and Thermal Calculator (PTC) shows the current power model status for the selected device. The power models in the Intel FPGA PTC can be in advance, preliminary, or final status:

- Advance power models are based on simulation results, process model projections, and design targets. Advance power models may change over time.
- Preliminary power models include post-layout simulation results, process data, and initial silicon correlation results. Preliminary power models may change over time.
- Final power models correlate to production devices with thousands of designs, and are not expected to change.

The accuracy of the power model is determined on a per-power-rail basis for both the Intel Quartus Prime Power Analyzer and the Intel FPGA Power and Thermal Calculator. For most designs, the Power Analyzer and the Intel FPGA PTC have the following accuracies, assuming final power models:

- Intel Quartus Prime Power Analyzer: Within 10% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates.
- Intel FPGA Power and Thermal Calculator: Within 15% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates.

1.2. Definitions of Power Terms Used in this Document

The total power consumption of an Intel Agilex or Intel Stratix 10 device consists of the following components:

- Static power—the power that the configured device consumes when powered up but no user clocks are operating. Static power is dependent on device size, device grade, power characteristics, and junction temperature. For Intel Stratix 10 devices, this excludes DC bias power of analog blocks, such as I/O and transceiver analog circuitry.
- Dynamic power—the additional power consumption of the device due to signal activity or toggling.
- Standby power—for Intel Stratix 10 devices only: additional power, independent of signal activity or toggling, that is consumed only when specific circuitry is enabled through configuration RAM settings. Standby power includes, but is not limited to, I/O and transceiver DC bias power.

2. Setting Up the Intel FPGA Power and Thermal Calculator

2.1. Availability

For Intel Agilex and Intel Stratix 10 devices, the Intel FPGA Power and Thermal Calculator (PTC) is integrated with the Intel Quartus Prime software. You can access the Power and Thermal Calculator from the **Tools** menu in the Intel Quartus Prime software, or by running the `quartus_ptc` command in your command shell.

For the convenience of designers who may be working only on power estimation and not running design compilations with the Intel Quartus Prime software, a standalone version of the Intel FPGA PTC is also available. The standalone version offers all the same features as the Intel FPGA Power and Thermal Calculator version integrated within the Intel Quartus Prime software.

2.2. Obtaining the Standalone Intel FPGA Power and Thermal Calculator

The standalone Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) is available from the *Additional Software* tab of the Intel Quartus Prime Pro Edition page of the *Download Center for FPGAs*.

Launching the Standalone Version

- To launch the Windows version of the standalone Intel FPGA PTC, click the icon in the **Start** menu.
- To launch the Linux version of the standalone Intel FPGA PTC, navigate to the folder where you installed the Intel FPGA PTC, and type `ptc` <Enter>.

2.3. Estimating Power Consumption with the Intel FPGA Power and Thermal Calculator

With the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC), you can estimate power consumption at any point in your design cycle.

The Intel FPGA PTC lets you estimate the power consumption when you have not yet begun your design, or when your design is only partially complete. Although the Intel FPGA PTC can provide a power estimate for your completed design, Intel recommends

that you use the Power Analyzer in the Intel Quartus Prime software when the design is available, for a more accurate estimate based on the exact placement and routing information of the completed design.

2.3.1. Estimating Power Consumption Before Starting the FPGA Design

Table 1. Advantage and Constraints of Power Estimation before Designing FPGA

Advantage	Constraint
• You can obtain power estimates before starting your FPGA design. • You can adjust design resources and parameters and see how those changes affect total power consumption.	• Accuracy depends on your inputs and your estimate of the device resources. Where this information may change (during or after your design is complete), your power estimation results will be less accurate. • The Intel FPGA PTC uses averages and not the actual design implementation details. The Power Analyzer has access to the full design details. For example, the Intel FPGA PTC uses average values for ALM configuration, while the Power Analyzer uses an exact configuration for each ALM.

To estimate power consumption with the Intel FPGA PTC before starting your FPGA design, follow these steps:

1. On the Main page of the Intel FPGA PTC, select the target device, device grade, package, and transceiver grade from the **Device**, **Device Grade**, **Package**, and **Transceiver Grade** drop-down lists.
2. Enter values for each page in the Intel FPGA PTC. Different pages display different power-consuming FPGA resources, such as clocks and phase-locked loops (PLLs).
3. The calculator displays the total estimated power consumption in the **Total Power** cell of the Power Summary.
4. Save the file as `<project_name>.ptc` for later use.

Note: For information on the individual pages of the Intel FPGA PTC, refer to the Power and Thermal Calculator Pages chapter.

2.3.2. Estimating Power Consumption While Creating the FPGA Design

If your FPGA design is partially complete, you can import a **.qptc** file (`<revision name>.qptc`) generated by the Intel Quartus Prime software into the Intel FPGA Power and Thermal Calculator. After importing the information from the **.qptc** file into the Intel FPGA PTC, you can edit the Intel FPGA PTC data to reflect the device resource estimates for your final design.

If you have instructed the Intel Quartus Prime Power Analyzer (QPA) to produce a **.qptc** file (see the **Processing ➤ Power Analyzer** menu in the Intel Quartus Prime software), the following assignment is written to the **.qsf** file:

```
set_global_assignment -name POWER_AND_THERMAL_CALCULATOR_EXPORT_FILE <filename>
```

When you open the Intel FPGA PTC with a Quartus project (either from the **Tools** menu, or if you specified a project on the `quartus_ptc` command line) it looks for this QSF assignment and attempts to open the specified file. If the specified file isn't found, an error message occurs. After dismissing the error message, you are free to use the Intel FPGA PTC to enter design information. If you want, you can remove this QSF assignment to suppress the error message when opening the Intel FPGA PTC.

Table 2. Advantages and Constraints of Power Estimation if your FPGA Design is Partially Complete

Advantage	Constraint
• You can perform power estimation early in the FPGA design cycle. • You can adjust design resources and parameters and see how those changes affect total power consumption. • Provides the flexibility to automatically populate the Intel FPGA PTC based on the Intel Quartus Prime software compilation results.	• Accuracy depends on your inputs and your estimate of the device resources; where this information may change (during or after your design is complete). Your power estimation results may be less accurate. • Unlike the Power Analyzer, which has access to the full design details, the Intel FPGA PTC uses averages and not the actual design implementation. For example, the Intel FPGA PTC uses average values for ALM configuration, while the Power Analyzer uses an exact configuration for each ALM.

Importing a File

Importing a **.qptc** file saves you time and effort otherwise spent on manually entering all the information into the Intel FPGA PTC. You can also manually change any of the values after importing a file.

You can create a **.qptc** file for an Intel Agilex- or Intel Stratix 10-based design, by selecting **Generate Power and Thermal Calculator Import File** from the **Project** menu in the Intel Quartus Prime software.

Importing Data into the Intel FPGA Power and Thermal Calculator

You must import the **.qptc** file into the Intel FPGA PTC before modifying any information. Also, you must verify all your information after importing a file.

Importing a file from the Intel Quartus Prime software populates all input values based on your design and design settings that were specified in the Intel Quartus Prime software. Alternatively, you can import values exported from an earlier version of the Intel FPGA PTC.

To import data into the Intel FPGA PTC, follow these steps:

1. On the **File** menu, click **Open**.
2. Browse to an existing Intel FPGA PTC file generated by the current or earlier version of the Intel FPGA PTC or the Intel Quartus Prime software, and click **Open**.
3. After the file is imported into the Intel FPGA PTC, the mouse cursor changes from busy to normal. If there are any warnings during the import, the Intel FPGA PTC displays the **PTC Import Warnings** dialog box. Analyze each warning carefully to understand the cause; if any of the warnings are unexpected, you must manually modify the corresponding fields in the Intel FPGA PTC after the import is completed. You can copy all warning messages to the clipboard for future reference by clicking **Copy**. Click **OK** to dismiss the **PTC Import Warnings** dialog box. (Examples of warnings that could occur, would be if device ordering codes

had changed such that previous values for Device Grade, Device, and Package and Transceiver Grade fields could not be imported directly, or if the V_{CC} voltage isn't applicable to the selected device.)

Importing .qptc Data for Intel Stratix 10 Devices into the Intel FPGA Power and Thermal Calculator for Intel Agilex Devices

If you want to import a data file originally exported from the Intel Quartus Prime software based on a design targeting Intel Stratix 10 devices, for use in the Intel Agilex version of the Intel FPGA Power and Thermal Calculator, follow these steps:

1. In the Intel Stratix 10 version of the Power and Thermal Calculator, open the existing **.qptc** file generated by the Intel Quartus Prime software based on a design targeting an Intel Stratix 10 device.
2. Save the file as a **.ptc** file, and exit the Intel Stratix 10 Power and Thermal Calculator.
3. Launch the Intel Agilex version of the Power and Thermal Calculator, and open the **.ptc** file created in step 2.
4. Select the appropriate Intel Agilex device and modify resources and other settings to reflect your planned design targeting the Intel Agilex device.

Importing an Early Power Estimator file from an Earlier Version to the Intel FPGA Power and Thermal Calculator (For Intel Stratix 10 devices only)

If you want to import a **.csv** file originally exported from the Intel Quartus Prime software version 19.4, or from the Early Power Estimator spreadsheet version 19.4, for a design targeting an Intel Stratix 10 device, for use in the Intel Stratix 10 version of the Power and Thermal Calculator version 20.3, follow these steps:

1. Open the Early Power Estimator **.csv** file exported from the 19.4 version of the Intel Quartus Prime software or Early Power Estimator spreadsheet in the Intel Stratix 10 version of the Power and Thermal Calculator.
2. Save the file as a **.ptc** file, and exit the Intel Stratix 10 Power and Thermal Calculator.

Note: Some general points about the import process:

- A **.qptc** file created for an Intel Agilex or Intel Stratix 10 design, can always be imported into the Intel FPGA PTC for use with the same device family.
- A **.ptc** file created for an Intel Stratix 10 design can be imported into the Intel FPGA PTC for use with the similar design targeting an Intel Agilex device.
- A **.qptc** file created for an Intel Agilex design, cannot be imported into the Intel FPGA PTC for use with an Intel Stratix 10 design.
- Some power-consuming resources — such as transceivers — of an original Intel Stratix 10 design, might not be carried through the import process.

2.3.3. Estimating Power Consumption After Completing the FPGA Design

If your design is complete, Intel strongly recommends that you do not use the Power and Thermal Calculator, and instead use the Power Analyzer in the Intel Quartus Prime software. The Power Analyzer uses toggle rates from simulation, user assignments, and placement-and-routing information to provide more accurate power estimates.

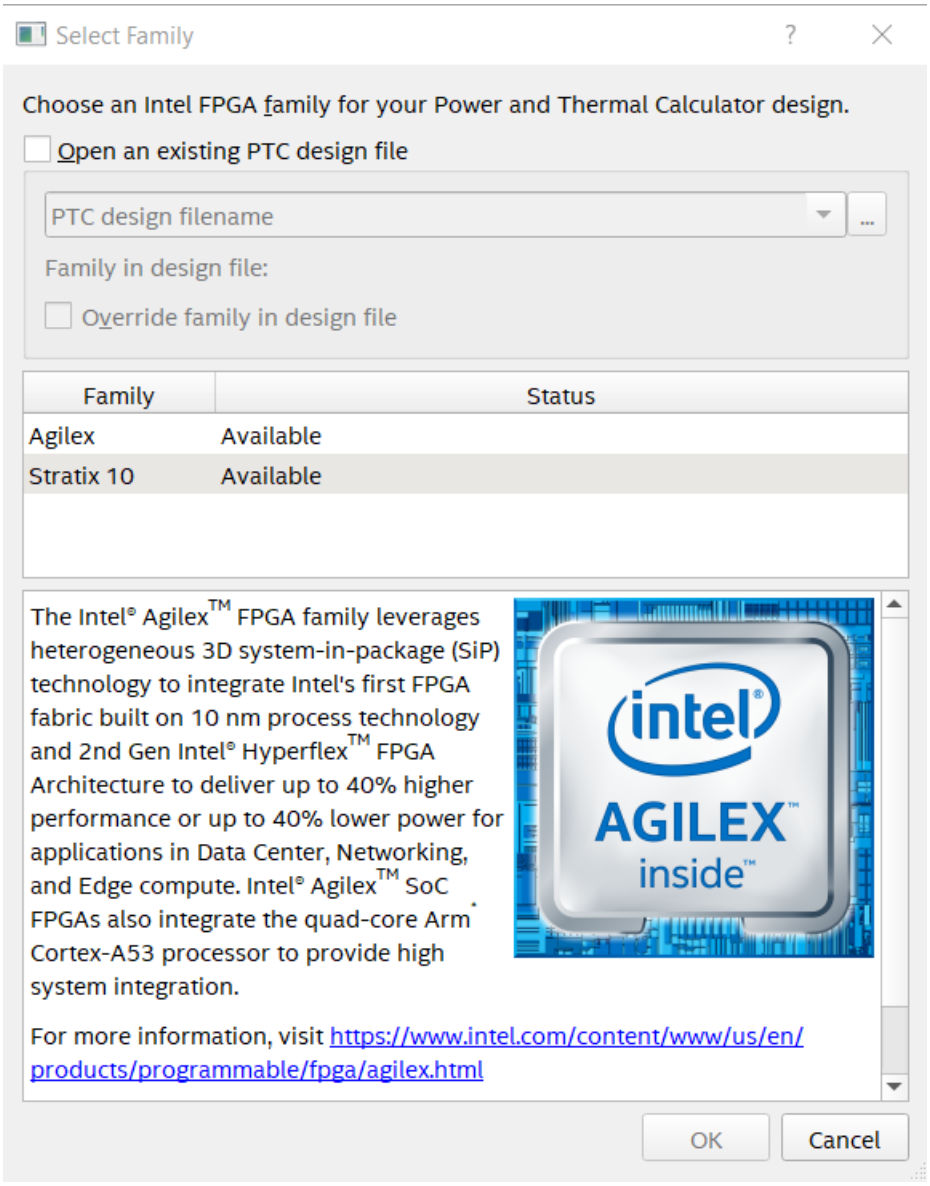
3. Intel FPGA Power and Thermal Calculator Graphical User Interface

The Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) employs a standard graphical user interface (GUI) similar to other tools in the Intel Quartus Prime software.

3.1. Intel FPGA PTC Select Family Dialog Box

When you launch the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC), the first dialog box that appears allows you to select the Intel FPGA family for your Intel FPGA PTC design.

Figure 1. Select Family Dialog Box



To proceed with the Intel FPGA PTC, select the desired device family, and click **OK**.

Note:

1. Once you have selected a device family to model, you cannot change that selection unless you start a new Intel FPGA PTC instance.
2. Currently, the Intel FPGA PTC supports the Intel Agilex and Intel Stratix 10 FPGA device families. You will notice some differences on the Intel FPGA PTC pages, depending on the device family selected.

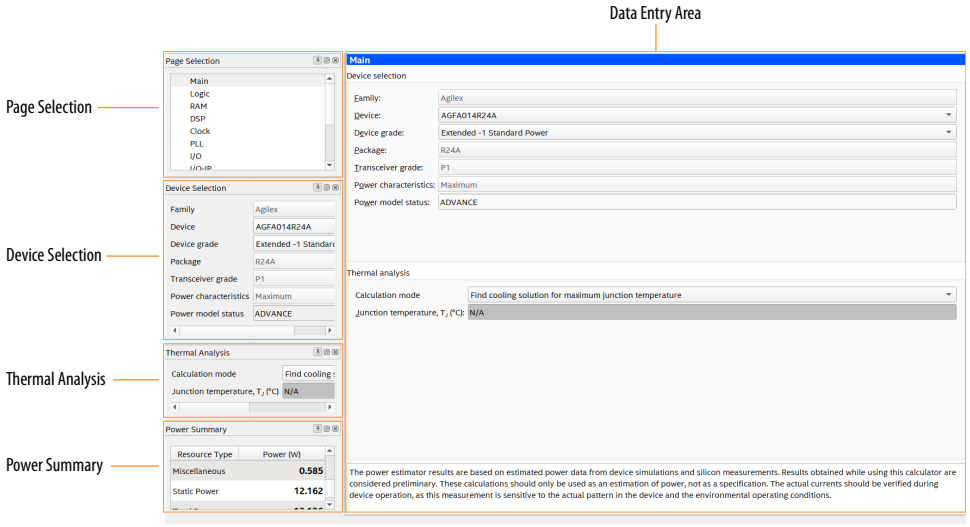
3.2. Intel FPGA PTC Basic GUI Components

The Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) GUI provides data entry pages, and dockable **Power Summary**, **Device Selection**, **Page Selection**, and **Thermal Analysis** windows.

Not all dockable windows may be visible by default. You can change which of the dockable windows are visible using the **View** menu.

The shading of input fields alternates between white and light gray; these fields are editable, either by double-clicking and selecting a value from a drop-down list or by typing a value directly. Output fields are shaded in a darker gray. Fixed input fields—those whose values are determined by settings elsewhere and therefore aren't directly editable—have their font dimmed.

Figure 2. Intel FPGA PTC Graphical User Interface (GUI)



Data Entry Area

The data entry area provides pages for entering parameters associated with various aspects of your design.

Power Summary

The Power Summary shows the calculated power consumption of various types of resources, based on the current values in the data entry pages. The fields of the Power Summary cannot be edited directly.

Device and Thermal Analysis Pages

The **Device** and **Thermal Analysis** windows summarize device characteristics and presumed thermal operating conditions, respectively. This information is also available on the **Main** and **Thermal** data entry pages, respectively.

Page Selection

The **Page Selection** window allows you to choose the data entry page that you want to display.

3.2.1. Intel FPGA PTC Data Entry Pages

The look and feel of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) is the same whether you are using the standalone version or the version integrated within the Intel Quartus Prime software. There are, however, differences depending on whether you are targeting Intel Agilex or Intel Stratix 10 devices.

The following are the pages within the Intel FPGA PTC:

- The **Main** page allows you to enter device, package, and cooling information, and displays thermal analysis information pertaining to constant junction temperature.
- The **Logic** page allows you to enter logic resources for all modules in your design.
- The **RAM** page represents design modules using RAM blocks. Among other information, enter RAM type, data width, RAM depth (if applicable), RAM mode, and port parameters.
- The **DSP** page represents DSP design modules. Among other information, enter DSP configuration, clock frequency, toggle percentage, and register usage.
- The **Clock** page represents clock networks of separate clock domains.
- The **PLL** page represents one or more PLLs in the device.
- The **I/O** page represents design modules using general-purpose I/O pins. This page does not apply to transceiver I/O pins. Among other information, enter I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load.
- The **I/O-IP** page represents design modules using complex I/O IP, such as DDR.
- The **Transceiver** page allows you to enter transceiver resources and their settings for all modules in your design.
- The **HPS** page applies to devices with HPS.
- The **HBM** page (Intel Stratix 10 devices only).
- The **Thermal** page.
- The **Report** page shows per-rail currents calculated by the Intel FPGA Power and Thermal Calculator (PTC).
- The **Intel Enpirion®** page.

3.2.2. Intel FPGA PTC Field Types

The Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) employs input fields with which you configure the tool for your design; the shading of input fields alternates between white and light gray. These fields are editable, either by double-clicking and selecting a value from a drop-down list or by typing a value directly.

Output fields report calculated values, and are shaded in a darker gray. Fixed input fields have their font dimmed.

3.2.3. Intel FPGA PTC Input Field Dependencies

The value you specify for some input fields may affect the allowed values for other fields.

For example, the device package that you select may determine what transceiver grades are selectable. If you change the selected device package, and the currently selected transceiver grade is still legal for the new package, the **Transceiver Grade** value does not change. However, if the currently selected transceiver grade is not compatible with the selected device package, the **Transceiver Grade** value automatically changes to one of the legal values.

Changes that you make on one page may affect values on another page, because of dependencies between input fields. For example, if you select a device that does not support the current I/O standard specified in the I/O page, that I/O standard automatically changes to one of the I/O standards supported by the new device.

In general, the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) does not automatically change an input value unless it is necessary to preserve the legality of the input. Changes in one field have minimal impact on other fields, while ensuring that overall combination of field values are legal. However, this can sometimes lead to unanticipated results. Consider the following example:

Assume that **Dev1** is selected in the Main page, and I/O standard **IO1** is selected in the I/O page. Assume also that device **Dev1** supports I/O standards **IO1** and **IO2**. Suppose that you change the device selection to **Dev2**, which supports only one I/O standard, **IO2**. As a result of you changing the device selection, the I/O standard in the I/O page changes to **IO2**. If you then reverted the device selection back to **Dev1**, the I/O standard does not change, because **IO2** is a legal I/O standard value for the device **Dev1**. The important point to note, is that the changing of device from **Dev1** to **Dev2** and back again, had the—potentially unintended—consequence of changing the I/O standard in the I/O page.

Note: In most cases, field dependencies are limited to the same page, and often even within the same row. However, device, device grade, package and transceiver grade selection can have a much wider impact, as illustrated above. A simple way to verify that no unintended changes resulted from changing a device is to use the **File ➤ Save As** function to export the Intel FPGA PTC state before and after the change in device selection. You can then compare the two `.ptc` files using a third-party *diff* utility to identify any fields that have changed.

3.2.4. Intel FPGA PTC Data Entry Error Messages

If the value you enter does not pass legality checks, or is inappropriate for the field, the system displays an error message. Typically the message may indicate the conditions under which a value is invalid, or specify a valid range of values.

Error Message Type: Invalid Value

If you enter an invalid value — such as a temperature value that is outside the allowed range for a selected family, device, transceiver grade, device grade and package combination — an error message appears, indicating that the entered value is invalid and stating the allowed range of values. You can click OK to dismiss the error message, and the field reverts to its previous value.

Error Message Type: Incorrect Format

Many fields require a specific type of data. If the data you enter is not of the type required, an error message appears. For example, if an integer value is expected and you enter a fractional value, the resulting error message indicates that the entered value cannot be converted to a valid value for the input field. After you click OK, the field reverts to its previous value.

Similarly, if a numerical value is expected and you enter a text value, the resulting error message indicates that the entered value cannot be converted to a valid value for the input field. After you click OK, the field reverts to its previous value.

4. Intel FPGA Power and Thermal Calculator Pages

The Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) is a tool that allows you to enter information onto pages based on architectural features. The Intel FPGA PTC then reports, in watts, subtotals of the power consumed by each architectural feature. For more information about each architectural feature refer to the respective page descriptions.

Note: Currently, the Intel FPGA PTC supports the Intel Agilex and Intel Stratix 10 FPGA device families. You will notice some differences on the Intel FPGA PTC pages, depending on the device family selected.

4.1. Intel FPGA PTC - Power Summary

The **Power Summary** tile of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) can be displayed at all times, and shows the calculated power consumption by resource type.

The values displayed in the **Power Summary** update in real time, as you change parameters on the data entry pages.

In addition to displaying total power consumption, the **Power Summary** displays power consumption values for the resource types listed in the following table.

Table 3. Resource Types Displayed in the Power Summary

Intel Agilex PTC Power Summary	
Resource Type	**Description**
Logic	The dynamic power consumed by adaptive logic modules (ALMs), flipflops (FFs) and routing fabric.
RAM	The dynamic power consumed by specialized blocks optimized for data storage and retrieval.
DSP	The dynamic power consumed by specialized blocks optimized for fast math operations.
Clock	The dynamic power consumed by clock networks. The clock dynamic power is affected by the selected device.
PLL	The dynamic power consumed by phase-locked loops (PLLs).
I/O	The dynamic power consumed by I/O pins and I/O subsystems.
Transceiver	The dynamic power consumed by transceiver blocks.
HPS	The dynamic power consumed by the hard processor system (HPS).
HBM	The dynamic power consumed by high-bandwidth memory (HBM) and the universal interface bus (UIB) modules.

continued...

Miscellaneous	The dynamic power consumed by other FPGA circuitry not included in other categories above.
Static Power	The power that the configured device consumes when powered up but with no user clocks operating. The static power (P_{STATIC}) is the power dissipated on the chip, independent of design activity. P_{STATIC} includes the static power from all FPGA functional blocks. P_{STATIC} is the only power component that varies with junction temperature and power characteristics (process). P_{STATIC} is also the only power component that varies significantly with selected device.
Total Power	The total power dissipated as heat from the FPGA. Does not include power dissipated in off-chip termination resistors. Total power dissipation in the FPGA may differ from the sum of power on all rails due to several factors including, but not limited to, power dissipated in off-chip termination resistors.
Intel Stratix 10 PTC Power Summary	
Resource Type	**Description**
Logic	The dynamic power consumed by adaptive logic modules (ALMs), flipflops (FFs) and associated routing.
RAM	The dynamic power consumed by RAMs and associated routing.
DSP	The dynamic power consumed by digital signal processing (DSP) blocks and associated routing.
Clock	The dynamic power consumed by clock networks. The clock dynamic power is affected by the selected device.
PLL	The dynamic and standby power consumed by phase-locked loops (PLLs).
I/O	The dynamic and standby power consumed by I/O pins and I/O subsystems.
Transceiver	The dynamic and standby power consumed by transceiver blocks.
Hard Processor	The dynamic and standby power consumed by the hard processor system (HPS).
High-Bandwidth Memory	The dynamic power consumed by high-bandwidth memory (HBM) and the universal interface bus (UIB) modules.
Static Power	The static power consumed regardless of clock frequency. This includes static power consumed by I/O and transceiver blocks, but does not include standby power.
Total, Before SmartVID Savings	The total power consumption before SmartVID power savings. Includes static power (PSTATIC) and power consumed by different blocks as reported above. Does not include power dissipated in off-chip termination resistors.
SmartVID Savings	The total power reduction (static and dynamic) resulting from the lower voltage that is made possible by SmartVID. This power reduction is dependent on the user design and device characteristics. The combination of these factors may result in different static and dynamic power savings, so the exact dynamic and static components are not identified separately, and the power reduction reported here is a worst-case result. The reduction reported in this field is already taken into consideration in the Total (W) field. The SmartVID Power Savings field applies only to devices that support SmartVID and only when Power Characteristics is set to Maximum.
Total Power	The total power dissipated as heat from the FPGA. Does not include power dissipated in off-chip termination resistors. Total power dissipation in the FPGA may differ from the sum of power on all rails due to several factors including, but not limited to, power dissipated in off-chip termination resistors.

4.2. Intel FPGA PTC - Common Page Elements

The Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) is divided into multiple pages, each allowing entry of a subset of FPGA resources. Some elements are common to more than one page.

Recalculate mode

The **Recalculate mode** pulldown is available at the top-left corner of the PTC, regardless of which page is displayed. The available settings are *Automatic* and *Manual*:

- Automatic: In *Automatic* mode, the system automatically recalculates all field values whenever you modify an input value. *Automatic* is the default mode.
- Manual: In *Manual* mode, the system does not recalculate values automatically. To recalculate, you must press the blue button immediately to the right of the **Recalculate mode** pulldown.

Tip: In *Automatic* mode, the system may appear to become unresponsive while recalculating. If you are making multiple changes, you may find it a better experience to select *Manual* mode, and recalculate only once, after you have entered all your changes.

Total Thermal Power

The Total thermal power field estimates the total thermal power consumed by all FPGA resources on the specific page. Some pages may also provide a breakdown of the components contributing to the total thermal power. The total thermal power displayed in individual pages does not include static power, which is reported in the Power Summary for the whole device.

Thermal power is the power dissipated in the device. Total thermal power is the sum of the thermal power of all the resources used in the device, including dynamic power. Total thermal power includes only the thermal component for the I/O page and does not include external power dissipation, such as from voltage-referenced termination resistors.

Resource Utilization

Most pages contain one or more fields that provide an estimate of the percentage resource utilization for the modules in the specific page. Such values are calculated based on the maximum available resources of a given type for a selected device. If resource utilization exceeds 100%, it indicates that the current device may not be able to support the resources entered into the page.

Power Rail Current Consumption

Most pages include a table showing the dynamic current consumption for all power rails used by the FPGA resources in the specific page. The same power rail may appear in multiple pages, and the dynamic currents reported in the **Report** page are the sums of all corresponding currents for a given rail at a given voltage in individual pages. The **Report** page also includes static currents, which are not reported in individual pages.

Note: If you want to resize columns within a page, that is most easily done with the page size maximized. You can also resize all columns on all pages by selecting **View ➤ Resize All Columns**, or by pressing F5 on your keyboard.

4.3. Intel FPGA PTC - Device Selection and Thermal Analysis Windows

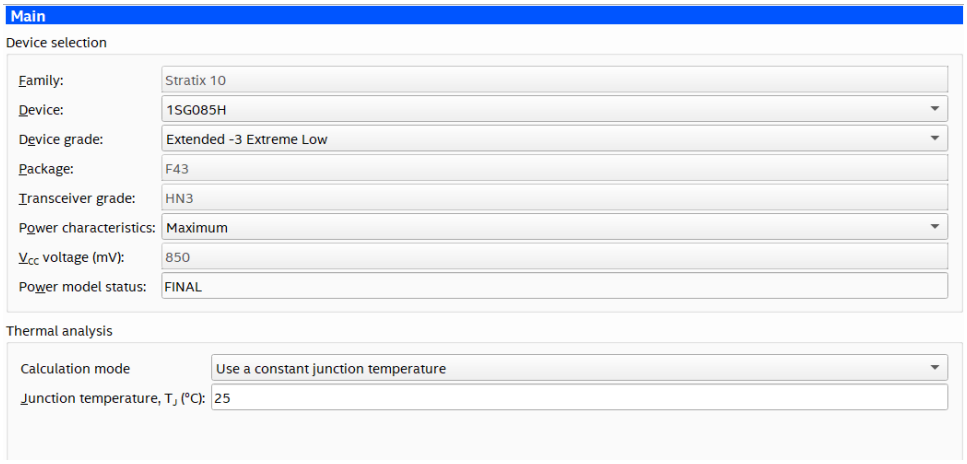
The **Device Selection** window displays information also available on the **Main** page; the **Thermal Analysis** window displays a subset of the information available on the **Thermal** page.

The **Device Selection** and **Thermal Analysis** pages can be displayed at all times, allowing you to view this information while working on a page other than the **Main** page.

4.4. Intel FPGA PTC - Main Page

The Main page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) allows you to enter device, package, and cooling information, and displays thermal analysis options.

Figure 3. Intel FPGA PTC Main Page



The required parameters depend on whether the junction temperature is manually entered or auto computed.

Table 4. Device Selection Parameters

Parameter	Description
Family	Shows the device family selected at startup, either directly or through the imported file.
Device	Select your device. Larger devices consume more static power and have higher clock dynamic power. All other power components are unaffected by device selection.
Device Grade	Select the combination of Operating Temperature, Speed Grade, and Power Option used. Refer to the device datasheet for available combinations.
Package	Select the device package. Larger packages provide a larger cooling surface and more contact points to the circuit board, thus they offer lower thermal resistance. Package selection does not affect dynamic power directly.

continued...

Parameter	Description
Transceiver Grade	Select the transceiver grade. *Note:* For information on transceiver grades, refer to the *Device Overview* document for a given device family.
Power characteristics	Select typical or theoretical worst-case silicon process. There is a process variation from die-to-die. This variation primarily affects static power consumption. If you choose *Typical* power characteristics, estimates are based on longterm projections of average power consumed by typical silicon. For FPGA board power supply design and thermal design, choose *Maximum* for worst-case values. (The *Typical* option is not yet available for Intel Agilex devices.)
V_{CC} Voltage (mV)	(This field appears in the Intel Stratix 10 PTC only.)
Power Model Status	Indicates whether the power model for the device is in advance, preliminary, or final status.

The Thermal Analysis section displays the junction temperature (T_J) and other thermal parameters, depending on the thermal analysis mode.

Table 5. Thermal Analysis

Column Heading	Description
Calculation mode	Specifies the conditions at which to run thermal analysis.
Junction temperature, T_J (°C)	Specify the junction temperature for all dies in the package. *Note:* This field is applicable only when the selected **Calculation mode** value is **Use a constant junction temperature**.

You can directly enter or automatically compute junction temperatures based on the information provided. To enter the junction temperature, select **Use a constant junction temperature** in the **Calculation mode** field, then enter the desired junction temperature in the **Junction temperature T_J (°C)** field in the **Thermal Analysis** section. In this mode, the junction temperatures for all dies in the package are assumed to have the specified value. To automatically compute junction temperatures, select one of the other options in the same field.

4.5. Intel FPGA PTC - Logic Page

The Logic of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) allows you to enter logic resources for all modules in your design.

Figure 4. Logic Page of the Intel FPGA PTC

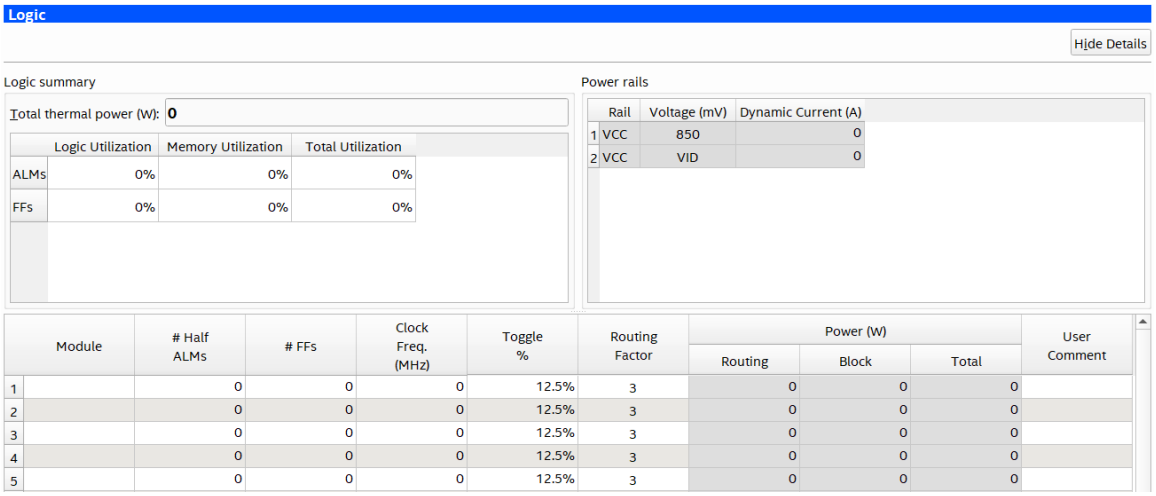


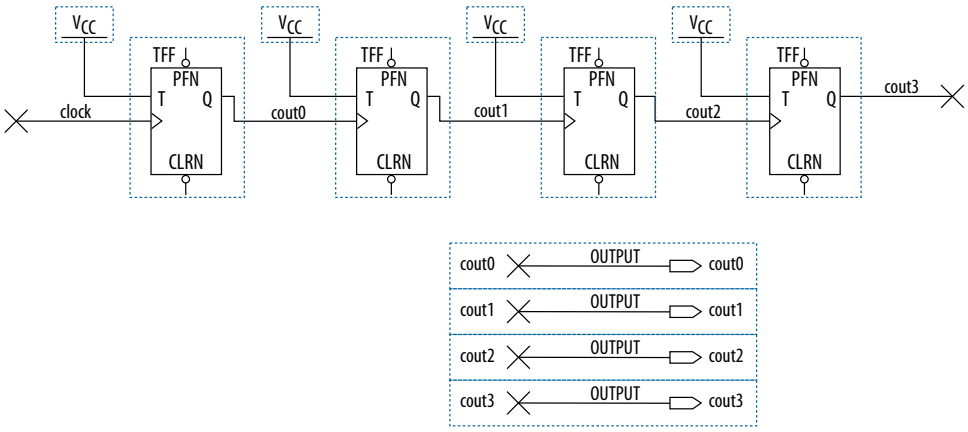
Table 6. Logic Page Information

Column Heading	Description
Module	Specify a name for each module of the design. This is an optional entry.
#Half ALMs	Enter twice the number of Adaptive Logic Modules (ALMs) used in your design, which you can find in the Compilation Report, by selecting **Fitter ➤ Place Stage ➤ Resource Usage Summary**. For power estimation purposes, the number of ALMs used in your design is the sum of the following values in the Compilation Report: • ALMs used for LUT logic and register circuitry • ALMs used for LUT logic • ALMs used for register circuitry • ALMs adjustment for power estimation The adjustment for power estimation is necessary because some unused ALMs may still consume power due to Fitter optimizations.
# FFs	Enter the number of **Primary logic registers**, plus **Secondary logic registers**, plus the number of registers reported as **Register control circuitry for power estimation**, all of which you can find in the Compilation Report, by selecting **Fitter ➤ Place Stage ➤ Resource Usage Summary**. The **Register control circuitry for power estimation** adjustment is necessary because some unused registers may still consume power due to fitter optimizations. Clock routing power associated with flipflops is calculated separately on the Clock page of the Intel FPGA PTC.
Clock Freq (MHz)	Enter a clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family. For Intel Stratix 10 devices, when you import a design from the Intel Quartus Prime software, some imported half ALMs and flipflops may have a clock frequency of 0 MHz; this can occur for one of two reasons: • The Intel Quartus Prime software did not have sufficient information to determine clock frequency due to incomplete clock constraints. • The Intel Quartus Prime software exported a `.qptc` file containing half ALMs where only flipflops are used. Such ALMs are imported as ALMs with clock frequency of 0 MHz, while their flipflops are imported into a separate row with the correct clock frequency. It is possible that due to the floating point precision used in the tool, the frequency reported may differ slightly from what is reported in the Timing Analyzer.

continued...

Column Heading		Description
Toggle %		Enter the average percentage of clock cycles when the block output signals change values. Toggle percentage is multiplied by clock frequency to determine the number of transitions per second. For example, 100 MHz frequency with a 12.5% toggle rate, means that each LUT or flipflop output toggles 12.5 million times per second (100MHz × 12.5%). The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. Most logic only toggles infrequently; therefore, toggle rates of less than 50% are more realistic. To ensure you do not underestimate the toggle percentage, use a realistic toggle percentage obtained through simulation. For example, a T flipflop (TFF) with its input tied to VCC has a toggle rate of 100% because its output is changing logic state on every clock cycle. Refer to the 4-Bit Counter Example below for a more detailed analysis. For any rows containing flipflops, toggle percentage cannot exceed 100%. A small portion of ALMs in a design may experience glitching that results in toggle percentage exceeding 100% for such ALMs. Enter such ALMs into a separate row with # FFs set to 0. For Intel Stratix 10 devices in the Intel FPGA PTC, toggle percentage cannot exceed 100% in any rows containing flipflops.
Routing Factor		Indicates the extent of the routing power of the outputs. Characteristics that have a large power impact and are captured by this factor include the following: • The fanout of the outputs • The number of routing resources used • The relative power usage of the different types of routing resources used The default value for this field is typical; the actual value varies between blocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Intel Quartus Prime software after compiling your design, because the Intel Quartus Prime software has access to detailed placement and routing information. In the absence of an Intel Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.
Power (W)	Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown are representative of routing power based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.
	Block	Indicates the power dissipation due to internal toggling of the ALMs and registers (in W). Logic block power is a combination of the function implemented and the relative toggle rates of the various inputs. The Intel FPGA PTC uses an estimate based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact synthesis of your design.
	Total	Indicates the estimated power (in W), based on information entered into the Intel FPGA PTC. It is equal to the sum of routing power and block power.
User Comment		Enter any comments. This is an optional entry.

Figure 5. 4-Bit Counter Example



The `cout0` output of the first TFF has a toggle percentage of 100% because the signal toggles on every clock cycle. The toggle percentage for the `cout1` output of the second TFF is 50% because the output toggles every two clock cycles. Similarly, the toggle percentage for the `cout2` and `cout3` outputs are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.

For more information about logic block configurations, refer to the Intel Agilex Logic Array Blocks and Adaptive Logic Modules User Guide.

4.6. Intel FPGA PTC - RAM Page

Each row in the RAM page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) represents a design module with RAM blocks of the same type, same data width, same RAM depth (if applicable), same RAM mode, and the same port parameters.

Each row in the RAM page of the Intel FPGA PTC represents a logical RAM module that you can implement using one or more physical RAM blocks. The Intel FPGA PTC implements each logical RAM module with the minimum number of physical RAM blocks, in the most power-efficient way possible, based on the specified logical width and depth.

You must know how your RAM is implemented by the Intel Quartus Prime Compiler when you are selecting the RAM block mode. For example, if a ROM is implemented with two ports, it is considered a true dual-port memory and not a ROM. Single-port and ROM implementations use only one port. Simple dual-port and true dual-port implementations use both Port A and Port B.

Note:

- The Power and Thermal Calculator reports MLAB power in the RAM page as described above, as well as in the *Power Summary* table.
- In the *Power Summary* table, the MLAB power for Intel Agilex devices is spread across three categories: RAM, Logic, and Miscellaneous; this is done to be consistent with the reporting provided in the Intel Quartus Prime Power Analyzer.

Figure 6. RAM Page of the Intel FPGA PTC

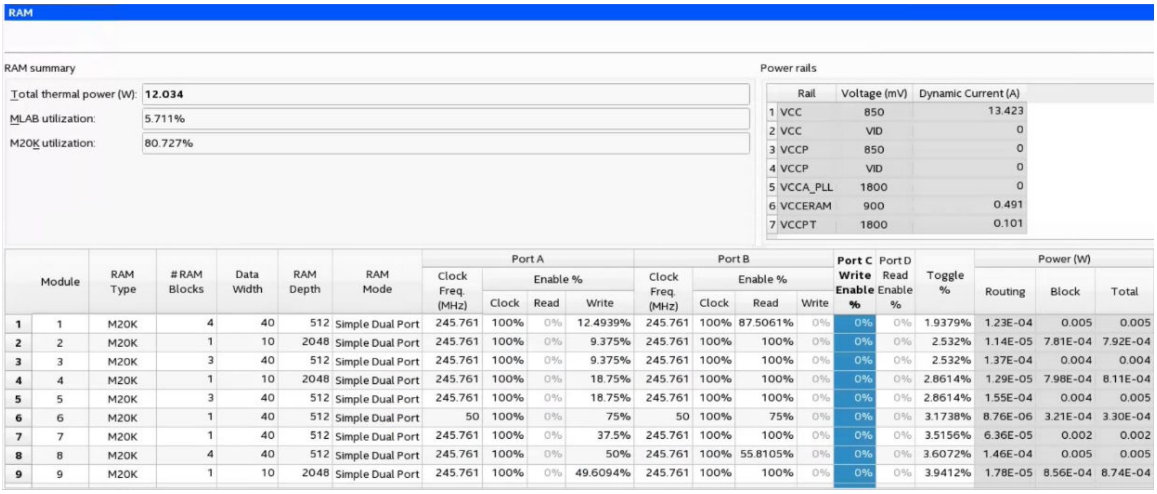


Table 7. RAM Page Information

Column Heading	Description
Module	Enter a name for the RAM module in this row. This is an optional value.
RAM Type	Select the implemented RAM type. You can find the RAM type in the *Type* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**.
# RAM Blocks	Enter the number of RAM blocks in the module that use the same memory type and mode and have the same port parameters. The parameters for each port are as follows: • Clock frequency in MHz • Percentage of time the RAM is enabled • Percentage of time the port is writing as opposed to reading You can find the number of RAM blocks in either the *MLAB cells* or *M20K blocks* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. *Note:* The value entered into this field represents the number of logical memory blocks. Depending on the specified memory depth and data width, more than one physical memory block may be required to implement one logical block. The Power and Thermal Calculator calculates the number of physical memory blocks based on the specified memory depth and data width, such that the minimum number of physical blocks is used, and assuming the most power efficient physical configuration.
RAM Data Width	Enter the width of the data for the RAM block. This value is limited based on the RAM type. You can find the width of the RAM block in the *Port A Width* or the *Port B Width* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. For RAM blocks that have different widths for Port A and Port B, use the larger of the two widths.
RAM Depth	Enter the depth of the RAM block in number of words. You can find the depth of the RAM block in the *Port A Depth* or the *Port B Depth* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**.

continued...

Column Heading	Description
RAM Mode	For MLAB and eSRAM RAM types, this field has only one possible value: Simple Dual Port. For M20K RAM type, select from the following modes: • Simple Dual Port • True Dual Port • Simple Dual Port with ECC • ROM • Simple Quad Port The mode is based on how the Intel Quartus Prime Compiler implements the RAM. If you are unsure how your memory module is implemented, you can compile a test case in the required configuration in the Intel Quartus Prime software. You can find the RAM mode in the *Mode* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. A single-port RAM has one port with a read and a write control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a read and a write control signal. ROMs are read-only single-port RAMs. A simple quad-port RAM has a total of four ports, two read ports and two write ports.
Port A - Clock Freq (MHz)	Enter the clock frequency for Port A of the RAM blocks (in MHz). This value is limited by the maximum frequency specification for the RAM type and device family.
Port A - Clock Enable %	The average percentage of time the Port A clock enable is active, regardless of activity on RAM data and address inputs. This number must be a percentage between 0% and 100%. RAM power is consumed primarily when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port A - Read Enable %	Enter the percentage of time Port A of the RAM block is in read mode. This field is applicable only for true dual port RAMs. This value must be a percentage number between 0 and 100%.
Port A - Write Enable %	Enter the average percentage of time Port A of the RAM block is in write mode. This field applies only for dual port, true dual port, and quad port RAMs. This value must be a percentage number between 0 and 100%.
Port B - Clock Freq (MHz)	Enter the clock frequency for Port B of the RAM blocks (in MHz).
Port B - Clock Enable %	Enter the average percentage of time the input clock enable for Port B is active, regardless of the activity on the RAM data and address inputs. The enable percentage ranges from 0 to 100%. RAM power is consumed primarily when a clock event occurs. Using a clock-enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port B - Read Enable %	Enter the percentage of time Port B of the RAM block is in read mode. This field is applicable only to dual port, true dual port, and quad port RAMs and ROMs. This value must be a percentage number between 0 and 100%.
Port B - Write Enable %	Enter the percentage of time Port B of the RAM block is in write mode. This field is available only for true dual-port mode. This value must be a percentage number between 0 and 100%.
Port C - Write Enable %	Enter the percentage of time the RAM block is writing to this port. In Simple Quad-Port Mode, clock and clock enable for all parts are shared and the same as Port A. This value must be a percentage number between 0 and 100%.
Port D - Read Enable %	Enter the percentage of time the RAM block is reading on this port. In Simple Quad-Port Mode, clock and clock enable for all parts are shared and the same as Port A. This value must be a percentage number between 0 and 100%.

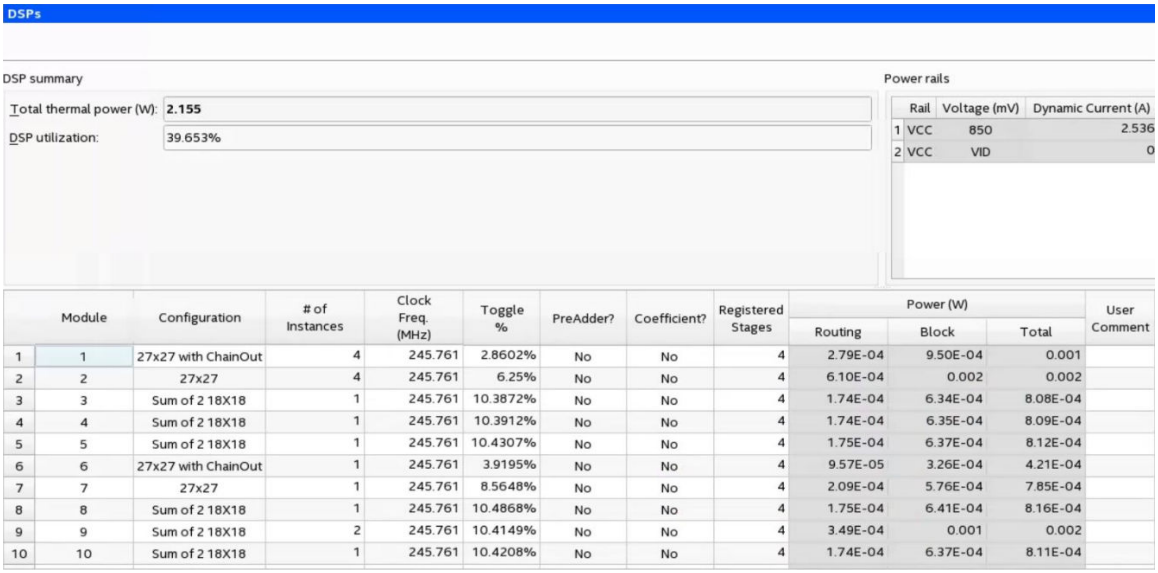
continued...

Column Heading		Description
Toggle %		The percentage of clock cycles when the block output signal changes value. This value is multiplied by the clock frequency and the enable percentage to determine the number of transitions per second. This value affects only routing power. 50% corresponds to a randomly changing signal, since half the time the signal holds the same value and thus not transition. This is considered the highest meaningful toggle rate for a RAM block.
Power (W)	Routing Power (W)	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.
	Block Power (W)	Indicates the power dissipation due to internal toggling of the RAM (in W). Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact RAM modes in your design.
	Total Power (W)	Indicates the estimated power (in W), based on information entered into the Intel FPGA PTC. Total power is equal to the sum of routing power and block power.
User Comments		Enter any comments. This is an optional entry.

4.7. Intel FPGA PTC - DSP Page

Each row in the DSP page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) represents a DSP design module where all instances have the same configuration, clock frequency, toggle percentage, and register usage.

Figure 7. DSP Page of the Intel FPGA PTC



	Module	Configuration	# of Instances	Clock Freq. (MHz)	Toggle %	PreAdder?	Coefficient?	Registered Stages	Power (W)			User Comment
									Routing	Block	Total	
1	1	27x27 with ChainOut	4	245.761	2.8602%	No	No	4	2.79E-04	9.50E-04	0.001	
2	2	27x27	4	245.761	6.25%	No	No	4	6.10E-04	0.002	0.002	
3	3	Sum of 2 18X18	1	245.761	10.3872%	No	No	4	1.74E-04	6.34E-04	8.08E-04	
4	4	Sum of 2 18X18	1	245.761	10.3912%	No	No	4	1.74E-04	6.35E-04	8.09E-04	
5	5	Sum of 2 18X18	1	245.761	10.4307%	No	No	4	1.75E-04	6.37E-04	8.12E-04	
6	6	27x27 with ChainOut	1	245.761	3.9195%	No	No	4	9.57E-05	3.26E-04	4.21E-04	
7	7	27x27	1	245.761	8.5648%	No	No	4	2.09E-04	5.76E-04	7.85E-04	
8	8	Sum of 2 18X18	1	245.761	10.4868%	No	No	4	1.75E-04	6.41E-04	8.16E-04	
9	9	Sum of 2 18X18	2	245.761	10.4149%	No	No	4	3.49E-04	0.001	0.002	
10	10	Sum of 2 18X18	1	245.761	10.4208%	No	No	4	1.74E-04	6.37E-04	8.11E-04	

Table 8. DSP Page Information

Column Heading		Description
Module		Enter a name for the DSP module in this column. This is an optional value.
Configuration		Select the DSP block configuration for the module.
# of Instances		Enter the number of DSP block instances that have the same configuration, clock frequency, toggle percentage, and register usage. This value is not necessarily equal to the number of dedicated DSP blocks you use. For example, it is possible to use two 18 × 18 simple multipliers that are implemented in the same DSP block in the FPGA devices. In this case, the number of instances would be two. To determine the maximum number of instances you can fit in the device for any particular mode, follow these steps: 1. Open the "Variable Precision DSP Blocks" chapter of the appropriate device family handbook. 2. In the "Number of DSP Blocks" table, take the maximum number of DSP blocks available in the device for the mode of operation. 3. Divide the maximum number by the "# of Mults" for that mode of operation from the "DSP Block Operation Modes" table. The resulting value is the maximum number of instances supported by the device.
Clock Freq (MHz)		Enter the clock frequency for the module (in MHz). This value is limited by the maximum frequency specification for the device family.
Clock Enable %		Specifies the percentage of time that the DSP block is enabled. (Intel Agilex devices only.)
Toggle %		Enter the average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 50%. The default value is 12.5%. For a more conservative power estimate, use a higher toggle percentage. 50% corresponds to a randomly changing signal, since half the time the signal holds the same value and thus not transition. This is considered the highest meaningful toggle rate for a DSP block.
Preadder?		Select **Yes** if the PreAdder function of the DSP block is turned on.
Coefficient?		Select **Yes** if the Coefficient function of the DSP block is turned on.
Registered Stages		Select number of the registered stages. Permitted values depend on the selected mode; some modes, such as floating-point multiply and accumulate cannot have 0 register stages.. • 0—None • 1—Input • 2—Input and Output • 3—Input, Output, and Multiplier • 4— Input, Output, Multiplier, and Pipeline Stage 2 • 5—Input, Output, Multiplier, Pipeline Stage 2, and Floating-Point Adder
Power (W)	Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs.
	Block	Indicates the estimated power consumed by the DSP blocks (in W).
	Total	Indicates the estimated power (in W), based on information entered into the Intel FPGA PTC. It is the total power consumed by the DSP blocks and is equal to the routing power and block power.
User Comments		Enter any comments. This is an optional entry.

4.8. Intel FPGA PTC - Clock Page

Each row in the Clock page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) represents a clock network or a separate clock domain.

Intel Agilex and Intel Stratix 10 devices support global, regional, and periphery clock networks. The Intel FPGA PTC does not distinguish between global or regional clocks because the difference in power is not significant.

Figure 8. Clock Page of the Intel FPGA PTC

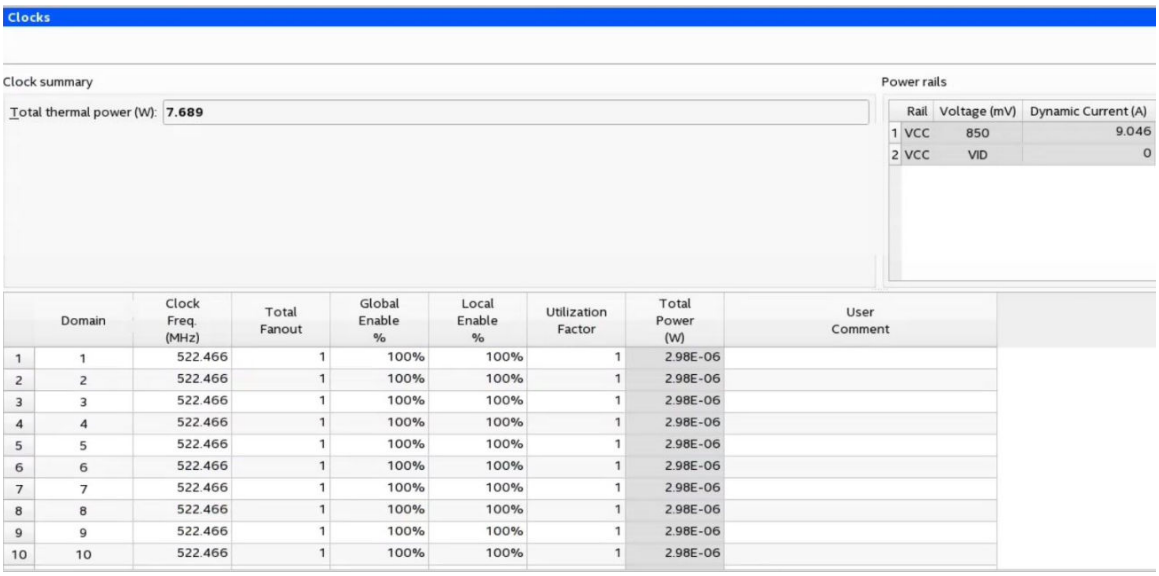


Table 9. Clock Page Information

Column Heading	Description
Module	Enter a name for the clock domain in this column. This is an optional value.
Clock Freq (MHz)	Enter the frequency of the clock domain. This value is limited by the maximum frequency specification for the device family. *Note:* When you import a design from the Intel Quartus Prime software, some imported clocks may have a frequency of 0 MHz, due to either of the following reasons: • The Intel Quartus Prime software did not have sufficient information to determine clock frequency due to incomplete clock constraints. • Clock resources were used to route a reset signal, which toggles infrequently, so its frequency is reported as 0 MHz.
Total Fanout	Enter the total number of flipflops, hyper-registers, RAMs, digital signal processing (DSP) blocks, and I/O pins fed by this clock. Power consumed by Intel Stratix 10 MLAB clocks is accounted for in the RAM page; therefore, clock fanout on this page does not include any MLABs driven by this clock domain, for Intel Stratix 10 devices. For Intel Agilex devices, MLAB is included in the fanout. The number of resources driven by every global clock and regional clock signal is reported in the *Fan-out* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Place Stage**. Select **Global & Other Fast Signals Summary** and observe the *Fan-out* value.
Global Enable %	Enter the average percentage of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that you can use to dynamically shut down the entire clock tree.
Local Enable %	Enter the average percentage of time that clock enable is high for destination flipflops.

continued...

Column Heading	Description
	Local clock enables for flipflops in ALMs are promoted to LAB-wide signals. When a given flipflop is disabled, the LAB-wide clock is disabled, cutting clock power and the power for down-stream logic. This page models only the impact on clock tree power.
Utilization Factor	Represents the impact of the clock network configuration on power. Characteristics that have a large impact on power and are captured by this factor include the following: • Whether the network is widely spread out • Whether the fanout is small or large • The clock settings within each LAB The default value for this field is typical; the actual value varies between clocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Intel Quartus Prime software after compiling your design, because the Intel Quartus Prime software has access to detailed placement information. In the absence of an Intel Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.
Total Power (W)	Indicates the total power dissipation due to clock distribution (in W).
User Comments	Enter any comments. This is an optional entry.

For more information about the clock networks of Intel Agilex devices, refer to the Intel Agilex Clocking and PLL User Guide.

4.9. Intel FPGA PTC - PLL Page

Each row in the PLL page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) represents one or more PLLs in the device.

Supported PLL types are family dependent, as outlined in the *PLL Page Information* table, below.

Figure 9. PLL Page of the Intel FPGA PTC

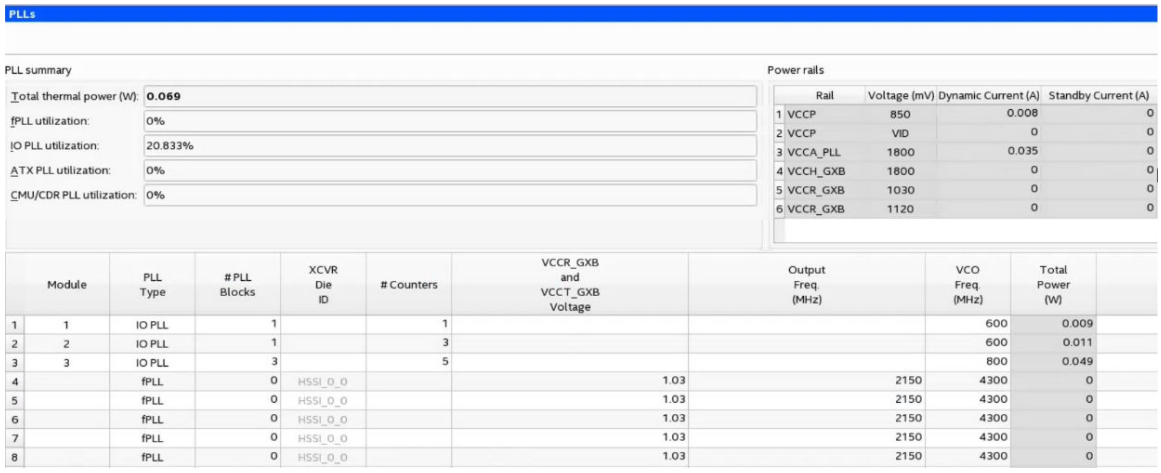


Table 10. PLL Page Information

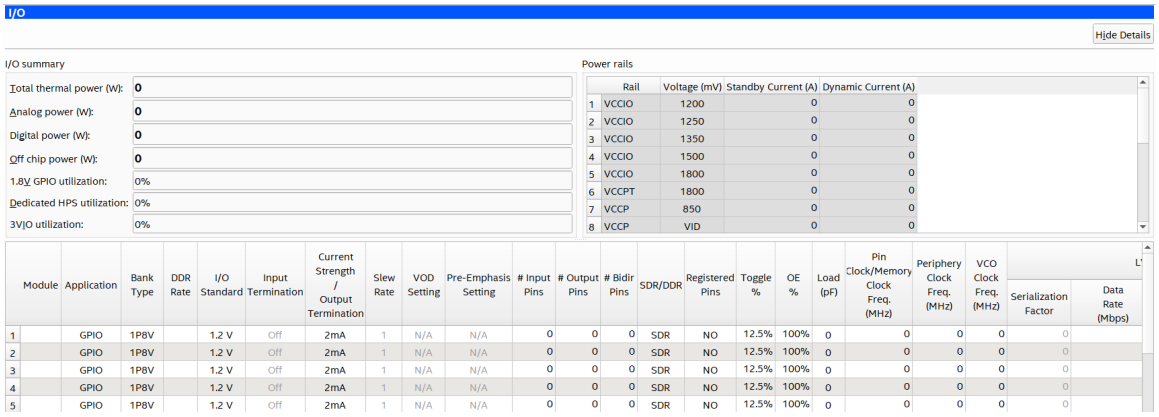
Column Heading	Description
Module	Specify a name for the PLL in this column. This is an optional value.
PLL Type	Specifies the type of PLL, which may include the following: • Fabric-feeding IOPLLs • I/O bank IOPLLs • fPLLs • CMU PLLs • I/O PLLs • ATX PLLs (The availability of some PLL types depends on the selected device.)
# PLL Blocks	Enter the number of PLL blocks with the same combination of parameters.
XCVR Die ID	Specify the transceiver die on which PLLs on this row are located. This field is not applicable for I/O PLLs, nor fabric-feeding I/O PLLs.
# Counters	Enter the number of counters of the PLL.
V_{CCR_GXB} and V_{CCT_GXB} Voltage	Specify the voltage of the V_{CCR_GXB} and V_{CCT_GXB} rails. This field is not applicable for I/O PLLs, nor fabric-feeding I/O PLLs.
Output Freq (MHz)	Specify the output frequency for CMU and ATX PLLs.
VCO Freq (MHz)	Specify the internal VCO operating frequency for PLLs.
Total Power (W)	Shows the total estimated power for this row (in W).
User Comments	Enter any comments. This is an optional entry.

For more information about the PLLs available in Intel Agilex devices, refer to the Intel Agilex Clocking and PLL User Guide.

4.10. Intel FPGA PTC - I/O Page

Each row in the I/O page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) represents a design module where the I/O pins have the same I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load.

Figure 10. I/O Page of the Intel FPGA PTC



The Intel FPGA PTC assumes that you are using external termination resistors as recommended for SSTL and high-speed transceiver logic HSTL. If your design does not use external termination resistors, choose the LVTTL/ LVCMOS I/O standard with the same VCCIO and similar current strength as the terminated I/O standard.

To use on-chip termination (OCT), select the **Current Strength/Output Termination** option in the Intel FPGA PTC.

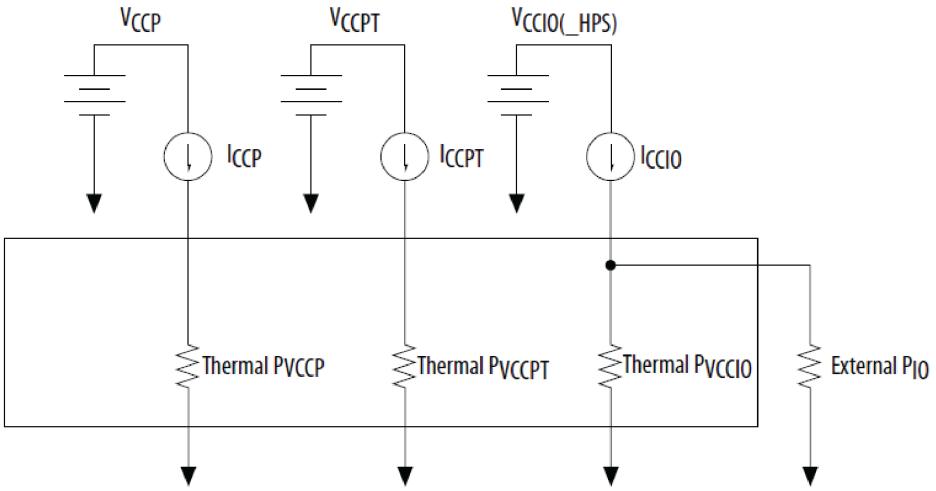
The power reported for the I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device from each power rail, as shown in the following equation.

Figure 11. Total Thermal Power

$$\text{thermal power} = \text{thermal } P_{VCCP} + \text{thermal } P_{VCCPT} + \text{thermal } P_{VCCIO}$$

The following figure shows the I/O power consumption. The I_{CCIO} power rail includes both the thermal P_{IO} and the external P_{IO}.

Figure 12. I/O Power Representation



The VREF pins consume minimal current (typically less than 10 µA), which is negligible when compared with the current consumed by the general purpose I/O (GPIO) pins; therefore, the Intel FPGA PTC does not include the current for VREF pins in the calculations.

Table 11. I/O Page Information

Column Heading	Description
Module	Specify a name for the I/O in this column. This is an optional value.
Application	Specify the application for this I/O row. GPIO and SerDes interfaces can be instantiated using this field. Use the I/O-IP page to instantiate external memory interface (EMIF) interfaces.
Bank Type	Specifies the type of Intel Stratix 10 I/O bank for this row.

continued...

Column Heading	Description
	• 1P8V banks support I/O standards up to 1.8V as well as LVDS I/O standards. • 3VIO banks support CMOS I/O standards up to 3.0V. • HPS banks include dedicated HPS pins. • HPS-1P8V banks are similar to 1P8V banks in terms of supported I/O standards; these banks can serve as either general purpose I/Os or as EMIF interfaces in HPS applications.
Data Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a quarter rate interface means that the PHY logic in the FPGA runs at 200MHz.
I/O Standard	Specifies the I/O standard used by the I/O pins in this module.
Input Termination	Specifies the input termination setting for the input and bidirectional pins in this module.
Current Strength/Output Termination	Specifies the current strength or output termination setting for the output and bidirectional pins in this module. Current strength and output termination are mutually exclusive.
Slew Rate	Specifies the slew rate setting for the output and bidirectional pins in this module. Using a lower slew rate setting helps reduce switching noise but may increase delay.
V_{OD} Setting	Specifies the differential output voltage (V_{OD}) for the output and bidirectional pins in the module. A smaller number indicates a smaller VOD which reduces static power.
Pre-Emphasis Setting	Specifies the pre-emphasis setting for the output and bidirectional pins in this module. A smaller number indicates a smaller pre-emphasis which reduces dynamic power. (This column appears in the Intel Stratix 10 PTC only.)
Programmable De-Emphasis	Specifies the de-emphasis setting for the output and bidirectional pins in this module. A larger number indicates a smaller pre-emphasis which reduces dynamic power. (This column appears in the Intel Agilex PTC only.)
Pin Direction	The pin's signal direction. Output, input, or bi-directional. (PTC for Intel Agilex devices only.)
# Pins	Number of pins used in the specified configuration. (This column appears in the Intel Agilex PTC only.)
# Input Pins	Specifies the number of input-only I/O pins in this module. Differential pin pairs count as one pin. (This column appears in the Intel Stratix 10 PTC only.)
# Output Pins	Specifies the number of output-only I/O pins in this module. Differential pin pairs count as one pin. (This column appears in the Intel Stratix 10 PTC only.)
# Bidir Pins	Specifies the number of bidirectional I/O pins in this module. Differential pin pairs count as one pin. The I/O pin is treated as an output when its output enable signal is active and is treated as an input when the output enable signal is disabled. An I/O pin configured as a bidirectional pin, but used only as an output, consumes more power than if it were configured as an output-only pin, due to the toggling of the input buffer every time the output buffer toggles (they share a common pin). (This column appears in the Intel Stratix 10 PTC only.)
Data Rate	Indicates whether I/O value changes once (Single-Data Rate) or twice (Double-Data Rate) per cycle.
Registered Pins	Indicates whether the pin is registered or not.

continued...

Column Heading	Description
Toggle %	Percentage of clock cycles when the I/O signal changes value. This value is multiplied by clock frequency to determine the number of transitions per second. If DDR is selected, the toggle rate is multiplied by an additional factor of two.
OE %	For modules with Input Termination set to **OFF**, enter the average percentage of time that: • Output I/O is enabled • Bidirectional I/O is an output and enabled During the remaining time: • Output I/O is tri-stated • Bidirectional I/O is an input Input Termination cannot be active while the Output I/O is enabled, so for modules with Input Termination not set to **OFF**, enter the average percentage of time that On-Chip Termination is inactive. (The average percentage of time that On-Chip Termination is inactive equals 100% minus the percentage of time that the On-Chip Termination is active.) This number must be a percentage between 0% and 100%.
Load (pF)	Specifies pin loading external to the chip (in pF). Applies only to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Include only off-chip capacitance.
Pin Clock Frequency (MHz)	Clock frequency (in MHz). 100 MHz with a 12.5% toggle percentage would mean that each I/O pin toggles 12.5 million times per second (100 MHz * 12.5%).
Periphery Clock Freq (MHz)	The I/O subsystem internal PHY clock frequency. This is an output-only field. In SerDes applications, the PHY clock frequency is a function of the SerDes rate and serialization factor. In external memory interface (EMIF) applications, the PHY clock frequency is a function of the memory clock frequency and DDR rate of the EMIF IP.
VCO Clock Freq (MHz)	The internal VCO operating frequency. This is an output-only field. In SerDes applications, VCO frequency is a function of SerDes Data rate. In external memory interface (EMIF) applications, the VCO frequency is a function of the memory clock frequency of the EMIF IP. The VCO frequency is not applicable in GPIO mode.
Digital Power (W)	Power dissipated in the digital domain of the I/O-subsystem including GPIO, EMIF controller and SerDes controller.
Analog Power (W)	Power dissipated in the analog domain of the I/O-subsystem, for example, I/O buffers.
Serialization Factor	Number of parallel data bits for each serial data bit. Used for SerDes-DPA.
Data Rate (Mbps)	The maximum data rate of the SerDes channels in Mbps.
Mode	The DPA mode in which the SerDes channels are operating.
# of Channels	The number of channels running at the data rate of this SerDes domain.
User Comments	Enter any comments. This is an optional entry.

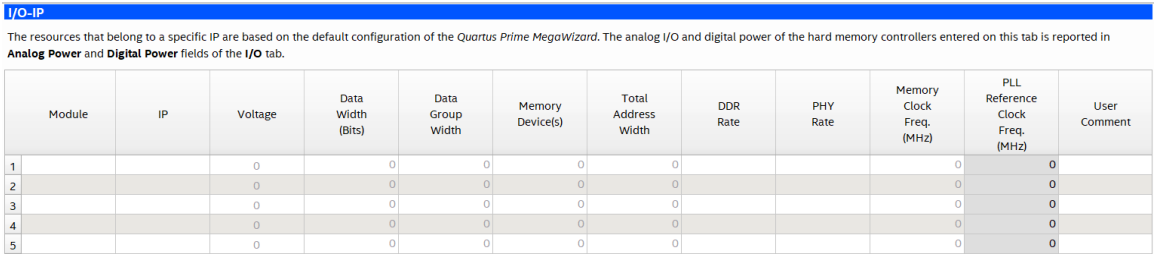
For more information about the I/O standard termination schemes, refer to *I/O and High Speed I/Os in Intel Agilex Devices*.

4.11. Intel FPGA PTC - I/O-IP Page

Each row in the I/O-IP page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) represents a design module. You can use the I/O-IP page to instantiate external memory interface and HPS IPs supported by the target device. The I/O-IP page populates other Intel FPGA PTC pages with resources used by a selected IP.

Analog I/O power and digital power of hard memory controllers and HPS IPs entered on this page are reported in the Analog Power and Digital Power fields of the I/O page. If the IP uses other resource types (for example Logic or PLL), the power is reported on the corresponding page.

Figure 13. I/O-IP Page of the Intel FPGA PTC


I/O-IP

The resources that belong to a specific IP are based on the default configuration of the *Quartus Prime MegaWizard*. The analog I/O and digital power of the hard memory controllers entered on this tab is reported in **Analog Power** and **Digital Power** fields of the **I/O** tab.

	Module	IP	Voltage	Data Width (Bits)	Data Group Width	Memory Device(s)	Total Address Width	DDR Rate	PHY Rate	Memory Clock Freq. (MHz)	PLL Reference Clock Freq. (MHz)	User Comment
1			0	0	0	0	0			0	0	
2			0	0	0	0	0			0	0	
3			0	0	0	0	0			0	0	
4			0	0	0	0	0			0	0	
5			0	0	0	0	0			0	0	

I/O-IP Page Information

Column Heading	Description
Module	Specifies a name for the IP in this column. The module name depends on the selected IP type. It helps to cross-reference each IP module and its corresponding auto-populated entries on other pages. This name is auto-populated when IP type is selected in the IP column and cannot be changed.
IP	Specifies the type of the IP in the design.
Voltage	Specifies the I/O voltage of the signaling between periphery device and interface.
Data Width (Bits)	Specifies the interface data width of the specific IP (in bits).
# of DQS Groups	Specifies the number of DQS groups.
Memory Device(s)	Specifies the number of memory devices connected to the interface.
Total Address Width	Specifies the total address width. This value is used to derive the total number of address pins required.
DDR Rate	Specifies the clock rate of user logic. Determines the clock frequency of user logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the user logic in the FPGA runs at 200MHz.
PHY Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the PHY logic in the FPGA runs at 200MHz.
Memory Clock Frequency (MHz)	Specifies the frequency of memory clock (in MHz).
PLL Reference Clock Frequency (MHz)	Specifies the PLL Reference Clock Frequency (in MHz).
User Comments	Enter any comments. This is an optional entry.

4.12. Intel FPGA PTC - Transceiver Page

The Transceiver page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) allows you to enter transceiver resources and their settings for all modules in your design. The power of transceiver I/O pins is included on this page.

Figure 14. Transceiver Page of the Intel FPGA PTC

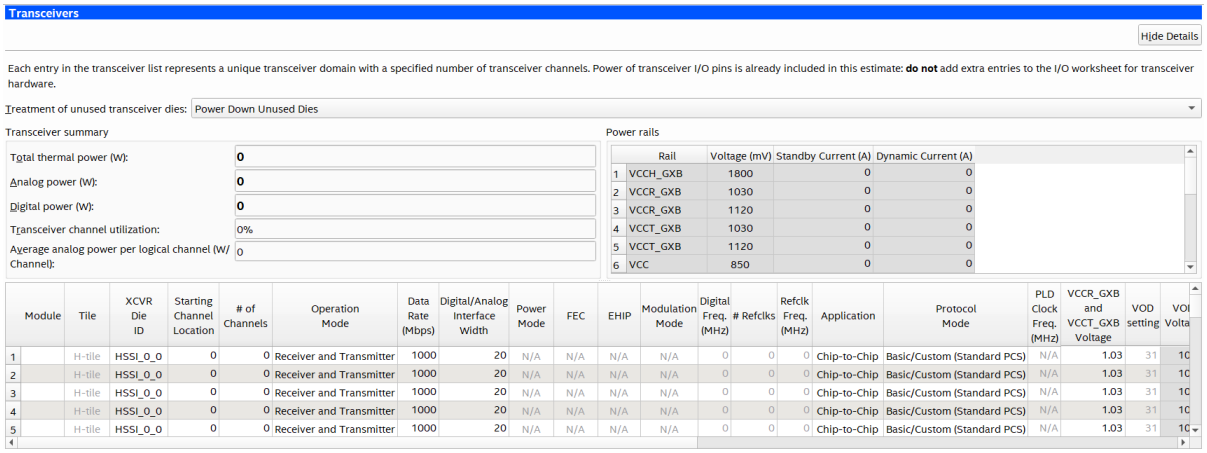


Table 12. General Settings in the Transceiver Page

Input Parameter	Description
Total Thermal Power (W)	Total power dissipated in all modules on this page (in watts).
Treatment of Unused HSSI Dies	• For Intel Agilex devices, all currently supported transceiver tiles always have to be powered up. Consequently, this field is currently always set to **Power Up Unused Dies**; **Minimize Leakage**. • For Intel Stratix 10 devices, if no transceiver channels or PLLs on an HSSI die are used, the die can be powered down or remain powered. The voltage of unused dies that are powered can be selected to minimize static power, or to minimize the number of power supply voltages required. For example, if active H-tile transceiver channels use VCCR_GXB=1.12V, selecting *Minimize Leakage* assumes that the unused-but-powered H-tile dies use VCCR_GXB=1.03V, which is the lowest supported voltage, thus minimizing leakage. Selecting *Minimize Number of Supply Voltages* assumes that the unused-but-powered banks use VCCR_GXB=1.12V, which is the voltage used by active channels, thus eliminating the need for the 1.03V power supply on VCCR_GXB. the Intel FPGA PTC uses information in the *XCVR Die ID*, *Starting Channel Location*, and *# of Channels* columns on the XCVR page, along with the *# PLL Blocks* and *XCVR Die ID* columns on the PLL page to determine whether dies are actively used. This setting does not apply to E-tile nor P-tile transceivers, because these transceiver dies can never be powered down.

Each row in the Transceiver page represents a separate transceiver domain. Enter the following parameters for each transceiver domain:

Table 13. Transceiver Page Information

Column Heading	Description
Module	Specifies a name for the module. This is an optional value.
Tile	Specifies the type of transceiver die on which transceiver channels are located. Some devices may include more than one type of transceiver die.

continued...

Column Heading	Description
	This field changes depending on the device options that you choose on the **Main** page.
XCVR Die ID	Specify the transceiver die on which transceiver channels on this row are located.
Starting Channel Location	Specify the starting location within the die for the channels specified in this row. For example, if a given row contains 3 channels, and starting location is specified to be 12, channels are assumed to be in locations 12, 13, and 14. Location 0 denotes the bottom-most channel on the transceiver die.
# of Channels	Specifies the number of channels used in this transceiver domain. Each row represents one transceiver domain. These channels are grouped together in one transceiver bank, or two or more adjacent transceiver banks and clocked by one or more common transmitter PLLs. For E-tile transceivers, if the selected modulation mode is *High Data Rate PAM4*, enter 2 physical channels to represent 1 logical channel.
Operation Mode	Specifies whether the hardware is configured in full duplex transceiver mode (receiver and transmitter), Receiver Only mode, or Transmitter Only mode. Allowed values depend on the selected tile and protocol mode.
Protocol Mode	Specifies the protocol mode. Allowed values depend on the selected tile.
Data Rate (Mbps)	Specifies the data rate (in Mbps) for the transceiver. Allowed values depend on the selected protocol mode and selected device.
Digital/Analog Interface Width	Specify the width of the parallel data bus between PCS and PMA. For E-tile PMA Direct, set to PMA parallel data width, even if FPGA FIFO widens the interface. As an example, for 25 Gbps PMA Direct you would typically set this value to 32. When the FEC or EHIP is used, you would set this value to 32 for NRZ mode and 64 for PAM4 mode.
Power Mode	E-tile transceivers can operate at either Normal Power Mode or Low Power Mode. For thermal analysis and regulator sizing, you must set the E-tile transceivers in the Normal Power Mode, because your board design must take into consideration the maximum power conditions. Refer to the E-tile Transceiver PHY User Guide for information on how to switch transceivers from Normal Power Mode to Low Power Mode.
FEC	Specify the Forward Error Correction setting. This field is applicable only to E-tile transceivers.
EHIP	Specify the Ethernet Hard IP protocol. This field is applicable only to E-tile transceivers.
Modulation Mode	Specify the data modulation mode of transceiver channels. This field is applicable only to E-tile transceivers. When you select *High Data Rate PAM4* for this field, 2 physical channels are paired to represent 1 logical channel. When specifying # of Channels, enter the number of physical channels (that is, in multiples of 2).
Digital Frequency (MHz)	Specify the digital frequency at which the digital portion of the transceiver (including FEC and EHIP) operates. This field is applicable only to E-tile transceivers.
# Refclks	Specify the number of reference clocks in use. If another interface on this tile is using the same reference clock, and you have already entered this clock in another row, enter 0 in this row to avoid double counting. This field is applicable only to E-tile transceivers.
Refclk Frequency (MHz)	Specify the reference clock frequency. This field is applicable only to E-tile transceivers.
Application	Specify the application type, which determines values for advanced channel options. Select Custom to enable manual editing of advanced channel options for the current row. This field is applicable only to L-tile and H-tile transceivers.

continued...

Column Heading	Description
Protocol Mode	Specifies the mode in which the PCS, HIP, and PCIE blocks operate. This mode depends on the XCVR tile and the communication protocol or standard that the channels on this row implement.
PLD Clock Frequency (MHz)	Specifies the PLD clock frequency. This is applicable only to P-tile transceivers, and when the selected protocol is PCIe gen4.
V_{CCR_GXB} and V_{CCT_GXB} Voltage	Specifies the voltage of the V_{CCR_GXB} and V_{CCT_GXB} rails. Allowed values depend on the selected device and selected data rate. This field is applicable only to L-tile and H-tile transceivers.
V_{OD} Setting	The output differential voltage (V_{OD}) setting of the transmitter channel PMA. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.
V_{OD} Voltage	The output differential voltage (V_{OD}) of the transmitter channel PMA (in mV). This voltage depends on the V_{OD} setting and the V_{CCT_GXB} voltage. This field is applicable only to L-tile and H-tile transceivers.
First Pre-Tap	Specifies the pre-emphasis setting used by the transmitter channel PMA. Set to Off if the tap value is 0; otherwise, set to On. If pre-emphasis settings are set to On, power consumption does not depend on the magnitude nor the sign (positive or negative) of individual taps. To enable these settings, select **Custom** in the **Application** column.
First Post-Tap	
DFE	Specify mode of the decision feedback equalizer (DFE). Allowed values depend on the selected data rate. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.
Adaptation	Specify if the adaptation feature is used. This option should be enabled if the channels use either CTLE adaptation or DFE adaptation. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.
Transmitter High-Speed Compensation	Specifies if the power distribution network (PDN) induced inter-symbol interference (ISI) compensation is enabled in the TX driver. To enable this setting, select **Custom** in the **Application** column. This field is applicable only to L-tile and H-tile transceivers.
Digital Power (W)	The total power of all digital circuitry associated with the channels specified on this row, such as the Embedded Multi-die Interconnect Bridge (EMIB). It excludes power of blocks whose power may be shared among multiple channels (and therefore multiple rows), such as the FEC and 100G EHIP in the case of E-tile usage.
Analog Power (W)	The total power of all analog circuity associated with the channels specified on this row. It excludes power of blocks whose power may be shared among multiple channels (and therefore multiple rows), such as the clock network.
User Comments	Enter any comments. This is an optional entry.

For more information about the transceiver architecture of the supported device families, refer to the appropriate *Transceiver PHY User Guide* for Intel Agilex devices.

4.12.1. Estimating E-Tile Channel PLL Power with the Intel Power and Thermal Calculator

You can estimate E-tile channel PLL power for Intel Stratix 10 devices, by adding a Transmitter-only row to the **Transceiver** page of the Intel FPGA Power and Thermal Calculator (PTC).

The following three examples illustrate the PTC configuration for various E-tile channel PLL requirements.

Table 14. E-Tile Channel PLL configured for: Reference clock = 200MHz, pll_clkout1 = 800MHz, pll_clkout2 = 400MHz

Operation Mode	Data Rate	Digital/ Analog Width	Power Mode	FEC	EHIP	Modulation	Digital Freq	# Refclks	Refclk Freq	VOD
Transmitter Only	12800	16	Normal Power	Bypass	Bypass	NRZ	0	1	200	0

Table 15. E-Tile Channel PLL configured for: Reference clock = 125MHz, pll_clkout1 = 500MHz, pll_clkout2 = 250MHz

Operation Mode	Data Rate	Digital/ Analog Width	Power Mode	FEC	EHIP	Modulation	Digital Freq	# Refclks	Refclk Freq	VOD
Transmitter Only	8000	16	Normal Power	Bypass	Bypass	NRZ	0	1	125	0

Table 16. E-Tile Channel PLL configured for: Reference clock = 307MHz, pll_clkout1 = 491MHz, pll_clkout2 = 245MHz

Operation Mode	Data Rate	Digital/ Analog Width	Power Mode	FEC	EHIP	Modulation	Digital Freq	# Refclks	Refclk Freq	VOD
Transmitter Only	19660.8	40	Normal Power	Bypass	Bypass	NRZ	0	1	307	0

Alternatively, you can instantiate an E-Tile Transceiver-native PHY IP in PLL mode in your Intel Quartus Prime project, compile the project, and view the configuration in the PTC.

4.13. Intel FPGA PTC - HBM Page (Intel Stratix 10 Devices Only)

The HBM page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) shows the power information pertaining to high-bandwidth memory (HBM).

Figure 15. HBM Page of the Intel FPGA PTC

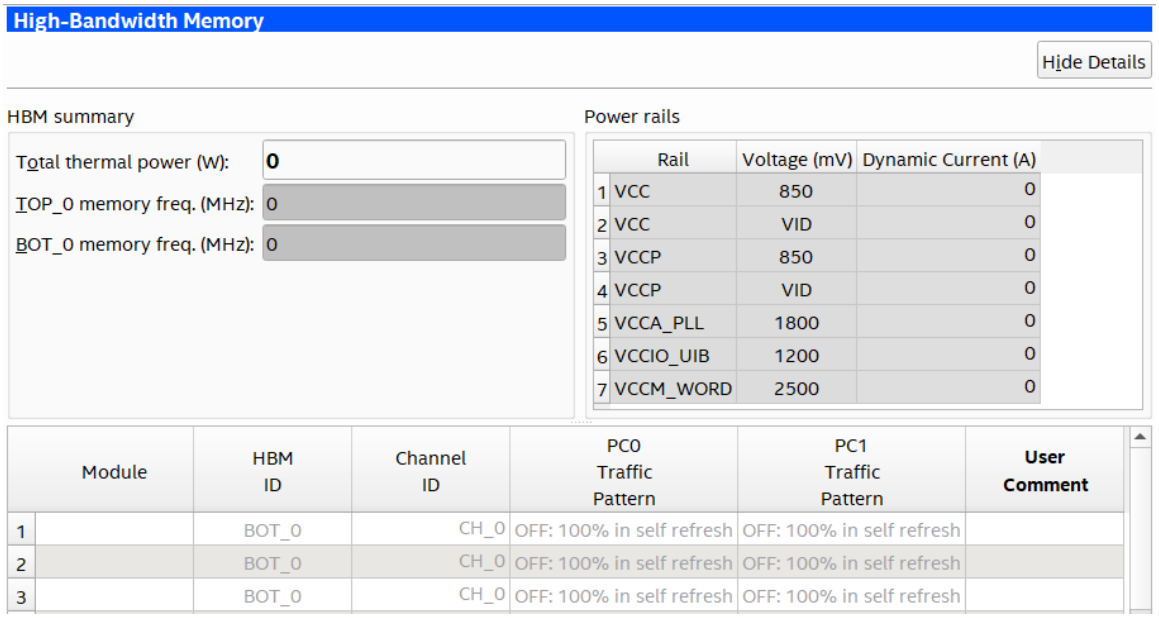


Table 17. HBM Channel Configuration

Column Heading	Description
Module	A user-editable field to name each module of the design.
HBM ID	Select the top or bottom HBM stack in devices that include multiple stacks.
Channel ID	Selects a particular die in the stack.
PC0 Traffic Pattern	Select the traffic pattern that most closely matches your application. (PC0 and PC1 refer to the two pseudo-channels that each physical channel [0-7] is divided into; you can select different traffic patterns for each pseudo-channel.)
PC1 Traffic Pattern	Select the traffic pattern that most closely matches your application. (PC0 and PC1 refer to the two pseudo-channels that each physical channel [0-7] is divided into; you can select different traffic patterns for each pseudo-channel.)

4.14. Intel FPGA PTC - Thermal Page

The Thermal page of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) allows you to enter temperature requirements for your design and displays thermal power and thermal analysis information.

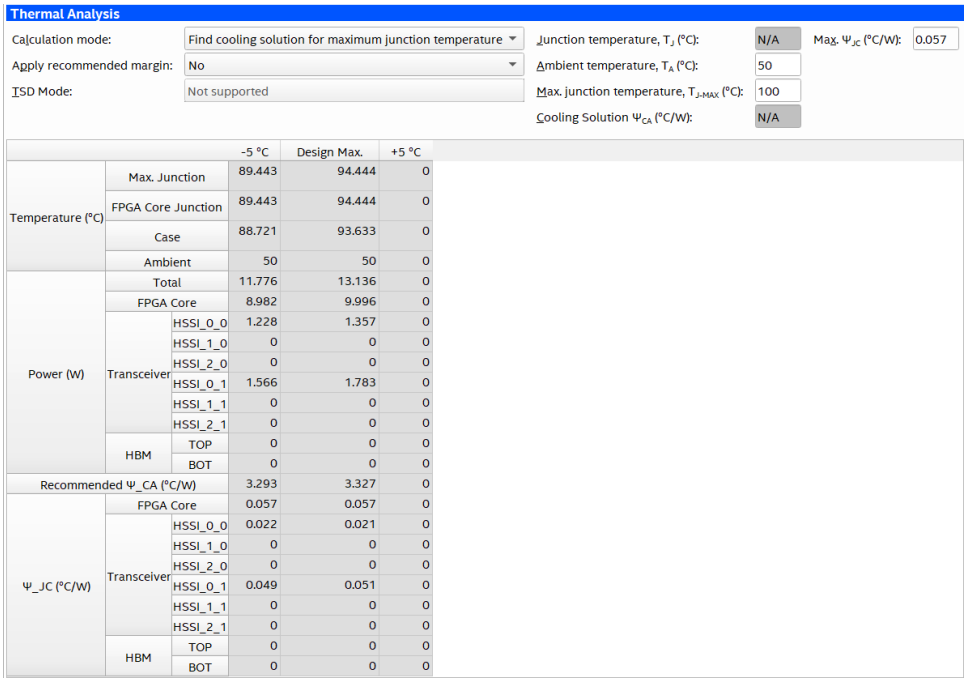
On the Main worksheet, verify that **Power Characteristics** is set to **Maximum**, and then select the desired **Calculation mode** from the drop-down menu. There are four choices:

- Use a constant junction temperature
- Find cooling solution for maximum junction temperature.
- Find maximum junction temperature for cooling solution.
- Find ambient temperature for specified cooling solution.

The Thermal page differs slightly, depending on whether you are targeting an Intel Agilex device or an Intel Stratix 10 device. Refer to the appropriate section for your targeted device, below:

Thermal Page for Intel Agilex Devices

Figure 16. Thermal Page of the Intel FPGA PTC — Intel Agilex Devices



			-5 °C	Design Max.	+5 °C
Temperature (°C)	Max. Junction		89.443	94.444	0
	FPGA Core Junction		89.443	94.444	0
	Case		88.721	93.633	0
	Ambient		50	50	0
Power (W)	Total		11.776	13.136	0
	FPGA Core		8.982	9.996	0
	Transceiver	HSSI_0_0	1.228	1.357	0
		HSSI_1_0	0	0	0
		HSSI_2_0	0	0	0
		HSSI_0_1	1.566	1.783	0
		HSSI_1_1	0	0	0
		HSSI_2_1	0	0	0
	HBM	TOP	0	0	0
		BOT	0	0	0
Recommended Ψ_CA (°C/W)			3.293	3.327	0
Ψ_JC (°C/W)	FPGA Core		0.057	0.057	0
	Transceiver	HSSI_0_0	0.022	0.021	0
		HSSI_1_0	0	0	0
		HSSI_2_0	0	0	0
		HSSI_0_1	0.049	0.051	0
		HSSI_1_1	0	0	0
		HSSI_2_1	0	0	0
	HBM	TOP	0	0	0
		BOT	0	0	0

Table 18. Input Parameter Information

Column Heading	Description
Calculation Mode	Specifies the calculation mode for the thermal solver to use.
Apply Recommended Margin	Specifies whether to apply recommended margins to power estimates for thermal analysis. Recommended margins are based on power model maturity, as follows: • All power components: 25% These margins apply only to thermal analysis results. Selecting **Yes** causes the total power to be higher on the Thermal worksheet than power reported elsewhere in the Early Power Estimator.
TSD Mode	Indicates the method by which the maximum junction temperature is measured.

continued...

Column Heading	Description
Junction temperature, T_J (°C)	Specify the junction temperature for all dies in the package. This field applies only when the selected **Calculation mode** value is **Use a constant junction temperature**.
Ambient Temp, T_A (°C)	Specify the temperature of the air that is cooling the device.
Max. Junction Temp, $T_{J\text{-}MAX}$ (°C)	Specify the maximum junction temperature that no part of any die in the package should exceed.
Cooling Solution Ψ_{CA}(°C/W)	Ψ_{CA} is the thermal resistance between the center of the package integrated heat spreader (IHS) and ambient temperature. The recommended Ψ_{CA} is the highest possible thermal resistance of the cooling solution that ensures no part of any die exceeds the specified maximum junction temperature.
Max. Ψ_{JC}(°C/W)	Ψ_{JC} is the thermal resistance between each of the dies in the package and the center of the package integrated heat spreader. This field shows the maximum Ψ_{JC} among all dies, assuming the recommended Ψ_{CA} value above.

Table 19. Temperature (°C)

Column Heading	Description
Max. Junction	The maximum junction temperature that no part of any die in the package should exceed.
FPGA Core Junction	The maximum junction temperature of the core die.
Case	The case temperature, which is the temperature at the top center of the integrated heat spreader, assuming the recommended Ψ_{CA} value listed above.
Ambient	The temperature of the air that is cooling the device.

Table 20. Power (W)

Column Heading		Description
Total		Provides total power consumption of all dies in the package.
FPGA Core		The total thermal power consumption of the main FPGA die containing core logic. The FPGA Core power is dependent on temperature of the core. (The FPGA core may or may not be the hot spot in the package.)
Transceiver	HSSI_0_0	The total power consumption of HSSI_0_0, assuming the recommended Ψ_{CA} value. This power is dependent on transceiver temperature. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_1_0	The total power consumption of HSSI_1_0, assuming the recommended Ψ_{CA} value. This power is dependent on transceiver temperature. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_2_0	The total power consumption of HSSI_2_0, assuming the recommended Ψ_{CA} value. This power is dependent on transceiver temperature. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.

continued...

Column Heading		Description
	HSSI_0_1	The total power consumption of HSSI_0_1, assuming the recommended Ψ_{CA} value. This power is dependent on transceiver temperature. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_1_1	The total power consumption of HSSI_1_1, assuming the recommended Ψ_{CA} value. This power is dependent on transceiver temperature. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_2_1	The total power consumption of HSSI_2_1, assuming the recommended Ψ_{CA} value. This power is dependent on transceiver temperature. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
HBM	Top	The total thermal power consumption of HBM TOP, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package.
	Bot	The total thermal power consumption of HBM BOT, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package.

Table 21. Recommended Ψ_{CA} (°C/W)

Column Heading	Description
Recommended ψ_{CA} (°C/W)	The thermal resistance between the center of the package integrated heat spreader and the ambient temperature, assuming the specific core temperature in the given table column. For each column, this is the Ψ_{CA} value that would cause the FPGA core junction temperature to be at the specific value for the given column.

Table 22. Ψ_{JC}(°C/W)

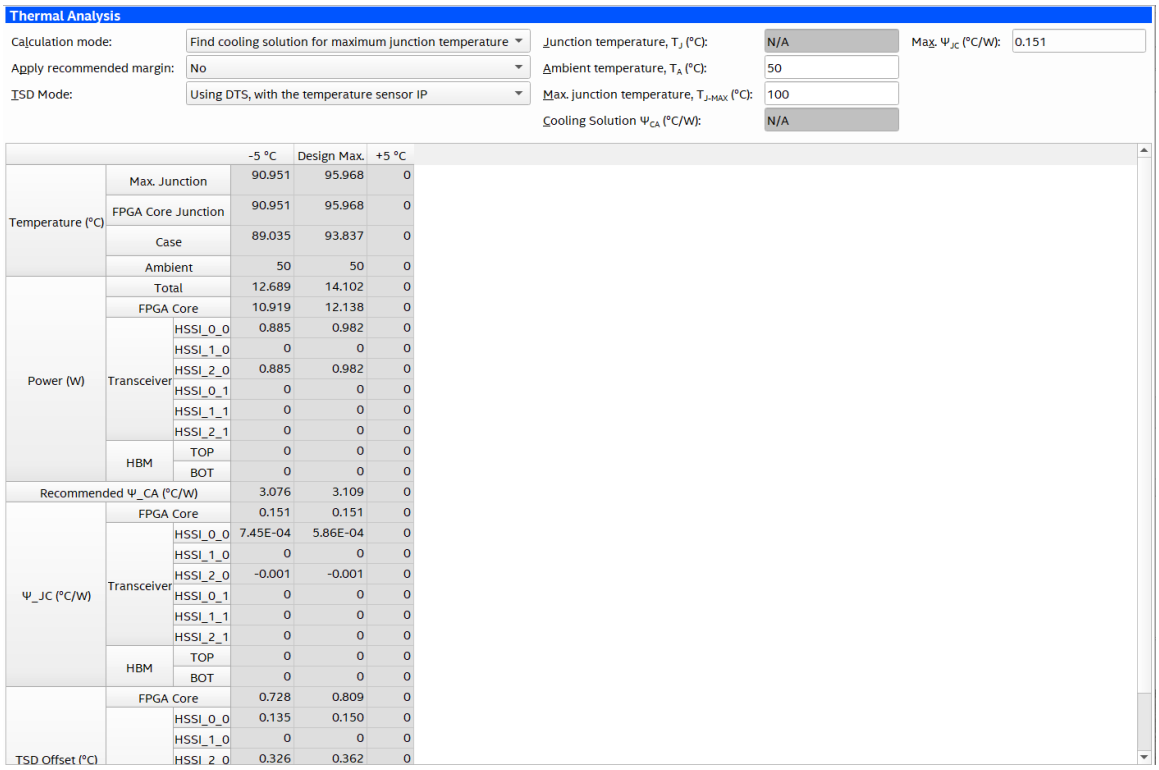
Column Heading		Description
FPGA Core		The thermal resistance between the main FPGA core die and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
Transceiver	HSSI_0_0	The thermal resistance between HSSI_0_0 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_1_0	The thermal resistance between HSSI_1_0 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_2_0	The thermal resistance between HSSI_2_0 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_0_1	The thermal resistance between HSSI_0_1 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.

continued...

Column Heading		Description
	HSSI_1_1	The thermal resistance between HSSI_1_1 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_2_1	The thermal resistance between HSSI_2_1 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
HBM	TOP	The thermal resistance between HBM TOP and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	BOT	The thermal resistance between HBM BOT and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.

Thermal Page for Intel Stratix 10 Devices

Figure 17. Thermal Page of the Intel FPGA PTC — Intel Stratix 10 Devices



			-5 °C	Design Max.	+5 °C
Temperature (°C)	Max. Junction		90.951	95.968	0
	FPGA Core Junction		90.951	95.968	0
	Case		89.035	93.837	0
	Ambient		50	50	0
Power (W)	Total		12.689	14.102	0
	FPGA Core		10.919	12.138	0
	Transceiver	HSSI_0_0	0.885	0.982	0
		HSSI_1_0	0	0	0
		HSSI_2_0	0.885	0.982	0
		HSSI_0_1	0	0	0
		HSSI_1_1	0	0	0
		HSSI_2_1	0	0	0
	HBM	TOP	0	0	0
		BOT	0	0	0
Recommended Ψ_CA (°C/W)			3.076	3.109	0
Ψ_JC (°C/W)	FPGA Core		0.151	0.151	0
	Transceiver	HSSI_0_0	7.45E-04	5.86E-04	0
		HSSI_1_0	0	0	0
		HSSI_2_0	-0.001	-0.001	0
		HSSI_0_1	0	0	0
		HSSI_1_1	0	0	0
		HSSI_2_1	0	0	0
	HBM	TOP	0	0	0
		BOT	0	0	0
TSD Offset (°C)	FPGA Core		0.728	0.809	0
		HSSI_0_0	0.135	0.150	0
		HSSI_1_0	0	0	0
		HSSI_2_0	0.326	0.362	0

Table 23. Input Parameter Information

Column Heading	Description
Calculation Mode	Specifies the calculation mode for the thermal solver to use.
Apply Recommended Margin	Specifies whether to apply recommended margins to power estimates for thermal analysis. Recommended margins are based on power model maturity, as follows: • All power components: 25% These margins apply only to thermal analysis results. Selecting **Yes** causes the total power to be higher on the Thermal worksheet than power reported elsewhere in the Early Power Estimator.

continued...

Column Heading	Description
TSD Mode	Specify the method by which offset temperatures are provided—such as from a thermal diode, or a digital temperature sensing mechanism.
Junction temperature, T_J (°C)	Specify the junction temperature for all dies in the package. This field applies only when the selected **Calculation mode** value is **Use a constant junction temperature**.
Ambient Temp, T_A (°C)	Specify the temperature of the air that is cooling the device.
Max. Junction Temp, $T_{J\text{-}MAX}$ (°C)	Specify the maximum junction temperature that no part of any die in the package should exceed.
Cooling Solution Ψ_{CA}(°C/W)	ψ_{CA} is the thermal resistance between the center of the package integrated heat spreader (IHS) and ambient temperature. The recommended Ψ_{CA} is the highest possible thermal resistance of the cooling solution that ensures no part of any die exceeds the specified maximum junction temperature.
Max. Ψ_{JC}(°C/W)	ψ_{JC} is the thermal resistance between each of the dies in the package and the center of the package integrated heat spreader. This field shows the maximum Ψ_{JC} among all dies, assuming the recommended Ψ_{CA} value above.

Table 24. Temperature (°C)

Column Heading	Description
Max. Junction	The maximum junction temperature that no part of any die in the package should exceed.
FPGA Core Junction	The maximum junction temperature that no part of any die in the package should exceed.
Case	The case temperature, which is the temperature at the top center of the integrated heat spreader, assuming the recommended Ψ_{CA} value listed above.
Ambient	The temperature of the air that is cooling the device.

Table 25. Power (W)

Column Heading		Description
Total		Provides total power consumption of all dies in the package.
FPGA Core		The total thermal power consumption of the main FPGA die containing core logic, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the core die, assuming the recommended Ψ_{CA} value. This temperature may be equal to the maximum junction temperature if the FPGA core die is at the highest temperature among all dies (also known as a hot spot). The FPGA core may also be at a lower temperature, if the hot spot is elsewhere in the package (i.e. on another die).
Transceiver	HSSI_0_0	The total power consumption of HSSI_0_0, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_1_0	The total power consumption of HSSI_1_0, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be

continued...

Column Heading		Description
		equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_2_0	The total power consumption of HSSI_2_0, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_0_1	The total power consumption of HSSI_0_1, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
	HSSI_1_1	The total power consumption of HSSI_1_1, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.

continued...

Column Heading		Description
	HSSI_2_1	The total power consumption of HSSI_2_1, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package. *Note:* Each transceiver die in the package reports a small amount of static power even when no channels are used in the corresponding transceiver tile and transceiver rails (V_{CCR_GXB}, V_{CCT_GXB}, and V_{CCH_GXB}) of that tile are grounded. This is an expected result.
HBM	Top	The total thermal power consumption of HBM TOP, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package.
	Bot	The total thermal power consumption of HBM BOT, assuming the recommended Ψ_{CA} value. This power is reported at the actual temperature of the specific die, assuming the recommended Ψ_{CA} value above. This temperature may be equal to the maximum junction temperature if a specific die is the hot spot, or it may be at a lower temperature if the hot spot is elsewhere in the package.

Table 26. Recommended ψ_{CA} (°C/W)

Column Heading	Description
Recommended ψ_{CA} (°C/W)	The thermal resistance between the center of the package integrated heat spreader and the ambient temperature, assuming the specific core temperature in the given table row. For each row, this is the Ψ_{CA} value that would cause the FPGA core junction temperature to be at the specific value for a given row.

Table 27. Ψ_{JC}(°C/W)

Column Heading		Description
FPGA Core		The thermal resistance between the main FPGA core die and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
Transceiver	HSSI_0_0	The thermal resistance between HSSI_0_0 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_1_0	The thermal resistance between HSSI_1_0 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_2_0	The thermal resistance between HSSI_2_0 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_0_1	The thermal resistance between HSSI_0_1 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_1_1	The thermal resistance between HSSI_1_1 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	HSSI_2_1	The thermal resistance between HSSI_2_1 and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
HBM	TOP	The thermal resistance between HBM TOP and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
	BOT	The thermal resistance between HBM BOT and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.

Table 28. TSD Offset (°C) (Intel Stratix 10 Devices Only)

Column Heading		Description
FPGA Core		The thermal resistance between the main FPGA core die and the center of the package integrated heat spreader, assuming the recommended Ψ_{CA} value.
Transceiver	HSSI_0_0	The temperature difference between the hot spot on the corresponding transceiver die and location of the thermal sensing diode (TSD) with the highest temperature reported using the Intel Temperature IP Sense software. (When the IP sense method is used to read the TSDs, all the TSD locations are read and the highest of these is reported.) (Intel Stratix 10 devices only) `FPGA transceiver temperature = FPGA transceiver TSD temperature measured using the IP sense method + Transceiver TSD offset.` (If you are not using the Intel Temperature IP Sense software to read the TSD offsets, contact your Intel support representative for a workaround to get the correct TSD temperature.)
	HSSI_1_0	
	HSSI_2_0	
	HSSI_0_1	
	HSSI_1_1	
	HSSI_2_1	

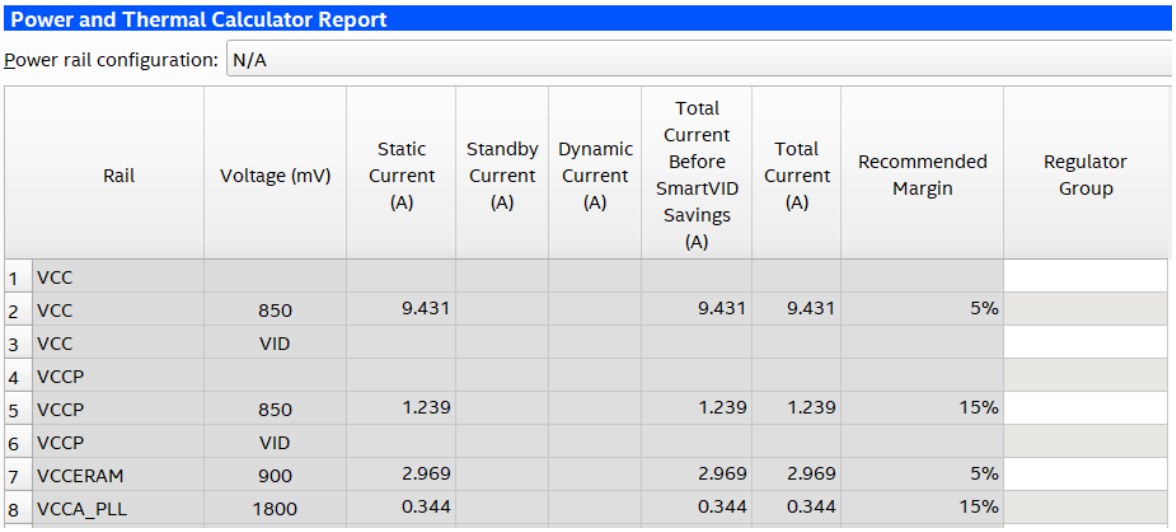
In extreme cases, such as thermal runaway, it may not be possible to calculate the values for +/- 5 degrees, in which case the Thermal worksheet displays the error message: *ERROR: Could not calculate parameter variation with core temperature. Try adjusting $T_{J\text{-}MAX}$ to obtain temperature-dependent parameters*. When this error occurs, the recommended Ψ_{CA} value and all other values above are valid, but the table showing variation of thermal parameters and power consumption with changing junction temperature of the main FPGA core die contains some invalid values. As the error text indicates, adjusting the maximum junction temperature may allow the thermal solver to calculate this dependence, albeit at a different range of FPGA core temperatures than the usual range.

For more information about thermal modeling, refer to AN-787: Thermal Modeling and Management.

4.15. Intel FPGA PTC - Report Page

The Report page shows per-rail currents calculated by the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC).

Figure 18. Report Page of the Intel FPGA PTC



Power and Thermal Calculator Report

Power rail configuration: N/A

	Rail	Voltage (mV)	Static Current (A)	Standby Current (A)	Dynamic Current (A)	Total Current Before SmartVID Savings (A)	Total Current (A)	Recommended Margin	Regulator Group
1	VCC								
2	VCC	850	9.431			9.431	9.431	5%	
3	VCC	VID							
4	VCCP								
5	VCCP	850	1.239			1.239	1.239	15%	
6	VCCP	VID							
7	VCCERAM	900	2.969			2.969	2.969	5%	
8	VCCA_PLL	1800	0.344			0.344	0.344	15%	

The Report page provides current requirements for each voltage rail, expressed in terms of static current, dynamic current, and total current.

Table 29. Current and Power Regulator Requirements Per Voltage Rail

Column Heading	Description
Rail	Name of the voltage rail.
Voltage (mV)	Rail voltage.
Static Current (A)	Indicates the component of current consumed from the specified power rail whenever the power is applied to the rail, independent of circuit activity (in A). This current is dependent on device size, device grade, power characteristics and junction temperature.
Standby Current (A)	Indicates the component of active current drawn from the specified power rail by all modules on all pages, independent of signal activity (in A). This current is independent of device grade, power characteristics and junction temperature. Standby current includes, but is not limited to, I/O and transceiver DC bias current. Device size has only a small impact on transceiver DC bias current. (This column applies only to Intel Stratix 10 devices.)
Dynamic Current (A)	Indicates the component of active current drawn from the specified power rail due to signal activity of all modules on all pages (in A). This current depends on device size, but is independent of device grade, power characteristics and junction temperature.
Total Current Before SmartVID Savings (A)	Indicates the total current consumed from the specified power rail before SmartVID savings (in A). The sum of static and dynamic currents.

continued...

Column Heading	Description
Total Current (A)	Indicates the total current consumed from the specified power rail (in A). For devices and rails supporting SmartVID, this column shows total current after SmartVID power savings; otherwise, the current reported in this column should equal the sum of static and dynamic currents.
Recommended Margin	Indicates the recommended margin on total current for regulator sizing. The recommended margin on the V_{CC} rail is calculated based on the ratio of dynamic to static power.
Regulator Group	Indicates the regulator group number to which this supply is assigned. Regulator group numbers correspond to the group numbers shown in the Intel Enpirion worksheet. If you select an automatic assignment mode in the **Power Rail Configuration** field, the regulator group numbers also correspond to the group numbers in the pin connection guidelines. To edit fields in this column manually, select **Custom** under **Power Rail Configuration**. (Intel Stratix 10 devices only.)

4.16. Intel FPGA PTC - Intel Enpirion Page

Each row in the *Enpirion Regulator Selection* table of the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) represents the power solution for a single regulator group.

Intel Enpirion power devices are available that satisfy the power requirements for the power rails on FPGA devices. Power devices are selected based on load current, input and output voltages, and power-delivery configuration.

Regulator groups are created by combining rails that can be supplied from the same voltage. device selection is enabled when **Power Characteristics** in the Main worksheet is set to **Maximum**, and the **Regulator Group** section of the Report worksheet is set up correctly with no grouping errors.

Figure 19. Intel Enpirion Page of the Intel FPGA PTC

Enpirion® Regulator Selection

Supplies are organized according to the power rail configuration specified on the **Report** tab. Please refer to the Pin Connection Guidelines for more information on the selected power rail configurations.

Switch-mode supplies can be used in place of linear supplies for currents over 100 mA.

Currents shown by supplies with downstream regulators include the total currents of those child regulators.

Power rail configuration: GX 15Gbps < DR <= 28.3Gbps

	Regulator Group	Is Intermediate Supply	Regulator Input Voltage (V)	Regulator Current Draw (A)	Output Voltage (V)	Output Current (A)	Margin Entry	Load Current Margin	Parent Group	Regulator Type	Power OK	Suggested Enpirion Part	Pin Compatible Parts	Note
1	1	No	0	0	0.85	1.530	N/A	30%	0	Switcher	No	N/A	N/A	N/A
2	2	No	0	0	0.9	0.236	N/A	30%	0	Switcher	No	N/A	N/A	N/A
3	3	No	N/A	0	N/A	0	N/A	30%	0	Switcher	No	N/A	N/A	N/A
4	4	No	0	0	N/A	0	N/A	30%	0	Switcher	No	N/A	N/A	N/A
5	5	No	0	0	3	1.580	N/A	30%	0	Switcher	No	N/A	N/A	N/A
6	6	No	0	0	2.4	8.74E-04	N/A	30%	0	Switcher	No	N/A	N/A	N/A
7	7	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
8	8	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
9	9	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
10	10	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
11	11	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
12	12	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
13	13	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
14	14	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
15	15	No	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 30. Intel Enpirion Worksheet Information

Column Heading	Description
Regulator Group	The regulator group number for this regulator. The regulator group numbers correspond to the group numbers shown in the Report worksheet.
Is Intermediate Supply	Indicate whether the supply is an intermediate supply. An intermediate supply is driven by a regulator that is not connected to any supply rails on the FPGA. Instead, such a regulator drives other regulators. If a regulator provides power to both the FPGA and other regulators, this field should be set to *No*.
Regulator Input Voltage (V)	Specifies the input voltage for the regulator. The input voltage must be higher than the output voltage. If this regulator has a parent, its input voltage is automatically set to the parent's output voltage.
Regulator Current Draw (A)	Specifies the required input current to the regulator. It is assumed that all regulators have a current efficiency of 85%.
Output Voltage (V)	Specifies the output voltage of the regulator. The voltage equals the voltage of the supply rail connected to this regulator.
Output Current (A)	Specifies the load current required by the pins from the regulator. This current equals the sum of all the supply currents that are connected to this regulator, multiplied by (1 + Load Current Margin). In addition, if this regulator is a parent of other regulators, the Load Current also includes the sum of all the children's input currents.
Margin Entry	Choose whether load current margin is calculated automatically from recommended margins in the Report page, or entered manually.
Load Current Margin	Margin added to the output current to account for component variability.
Parent Group	The group number of the regulator that supplies input voltage to the regulator in the current row. This value is applicable only when the input voltage is provided by another regulator on this worksheet.
Regulator Type	Choose the type of the regulator.
Power OK	Select **Yes** to select a regulator with a Power OK (**POK**) output to assist with sequencing.
Suggested Enpirion Part	Specifies suggested parts to implement regulator for a given row, which meet the voltage and current requirements for this row. To finalize regulator selection, evaluate VRM voltage ripple specification and efficiency against the FPGA device requirement from the appropriate data sheets.
Pin Compatible Parts	Pin compatible parts are devices with equivalent or higher current capabilities that can be placed on the same PCB footprint as the suggested Intel Enpirion part. Additional components or changes to component values may be required when using a pin compatible part.
Note	A note may be displayed here, depending on the value chosen under **Suggested Enpirion Part**.

5. Factors Affecting the Accuracy of the Intel FPGA Power and Thermal Calculator

Many factors can affect the estimated values displayed in the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC). In particular, the input parameters entered concerning toggle rates and temperature must be accurate to ensure that the system is modeled correctly in the Intel FPGA PTC.

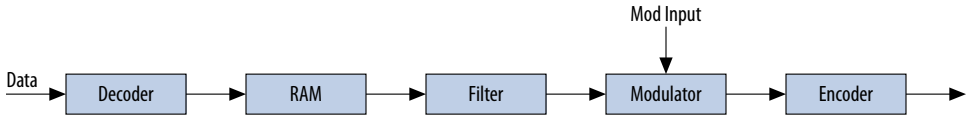
5.1. Toggle Rate

The toggle rates specified in the Intel FPGA Power and Thermal Calculator (Intel FPGA PTC) can have a large impact on the dynamic power consumption displayed. To obtain an accurate estimate, you must input toggle rates that are realistic. Determining realistic toggle rates requires knowing what kind of input the FPGA is receiving and how often it toggles.

To get an accurate estimate if the design is not complete, isolate the separate modules in the design by function, and estimate the resource usage along with the toggle rates of the resources. The easiest way to accomplish this is to use previous designs to estimate the toggle rates for modules with similar function.

The input data in the following figure is encoded for data transmission and has a roughly 50% toggle rate.

Figure 20. Decoder and Encoder Block Diagram



In this case, you must estimate the following:

- Data toggle rate
- Mod Input toggle rate
- Resource estimate for the Decoder, RAM, Filter, Modulator, and Encoder module
- Toggle rate for the Decoder, RAM, Filter, Modulator, and Encoder module

You can generate these estimates in many ways. If you used similar modules in the past with data inputs of roughly the same toggle rates, you can use that information. If MATLAB* simulations are available for some blocks, you can obtain the toggle rate information from the simulations. If the HDL is available for some of the modules, you can simulate them to obtain toggle rates.

If the HDL is complete, the best way to determine toggle rates is to simulate the design. The accuracy of toggle rate estimates depends on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Intel Quartus Prime software can determine toggle rates of each resource used in the design if you provide information from simulation tools. Designs can be simulated in many different tools and the information provided to the Intel Quartus Prime software through a Signal Activity File (`.saf`) or Value Change Dump (`.vcd`) file. The Intel Quartus Prime Power Analyzer provides the most accurate power estimate.

6. Intel FPGA Power and Thermal Calculator User Guide Archive

Intel Quartus Prime Version	User Guide
20.1	Intel FPGA Power and Thermal Calculator User Guide
19.4	Intel FPGA Power and Thermal Calculator User Guide

7. Document Revision History for the Intel FPGA Power and Thermal Calculator User Guide

Document Version	Intel Quartus Prime Version	Changes
2021.01.21	20.3	In the *Intel FPGA Power and Thermal Calculator Pages* chapter: • In the *I/O Page* topic, modified the description of the *OE %* column. • Under the *Transceiver Page* topic, added the *Estimating E-Tile Channel PLL Power with the Intel Power and Thermal Calculator* topic.
2020.10.05	20.3	• In the *Setting Up the Intel FPGA Power and Thermal Calculator* chapter, made minor changes to the following topics: — *Obtaining the Standalone Intel FPGA Power and Thermal Calculator* — *Estimating Power Consumption While Creating the FPGA Design* • In the *Intel FPGA Power and Thermal Calculator Graphical User Interface* chapter, made minor changes to the following topics: — *Intel FPGA PTC Select Family Dialog Box* — *Intel FPGA PTC Basic GUI Components* — *Intel FPGA PTC Data Entry Pages* — *Intel FPGA PTC Field Types* — *Intel FPGA PTC Data Entry Error Messages* • Made changes to every topic in the *Power and Thermal Calculator Pages* chapter.
2020.07.24	20.1	In the *Power and Thermal Calculator Tabs* chapter, implemented changes to the *Intel FPGA PTC - ADC/DAC Tab (Intel Stratix 10 Devices Only)* topic.
2020.05.28	20.1	In the *Intel FPGA PTC - Thermal Tab* topic: • Modified the *FPGA Core TSD Offset (°C)* description in the *HBM Die Ψ_{JC}(°C/W)* table. • Modified and consolidated the descriptions for the entries in the *Transceiver Die TSD Offset (°C)* table.

continued...

Document Version	Intel Quartus Prime Version	Changes
2020.04.27	20.1	In the *Power and Thermal Calculator Tabs* chapter, updated the figure and revised the table contents, in the *Intel FPGA PTC - ADC/DAC Tab (Intel Stratix 10 Devices Only)* topic.
2020.04.13	20.1	• Added support for Intel Stratix 10 devices, throughout. • In the *Setting Up the Intel FPGA Power and Thermal Calculator* chapter: — Modified the *Licensing* information in the *Availability* topic. — Modified the *Importing* information in the *Estimating Power Consumption While Creating the FPGA Design* topic. • In the *Power and Thermal Calculator Graphical User Interface* chapter: — Added the *Intel FPGA PTC Select Family Dialog Box* and *Intel FPGA PTC Basic GUI Components* topics. • In the *Power and Thermal Calculator Tabs* chapter: — Added a *Notice* statement to the *Power and Thermal Calculator Tabs* topic. — Added the *Intel FPGA PTC - ADC/DAC Tab* topic. — Added the *Intel FPGA PTC - HBM Tab* topic. — Added the *Intel FPGA PTC - Thermal Tab* topic. — Added the *Intel FPGA PTC - Intel Enpirion Tab* topic. • Added the *Intel FPGA Power and Thermal Calculator User Guide Archive*.
2020.02.14	19.4	Initial release.

A. Measuring Static Power

Follow these steps to measure static power in your design.

1. Verify that the device is properly configured and in user mode. (CONF_DONE, NSTATUS, NCONFIG, and INIT_DONE values should be high.)
2. Wait until a stable junction temperature (thermal equilibrium) is reached.
   - Use of a thermally controlled chamber is recommended.
   - You can measure the junction temperature of the FPGA using the on-chip temperature sensing diode (TSD). Refer to your device documentation for details on using the TSD. Alternatively, you can measure the junction temperature with the Intel Agilex Temperature Sensor IP Core, but with reduced accuracy.
   - If a thermally controlled chamber is not available, use temperature feedback from the on-chip TSD or Intel Agilex Temperature Sensor IP Core to control a heat sink fan to achieve a desired junction temperature.
   - You can also use a heat gun to achieve a desired temperature; however, this method offers less thermal control.
3. Keep all inputs constant and do not toggle any I/Os or any clock signals (except for the clock to the Intel Agilex Temperature Sensor IP Core, if you are using the Intel Agilex Temperature Sensor IP Core to measure temperature.)
4. Depending on the board design, you can measure static current in one of several ways:
   - Use a regulator with the ability to measure voltage drop across a shunt resistor, and query the power measurement through the power management bus (PMBus)/system management bus (SMBus) interface.
   - If a regulator with PMBus/SMBus support is not available, you can measure the voltage drop across the shunt resistor manually for each power supply and calculate the current from the voltage drop.
   - If you use an external power supply, query the current measurement from the power supply according to the manufacturer's specifications.
5. If you want to isolate and understand the static power component of your design's total power consumption, take several current measurements across a range of temperatures and record the junction temperature of each measurement. Refer to the junction temperatures to correlate static power measurements with their corresponding total power measurements.
6. The silicon static power measurements can be compared with the static power estimate from the Intel Quartus Prime Power Analyzer report or the static values shown on the **Report** tab in the Intel FPGA Power and Thermal Calculator.