Quartus II Software Release Notes

November 2008 **Quartus II software version 8.1**

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **\altera\<*version number*> \quartus** directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes* on the Altera website at **http://www.altera.com/literature/lit-qts.jsp.**

New Features & Enhancements

The Quartus II software version 8.1 includes the following new features and enhancements:

- The new JTAG Chain Debugger allows you to set up and run JTAG debugging for the JTAG devices in a JTAG chain.
- The Chip Planner now has a new **Routing Congestion Settings** dialog box that allows you to determine the percentage of utilization for specified types of interconnects, and to highlight in the Chip Planner those areas where routing congestion exceeds a specified threshold.
- The **Auto-Partition** command in the Design Partition Planner automatically creates design partitions for a selected entity hierarchy.
- The new Auto Gated Clock Conversion logic option automatically converts gated clocks to functionally equivalent logic supported by the FPGA architecture.
- The new SignalTap II Storage Qualifier allows you to specify what data are stored in memory, so that you can optimize the available on-chip memory usage and display to debug your design.
- The new Pin Advisor provides tips on I/O planning and implementation, and I/O rule checks and validation.
- Advance support for these Stratix IV devices: EP4SGX70, EP4SGX110, EP4SGX230, EP4SGX290, EP4SGX360, and EP4SGX530.
- Initial support for this Stratix IV device: EP4SE530.

EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify & Synplify Pro	9.6.2	✓
Mentor Graphics Precision RTL Synthesis	2008a	✓
Mentor Graphics LeonardoSpectrum	2008a update 1	✓
Synopsys Design Compiler	2004.12-SP4	
Magma Design Automation Blast FPGA	2.4	✓
Agility DK Design Suite	5.0 SP5	
Simulation Tools	**Version**	**NativeLink Support**
Mentor Graphics ModelSim	6.3g	✓
Mentor Graphics ModelSim-Altera	6.3g	✓
Cadence NC-Sim (Linux only)	IUS 6.2 (Linux only)	✓
Synopsys VCS / VCS MX	Y-2006.06-SP1 (Linux only)	✓
Aldec Active-HDL	7.3 SP1	✓
Formal Verification Tools (Equivalence Checking)	**Version**	**NativeLink Support**
Cadence Encounter Conformal	7.2	
Chip Level Static Timing Analysis	**Version**	**NativeLink Support**
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	**Version**	**NativeLink Support**
Mentor Graphics TAU	3.7	
Board Level Symbol/Pin-out Management	**Version**	**NativeLink Support**
Mentor Graphics I/O Designer	7.3	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 8.1	
The Quartus II software version 8.1 supports Mentor Graphics ModelSim 6.3g. Mentor Graphics ModelSim-Altera Edition and Web Edition are labeled as 6.3g_p1.	
The Quartus II software version 8.1 automatically adds a clock frequency constraint of 10 MHz for the JTAG TCK clock pin for Cyclone III devices, Stratix III devices, and newer FPGA families.	
Version 8.0 SP1	
Exporting a Memory Initialization File (**.mif** or **.hex**) to a RAM Initialization File (**.rif**) format is no longer supported in Quartus II software versions 8.0 and later.	

Description	Workaround
Version 8.0	
The ALTMEMPHY megafunction for DDR3 SDDRAM in the Quartus II software version 8.0 has following hardware, compilation, and simulation support. Hardware support: • x8 DDR3 SDRAM in UDIMM, SODIMM, and MicroDIMM format • x8 DDR3 SDRAM device support up to and including 80-bit interface widths. DDR3 SDRAM memory interfaces using devices must follow Altera-recommended layout guidelines • Single chip select support • 360MHz to 400MHz full hardware calibration Compilation support: • x4 and x8 DDR3 SDRAM device compilation support for pinout checking and timing closure • 300MHz to 533MHz compilation support. Full DDR3 SDRAM interface calibration on hardware is currently supported only using x8 DDR3 SDRAM device-based interfaces between 360MHz and 400MHz Simulation support: • Skip calibration simulation mode between 300MHz and 533MHz for x4 and x8 DDR3 SDRAM device based modules • Quick calibration simulation mode between 300MHz and 533MHz for x8 DDR3 SDRAM device-based modules only • Full calibration simulation mode between 360MHz and 533MHz for x8 DDR3 SDRAM device-based modules only	

Description	Workaround
Version 7.2 SP2	
In the Quartus II software version 7.2 SP2, the SOPC Builder Component Editor properly analyzes a VHDL-based component with generics regardless of the case of the entity (lowercase, capitals, or mixed). In the Quartus II software versions 7.2 and 7.2 SP1, it failed to process VHDL-based components with entity names that were not all lowercase.	
Version 7.2	
The **Generate back-annotation data for time closure** option in the **Design Entry/Synthesis** page under **EDA Tool Settings** in the **Settings** dialog box is no longer available.	

Constraining cells or routing causes problems for designs ported from the Quartus II software version 7.1 or 7.1 SP1 to the Quartus II software version 7.2, because location assignments to the following block types are incompatible:
 	
`IOPAD`
`IOIBUF`
`IOOBUF`
`FF`
`DDIOOUTCELL`
`DDIOOECELL`
`PSEUDODIFFOUT`
`CLKCTRL` (if specified as X,Y,N instead of as a user string)
	To prevent this incompatibility, remove the location assignments and the routing constraints.

For the alt2gxb megafunction, when adaptive equalization is activated for a specific channel, `rx_eqctrl` writes to that channel do not have any effect.	
In the Quartus II software version 7.2, there is no support for DQSB pins in Arria GX devices, but some Quartus II version 7.2 designs require DQSB pins.	
The Quartus II software no longer supports Synopsys Formality software.	

Description	Workaround
The Quartus II software no longer supports the Synopsys PrimeTime VHDL software.	Use the PrimeTime Verilog software to perform timing analysis for your design. To generate the PrimeTime Verilog files, select **Verilog** in the **Format for output netlist** list on the **Timing Analysis** page under **EDA Tool Settings**.
The TimeQuest Timing Analyzer supports clock-as-data analysis in the Quartus II software version 7.2, while previous versions of the Quartus II software did not. This results in the TimeQuest analyzer reporting new timing paths where the start point (from node) of the path is a clock node (the target of a **create_clock** or a **create_generated_clock** command. The Classic Timing Analyzer does not support clock-as-data analysis.	The behavior, which is correct, is documented in "The Quartus II TimeQuest Timing Analyzer" chapter in the *Quartus II Handbook*. You may need to modify your constraints to compensate for the clock-as-data analysis support if new timing violations are listed for your design, and you believe these violations are overly conservative for your design.
The functionality of the earlier TimeQuest SDC File Editor has been merged into the main Quartus II Text Editor. The Constraints menu from the earlier TimeQuest SDC File Editor is now located in the Quartus II Text Editor on the Edit menu on the Insert Constraints submenu.	
Starting in the Quartus II software version 7.0, when you use OC-12 with 155.52 Mhz inclock, the alt2gxb megafunction generates a design with incorrect data rate. The incorrect data rate is double of what you designed.	Starting in the Quartus II software version 7.2, when you use the SONET OC-12 protocol with the input clock frequency of 155.52 Mhz, refclk divider is generated by the alt2gxb megafunction in order to obtain the correct data rate.
The TimeQuest Timing Analyzer now performs multicorner timing analysis by default during full compilation. This behavior can be changed in the **TimeQuest Timing Analyzer** page in the **Settings** dialog box.	
Version 7.1	
When using the SignalTap II Logic Analyzer, if you select a signal to be tapped that cannot be found in the netlist, the Quartus II software will give a critical warning and proceed with compilation. This is a change of behavior from version 6.1 in which compilation would stop with an error message.	To remove the warnings, remove non-existent nodes from the SignalTap II Logic Analyzer. To revert to the behavior of version 6.1 and earlier, you can promote all critical warnings to error messages in the Messages section of the **Options** dialog box.

Description	Workaround
The altlvds_tx megafunction shows the actual phase shift of the `tx_outclock` generated instead of the core clock frequency. This change is only a change in the information that is displayed, and does not change the actual implementation.	
PLLs in Stratix II and Cyclone II devices now have a new parameter, `sim_gate_lock_device_behavior`, that is `OFF` by default. This new parameter uses a fixed, internal value of `7` to simulate the gate lock feature. If the value is set to `ON`, you can simulate the actual device behavior for gated lock using the parameter value `gate_lock_counter`, as you could in earlier versions of the Quartus II software.	
The Quartus II software version 7.1 Power Analyzer enhances the accuracy of the maximum static power estimate for Stratix II and Stratix II GX devices. The maximum static power drawn from the VCCPD power supply for Stratix II and Stratix II GX devices utilizing maximum power characteristics increases in the Power Analyzer power estimate by at most 15mW (depending on the device size.)	

Description	Workaround
The Quartus II software version 7.1 issues the error: "Error (10621): VHDL Use Clause error at <location>: more than one Use Clause imports a declaration of simple name "<name>" -- none of the declarations are directly visible." However, the Quartus II software version 7.0 and earlier did not issue the error for the same design. This changed behavior arises when a design imports overloaded subprograms with the same signature from different packages such as STD_LOGIC_UNSIGNED and STD_LOGIC_SIGNED. Both these packages define binary operations on STD_LOGIC_VECTOR arguments. Earlier versions of the software incorrectly favored the first imported declaration.	Remove one of the conflicting Use Clauses. For example, use either STD_LOGIC_SIGNED or STD_LOGIC_UNSIGNED, but not both.

Description	Workaround

The format for Conversion Setup Files (**.cof**) has changed. The element defined below (in DTD syntax) has been introduced:
 	
`<!ELEMENT hex_block (hex_filename,hex_addressing, hex_offset)>`
`<!ELEMENT hex_filename (#PCDATA)>`
`<!ELEMENT hex_addressing (#PCDATA)>`
`<!—hex_addressing value is either relative or absolute -->`
`<!ELEMENT hex_offset (#PCDATA)>`
 	
In addition the following elements have been deprecated:
 	
`<!ELEMENT bottom_boot_block (bottom_boot_filename,bottom_ addressing)>`
`<!ELEMENT main_block (main_filename, main_addressing)>`	

A key change since SOPC Builder version 7.1 is the new file format for storing system design data. Previously, SOPC Builder used a proprietary file format (PTF) to store system designs, while SOPC Builder version 7.1 uses an industry-standard XML file format for data storage. By convention, these files are given the extension **.sopc**. When you open an SOPC Builder system created in a previous version of the tools, you are asked to upgrade the system to the new format. Click **More Information** in that dialog box for details on migrating your projects and the changes in SOPC Builder file formats.	

Description	Workaround
Version 6.0	
The TimeQuest Timing Analyzer's **QSF2SDC** conversion utility cannot properly convert all Classic Timing Analyzer timing assignments. The results from the TimeQuest Timing Analyzer may also be different from the Classic Timing Analyzer due to other default behavior differences.	The **QSF2SDC** conversion utility is considered a guide to help reduce the time to switch to the TimeQuest analyzer, and it is not intended to make the TimeQuest analyzer a plug-in replacement for the Quartus II Classic Timing Analyzer. You should review all converted SDC constraints for correctness and completeness. Refer to the *Switching To the TimeQuest Timing Analyzer* chapter in the Quartus II Software Handbook for more information.
Beginning in the 6.0 release, the Quartus II Parallel Flash Loader megafunction (altparallel_flash_loader) erases flash memory blocks before programming them.	No action is required.
Beginning in the 6.0 release, Quartus II integrated synthesis handles bidirectional pins differently. For example if `bidir1` and `bidir2` are declared as `inouts`, the assignment `bidir1 <= bidir2` creates a directional connection in which data flows from `bidir2` to `bidir1`. In the Quartus II software version 5.1 and earlier, a bidirectional connection was created.	If your design requires that data flow in both directions, you must directly connect the bidirectional pins together without using an assignment statement. Assignment statements always produce a unidirectional data flow.
Version 5.1 SP2 and earlier	
The following megafunctions have clear box models that contain assignments that are not stored in the Quartus Settings File (**.qsf**) and are not written out to a Verilog Quartus Mapping File (**.vqm**): altdqs altdq altddio_bidir altddio_out altddio_input altlvds_rx altlvds_tx altufm_i2c dcfifo alt2gxb_reconfig	Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 8.1	
In the Quartus II software version 8.1 and later, the Tcl **project_open** and **set_current_revision** commands no longer overwrite the compilation database when the database version is incompatible with the current version of Quartus II software. Instead, they generate an error.	To avoid the error and overwrite the database, run `project_open -force` or `set_current_revision -force`.
The Assignment Editor does not allow you to edit the location assignment of the GXB Central control unit.	Modify the assignment manually in the Quartus II Settings File (**.qsf**) while the project is closed.
When LVDS transmitter is implemented using logic cells and when you select **Odd deserialization factor**, the MegaWizard allows you to choose between the `tx_inclock` and `tx_coreclock` port to register the `tx_in` port. However, it is incorrect to register `tx_in` using the `tx_coreclock`. This issue does not affect LVDS implementations using the hard SERDES or any implementation using even deserialization factors.	Either preregister the `tx_in` using a clock with frequency of (`output_data_rate/deserialization_factor`), or supply a clock of this frequency to the LVDS via the `tx_inclock` input port and use that clock to register the `tx_in` inputs.
The timing constraints auto-generated by the Quartus II software for the `altlvds rx_divfwdclk` output (that is, when in Soft-CDR mode) were incorrect in versions of the Quartus II software earlier than 8.1. The constraints did not correctly account for an inversion in the `rx_divfwdclk` clock path.	This issue has been resolved in the Quartus II software version 8.1. Modify designs using a Synopsys Design Constraints File (**.sdc**) with `rx_divfwdclk` timing constraints generated by a version of the Quartus II TimeQuest Timing Analyzer earlier than 8.1 to use the correct timing constraints (as generated with the current version of the TimeQuest analyzer).
The **Enable** column in the Pin Planner shows only location assignments, and does not show whether other types of assignments are disabled or enabled.	Use the Assignment Editor to view and disable assignments.

Issue	Workaround
In the Quartus II software version 8.1, the Design Assistant does not recognize one of the components in `dqs_enable_atom` as part of the WYSWYG atom and generates an incorrect warning of C101 and C103.	You can safely ignore this warning, and you can suppress the warning with the Design Assistant rule suppression.
You receive an error message `"found unknown error in a Block Symbol File"` when you insert a new symbol in the Quartus II Block Editor using the MegaWizard.	In the MegaWizard, on the **Summary** page, select the option to generate the Block Symbol File (**.bsf**).
When you convert programming files that include a Hexadecimal (Intel-Format) File (**.hex**) to program the data for a device into an EPC configuration device, the Hexadecimal (Intel-Format) File is not processed, and the processing of the rest of the file stops.	
In Design Space Explorer, Parallel DSE uses source files for a partition although the partition has a **Post-Fit Netlist Type** setting.	Ensure that you have fully compiled the design with the Quartus II software version 8.1 before using Parallel DSE.
After you use the **Auto Detect** command to detect a device in a chain with PFL multiple flash programming support, you can attach a Programmer Object File (**.pof**) to the chip. When you attempt to run any operation on the chip and the first CFI device at the same time, the operation will not start correctly and end with flash programming failure. This failure does not occur in PFL single flash programming.	When you want to perform any operation in PFL multiple flash programming, do not attach the Programmer Object File to the chip, or attach the Programmer Object File to the chip when you want to reprogram only the chip.
Using a Jam File (**.jam**) or a Jam Byte Code File (**.jbc**) that contains PFL instance with the **quartus_jli** executable or JAM player results in “out of bit size boundary” error.	Use a Jam File or a Jam Byte Code File that contains PFL instance only through the Quartus II Programmer.
Version 8.0	
If you compile a project in the command line, and you open the Quartus II software GUI on that project, you may experience unexpected and/or incorrect results.	While compiling a project in the command line, do not open the Quartus II software GUI on that project.
The **Open** dialog box does not display all files.	Restart the Quartus II software to see all the files.

Issue	Workaround
Creating a new project from the TimeQuest Timing Analyzer GUI can crash the TimeQuest analyzer GUI.	Because the TimeQuest analyzer GUI depends on the open project in the main Quartus II software GUI, create or change projects in the main Quartus II software GUI and not the TimeQuest analyzer GUI.
If you run Analysis & Elaboration after a successful compilation and then run Partition Merge, you may receive an Internal Error or see unexpected behavior due to the loss of assignments.	Run Analysis & Synthesis or run a full compilation before running Partition Merge.
The following error occurs when you manually connected the `seriesterminationcontrol` and `parallelterminationcontrol` ports on an output buffer atom, but did not make a termination assignment to the corresponding I/O that uses calibrated on-chip termination: `"Output buffer atom <name> has port <name> connected, but does not use calibrated on-chip termination"`	Disconnect the `seriesterminationcontrol` and `parallelterminationcontrol` ports on the specified output buffer atom, or make an **Input Termination** or **Output Termination** assignment to the corresponding pin that uses a value that includes **With Calibration**.
When you connect the dynamic termination control port on the output buffer of a dedicated output I/O, the error `"Output I/O <name> has dynamic termination control connected"` occurs in a design with no previous errors.	If the I/O was generated as part of an IP block, regenerate the IP block. If the I/O was user generated, then disconnect the `dynamicterminationcontrol` port, or connect it to `0` or logical ground.
An error is issued saying that an output is inverted when feeding the `dynamicterminationcontrol` port of an output buffer atom.	Remove the specified inversion.

Issue	Workaround
If there are **Dynamic Termination Control Group** assignments to two different I/Os in the design that have different dynamic termination controls but are assigned to the same group, you will receive the following error: `"Atoms <name> and <name> are assigned to the same dynamic termination control group, but their dynamic termination controls are not compatible"`	Remove all **Dynamic Termination Control Group** assignments from the design, because they are no longer necessary. If the assignments were created by an IP block, regenerate the block.
The Merged Registers and the Inverter Push-Back Through Register report panels under the Analysis & Synthesis Formal Verification report may be missing or incomplete in the Quartus II software versions 8.0 and later.	The information is available in the following two report panels in the Analysis & Synthesis Optimization Results report under Register Statistics: • Registers Removed During Synthesis (for merged registers) • Inverted Register Statistics (for inverted registers)
In the Quartus II software versions 8.0 and later, I/O primitives do not support exact pin location assignments for designs targeting Cyclone III, Stratix III, and Stratix IV devices. If your design contains I/O primitives with exact pin location assignments, you will see the following error: `The location assignment on the I/O Primitive instance "inst1" specifies an exact pin location`	Instead of using an I/O primitive you can set an exact location using the `chip_pin` attribute, or through the Assignment Editor.
When two PLLs that both use dynamic reconfiguration are cascaded, dynamic configuration may not work correctly.	Assign the `preserve_pll_counter_order` assignment to both PLLs. Using this assignment will prevent the Fitter from reordering PLL clock outputs. If the Quartus II software cannot route the clock outputs because the Fitter cannot reorder PLL clock outputs, manually change the clock ordering in the MegaWizard Plug-In Manager.

Issue	Workaround
Projects created in versions of the Quartus II software earlier than version 8.0 that use Incremental Compilation will not work properly with the smart compilation feature in the Quartus II software versions 8.0 and later. A message specifying a detected change in the `partition_hierarchy` assignment is issued and all stages of the flow are executed. Design Space Explorer, which leverages smart compilation technology, is also affected.	In the Quartus II software versions 8.0 and later, open the project in the GUI and re-save the project before using the Design Space Explorer or smart compilation.
In the Quartus II software version 8.0, the HSSI `rx/tx_coreclk` megafunction inputs have to come from HSSI clocks (`clkout`, `coreclkout`, and so on), and not from user I/Os or GPLLs unless the `coreclk` input has a **GX 0 PPM core clock** setting on it.	
In the Quartus II software version 8.0, synchronization registers have been added in the altlvds_rx megafunction. The number of registers added depends on the device family selected and the number of bits per channel (deserialization factor). However, these changes have not been propagated to the formal verification model.	
A new assignment check was introduced in Quartus II software version 8.0 that checks whether I/Os are fully constrained. Any I/Os that are not fully constrained appear as a line in a table in the Fitter report under I/O Assignment Analysis Warnings. The reason for the warning appears in the table. Certain conditions are warnings; others are errors. For example, an I/O with no assignments at all will have a reason of "Incomplete set of assignments" and an I/O with only an I/O standard assignment will have a reason of "Missing drive strength and slew rate".	Fully constrain I/Os to remove these warnings.

Issue	Workaround
In the Design Assistant, you can receive an incorrect error R101 even though your design does not contain errors when you use the TimeQuest timing analyzer, your design targets a Stratix IV device, and a clock control (clkctrl) feeds a reset port.	
In the Design Assistant, you can receive an incorrect error D103 even though your design does not contain errors when you use the TimeQuest Timing Analyzer, you use Linux, your design targets a Stratix II GX device, and there is a proper synchronizer.	
The documentation for the Quartus II software versions 8.0 and 8.1 does not include the following information about the Enable Beneficial Skew Optimization logic option: • The default value of `auto` for the project-wide `enable_beneficial_skew_optimization` assignment is equivalent to `off`. • The value of `auto` for instance level `enable_beneficial_skew_optimization` assignments means that the node in question adopts the value of the project-wide setting. • The HardCopy series of device families does not support the beneficial skew optimization feature. • Instance level `enable_beneficial_skew_optimization` assignments can be made to any node that is a clock source or destination, including pins, PLL outputs, outputs of user-instantiated clock control blocks, combinational nodes made global automatically, and any register node.	
All PLL scan chain reconfig Memory Initialization Files (**.mif**) that were generated in the Quartus II software versions 7.2 SP3 and earlier will have an incorrect bit setting value for the VCO post scale bit.	Re-generate or update the Memory Initialization Files with the Quartus II software version 8.0.

Issue	Workaround
Beneficial skew benefits can be lost when using incremental compilation.	When using the beneficial skew optimization feature together with incremental compilation, make sure that the top partition preserves routing. Otherwise, performance preservation is not guaranteed and may possibly lead to f_{MAX} degradation. That is, in the Design Partitions window, set **Netlist Type** to **Post-Fit**. Set **Fitter Preservation Level** to **Placement and Routing** or **Placement**.
The Quartus II online Help does not include a Rule attribute element for custom Design Assistant rules.	The CUT element is an additional optional element for the Rule attribute declaration: CUT--This optional, string-type attribute can have the values `on` or `off`. Setting this attribute to `on` causes the Design Assistant not to check the rule on a user cut path or false path. The default value is `off`.
The Quartus II online Help refers to the `<LOCAL_DECLARE>` and `</LOCAL_DECLARE>` tags for the Rule definition attribute for custom Design Assistant rules.	You can specify local nodes in the Rule definition `<BASIC>`, `<REQUIRED>`, `<REQUIRED_EXCEPTION>`, `<FORBID>` or `<FORBID_EXCEPTION>` subsections with the command `<NODE NAME=<node name> ...>` A local node declaration can exist more than once within a rule definition section. If more than one local node declaration exists for a given node, the last occurrence is the declaration honored. If no local node declaration exists, global node declarations are honored.

Issue	Workaround
Version 7.2 SP1	

When reading a Memory Initialization File (**.mif**), Quartus II software versions 7.2 and later generate "uninitialized memory addresses" messages, such as:
 	
`Warning: 2 out of 32 addresses uninitialized. Initializing them to "0". 2 warnings found.`
`Warning: Address 1 is not initialized.`
`Warning: Address 3 is not initialized.`
 	
Quartus II software versions earlier than version 7.2 do not have this issue.
	Open the affected Memory Initialization File and search for the "`%`" character.
	
	Because the Quartus II software version 7.2 supports multiline commenting beginning with a "`%`" and ending with a "`%`", if the "`%`" character is found in the Memory Initialization File, ensure that it does not act as a multiline separator that treats the address data as a comment, or remove the "`%` in the Memory Initialization File.

Version 7.2	
Live I/O check may produce an error if reserved pin directions are changed while live I/O check is enabled.	Turn live I/O check off and back on again to remove the error.
The Quartus II software unexpectedly exits when importing more than one partition containing JTAG logic.	Keep all JTAG logic within one imported partition, or define the logic in the top-level project instead of importing from another project.
Using Parallel Flash Loader IP optimized for speed adversely affects the CFI device programming time when using the EthernetBlaster download cable.	Use the USB Blaster or ByteBlaster II download cable instead of the EthernetBlaster Download Cable, or use the Parallel Flash Loader IP optimized for area instead of speed.
Version 7.1	
On Windows, the following cores may fail to run when the `PERL5LIB` environment variable is set: • 8B10B Encoder-Decoder • POS-PHY Level 4 • RapidIO • SerialLite II	Delete the `PERL5LIB` environment variable: 1. Right-click My Computer and click **Properties**. 2. Click the **Advanced** tab, and then click **Environment Variables**. 3. Delete **PERL5LIB** under both **User variables** and **System variables**. 4. Restart the Quartus II software.

Issue	Workaround
The Quartus II software can reduce RAM by modifying control signals while maintaining functionality. For example, in many cases a read enable can be converted into a clock enable.	This optimization is performed in Analysis & Synthesis, and can be controlled by the `optimize_power_during_synthesis` Quartus II Settings File (**.qsf**) variable. For Cyclone III, Stratix III, and Stratix IV devices, the optimization is also performed by the Fitter, and can be controlled by the `optimize_power_during_fitting` setting. Both the `optimize_power_during_synthesis` and the `optimize_power_during_fitting` variables are global settings and may also be applied to particular instances using the Assignment Editor.
If you open the **Print** dialog box or the **Page Setup** dialog box in the Quartus II software, and if you use an HP Business Inkjet 1200 series printer, the Quartus II software may produce an unexpected error.	If you have this printer, Altera recommends updating to the latest version of the drivers, available for free download from the HP website.
Altera recommends that all soft-CDR channels driven by a PLL are within a distance of 25 SERDES rows (including the unbonded SERDES) from that PLL.	
When you launch documentation (PDF and HTML files) from the MegaWizard Plug-In Manager, the MegaWizard uses the **Web browser** option in the **Internet Connectivity** page of the Quartus II **Options** dialog box. The MegaWizard will sometimes use a setting from a previous version of the Quartus II software than the present version. This can lead to errors if the web browser does not exist on your machine.	Manually edit the `WEB_BROWSER` variable in the **quartus2.ini** file and remove the reference to the non-existent web browser.

Issue	Workaround
Version 6.1	
You may get one or more messages "Error: Can't generate programming files for project because design file "<*name*>" is encrypted. It does not have license file support that allows generation of programming files" from the Assembler when compiling a design that is using Altera IP with the OpenCore Plus evaluation feature when your design has VHDL source files that have the construct "use work.all;".	The errors are reported for IP source files that were added to your project by IP Toolbench, but which are not actually used during compilation. Remove the files listed in the error messages from your project file list and recompile the design.

The Quartus II software version 6.1 may run out of memory when Formal Verification is turned on and you are using the Quartus II Integrated Synthesis flow. This happens only when Quartus II Integrated Synthesis extracts finite state machines from the design.	To avoid the out of memory issue in the Quartus II software version 6.1, turn off state machine extraction and rerun synthesis. To turn off state machine extraction, use the following settings in the Quartus II project:
	
	`set_global_assignment -name EXTRACT_VERILOG_STATE_MACHINES OFF`
	`set_global_assignment -name EXTRACT_VHDL_STATE_MACHINES OFF`
	
	You can also use the Quartus II GUI:
	1. On the Assignments menu, click **Settings**.
	2. Select **Analysis & Synthesis Settings**, and click **More Settings**.
	3. Turn off **Extract Verilog State Machines** and **Extract VHDL State Machines**.

When a design contains IP that is evaluated using the OpenCore Plus hardware evaluation feature, the Quartus II software produces a sequence of Info messages beginning with Info: Elaborated megafunction instantiation "pzdyqx:nabboc".	These messages can be safely ignored.

Issue	Workaround
Version 6.0 SP1	
Running multiple instances of the Quartus II software using the same Quartus Project File (**.qpf**) may cause unpredictable results or may cause the Quartus II software to crash.	Altera recommends that you not open multiple instances of the Quartus II software using the same project.
Version 6.0	
In the classic Timing Analyzer, when a clock (base or derived) is assigned to an internal register, then data paths to and from the register are not analyzed for clock setup and clock hold analysis.	First, analyze the design with the clock settings assigned to the internal registers. Then remove the clock settings from the internal registers and perform a second analysis, checking only paths to and from those registers. The other resolution is to use the TimeQuest Timing Analyzer instead of the classic Timing Analyzer.
The TimeQuest Timing Analyzer erroneously analyzes paths to the asynchronous data pins of registers (that is, the `adata` pin) during a recovery/removal analysis.	Apply the `set_false_path` command from the asynchronous data signal's source port or register to declare these paths as false paths.
If you change the type of a parameter setting in the Quartus II Settings File (**.qsf**) or a Block Design File (**.bdf**) and recompile your design, your change appears to have no effect. The type of a parameter is denoted by appending a prefix such as "B" (binary), "D" (decimal). For example, B"10101" represents the binary string "10101", but D"10101" represents the decimal number 10101.	Delete the **<*project*>\db** directory and recompile the design.
Version 5.1 SP2 and earlier	
Path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to Windows and Linux platforms.
If you make a single-point `CUT=ON` assignment to a node, and then override it with a point-to-point `CUT=OFF` assignment on a specific path, the `OFF` assignment will not be honored.	
The Classic Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.

Issue	Workaround
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name **file.eda.edif**.	Use design file names with only one extension.
Running individual Quartus II software executables (**quartus_map**, **quartus_fit**, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	Run individual executables either from within the Quartus II scripting shell (**quartus_sh**) or directly at a command prompt.
Do not open, change permissions, or delete the **/<*project directory*>/db** directory or any file therein while any Quartus II executable is running.	

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 8.0	
The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network, including displaying popups.	To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (**support.microsoft.com/?kbid=896054**) for more information about possible workarounds.
The ByteBlaster driver is no longer installed automatically on a PC running Windows Vista 32-bit.	If you want to use a ByteBlaster cable on a PC running Windows Vista 32-bit, install the ByteBlaster driver manually.
When you open a new design file in the Quartus II software on a PC running Windows 64-bit, then open the **Page Setup** dialog box, and click **Cancel**, the Quartus II software hangs.	

Issue	Workaround
Version 7.2 SP1	
When you install the Quartus II software version 7.2 SP1, the Nios II IDE, or any Altera-provided patches on Windows Vista with **User Account Control (UAC)** turned on, the Program Compatibility Assistant issues the warning: `"This program might not have installed correctly."`	You can safely ignore this message by selecting **This program installed correctly** or you can turn off UAC before installing the software.
Version 5.1 SP2 and earlier	
If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly, for example: • Software guards (parallel and USB) • Programming with JTAG server	Altera recommends that you have Administrator privileges when installing the Quartus II software.
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report `"JTAG Server -- internal error code 82 occurred"` when you click the **Add Hardware** button in the **Hardware Setup** dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the **jtagserver.exe** program and at a command prompt for that directory, type `jtagserver --install` <Enter>

Linux

Issue	Workaround
Version 8.1	
The Altera Complete Design Suite version 8.1 cannot be installed from the default DVD mount point on Red Hat Linux 5.0 32-bit and 64-bit machines.	To install the Altera Complete Design Suite version 8.1 on Linux 5.0: 1. Insert the DVD disc. 2. `Run mount -o ro,nosuid,nodev,uid=0 /dev/<`*cd_device_node*`> /<`*mount_directory*`>` If you are using CentOS 5, <*cd_device_node*> is **hdc**. 4. Run `/<`*mount_directory*`>/install`.
On Linux 64-bit, using a Jam File (**.jam**) or a Jam Byte Code File (**.jbc**) that contains all SRAM-based Altera devices with the Quartus II Programmer GUI results in a fatal error.	Configure or program the Jam File or the Jam Byte Code File through the command line with the **quartus_jli** executable or Jam player.
On Linux 64-bit, using a Jam File (**.jam**) or a Jam Byte Code File (**.jbc**) with the **quartus_jli** executable with the `64bit` option results in a fatal error.	Do not specify the `64bit` option operation when using a Jam File or a Jam Byte Code File using the **quartus_jli** executable.
On Linux, the MegaWizards for ALTFP_INV, ALTFP_INV_SQRT, ALTFP_EXP, and ALTFP_LOG may exit unexpectedly if you don't wait for the resource estimate display to finish updating. For wide data, this update could take several minutes. If you click **Finish** before the resource display is updated, the wizard results are still valid, but the MegaWizard may exit unexpectedly after it completes.	It is safe to ignore this unexpected exit.
Under Linux Red Hat Enterprise version 5 64-bit, opening the Text Editor during a compilation may occasionally cause the Quartus II software to crash.	Wait until the compilation completes before opening the Text Editor.
Version 7.2	
Using the Quartus II software with Linux kernel 2.4 results in slower performance than Linux kernel 2.6.	For improved performance, use Red Hat Enterprise Linux 4 or later, which is a 2.6-based kernel.

Issue	Workaround
Version 7.0	
When you are running the Quartus II software on Red Hat Enterprise Linux 4.0 and using the GNOME desktop, you may receive an internal error when you create a LogicLock region, and then use the **Add Path** dialog box to add a node for the source name with the Node Finder, and then click **Cancel** in the **Add Path** dialog box.	Do not click **Cancel** in the **Add Path** dialog box after you add a node for the source name with the Node Finder.
Version 6.1	
Under some circumstances, your web browser software may fail to launch correctly from the IP MegaStore MegaWizard Plug-In Manager. The web browser defined in the MegaWizard Plug-In Manager for the IP MegaStore inherits the environment settings from the Quartus II software. Specifically, the `LD_LIBRARY_PATH` environment variable may contain entries that conflict with web browsers such as FireFox, preventing them from starting correctly.	Edit the script that launches the web browser to make sure the Quartus II directories are the last entries in the `LD_LIBRARY_PATH` variable.
Version 6.0	
While any shortcut menu is open from an undocked dockable window, if you right-click the title bar, then all activity in the title bar (left-click and drag, shortcut menu, '**X**' close button) stops working.	Display a shortcut menu again and perform any action except right-clicking in the title bar to restore normal operation.

Device Family Issues

Arria GX

Issue	Workaround
Version 8.0	
The Verilog simulation netlist generated for a design that targets an Arria GX device is incorrect when the reconfiguration feature is used from the ALTGX or ALT2GXB MegaWizard Plug-in Manager.	Modify the netlist by moving the parameter `starting_channel_number` definition to the line above.

Stratix II GX & Stratix IV

Issue	Workaround
Version 8.0	
When the live I/O check feature of the Pin Planner is turned on and transceiver pins are present in the design, errors similar to the following occur even though the design will pass I/O assignment analysis: `"Pin <name> does not support I/O standard <default I/O standard> for <name>"`	Manually assign the proper transceiver I/O standard to the pin.

Cyclone, Stratix & Stratix GX

Issue	Workaround
Version 6.0	
The method used to report power for clock networks is different between the Quartus II PowerPlay Power Analyzer and the PowerPlay Early Power Estimator (EPE). The Quartus II PowerPlay analyzer reports the power for the resource (pin or PLL) that drives the network, while the EPE reports the power in the Clock Network section of the spreadsheet.	No action is necessary.

Cyclone III and Stratix III

Issue	Workaround
Version 7.1	
Location and other assignments made to the altpll megafunction name and intended only for the PLL WYSIWYG are also applied to logic cells created by the altpll megafunction. As a result, you may see errors indicating PLL assignments do not apply to logic cell nodes.	Make assignments intended only for the PLL on the PLL WYSIWYG name only and not on the higher-level altpll hierarchy name.

Cyclone III, Stratix III, and Stratix IV

Issue	Workaround
Version 8.1	
In the Quartus II software version 8.1, connecting the **stratixiii_crcblock atom** to the dedicated CRCERROR pin in a design causes the pin to be connected using Single Event Upset (SEU)-vulnerable core logic instead of the dedicated route unless the **Enable error detection CRC** option is turned on in the **Device and Pin Options** dialog box.	When instantiating the **stratixiii_crcblock** or **cycloneiii_crcblock** atom, turn on the **Enable error detection CRC** option.
Version 8.0 SP1	
In the Quartus II software version 8.0, incorrect behavior results in designs targeting Cyclone III, Stratix III, or Stratix IV devices when the register has an inverted `sload` signal and the `sdata=GND`, and register is packed into either the output register or input register, then the inversion is lost. This behavior is seen as incorrect because the register clears at the wrong times.	This issue is fixed in the Quartus II software version 8.0 SP1.
Version 8.0	
In the Quartus II software version 8.0, the I/O primitives do not support exact pin location assignments in designs that target Stratix III, Cyclone III, and Stratix IV devices.	Set the pin location assignment using the Assignment Editor. Note that this issue is present only when an exact pin location is specified. The location assignment is honored correctly when an IOBANK location or an EDGE location is specified.

Stratix and Stratix GX

Issue	Workaround
Version 6.0	
The Quartus II PowerPlay Power Analyzer reports PLL, XGMII state machine, GXB transceiver, and I/O pin power as contributors to the power reported for High Speed Transceiver blocks. However, the PowerPlay Early Power Estimator (EPE) spreadsheet reports this power in a “High Speed Transceiver Blocks” section as well as an entry in the “Clock Networks” section. Similarly, the PLL, SERDES blocks, and I/O pins of an LVDS block are reported in the PowerPlay Power Analyzer, and as entries in the Clock Networks and HSDI sections of the EPE spreadsheet.	

Stratix

Issue	Workaround
Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.	

Stratix II

Issue	Workaround
Version 8.0	
Compiling a Stratix II PLL in external feedback mode with its compensated clock output connected to a virtual pin triggers an Internal Error.	In external feedback mode, always connect Stratix II PLL compensated clock output to an output pin.

Stratix GX

Issue	Workaround
Version 6.0	
Timing simulation performed in the Quartus II software on designs that use the altgxb megafunction in Stratix GX devices is not accurate on the `rx_clkout` and `rx_out` outputs. The simulation is functionally correct, but the relative timing delays between the signals are not accurate.	Perform your timing simulation in another tool such as ModelSim.

Stratix II GX

Issue	Workaround
Version 8.1	
Versions of the Quartus II software earlier than 8.1 allowed illegal GXB configurations with very high PLL input clock frequency and very lower GXB datarate. Compiling these configurations in the Quartus II software version 8.1 produces an error.	For the Quartus II software version 8.1, re-generate the design with the MegaWizard, and change to the frequency and datarate to adhere to the new limits, as necessary.
Version 7.2	
The VCS flag `-ntb_opts +check` can produce the following error when running Synopsys VCS simulation using **stratixiigx_hssi_atoms.v** (alt2gxb simulation library): `Error: Illegal array access.` This out-of-bound/illegal array access at time 0 happens at unused channels/blocks where default parameter values and initial values of ports are not consistent.	Remove the `+check+` option when compiling **stratixiigx_hssi_atoms.v**. The check is to report specifically out-of-bound or illegal array access (no other type of checking).
Stratix II GX post-fit compiler databases created in the Quartus II software version 7.1 are not backwards compatible with the Quartus II software version 7.2.	Rerun the Fitter after importing Stratix II GX projects compiled in the Quartus II software version 7.1.

Issue	Workaround
Version 6.0	
The latency of alt2gxb megafunction simulations on Stratix II GX is not accurate in comparison to the device. This is due to approximation used in the Quartus II simulation in modeling the analog portion of the hardware. The latency on the digital portion is within the range of a few clock cycles of the device. The latency is an exact match with the hardware when input vectors are carefully made and do not contain any race conditions.	The Stratix II GX handbook has specified latency range information. The latency information from Quartus II simulations is a good approximation.

Stratix II and Stratix II GX

Issue	Workaround
Version 8.0 SP1	
In Quartus II software versions 8.0 and earlier, the altlvds_tx simulation model for EDA simulation shows that the `tx_outclock` signal is edge aligned with the `tx_out` signal when `OUTCLOCK_ALIGNMENT` is **180_DEGREES** and `USE_EXTERNAL_PLL` is **ON**.	Simulate the design in the Quartus II software version 8.0 SP1.

Stratix III

Issue	Workaround
Version 8.1	
When you compile a Stratix III design, the HardCopy Device Resource Guide report panel's **Memory LABs and DSP elements** rows may show Orange/Red when they should have shown Green.	If the Orange/Red rows are false and should actually be Green, no action is required. However, if the Orange/Red rows are real, you may need to take some action so that the design fits in the selected HardCopy device.

Issue	Workaround
Using the Project wizard to create a new design that targets a Stratix III device that has more than one voltage (that is, EP3SE50F484C4L has a core voltage of 0.9 V or 1.1 V) causes the Fitter to fail during compilation.	Before compiling the design, open the **Device** page in the **Settings** dialog box. Click any other device, and then click the originally selected device. Click **OK** to close the **Settings** dialog box.
Version 8.0	
You may see an Internal Error during timing analysis on a design targeting a Stratix III device to an I/O with a current strength setting of **Minimum Current** or **Maximum Current**.	Replace the current strength setting on the I/O with a correct current strength setting (for example, 12mA), instead of a maximum or minimum.
Version 7.2	

In the Quartus II software version 7.2, Stratix III devices do not support the following three primitives:
`ALT_OUTBUF_TRI_DIFF`
`ALT_IOBUF_DIFF`
`ALT_BIDIR_DIFF`	

Version 7.1	
If a design that targets Stratix III devices uses LVDS RX in an I/O row, you cannot use half-rate DDR on the TX pins of the same I/O row. As a result, you cannot use DQ pins of a DDR memory interface together with LVDS RX in any Horizontal I/O row.	

Issue	Workaround
Version 8.1	
In the Quartus II software versions 8.1 and earlier, the version-compatible database is not available for Stratix III or Stratix IV devices. The **Export Database** command and the **Version-compatible database files (For future versions of the Quartus II software)** option in the **Archive Project** dialog box are typically not available for devices that include any preliminary information in the Quartus II software, and Stratix III devices share the database structure with Stratix IV devices that have preliminary support in the software.	
If you instantiated the altlvds_rx megafunction in the Quartus II software versions earlier than 8.1, you receive this error in the Quartus II software version 8.1: `Error: LVDS_RX "rx[0]" has parameter reset_fifo_at_first_lock with illegal value true -- only value false is legal`	Generate the megafunction in the Quartus II software version 8.1.
Version 8.0	
Using the altlvds_rx megafunction in designs that target Stratix III and Stratix IV devices and not registering the output does not generate the correct warning.	

Arria GX and Stratix IV GX

Issue	Workaround
Version 8.1	
When you clock an HSSI calibration block and an HSSI PLL from the same source, an uncaught exception occurs (not an internal error).	Insert logic (a wire-LUT or LCELL for example) between the clock source and calibration block.

Issue	Workaround
The transmitter analog setting **VCCH** can be set to **Auto** and is automatically promoted to 2.5 or 3.0 volts by the Fitter. An error occurs if the promoted voltage does not match the user-assigned I/O standard on the associated transmitter pin. If it does not match, an error similar to this error occurs: `Error: I/O standard "1.5-V PCML" on I/O pin "tx dataout[0]" is incompatible the GXB channel's VCCH voltage setting "1.4V"`	Remove the I/O standard setting on the transmitter pin, match the I/O standard on the transmitter pin to the promoted V_{CCH} voltage, or set the V_{CCH} voltage to match the pin's I/O standard.

Stratix IV

Issue	Workaround
Version 8.1	
Starting in the Quartus II software version 8.1, an altgx megafunction in a design that targets Stratix IV devices generates **reconfig_togxb[3:0]** input bus. `Rx_analogreset` is ignored and `rx_pll` may not work properly in Quartus II simulation if these ports are not connected appropriately.	You must connect `reconfig_togxb` with reconfiguration controller because of silicon requirements. For functional simulation or module level simulation, you can connect **reconfig_togxb[3:0]** = **4'b0010** if you do not have a reconfiguration controller in the same scope to connect.
If you use the `GXB_0PPM_CORE_CLOCK` setting, you may get the following error: `Error: Input port CORECLK of GXB Transmitter (or Receiver) channel PCS "<name>" must be fed by output port CLOCK OUT of GXB Transmitter (or Receiver) channel PCS "< name>" because the GXB transmitters (or receivers) have the same clock rate or are operating in bonded x4/x8 mode`	Update the `GXB_0PPM_CORE_CLOCK` setting. • The `-from` field can be a clock source from an I/O, PLL, or transceiver (receiver or transmitter) clock. The transceiver clock can be identified by the transceiver pin name, the transceiver PCS node name, or the transceiver clock signal name. • The `-to` field can be transceiver (receiver or transmitter). The transceiver can be identified by the transceiver pin name, or the transceiver PCS node name
The Quartus II software version 8.1 incorrectly allows full-rate ALTMEMPHY interfaces to compile successfully even when the DQ and DQS pins are spread over two edges (top/bottom and side edges).	Memory interfaces where the DQ and DQS pins are spread over more than one side of the device are not supported for Stratix IV devices.

Issue	Workaround
In the Quartus II software version 8.1, when you compile a design that contains LVDS PLLs and targets either EP4SGX290HF29C devices or EP4SGX360FH29C devices, you receive an internal error. LVDS is not supported for these devices.	
The legal input clock frequencies are not being displayed correctly for datarates higher than 6500 Mbps. The Compiler limits the multiplier of the HSSI PLL to 10 and the L value to 1 so the PLL will have the highest likelihood of low jitter at high datarates.	If you are using a datarate above 6500 Mbps, divide the datarate by 20. That is the only allowed input clock frequency in the list. For further assistance, contact Altera Technical Support by creating a Service Request at **www.altera.com/mysupport** and provide them the reference number **rd10302008_319**.
Although the ALTGX MegaWizard allows disabling the **Insertion of deletion of consecutive characters or order sets** option under **Rate Match FIFO** on the **Rate match/Byte** order page, this option should not be disabled.	You must turn on the **Enable insertion or deletion of consecutive characters or ordered sets** option if the ALTGX configuration meets all of the following requirements: • Basic protocol • Double serializer block width • Rate Math FIFO enabled
When you choose a base datarate of 6500 Mbps or more and the effective datarate is 1/2 or 1/4 of the base datarate, only an input clock frequency that is 1/20 the base datarate should be allowed. However, the MegaWizard and Compiler currently allow multiple input clock frequencies.	When you choose a base datarate of 6500 Mbps or more, do not choose an effective datarate that is different from the base datarate.
If you select Stratix IV (GX/E) in the **Family** list and **Fastest** in the **Speed grade** list in the **Device** page of the **Settings** dialog box, only the HF35 package is shown for devices that are available in both the HF 35 and FF 35 packages. Not all parts are shown due to a filtering issue.	Select a specific speed grade in the list.

Issue	Workaround

When you lock a PCS transceiver channel, which is not PMA only, to a central channel (5 or 6) two things might occur:
An internal error:
`Internal Error: Sub-system: FHSSI, File: /quartus/fitter/fhssi/fhssi_placer.cpp, Line: 2805 golden_bin == channel_bin`
Or a no-fit error:
`Error: Can't place GXB Central Control Unit atom "top_alt4gxb_0es9:top_alt4gxb_0es9_component|cent_unit0" File: D:/designs/tgx/top.v Line: 633 Error: Atom "top_alt4gxb_0es9:top_alt4gxb_0es9_component|cent_unit0" of type "GXB Central control unit" cannot be placed at location CMU_X0_Y10_N139 that is in a different transceiver block location than the following atom(s) File: D:/designs/tgx/top.v Line: 633.`
	Remove the location constraint on the pin and/or related atoms or lock the pin down to a regular transceiver channel (1 through 4).

For designs that target Stratix IV GX devices, the EDA netlist writer may issue the following error message when any EDA tool or format is selected in any EDA tool category (except EDA simulation tool) on the **EDA Tool Settings** page: `Error: Unable to generate the EDA timing simulation netlist files because the Quartus II software does not currently support timing simulation for the Stratix IV GX devices`	In the Quartus II GUI, select any EDA simulation tool in the **Simulation** page of the **EDA Tool Settings** page in the **Settings** dialog box, and turn on the **Generate netlist for functional simulation only** option in the **More Settings** dialog box. Or, in the Quartus II Tcl shell, issue these two commands `set_global_assignment -name EDA_GENERATE_FUNCTIONAL_NETLIST ON -section_id eda_simulation` followed by `export_assignments`.

Issue	Workaround
Version 8.0 SP1	
Back-annotating a design that targets a Stratix IV device with transceivers and then compiling might result in the following error: "Error: Can't fit design in device -- nodes in regions on the device require more global signals than are available."	Remove the location assignments on the registers or logic specified in the submessages.
Version 8.0	
Transceiver blocks will not be included when you generate a PowerPlay Early Power Estimator file from the Quartus software for a Stratix IV device. Only transceiver blocks are ignored; all the other blocks (logic, RAM, I/O, and so on) are still included.	
Disabling the output termination assignment on a Stratix IV transmitter transceiver pin (Example: `set_instance_assignment -name output_termination OFF -to tx_dataout`) without a valid transceiver I/O standard assignment on the pin will result in the following error: "Error: One or more pins are missing I/O standard assignments"	Make a valid HSSI transceiver I/O standard assignment on the pin or enable the `output_termination` setting.
PCIE Gen 2 x8 will have 8 rateswitch control ports (if 8 channels are used) and only `rateswitch[0]` will control the operation. `rateswitch[7:1]` does not have any affect. The same applies to PCIE Gen2 x4 mode (`rateswitch[3:1]` has no affect).	
In designs that contain the alt4gxb megafunction, which is available through the ALTGX MegaWizard Plug-In, and that target Stratix IV devices, simulation on the output port `rx_phase_comp_fifo_error` is incorrect.	
You may be able to compile memory interface designs exceeding the *Stratix IV Device Handbook* limits.	You cannot go to production with Quartus II software version 8.0 compilation limit. Refer to the *Stratix IV Device Handbook* for actual device maximum performance.

Issue	Workaround
Designs with Stratix IV transceivers containing PCI Express hard IP atoms might not fit and might give errors related to transceiver blocks. The errors might not be specific to PCI Express hard IP–related transceivers.	Manually lock down at least one pin of transceivers that use PCI Express hard IP blocks.

Cyclone III

Issue	Workaround
If you use DDR or DDR2-SDRAM memory interfaces in designs targeting Cyclone III devices, you may receive the following warning from the TimeQuest Timing Analyzer: `Critical Warning: The register <name> fed by pin <DQ or CK0 pin> must be placed in adjacent LAB <name of adjacent LAB> instead of <name of current FF location> to the result.`	If the adjacent LAB is already used by DDIO input registers for other pins, you may receive this warning because no more than two global clocks (inverted clocks are counted separate from non-inverted clocks) may feed a LAB. To fix the warning, you need to move the CK0/CK0# pins to a location with a free adjacent LAB. A possible solution is to swap CK0/CK0# with CK1/CK1# or CK2/CK2#.

When you receive one of the following messages, there is a timing violation issue that needs to be fixed:
`Critical Warning: The register <name> fed by pin <DQ or CK0 pin> must be placed in adjacent LAB <name of adjacent LAB> instead of <name of current FF location> to the result`
`Critical Warning: Fitter could not properly route signals from DQ I/Os to DQ capture registers because the DQ capture registers are not placed next to their corresponding DQ I/Os`
`Info: DQ capture register <name> at <location> is not assigned to the adjacent LAB of the corresponding DQ I/O <name> at <location>`
	Fix the problem to avoid violating assumptions made with the macro timing analysis used for Cyclone III devices. A possible solution is to swap CK0/CK0# with CK1/CK1# or CK2/CK2#.

HardCopy II

Issue	Workaround
Version 8.0	
Behavior of region constraints on HardCopy II is changed in the Quartus II software version 8.0 such that all HCell-based logic must be placed within the region boundaries. In Quartus II software versions 7.2 SP3 and earlier, this restriction was not necessary, and there was a 20 HCell tolerance at region boundaries. This new behavior allows you to enable more advanced incremental compilation flows.	The change in behavior can cause no-fits because the available area for a region constraint is now smaller than in earlier releases. You may need to increase region sizes in order to achieve a fit.
Version 7.2	
When compiling a HardCopy II design and using the HardCopy II Advisor to compare timing against the Stratix II FPGA flow, the timing for the I/Os may be different. This difference is because the FPGA compilation used Advanced I/O Timing, which is unsupported for HardCopy II devices, to get I/O delays.	When compiling the FPGA, disable Advanced I/O Timing by setting the Quartus II Settings File (**.qsf**) assignment `ENABLE_ADVANCED_IO_TIMING` to `OFF` or turn off **Enable Advanced I/O Timing** in the **Timing Quest Timing Analyzer** page in the **Settings** dialog box.
Version 6.0	
Under certain circumstances, you may receive the following error message when migrating your Stratix II design that contains RAM blocks to HardCopy II: "`Error: Source file <`*file*`> in directory <`*dir*`> was compiled at <`*time*`> and saved at <`*time*`>. The problem reported for the file is: Only in HardCopy II (<`*design*`>).`"	Turn off the **Auto RAM Block Balancing** option for your Stratix II design and recompile the design. Then proceed with the migration process.

EPC2 Configuration Devices

Issue	Workaround
Version 6.0	
When using the EPC2 configuration device to configure an Altera FPGA using a compressed configuration bit stream, you may encounter a configuration failure due to the CONF_DONE error checking feature. The failure mode occurs when the FPGA releases the CONF_DONE signal outside the acceptable time window. The reason this may occur is because the compression ratio varies depending on the design file. Since the configuration file size varies due to compression there may be insufficient padding at the end of the configuration file. This issue can result in a configuration failure, as indicated by the nSTATUS pin transitioning low near the end of configuration. The error occurs because the CONF_DONE signal is released by the FPGA before the EPC2 device expects it to be released.	For assistance implementing the workaround, contact Altera Technical Support at **www.altera.com/mysupport** and provide the reference number **rd01232008_817**.

SOPC Builder Issues

Issue	Workaround
Version 8.1	
For parameters of type `std_logic_vector`, component authors cannot set the vector's width from within Component Editor.	After saving the **_hw.tcl** file in Component Editor, modify the **_hw.tcl** file to add the parameter's range. The width of the `std_logic_vector` parameter is derived from the range. For example, a range of `0..511` would imply 1 9-bit vector.
The `--jdi` option scans the JTAG chain, gets the first device it finds from the JTAG chain, and applies the JDI information to that device node blindly.	If there is more than one device in the chain, please load JDI information using the new **device_load_jdi** command as part of the device service, inside System Console. With that command, specify the virtual file system path to the device node of interest, so that there is no ambiguity.

Issue	Workaround

In the Quartus II software versions 7.1 SP1 and later, you may encounter the following error if you have McAfee VirusScan 8.0.0 Enterprise Edition installed during system generation in SOPC Builder or while doing a build in the Nios II IDE.
 	
`4 [main] ? (3920) C:\altera\80\quartus\bin\cygwin\bin\sh.exe: *** fatal error - couldn't allocate heap, Win32 error 487, base 0x6D0000, top 0x6F0000, reserve_size 126976, allocsize 131072, page_const 4096`
`3 [main] sh 420 fork: child -1 - died waiting for longjmp before initialization, retry 0, exit code 0x100, errno 11`
	Either temporary disable McAfee VirusScan 8.0.0 or upgrade to VirusScan 8.5.0i.

In previous versions of SOPC Builder, if your **_hw.tcl** file didn't match the HDL file, the **_hw.tcl** file was considered the correct file. In the Quartus II software version 8.1, the HDL file is considered the correct file. If correct functioning of your component relies on the **_hw.tcl** file description overriding the HDL description, your component may not operate correctly.	Ensure that the description of your component that you provide in your **_hw.tcl** file matches the HDL.
Incorrect clock interface wiring in generated HDL can occur when Tcl-based components containing clock sources are used. The problem is caused by an incorrect setting in the component hardware Tcl file, for example: set_interface_property clock_source ptfSchematicName Component Editor makes this incorrect assignment when clock source interfaces are created.	To resolve the problem, change the **ptfSchematicName** value to a system-unique string value, rather than an empty string. A sensible value to use is the name of the clock source interface, but this does not work if multiple instances of the clock-sourcing component are used. To support multiple instances, the component can provide a string parameter, which you must assign with a system-unique value. The clock-sourcing component can make the **ptfSchematicName** assignment from this string parameter in an elaboration callback.

Issue	Workaround
When you launch System Console in SOPC Builder, with no board (no SLD devices) attached to the system, and then exit System Console, a window opens with the messages that describe the exception and stack trace. Because System Console is designed to interface to boards, when no boards are attached, it throws an exception. The SLD_NO_DEVICE exception signals that no JTAG devices were found, and a warning should have been displayed instead of an error.	
Version 8.0	
The system interconnect fabric that is automatically created when you generate your system in SOPC Builder does not correctly resolve the bytes that are not selected by the byteenable lines on a 64-bit write to a 32-bit Avalon-MM slave interface with no byteenable capability. If a master module sends a 64-bit write request to a system component 32-bit Avalon-MM slave interface, the write arrives at the slave port as two separate 32-bit writes to consecutive addresses. If the byteenable lines indicate a single 32-bit write to the destination address, because the byte enables are not asserted for the second half of the 64 bits, the write nevertheless occurs at both addresses. Therefore, if the byteenable lines for the second half of the 64-bit write are not asserted, the address following the destination address is written erroneously.	Perform the following workaround for each 32-bit, byteenable-free slave port in your SOPC Builder system component: 1. In SOPC Builder, on the **System Contents** tab, add an Avalon-MM Pipeline Bridge component. 2. In the Avalon-MM Pipeline Bridge editor, under **Pipeline** options, configure the pipeline bridge with all three pipeline options turned off. 3. Under **Data** options, set **Data width** to 32 bits. 4. Under **Burst** options, turn on **Allow bursts** and set the **Maximum burst size** to **2**. 5. Connect the Avalon Memory-Mapped Master Port of the pipeline bridge to the slave port in your SOPC Builder system component. 6. Connect the Avalon Memory-Mapped Slave Port of the pipeline bridge to the master module that would otherwise be connected directly to the slave module.
A component originally provided and created with SOPC Builder component version 7.2 with multiple clock ports generates an error in the Quartus II software version 8.0.	Edit the Tcl Script File (**.tcl**) associated with the component to remove any derived clocks. This clocking scheme is not supported for the component.

Issue	Workaround
The System Console hangs with the message `NIOS2OCI::internal_unlock(): Assertion `m_locked' failed.` when accessing a service provided by a Nios II processor and services provided by other modules simultaneously.	Open as many System Consoles as are required before issuing any commands to any of them.
When masters execute write transactions to narrower-data width slaves, unintended write transactions can occur. The problem can occur only for dynamically-aligned slaves that do not have byteenable ports.	When possible, dynamically-aligned slaves should be provided with byteenable ports. In cases where the slave component cannot be modified, a simple workaround for this problem is to insert an Avalon-MM pipeline bridge in between the master and slave. (If this bridge is configured with all three of its pipeline options turned off, the component consists only of wires, and thus consumes no logic resources.)
The **Launch Altera's ALTPLL MegaWizard** button in the Edit Module wizard for the PLL component has no effect when the path to the project directory contains a space.	Instantiate the ALTPLL megafunction outside the SOPC Builder system, or move the project to a location that does not contain a space.
Tooltip information entered into Component Editor is not saved in the component's Tcl Script File (**.tcl**).	The tooltip can be added to the Tcl Script File manually as the last argument to the **add_parameter** command.
If VHDL components have a generic of type **'std_logic_vector'**, the width of the vector cannot be greater than 32 bits.	Use generics of type **integer**, or that are less than 32 bits wide.
On systems where adapters are inserted in front of the widest Avalon-MM slave in the system, generation may fail with the following message: `Base address for module_name must be a multiple of its span`	Manually readdress the slaves according to the span provided in the error message.
On Windows Vista-64, when using the 64-bit version of the Quartus II software, SOPC Builder occasionally hangs while generating the system, or while upgrading SOPC Builder system version 6.2 or earlier.	Use 32-bit version of the Quartus II software instead of the 64-bit version.

Issue	Workaround
The Nios II processor is configurable and may or may not include an MMU, MPU, and extra exception (EE) handling. However, the System Console always presents all registers from these modules as a response to **processor_get_register_names**, even when these registers don't exist. Reading MMU, MPU, and extra exception handling registers when they don't exist returns the value of other registers.	Don't read registers in the MMU, MPU, or EE modules when the Nios II processor does not include these options.
Sourcing **pci_constraints.tcl** for the PCI Lite component will fail if **Simulation** is not turned on in the **SOPC System Generation** tab.	Turn on **Simulation** in the **SOPC System Generation** tab before sourcing **pci_constraints.tcl**.
Version 7.2 SP1	
Access to bursting components, such as DDR SDRAM, may fail in SOPC Builder.	The cause for some bursting failures is related to the different bursting capabilities of Avalon-MM master and slave ports. DDR SDRAM supports burst wrapping whereas other components do not. To resolve this issue, ensure that burst boundaries are not crossed during burst transactions.
Version 7.2	
In a Nios II system, if you turn on **Enable bursts** for the **Data master** settings in the Nios II processor, data master burst reads of size > 1 from unassigned locations result in system lockup.	Avoid making data master reads from unassigned locations.
When a latent-aware Avalon master does a read access to a nonexistent location, the Avalon bus fabric returns a dummy response so that the reading master does not stall. However, only a single response (`readdatavalid` pulse) is returned. If a burst read is done to a nonexistent location, the bursting master receives only the single response, and stalls while awaiting the remaining `readdatavalid` pulses.	

Issue	Workaround
SOPC Builder generation may fail with Java errors when the system is generated from the command line using a Tcl script. These errors occur if no Xserver is running on your machine.	Set up an Xserver on your machine and regenerate the SOPC Builder system.
The SOPC Builder may generate errors regarding address span overlap when generating systems with bursting masters and wide data path widths of 32 bits or more.	Move the native addressing components farther apart so that base addresses won't overlap even if the span grows by a factor of 2 (or 4 if the data width is 128 bits).
Version 7.1	
Custom components created in versions of SOPC Builder earlier than 7.1 that have data widths that are not multiples of two and greater than 8 bits will not upgrade properly.	Import your custom logic into Component Editor and specify a data width that is at least eight bits wide and a multiple of two (8, 16, 32, 64, etc...) If you increase the width of your component to comply with these limits, the Quartus II software automatically removes any unused bits during synthesis.
An Avalon-MM master connected through an Avalon-MM pipeline bridge or Avalon-MM clock crossing bridge to Avalon-MM slaves that use native addressing will fail if the bridge is wider than the master.	Do not connect a narrow Avalon-MM master to a wider Avalon-MM bridge if that master accesses an Avalon-MM slave that uses native addressing through the bridge.
The Component Editor in SOPC Builder does not support Verilog HDL design files (**.v**) that have multiple modules or VHDL design files (**.vhd**) with multiple entities.	Use only one module for each Verilog HDL design file and one entity for each VHDL design file.
If a module dependency loop is reported between the DMA controller and pipeline bridge, the resulting system may still be functional.	The system can be generated by holding down Ctrl and clicking the **Generate** button.
Version 7.0	
If a one-bit port on a VHDL component is defined as a `STD_LOGIC_VECTOR(0 downto 0)` the port width will be mis-interpreted during SOPC Builder system generation.	Define all single-bit ports as `STD_LOGIC`.

EDA Integration Issues

Issue	Workaround
Version 8.1	
ModelSim version 6.3g has optimization turned on by default. Optimization can generate incorrect simulation results, especially when there is a race condition or there are unconnected input ports in Verilog designs.	Turn off optimization in one of the following ways: • Comment out the following line in your **modelsim.ini** file: `;VoptFlow = 1` • Specify `-novopt` with the **vsim** command.
Version 8.0	
The clock path delays reported by the PrimeTime software may not be accurate for Stratix III family, due to a limitation in min/max clock path modeling. The clock path delays reported by the PrimeTime software may be off by a few hundred picoseconds, compared to those reported by the TimeQuest Timing Analyzer.	
The Quartus II software may show false errors when you exit the Aldec Active-HDL 7.3 GUI containing the waveform window, when the Active-HDL 7.3 GUI was launched via the NativeLink interface.	Set waveform mode to standard waveform in Active-HDL 7.3 GUI by running the command **waveformmode awf**, either from the Active-HDL console window or from within the do file, before initializing simulation. You need to complete this process only once because the waveform mode is stored in the registry.

If you want to upgrade to Mentor Graphics ModelSim 6.3f release, which is more recent than the Altera- supported version of 6.1g, you can expect some speed up in simulation time. However, there are known issues with the 6.3f release.	Possible solutions include the following:
	• For designs that are giving incorrect simulation results, turn off the optimizer by commenting out the following line in the **modelsim.ini** file:
	`; VoptFlow = 1`
	• If you use altera_mf.vhd and simulate altsyncram model, avoid the known bug in version 6.3f by typing the following:
	`vcom -opt=-clkOpt altera_mf.vhd`
	instead of the normal compilation:
	`vcom altera_mf.vhd`

Issue	Workaround
Version 7.2	
When reporting timing, the Synopsys PrimeTime software issues an error message (UITE-461) that states that **rise_edge** or **fall_edge** cannot be satisfied, and assumes zero source latency for certain derived clocks.	Set variable **timing_edge_specific_source_latency** to **false** in the PrimeTime shell before reporting timing.
Mentor Graphics ModelSim Altera Edition 6.1g and the ModelSim SE 6.1g software may run out of memory with an error on the Windows platform, when compiling or simulating a large post-fit netlist.	Use a 64-bit computer running the Linux operating system to compile and simulate the design. Contact Mentor Graphics for additional support.
Version 6.1	
If there are virtual I/O pin assignments at the time of generating board-level timing files in the STAMP format, and if there is any other tool or format selected in any EDA tool category on the **EDA Tool Settings** page, you may receive an error when you run the EDA Netlist Writer.	If the design has virtual I/O pin assignments, and you want to generate board-level timing files in the STAMP format, then either remove the virtual I/O pin assignments from the Quartus II Settings File (**.qsf**) and recompile the design, or make sure the following is true before running quartus_eda: All tool and format settings in all categories are set to None with the exception of Board-Level timing analysis tool category. STAMP is selected as the EDA format in the **Board-Level Timing Analysis** tool category in the **Board-Leve**l page under **EDA Tool Setting**s. Or, you can run the following command at a system command prompt: `quartus_eda --format=stamp --board_timing <`*project*`> -c <`*revision*`>`
Version 6.0	
The ModelSim software may fail to simulate a design if **Glitch Filtering** is turned on in the EDA Simulation Settings page and the `+nospecify` option is passed to the ModelSim **vsim** command.	Remove the `+nospecify` option from the ModelSim **vsim** command.

Issue	Workaround
If you add or change a component in a Library Mapping File (**.lmf**), the Quartus II software does not recognize the changes upon the next compilation.	Delete the project database (**db**) directory and recompile.

Memory Interfaces Issues

Issue	Workaround
Version 8.1	
The Quartus II software version 8.1 incorrectly allows full-rate ALTMEMPHY interfaces to compile successfully even when the DQ and DQS pins are spread over two edges (top/bottom and side edges).	Memory interfaces where the DQ and DQS pins are spread over more than one side of the device are not supported for Stratix IV devices.
A number of warnings similar to the following warning should be expected for all RLDRAM2 CIO interfaces: `"Warning: The pin <write data pin name> must be placed on a DQ pin associated with the DQS pin for <write clock pin name>"`	Place the write clock pins in DQS-capable pins within the DQS group. However, ignore the warnings, which still appear. If there are no more DQS-capable pins in the DQS group (which is possible for x9-width interfaces), place the write clocks in pins adjacent to the DQS group that are within the same I/O bank.
ALTMEMPHY QDRII variations generated in the Quartus II software version 8.0SP1 or earlier using pseudo-x36 mode exits in the TimeQuest Timing Analyzer with an error that includes `Missing Stratix III timing model for derated tSW of HSTL_I HPAD`	Re-generate the ALTMEMPHY variation with the ALTMEMPHY MegaWizard in the Quartus II software version 8.1.
Version 8.0 SP1	
Designs with the QDRII ALTMEMPHY megafunction could fail due to an incorrect `mem_doff_n` operation. Calibration could begin before the required 2048 clock cycles (to allow the DLL on the memory device to lock) following the deassertion of `mem_doff_n`.	The ALTMEMPHY megafunction in the Quartus II software version 8.0 SP1 contains logic to ensure this condition will not occur. Regenerate the QDRII ALTMEMPHY megafunction with the Quartus II software version 8.0 SP1.

Issue	Workaround
Designs with the ALTMEMPHY megafunction generated in the Quartus II software version 8.0 or earlier and that target Stratix III devices for DDR or DDR2 SDRAM interfaces have insufficient SDC timing constraints on the datapath reset logic. This may cause the design to fail power up calibration in some cases.	Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0 SP1 to update the SDC timing constraints.
Designs with the ALTMEMPHY megafunction or the DDR/DDR2 SDRAM High Performance Controller IP created in the Quartus II software version 8.0 that target DDR or DDR2 SDRAM could fail to calibrate correctly in hardware under certain conditions. All variations and device families are potentially affected by this issue.	Regenerate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0SP1.
Version 8.0	
The SDC and Tcl scripts generated in Quartus II software versions 7.2 SP3 and earlier for all ALTMEMPHY-based memory interfaces (including the DDR High Performance Controller, the DDR2 High Performance Controller, and the DDR3 High Performance Controllers for all device families) are incompatible with the Quartus II software version 8.0. Compilation may fail in the Fitter with the error: `Error: can't read "pll_ref_clk": no such variable` and timing analysis will not run. This error occurs because the node types in the timing netlist generated by the TimeQuest Timing Analyzer in the Quartus II software version 8.0 are different from those generated in version 7.2. An SDC update is required to traverse it correctly.	Regenerate the ALTMEMPHY megafunction with the Quartus II software version 8.0.

Issue	Workaround
When you compile an ALTPMEMPHY QDRII/QDRII+ SRAM interface in the Quartus II software version 8.0, you may receive this error: `Error: Bidirectional I/O "mem_dqsn[0]" uses parallel termination but does not have dynamic termination control connected`	Regenerate the ALTMEMPHY megafunction with the Quartus II software version 8.0, or change the bidir pins `mem_dqs`, `mem_dqsn`, and `mem_dq` into input-only pins.
The ALTMEMPHY megafunction does not support DDR3 SDRAM with a row address width of 12 bits. The MegaWizard Plug-In Manager does not enforce this restriction, and selecting this option will create a non-working design.	Select a row address width of 13 bits and make sure your design accesses only row addresses in the DDR3 SDRAM within the supported 12-bit address space.
The default t_{DS}, t_{DH}, t_{IS}, and t_{IH} parameters in the ALTMEMPHY and DDR2/DDR3 High Performance Controller MegaWizard Plug-in Manager may be too optimistic, and so the timing analysis is too optimistic. These values need to be adjusted based on the specifications of the memory device and their board slew rates.	Make sure that the memory parameters t_{DS}, t_{DH}, t_{IS}, and t_{IH} entered into the Megawizard are referenced to VREF instead of to VIH or VIL. Referencing to VREF should include the time for the signal to go from VREF to VIH/VIL. The nominal slew rate for our devices is 1 V/ns for single-ended outputs and 2 V/ns for differential outputs. The computation should be: (differential DQS) $t_{DS} = t_{DSa}$(base)+ VIH(ac)min/DQ_slew_rate (differential DQS) $t_{DH} = t_{DHa}$(base) + VIH(dc)min/DQ_slew_rate (single-ended DQS) $t_{DS} = t_{DS1a}$(base)+ (VIH(ac)min / DQ_slew_rate) + (VIH(dc)min / DQS_slew_rate) (single-ended DQS) $t_{DH} = t_{DH1a}$(base) + (VIH(dc)min / DQ_slew_rate) + (VIH(dc)min / DQS_slew_rate) $t_{IS} = t_{IS}$(base) + VIH(ac)min/addr_cmd_slew_rate $t_{IH} = t_{IH}$(base) + VIH(dc)min/addr_cmd_slew_rate

Issue	Workaround
The calibration sequencer in the ALTMEMPHY megafunction for QDRII SRAM interfaces has been updated to make the calibration algorithm more robust under certain hardware conditions.	To guarantee reliable calibration, regenerate all QDRII and QDRII+ SRAM ALTMEMPHY variations in the Quartus II software version 8.0.
If you generate a DDR/DDR2/DDR3 HP Controller or ALTMEMPHY with **Enable dynamic parallel on-chip termination (OCT)** turned on, and then re-generate with it turned off, you will have the old OCT assignments still preset.	To avoid this issue, either remove all assignments from your project before running the assignments script from the re-generated project, or use the Pin Planner to apply the assignments in the first instance, and re-generate the assignments. The Pin Planner should then remove the old assignments when you update the IP instance.
If the PLL reference clock IO voltage does not match the IO voltage of your memory interface, you receive “no fit” errors on DDR/DDR2/DDR3 HP Controller or ALTMEMPHY of the form: `Error: Can’t use clock type External Clock Output at location CLKCTRL PLLL2E1 for clock control block or source node <snip>altmemddr2_phy_alt_mem_phy_clk_reset_siii:clk|mem_clk_2x with clock type Dual-Regional Clock -- clock types do not match`	To resolve the issue, make sure to set an I/O standard on the PLL input clock that has the same voltage as that for your memory interface.
Cyclone III DDR/DDR2-SDRAM High Performance Controller IP generated prior to the Quartus II software version 8.0 will show the following warning message: `Read and write timing characteristics of memory interface <instance name> are preliminary`	To remove the message, re-generate the memory interface using the IP generated in the Quartus II software version 8.0.

Issue	Workaround
Designs with the ALTMEMPHY megafunction created in the Quartus II software version 7.2 SP3 and earlier that target Stratix III devices for full-rate DDR or DDR2 SDRAM interfaces incorrectly handle incomplete write bursts causing the remaining write operations in the burst not to be masked due to the DM signals not being returned to the high state.	Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0.
The Quartus II software does not automatically place the CK/CK# pins for DDR/DDR2/DDR3 memory interfaces on the same edge as the interface's DQ pins. As a result, you may see the following warning message: `Critical Warning: Pin <CK pin> must be placed on a <edge> I/O to match the path of the read data pins`	Place the specified CK pin on the specified edge of the device.
You cannot achieve timing closure for designs targeting Stratix III and Stratix IV devices running DDR3 SDRAM at 533MHz in -2 speed grades, and DDR2 SDRAM at 333MHz in –C4, -C4L, and –I4L speed grades at 1.1V.	These designs can be used for prototyping and testing but you should not go to production until Altera releases IP able to achieve these speeds. To meet timing at 333MHz in -C4, -C4L, and –I4L speed grades at 1.1V, use 400MHz-rated DDR2 memory and underclock it to run at 333MHz.
The ALTMEMPHY megafunction does not guarantee timing closure when address and command signals are on a side that is across from the DQS/DQ pins (for example, DQS/DQ pins are on the top side and address/commands are on the bottom side of the device).	Some of the Stratix IV GX devices do not have user I/Os on the left/right I/O banks as the banks are used for transceivers, forcing the address and command signals to be in the same bank as the DQS/DQ pins limiting the width of your memory interface.
RLDRAM II Controller MegaCore functions that were generated in the Quartus II software versions 7.2 SP3 and earlier are missing timing constraints for the capture data between IOE and the FPGA fabric.	Regenerate the RLDRAM II Controller MegaCore function, and rerun DTW. For detail information, please refer to the *MegaCore IP Library Release Notes and Errata* on the Altera website.

Issue	Workaround
Stratix III designs using external memory interfaces may cause a compilation error if the data pins of your external memory interface use I/O pins on more than one side of the device. External memory interfaces with DQ pins exclusively bound in top, bottom, left, or right side I/O pins are not affected. The error message is "`Error: Cannot place DQ I/O "mem_dq[nn]" to I/O location Pin Nn since its memory interface I/O group cannot be placed.`"	Altera recommends that data groups for external memory interfaces be grouped on a single side of your Stratix III FPGA. If you cannot group your DQ pins on a single side or if you want more information on this issue, contact Altera Technical Support at **www.altera.com/mysupport** and provide the reference number **rd05232008_407**.
Version 7.2 SP1	
Designs with the ALTMEMPHY megafunction and that target Stratix II devices for 333 MHz DDR2 SDRAM interfaces may not meet setup timing on the postamble paths in a default compilation.	Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 7.2 SP2. Place the registers manually on the resynchronization and postamble paths close to the I/O pins. Postamble setup slacks may be further increased in ~50 ps increments by applying the **DQS Bus to Input Register Delay** logic option in the Assignment Editor to the DQS pin names to increment the slack to the DQS pins in the interface, but with the trade-off cost of decreased postamble enable/disable setup slack. If you use the logic option to increase the delay, make sure your design meets timing on all postamble and postamble enable/disable paths.
The ALTMEMPHY megafunction does not support DDR SDRAM with **CAS Latency** setting **2.0** or **2.5** on the Stratix III device family. The MegaWizard does not enforce this restriction, and selecting this option will create a non-working design.	Use a **CAS Latency** setting of **3.0**.

Issue	Workaround
Version 7.2	
If you have, in the same project, more than one ALTMEMPHY variation generated in different versions of the Quartus II software, you may see a Verilog syntax error reported by synthesis. This error is caused by a common file used by all ALTMEMPHY variations, that has changed from an earlier version of the Quartus II software.	Open all the variations in the ALTMEMPHY MegaWizard in the latest version of the Quartus II software and regenerate them.
The Quartus II software version 7.2 does not support automatic placement of the write data clock output pins when you use the ALTMEMPHY megafunction. For Stratix III DDR/DDR2/DDR3 SDRAM High Performance Controllers, the Quartus II software automatically places the write data clock output pins correctly, but not for the QDRII+/QDRII SRAM ALTMEMPHY interface.	If your design targets Cyclone III or Stratix III devices, fix this issue by regenerating the memory interface IP in the Quartus II software version 8.0. However, if you use Pseudo x 36 mode for QDRII-SRAM or QDRII+-SRAM on Stratix III devices, place the `mem_clk` pin for clocking write data on a DQS pin for QDRII+/QDRII SRAM memory interfaces.
Designs with the ALTMEMPHY megafunction that target Stratix II devices for 333MHz DDR2 SDRAM interfaces may not meet timing on the postamble paths in a default compilation.	Place the registers manually on the resynchronization and postamble paths close to the I/O pins. Some designs may require additional modification. For further assistance, contact Altera Technical Support by creating a Service Request at **www.altera.com/mysupport** and providing the reference number **rd10182007_886**.
Version 6.1	
The assignments generated for the ALTMEMPHY megafunction, in the <*variation_name*>**_pin_assignments.tc**l file, assume that the top-level pin names match the pins on the ALTMEMPHY variation. Using different names for your top level pins, including using single bit signals instead of one-bit busses, will result in incorrect behavior.	Use the Assignment Editor or Pin Planner to change the assignments to match the top-level pin names in your design.

Simulation Model Changes

altera_mf Models

Model	Changes
scfifo	• The scfifo megafunction outputs 'x' for overflow and underflow cases.
dcfifo	• Added metastability protection when dcfifo is manually instantiated with parameter `wrsync_delay_pipe` or `rdsync_delay_pipe` left at the default value.
altsyncram	• Added support to display hierarchy name in Verilog error or warning messages. • Added support for byte-addressed Hexadecimal (Intel-Format) File (**.hex**).

220model

Model	Changes
lpm_clshift	• Added support for pipelining o New parameters: `lpm_pipeline` o New ports: `clock`, `clken`, `aclr`

Latest Known Quartus II Software Issues

For more information about known software issues, look for information in the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

Software Issues Resolved

This section list the numbers of the Customer Service Requests that were fixed or otherwise resolved in this version of the Quartus II software.

Customer Service Request Numbers Resolved in this Release					
10302995	10330385	10344568	10382706	10416070	10455720
10473426	10491614	10494944	10507912	10508678	10510674
10512623	10522887	10538257	10539927	10551868	10556254
10556652	10561225	10564908	10566735	10570988	10575051
10575140	10575400	10575547	10576021	10580637	10581941
10582468	10584548	10585930	10585943	10586301	10586647
10587132	10588047	10588672	10588871	10591027	10591357
10593512	10594027	10596033	10596062	10597615	10597841
10598883	10600688	10603723	10603746	10605832	10606485
10606683	10607081	10608079	10608505	10608594	10608915
10609599	10609760	10609878	10610795	10610834	10611349
10611453	10611512	10611764	10611971	10613190	10613957
10614278	10614454	10614959	10615134	10615368	10617366
10618014	10618555	10618783	10619172	10619328	10619587
10620028	10620396	10620441	10620834	10621397	10621999
10622232	10623120	10623150	10623341	10623801	10624153
10624992	10625302	10625593	10625669	10625858	10625930
10626210	10626311	10626575	10626785	10627180	10628237
10628764	10628961	10629541	10629639	10630605	10631261
10632655	10632880	10632940	10633017	10633287	10633758
10633908	10633909	10634003	10634264	10634451	10634509

Customer Service Request Numbers Resolved in this Release					
10634525	10634529	10634653	10634741	10634782	10635065
10635637	10635946	10635991	10636076	10636144	10636233
10636410	10636701	10636871	10636959	10637118	10637268
10637287	10637575	10637775	10638300	10638464	10638679
10638782	10638794	10639030	10639276	10639651	10639691
10639887	10640133	10640307	10640483	10640543	10640575
10640621	10640747	10640832	10640959	10640998	10641615
10641897	10642203	10642774	10642867	10642942	10643071
10643160	10643171	10643529	10643648	10643669	10643717
10643720	10643755	10643785	10643786	10643875	10643876
10643916	10644182	10644332	10644403	10644411	10644431
10644577	10644659	10644750	10644798	10644837	10644919
10644954	10644965	10644977	10645012	10645154	10645155
10645169	10645213	10645238	10645341	10645603	10645608
10645699	10645745	10645815	10645871	10645940	10646148
10646270	10646474	10646489	10646539	10647095	10647100
10647104	10647193	10647218	10647247	10647375	10647486
10647558	10647876	10647920	10648066	10648115	10648273
10648580	10648611	10648671	10648900	10648972	10648973
10648975	10649053	10649054	10649102	10649163	10649196
10649228	10649371	10649389	10649401	10649409	10649446
10649449	10649477	10649634	10649638	10649654	10649689
10649744	10649771	10649876	10649979	10649994	10650027
10650030	10650082	10650095	10650108	10650143	10650171
10650230	10650249	10650370	10650459	10650518	10650587
10650621	10650811	10650814	10650825	10650858	10650900
10650925	10650938	10651160	10651272	10651336	10651448
10651455	10651459	10651464	10651599	10651666	10651667
10651673	10651751	10651822	10651957	10652007	10652010
10652019	10652151	10652155	10652191	10652222	10652232

Customer Service Request Numbers Resolved in this Release					
10652253	10652273	10652350	10652385	10652492	10652599
10652624	10652626	10652628	10652667	10652753	10652759
10653014	10653128	10653139	10653228	10653269	10653330
10653345	10653477	10653517	10653553	10653594	10653654
10653686	10653867	10653903	10654002	10654055	10654114
10654260	10654407	10654443	10654512	10654541	10654554
10654585	10654647	10654993	10655155	10655161	10655180
10655184	10655205	10655305	10655308	10655337	10655415
10655454	10655530	10655625	10655681	10655756	10655973
10656046	10656218	10656276	10656572	10656662	10656777
10656843	10656864	10656890	10656893	10656962	10657016
10657075	10657077	10657081	10657106	10657395	10657504
10657533	10657598	10657621	10657651	10657653	10657655
10657679	10657730	10657769	10657896	10657991	10658025
10658038	10658060	10658089	10658158	10658175	10658206
10658252	10658295	10658458	10658630	10658765	10658864
10658870	10659016	10659112	10659139	10659245	10659389
10659403	10659408	10659623	10659632	10659744	10659818
10659912	10660036	10660157	10660354	10660461	10660477
10660492	10660528	10660587	10660609	10660627	10660631
10660651	10660779	10660859	10661098	10661243	10661457
10661538	10661614	10661662	10661671	10661742	10661749
10661763	10661856	10661925	10661933	10662175	10662242
10662289	10662333	10662366	10662398	10662416	10662471
10662584	10662585	10662594	10662848	10662931	10662987
10663001	10663035	10663036	10663189	10663341	10663374
10663458	10663944	10664158	10664331	10664413	10664425
10664434	10664513	10664565	10664616	10664642	10664730
10664804	10664929	10664986	10664996	10665005	10665008
10665148	10665210	10665211	10665252	10665274	10665288

Customer Service Request Numbers Resolved in this Release					
10665736	10665798	10665839	10665946	10665948	10665983
10666192	10666276	10666287	10666546	10666776	10666973
10667144	10667364	10667434	10667501	10667865	10667959
10668161	10668463	10668633	10668727	10669328	10669591
10669675	10669770	10670055	10670339	10670745	10671206
10672637	10656926	10652892			

Revision History

Revision	Description
1.1	Initial Release