Quartus II Software Version 12.0 Release Notes

This document provides late-breaking information about the following areas of the Altera® Quartus® II software version 12.0.

For information about operating system support, refer to the **readme.txt** file in your **altera/<*version number*>/quartus directory**. For information about disk space, memory requirements, and device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Version 12.0 Device Support Release Notes*. For the latest information about the MegaCore® IP Library, refer to the *MegaCore IP Library Release Notes and Errata*.

New Features & Enhancements

The Quartus II software version 12.0 includes the following new features and enhancements:

- Programming file support for the following Arria V ES device: 5AGXB3ES.
- Programming file support for the following Stratix V production devices: 5SGXA3, 5SGXA4, 5SGXA5, 5SGXA7, 5SGSD4, 5SGSD5.
- Initial support for Arria V GT, Cyclone V E, Cyclone V GT, and Cyclone V SoC devices.
- Advance compilation support for upcoming devices in the Arria V, Cyclone V, and Stratix V device families.
- Qsys now supports the ARM® AMBA® AXI3™ and PCI Express® (PCIe®) Gen3x4 interface protocols.
- DSP Builder now allows you to communicate with board memory from MATLAB with the System Console.

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- The Chip Planner provides additional tools that allow you to view the placement of your design.
- Quartus II Help can be used with the following browsers:
  - Local Quartus II Help (Help on a local drive installed by the Altera Installer) is fully compatible with Microsoft Internet Explorer 8, Mozilla Firefox 7.0, and Safari 5 running on Windows 7 operating systems. You can view the Quartus II Help in Google Chrome; however, you cannot open a Chrome browser from the Quartus II GUI. You must start Chrome with the `--allow-file-access-from-files flag` and then navigate to *<quartus installation directory>***/common/help/master.htm**.
  - Local Quartus II Help is fully compatible with Mozilla Firefox 3.6 running on Linux 32-bit systems.
  - Quartus II Web Help (hosted at http://quartushelp.altera.com/current) is fully compatible with Microsoft Internet Explorer 8, Mozilla Firefox 7.0, Safari 5, and Google Chrome.
  - Some Help features require you to disable pop-up blocking.

EDA Interface Information

The Quartus II software version 12.0 supports the following EDA tools:

Synthesis Tools	Version	NativeLink Support
Mentor Graphics® DK Design Suite	5.0 SP5	✓
Mentor Graphics Precision RTL Synthesis	2012a	✓
Mentor Graphics LeonardoSpectrum™	2012a	✓
Synopsys Synplify, Synplify Pro, and Synplify Premier	E-2012.03-SP1	✓
Simulation Tools	**Version**	**NativeLink Support**
Aldec Active-HDL	9.1 (Windows only)	✓
Aldec Riviera-PRO	2012.02	✓
Cadence NC-Sim	11.10.002 (Linux only)	—
Mentor Graphics ModelSim® SE	10.0d	✓
Mentor Graphics ModelSim PE	10.0d	✓
Mentor Graphics QuestaSim	10.0d	✓
Mentor Graphics ModelSim-Altera	10.0d	✓
Synopsys VCS / VCS MX	2011.12	✓
Formal Verification Tools (Equivalence Checking)	**Version**	**NativeLink Support**
Cadence Encounter Conformal	8.1	—

Chip Level Static Timing Analysis	Version	NativeLink Support
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing	**Version**	**NativeLink Support**
Mentor Graphics TAU	—	—
Chip Level Static Timing Analysis	**Version**	**NativeLink Support**
Mentor Graphics I/O Designer	—	—

Changes to Software Behavior

This section documents instances in which the behavior and default settings of the Quartus II software have been changed from earlier releases of the software.

Refer to the Quartus II Default Settings File (**.qdf**), *<Quartus II installation directory>***/quartus/bin/assignment_defaults.qdf**, for a list of all the default assignment settings for the latest version of the Quartus II software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 12.0	
The Quartus II software will no longer support the SUSE Linux Enterprise operating system beginning with version 12.1	The Quartus II software version 12.0 SP2 will be the last version to support the SUSE Linux operating system.
For ALTGX megafunctions operating in **Basic (PMA Direct)** transmitter mode, the Quartus II software version 12.0 adds the following delays to the Stratix IV timing model to correct the core-to-PMA timing path: ■ For Stratix IV 530 and 360 devices, 550 ps ■ For Stratix IV 230 and 110 devices, 350 ps These added delays affect only Stratix IV designs that use the ALTGX megafunction in **Basic (PMA Direct)** transmitter mode.	To use the corrected core-to-PMA timing model, recompile the design (or, at a minimum, perform timing analysis) in the Quartus II software version 12.0. The added delay might make timing closure more difficult. If you have difficulty with timing closure, refer to *How can I optimize timing performance for PMA Direct interfaces in Stratix IV devices?* on the Altera website.
If during a compilation, I/O placement succeeds but the design fails to meet timing, you can now perform a seed sweep and keep the successful I/O placement by making a PERIPHERY_SEED assignment and setting its value to the SEED value of the successful I/O placement operation. For example, you can now make the following QSF assignment: `set_global_assignment -name PERIPHERY_SEED 1` By default, the initial SEED value is 1.	

Known Issues & Workarounds

This section provides information about the following known issues that affect the Quartus II Software.

For more information about known software issues, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

General Quartus II Software Issues
Simulation of transceiver IP with Mentor Graphics ModelSim SE 10.0d might fail
Fatal Error: Access Violation at 0X00000000067110F0A Module: quartus.exe while setting multicycle paths in the TimeQuest Timing Analyzer
ALTFP_ATAN megafunction incorrectly ties its clock enable port to ground
In the ALTGX MegaWizard Plug-In Manager, changing the protocol setting might result in creation of an extraneous port
ALTPLL megafunction: Warning (15567): Can't achieve requested Medium bandwidth type; current PLL requires a bandwidth value of between 0.500 Mhz and 2.000 Mhz -- achieved bandwidth of 1.98 MHz to 2.97 MHz
ALTPLL_RECONFIG megafunctions cannot be simulated with the NativeLink flow
Recovery and removal timing violation warnings when compiling a DCFIFO megafunction
In Qsys, a clock source connected to an external clock and an internal reset does not automatically include the clock signal on the reset controller
Qsys: Error (12007): Top-level design entity "<entity name>" is undefined
In Qsys-generated systems, Avalon slaves might be unable to accept write transfers from AXI masters in some circumstances
Maximum pending read values in clock crossing bridges for designs migrated from SOPC Builder to Qsys might cause an out of memory error
Qsys validation does not check AXI slave ID width

Simulation of transceiver IP with Mentor Graphics ModelSim SE 10.0d might fail

Description

If you attempt to perform a post-fit VHDL simulation of a design that contains transceiver IP with Mentor Graphics ModelSim SE 10.0d, the simulation might fail.

Workaround

In the MentorSim SE software, turn off the vopt optimizer by running `vsim` with the `-novopt` option.

Fatal Error: Access Violation at 0X0000000067110F0A Module: quartus.exe while setting multicycle paths in the TimeQuest Timing Analyzer

Description

In the **Summary of Paths** tab in the TimeQuest Timing Analyzer, if you select more than one clock, and then run **Set Multicycle (between clocks)**, TimeQuest might exit with an error similar to the following:

```
Fatal Error: Access Violation at 0X0000000067110F0AModule: quartus.exe
```

Workaround

In the **Summary of Paths** tab, select only one clock before selecting the **Set Multicycle (between clocks)** command. Specify the other clock in the **Set Multicycle Path** dialog box that opens after you select the command.

ALTFP_ATAN megafunction incorrectly ties its clock enable port to ground

Description

In the ALTFP_ATAN megafunction, the `clk_en` port is incorrectly tied to ground if you do not enable the port in the MegaWizard Plug-In Manager.

Workaround

In the ALTFP_ATAN MegaWizard Plug-In Manager, enable the `clk_en` port and either tie it to VCC or control the port as required for your design.

In the ALTGX MegaWizard Plug-In Manager, changing the protocol setting might result in creation of an extraneous port

Description

If you begin to configure an ALTGX megafunction in the MegaWizard Plug-In Manager and then change the protocol, the generated megafunction might retain some extraneous ports from the initial protocol.

For example, extraneous ports might be retained if you:

1 Change the ALTGX protocol to **Basic (PMA Direct)**.

2 Change the ALTGX protocol to **GIGE**.

3 Turn on **rx_invpolarity mode**.

4 Change the ALTGX protocol back to **Basic (PMA Direct)**.

The generated ATLGX megafunction will have an `rx_invpolarity` port even though the PMA Direct protocol has no `rx_invpolarity` port.

Workaround

Avoid repeatedly changing the ALTGX protocol. If you have begun to configure the megafunction and want to change its protocol, restart the MegaWizard Plug-In Manager.

ALTPLL megafunction: Warning (15567): Can't achieve requested Medium bandwidth type; current PLL requires a bandwidth value of between 0.500 Mhz and 2.000 Mhz -- achieved bandwidth of 1.98 MHz to 2.97 MHz

Description

On the **Bandwidth/SS** page of the **Parameter Setting** tab of the ALTPLL MegaWizard Plug-In Manager, if you select **Auto** under **How would you like to specify the bandwidth setting?**, during compilation the Quartus II software might generate a message similar to the following:

```
Warning (15567): Can't achieve requested Medium bandwidth type; current
PLL requires a bandwidth value of between 0.500 Mhz and 2.000 Mhz --
achieved bandwidth of 1.98 MHz to 2.97 MHz.
```

The Quartus II software generates this message even though you did not request a **Medium** bandwidth type.

Workaround

You may safely ignore this message.

ALTPLL_RECONFIG megafunctions cannot be simulated with the NativeLink flow

Description

If you start simulation of a design that contains an ALTPLL_RECONFIG megafunction from the Tools menu of the Quartus II software, the simulation incorrectly reports no toggling of the `reconfig` and `output` clock signals.

Workaround

Run simulation from your simulation tool.

Recovery and removal timing violation warnings when compiling a DCFIFO megafunction

Description

During compilation of a design that contains a DCFIFO megafunction, the Quartus II software may issue recovery and removal timing violation warnings.

Workaround

You may safely ignore warnings that pertain to cut paths. To ensure that the design meets timing, enable the ACLR synchronizer for both read and write domains and set an achievable timing constraint.

The DCFIFO megafunction has been tested with no timing violations using the default 1 GHz TimeQuest timing constraint with 500-800 MHz F_{MAX} timing expectations.

In Qsys, a clock source connected to an external clock and an internal reset does not automatically include the clock signal on the reset controller

Description

In a Qsys design, if a clock source component is connected to an internal reset and an external clock, the HDL generated by Qsys does not include the external clock signal on the reset controller. During generation, Qsys issues a message similar to the following:

```
Cannot find clock source for <clock_input>. If <clock_input> is exported
please use a clock bridge and reset bridge instead of a clock source.
Reset synchronizer, <sync name>, may not function if not connected to a
clock source.
```

Workaround

Altera recommends using a clock bridge connected to a reset bridge instead of a clock source component.

Qsys: Error (12007): Top-level design entity "<entity name>" is undefined

Description

In Qsys, if you use uppercase letters in your entity names, the Quartus II software might convert the Qsys project path, Quartus II IP file name (**.qip**), and top level design name to lowercase. During compilation, for entity names that include uppercase letters, the Quartus II software might generate an error similar to the following:

```
Error (12007): Top-level design entity "<entity name>" is undefined
```

Workaround

To ensure that these entity names match, follow these steps:

1. In the Quartus II software, on the Assignments menu click **Settings**. In the **Settings** dialog box, select **General**.
2. Edit the entity names to match the names in Qsys.

In Qsys-generated systems, Avalon slaves might be unable to accept write transfers from AXI masters in some circumstances

Description

In a Qsys-generated system, if an AXI master issues a write transfer with all write strobes deasserted to a nonbursting Avalon slave, the slave sees a write with all byteenables deasserted. A nonbursting Avalon slave might be unable to accept this byteenable pattern.

Workaround

If the slave cannot accept this byteenable pattern or does not have the bytenable signal, you can edit the Qsys-generated HDL files to avoid this problem.

The top-level Qsys file has an altera_merlin_slave_agent instance with the name <*slave name*>_<*slave interface name*>_agent. Modify the parameter value of `SUPPRESS_0_BYTEEN_CMD` of this instance to `1`.

Because the HDL file is regenerated each time you regenerate the system, you may want to make a backup of the modified file so that you can reapply the parameter value edit after a subsequent regeneration.

Maximum pending read values in clock crossing bridges for designs migrated from SOPC Builder to Qsys might cause an out of memory error

Description

In a design migrated from SOPC Builder to Qsys, the clock crossing bridge might be parameterized with a large maximum pending reads value. The maximum value causes Qsys to attempt to generate a very deep FIFO buffer in the interconnect, possibly resulting in an out of memory error.

Workaround

To avoid the creation of a very deep FIFO buffer, perform the following steps:

1. Instantiate a pipeline bridge that has the same parameterization for address, data width, and maximum burst size before the clock crossing bridge and then disable pipelining. This ensures that no logic is generated between the pipeline bridge and the clock crossing bridge.
2. Set the maximum pending read transactions value of the pipeline bridge to a maximum of 32. This limits the FIFO buffer depth to the specified value.

Qsys validation does not check AXI slave ID width

Description

In Qsys, interconnect validation does not check whether an AXI slave's ID width is wide enough to accept a concatenation of a master's ID width and the interconnect-assigned ID.

Workaround

Ensure that you parameterize AXI slaves so that their ID widths are equal to or larger than `maximum_id_with_of_connected_masters` + $\log_2$(`number_of_connected_masters`).

Platform-Specific Issues

This section provides information about the following known issues that affect the Quartus II software when it is running on specific operating systems:

Issues That Affect Linux Operating Systems
Error: The Quartus II software cannot be started because the current platform, 'linux64', does not appear to be installed in: <installation directory>
Dell computers running Red Hat Enterprise Linux 6 might be unable to connect to a Quartus licensing server
Cadence NC-Sim error: ncelab: *F,INTERR: INTERNAL EXCEPTION

Error: The Quartus II software cannot be started because the current platform, 'linux64', does not appear to be installed in: <installation directory>

Description

If you install the 32-bit version of the Altera Complete Design Software to a 64-bit Linux operating system, starting the Quartus II Programmer or the Nios II Software Build Tools for Eclipse generates the error:

```
The Quartus II software cannot be started because the current platform,
'linux64', does not appear to be installed in: <installation directory>
```

Workaround

If you do not use the jtagserver to program or debug your FPGA, you may safely ignore this message. The Quartus II Programmer and Nios II Software Build Tools for Eclipse will start normally.

If you use the jtagserver, install the 64-bit version of the Altera Complete Design Software. Running the 32-bit jtagserver on a 64-bit Linux operating system is unreliable.

Dell computers running Red Hat Enterprise Linux 6 might be unable to connect to a Quartus licensing server

Description

Dell PowerEdge, C Series, and Precision Workstation systems running Red Hat Enterprise Linux 6 may be unable to contact a Quartus II licensing server. In the **License Setup** page of the **Options** dialog box of the Quartus II software, affected systems have a **Network Interface Card (NIC) ID** of **000000000000**.

Red Hat has changed the default network device names for network interfaces from `eth[n]` to `em[n]`. The new `em[n]` names are not compatible with Quartus II licensing.

Workaround

For detailed information about Red Hat's new network device naming, refer to Consistent Network Device Naming on the Red Hat website.

To revert to the previous network device naming convention (which is compatible with Quartus II licensing), refer to A.3. Enabling and Disabling the Feature on the Red Hat website.

Cadence NC-Sim error: ncelab: *F,INTERR: INTERNAL EXCEPTION

Description

Simulation with Cadence NC-Sim version 11.10 might fail under one or more of the following conditions:

- You attempt to perform post-fit simulation on a design that includes Stratix V transceiver blocks.
- You attempt to perform RTL simulation of a design that includes Ethernet IP variations.

Under these conditions, NC-Sim generates the following error message:

```
ncelab: *F,INTERR: INTERNAL EXCEPTION
```

Workaround

Install the latest hotfix versions of Cadence NC-Sim.

Device Family Issues

This section provides information about the following known issues that affect designs that target specific device families in the Quartus II software:

Arria II Known Issues

The following known issue affects designs that target the Arria II device family:

Issues That Affect Arria II Devices
Error (21216): Cannot enable error detection cyclic redundancy check without instantiating the ALTERA_CRCERROR_VERIFY megafunction.

For more information about known Quartus II software issues that affect the Arria II device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_aii_ki

Arria V Known Issues

The following known issues affect designs that target the Arria V device family:

Issues That Affect Arria V Devices
Error: (vsim-3694) The implicit port connection (.*) did not find a matching port, net, variable or interface instance
Arria V designs that include fractional PLL and CMU PLL cascading fail to simulate
Setup and hold timing violations on the rx_clkout domain of a Deterministic Latency PHY megafunction
The Design Assistant generates spurious warnings for Arria V designs that include 10GBASE-R PHY v12.0 megafunctions
10 Gigabit Ethernet PCS megafunctions might fail timing
The clocks of an LVDS interface or an external memory interface might be driven by nonoptimal PLL output counters
Error (12002): Port "<port name>" does not exist in macrofunction "<pll instance name>" in a design containing an Altera PLL megafunction
Altera PLL v12.0: Entering output phase shift in degree units causes incorrect simulation
For designs that target Arria V and Cyclone V devices, unused GXB RX and GXB REFCLK pins should be connected directly to GND
Internal Error: Sub-system: ASMDB, File: /quartus/db/asmdb/asmdb_param.cpp, Line: 522 iter != m_enum_map-&gt
Internal Error: Sub-system: PGMIO, File: /quartus/pgm/pgmio/pgmio_devices.cpp, Line: 7667 Cannot locate the SFL sof file

For more information about known Quartus II software issues that affect the Arria V device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_av_ki

Cyclone V Known Issues

The following known issues affect designs that target the Cyclone V device family:

Issues That Affect Cyclone V Devices
Error (12002): Port "<port name>" does not exist in macrofunction "<pll instance name>" in a design containing an Altera PLL megafunction
Altera PLL v12.0: Entering output phase shift in degree units causes incorrect simulation
For designs that target Arria V and Cyclone V devices, unused GXB RX and GXB REFCLK pins should be connected directly to GND
Internal Error: Sub-system: ASMDB, File: /quartus/db/asmdb/asmdb_param.cpp, Line: 522 iter != m_enum_map-&gt

For more information about known Quartus II software issues that affect the Cyclone V device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_cv_ki

Stratix IV Known Issues

The following known issue affects designs that target the Stratix IV device family:

Issues That Affect Stratix IV Devices
Error (21216): Cannot enable error detection cyclic redundancy check without instantiating the ALTERA_CRCERROR_VERIFY megafunction.

For more information about known Quartus II software issues that affect the Stratix IV device family, look for information on the Knowledge Base page at the following URL:

http://www.altera.com/support/kdb/kdb-browse.jsp?keyword=q_ii_siv_ki

Stratix V Known Issues

The following known issues affect designs that target the Stratix V device family:

Issues That Affect Stratix V Devices
Setup and hold timing violations on the rx_clkout domain of a Deterministic Latency PHY megafunction
Incorrect .sof generated for Stratix V PMA Direct Channels
TimeQuest Timing Analyzer incorrectly reports Stratix V VCC

Issues That Affect Stratix V Devices
The TimeQuest Timing Analyzer might report timing violations for 10GBASE-R PHY and Interlaken PHY megafunctions
rx_use_coreclk parameter is not generated correctly for 10GBASE-R PHY v12.0 megafunctions that target the Stratix V device family
10 Gigabit Ethernet PCS megafunctions might fail timing
The clocks of an LVDS interface or an external memory interface might be driven by nonoptimal PLL output counters
ALTLVDS_RX and ALTLVDS_TX: incorrect load enable phase setting can cause failures in hardware
Error (12002): Port "<port name>" does not exist in macrofunction "<pll instance name>" in a design containing an Altera PLL megafunction
Altera PLL v12.0: Entering output phase shift in degree units causes incorrect simulation
Internal Error: Sub-system: ASMDB, File: /quartus/db/asmdb/asmdb_param.cpp, Line: 522 iter != m_enum_map-&gt
Parallel Flash Loader: Dual P30 and P33 flash programming is not available for Stratix V devices
Internal Error: Sub-system: PGMIO, File: /quartus/pgm/pgmio/pgmio_devices.cpp, Line: 7667 Cannot locate the SFL sof file
Functional simulation netlist generated for Stratix V devices contains an erroneous reference to an .sdo file

Error (21216): Cannot enable error detection cyclic redundancy check without instantiating the ALTERA_CRCERROR_VERIFY megafunction.

Description

The Error Detection CRC feature of Arria II GZ and Stratix IV devices requires instantiation of an Altera CRCERROR Verify v12.0 megafunction. However, the Altera CRCERROR Verify v12.0 megafunction is not available in the Quartus II software version 12.0. During compilation of a design that uses the Error Detection CRC feature, the Quartus II software reports one of the two following errors:

```
Error (21216): Cannot enable error detection cyclic redundancy check
without instantiating the ALTERA_CRCERROR_VERIFY megafunction
```

```
Error (21217): ALTERA_CRCERROR_VERIFY megafunction is not instantiated
for arriaiigz_crcblock primitive instance "crcblock_component"
```

Workaround

If you require the Error Detection CRC feature, contact Altera support.

Error: (vsim-3694) The implicit port connection (.*) did not find a matching port, net, variable or interface instance

Description

For designs that target Arria V ES devices, if your test bench uses System Verilog implicit port connections (.*), postlayout simulation netlist files fail during simulation in Mentor Graphics ModelSim with an error similar to the following:

```
Error: (vsim-3694) The implicit port connection (.*) did not find a
matching port, net, variable or interface instance
```

Workaround

For test benches that target Arria V ES postlayout simulation, replace implicit port connections (`.*`) with explicit port connections.

Arria V designs that include fractional PLL and CMU PLL cascading fail to simulate

Description

Designs that target an Arria V device and that include fractional PLL and CMU PLL cascading fail to simulate with the default Quartus II simulation model.

Workaround

On the **Reconfiguration** tab of the Custom PHY v12.0 MegaWizard Plug-In Manager, turn on **Allow PLL/CDR Reconfiguration**.

This option allows simulation to use an alternative simulation model that supports the fractional PLL and CMU PLL cascading feature.

Setup and hold timing violations on the rx_clkout domain of a Deterministic Latency PHY megafunction

Description

In designs that target Arria V or Stratix V devices, Deterministic Latency PHY megafunction instances may exhibit setup and hold timing violations in the `rx_clkout` domain.

Workaround

Make the following assignment in your Quartus II Settings File (**.qsf)**:

```
set_instance_assignment -name GLOBAL_SIGNAL "PERIPHERY CLOCK" -to
*pld8grxclkout
```

The Design Assistant generates spurious warnings for Arria V designs that include 10GBASE-R PHY v12.0 megafunctions

Description

For designs that target the Arria V device family and that contain a 10GBASE-R PHY v12.0 megafunction, if you run the Design Assistant after fitting, the Design Assistant generates the following four critical warnings:

- `Critical Warning (332012): Synopsys Design Constraints File file not found`
- `Critical Warning (308019): (Critical) Rule C101: Gated clock should be implemented according to the Altera standard scheme`
- `Critical Warning (308060): (High) Rule D101: Data bits are not synchronized when transferred between asynchronous clock domains`
- `Critical Warning (308067): (High) Rule D103: Data bits are not correctly synchronized when transferred between asynchronous clock domains`

These warnings pertain to timing analysis, which the Quartus II software version 12.0 does not support for Arria V devices.

Workaround

For compilation and functional simulation, you may safely ignore these warnings.

10 Gigabit Ethernet PCS megafunctions might fail timing

Description

Timing analysis of 10 Gigabit Ethernet Physical Coding Sublayer (PCS) megafunctions that target Arria V or Stratix V devices might result in timing violations between the megafunction instance and the core. These timing violations are caused by cross-clock domain transfers.

Workaround

Closing timing deterministically might not be possible. If your design requires cross-clock domain transfers and your design fails timing, insert synchronization registers or FIFO buffers. If your clock groups are asynchronous or mutually exclusive, in your Synopsys Design Constraints file (**.sdc**) cut these failing paths from the timing analysis.

The clocks of an LVDS interface or an external memory interface might be driven by nonoptimal PLL output counters

Description

For designs that target Arria V or Stratix V devices, the clocks of an LVDS interface or an external memory interface with a PLL in fractured mode might be driven by non-optimal PLL counters.

Workaround

Constrain the locations of the output counters with QSF assignments. `loaden` and `fclk` should use output counters `C0` to `C3` for `FPLL_0`, and `C14` to `C11` for `FPLL_1`. For example, to constrain the `fclk` use the following QSF assignment:

```
set_location_assignment PLLOUTPUTCOUNTER_X98_Y108_N1 -to
"rx:rx0|altlvds_rx:ALTLVDS_RX_component|rx_lvds_rx:auto_generated|pll_
fclk~PLL_OUTPUT_COUNTER"
```

Error (12002): Port "<port name>" does not exist in macrofunction "<pll instance name>" in a design containing an Altera PLL megafunction

Description

Regeneration of an Altera PLL megafunction that was generated in a previous version of the Quartus II software fails during compilation with the error:

```
Error (12002): Port "<port name>" does not exist in macrofunction "<pll instance name>"
```

Workaround

With the MegaWizard Plug-In Manager, configure and generate a new Altera PLL v12.0 megafunction that matches the configuration of your old megafunction.

Altera PLL v12.0: Entering output phase shift in degree units causes incorrect simulation

Description

By default, phase shifts in the Altera PLL v12.0 MegaWizard Plug-In Manager are specified in degree units. However, if you specify an output phase shift in degree units, the phase shift is not simulated correctly.

Workaround

To simulate the phase shift correctly, either specify the output phase shift in picoseconds or, in your **.vo** or **.vho** file include ps in your instantiation. For example, in the **.vo** or **.vho** file change

```
xxxxx.phase_shift0 = 5000
```

to

```
xxxxx.phase_shift0 = “5000 ps”
```

For designs that target Arria V and Cyclone V devices, unused GXB RX and GXB REFCLK pins should be connected directly to GND

Description

For Arria V and Cyclone V devices, the pin-out generated by the Quartus II software version 12.0 incorrectly indicates that unused `GXB RX` and `GXB REFCLK` pins should be connected to `GXB_GND*`.

Workaround

For Arria V and Cyclone V devices, connect unused `GXB RX` and `GXB REFCLK` pins directly to `GND`.

Internal Error: Sub-system: ASMDB, File: /quartus/db/asmdb/asmdb_param.cpp, Line: 522 iter != m_enum_map-&gt

Description

For designs that target an Arria V, Cyclone V, or Stratix V device, if you create an I/O node with and ECO change in the Chip Planner, a subsequent Check and Save All Netlist Changes operation fails with the error

```
Internal Error: Sub-system: ASMDB, File:
/quartus/db/asmdb/asmdb_param.cpp, Line: 522 iter != m_enum_map-&gt
```

Workaround

For affected device families, I/O node creation with ECOs is not supported by the Quartus II software version 12.0.

Internal Error: Sub-system: PGMIO, File: /quartus/pgm/pgmio/pgmio_devices.cpp, Line: 7667 Cannot locate the SFL sof file

Description

Attempting to program an Arria V or Stratix V device with JTAG Indirect Configuration File (**.jic**) might fail with an error similar to the following:

```
Internal Error: Sub-system: PGMIO, File: /quartus/pgm/pg-
mio/pgmio_devices.cpp, Line: 7667

Can not locate the SFL sof file
```

Workaround

Manually instantiate and compile a Serial Flash Loader (SFL) megafunction by following the instructions in *Instantiating SFL Megafunction in the Quartus II Software* in AN 370: Using the Serial FlashLoader with the Quartus II Software on the Altera website. Then program the device.

Incorrect .sof generated for Stratix V PMA Direct Channels

Description

The SRAM Object Files (**.sof**) generated by the Quartus II Assember are nonfunctional. One possible symptom is nonresponsive receiver channels.

Workaround

This issue will be corrected in a future release of the Quartus II software.

TimeQuest Timing Analyzer incorrectly reports Stratix V VCC

Description

For Stratix V C2 devices, the TimeQuest Timing Analyzer incorrectly reports VCC voltage as 850 mV.

Workaround

The correct VCC voltage for Stratix V C2 devices is 900 mV.

The TimeQuest Timing Analyzer might report timing violations for 10GBASE-R PHY and Interlaken PHY megafunctions

Description

The TimeQuest Timing Analyzer might report hold, setup, and minimum pulse width violations for designs that target a Stratix V device and that include a 10GBASE-R PHY or Interlaken PHY megafunction that was generated with a version of the Quartus II software prior to version 12.0.

Workaround

If your design contains a 10GBASE-R PHY or Interlaken PHY megafunction, regenerate the megafunction with the MegaWizard Plug-In Manager version 12.0 before performing compilation or timing analysis with the Quartus II software version 12.0.

rx_use_coreclk parameter is not generated correctly for 10GBASE-R PHY v12.0 megafunctions that target the Stratix V device family

Description

10GBASE-R PHY v12.0 megafunctions that target Stratix V devices do not generate `rx_use_coreclk` parameters correctly; the generated HDL file does not pass the `rx_use_coreclk` parameter to the sv_xcvr_10gbaser_nr instance.

Workaround

Update the generated HDL file to pass the parameter. For a file generated in System Verilog, add the line commented in the example below:

```
sv_xcvr_10gbaser_nr  #(
          .num_channels      (num_channels      ),
          .operation_mode    (operation_mode    ),
          .sys_clk_in_mhz        (mgmt_clk_in_mhz  ),
          .ref_clk_freq      (ref_clk_freq      ),
          .rx_use_coreclk    (rx_use_coreclk    ), //add this line
          .pll_type          (pll_type          ),
          .RX_LATADJ        (rx_latadj),
          .TX_LATADJ        (tx_latadj)
        )xv_xcvr_10gbaser_nr_inst(
```

ALTLVDS_RX and ALTLVDS_TX: incorrect load enable phase setting can cause failures in hardware

Description

For designs that target a Stratix V device, if an ALTLVDS_RX or ALTLVDS_TX megafunction is configured to use an external PLL, the Quartus II software does not analyze the load enable transfer from the PLL to the register that is captured by `fclk`.

Because this path is not analyzed, if you set the phase of load enable incorrectly the Quartus II software does not report a timing failure. An incorrect phase setting can cause a failure in hardware.

Workaround

To set the correct phase, follow the instructions in the *LVDS SERDES Transmitter / Receiver (ALTLVDS_TX and ALTLVDS_RX Megafunction User Guide*.

Parallel Flash Loader: Dual P30 and P33 flash programming is not available for Stratix V devices

Description

For Stratix V devices, Dual P30 and P33 flash programming with the Parallel Flash Loader megafunction is not available. If you attempt to program a Stratix V device with Dual P30 or P33 flash programming, the Quartus II Programmer does not issue an error; however, the FPGA is not programmed.

Workaround

To program a Stratix V device with Dual P30 or P33 flash programming, use the Quartus II Programmer version 11.1 SP2.

Functional simulation netlist generated for Stratix V devices contains an erroneous reference to an .sdo file

Description

Beginning with the Quartus II software version 12.0, for designs targeting Stratix V and later families, the EDA Netlist Writer generates a functional simulation netlist even when post-fit timing simulation netlist generation is enabled in EDA simulator tool settings.

In designs that target the Stratix V device family, the functional simulation netlist generated for post-fit timing simulation incorrectly includes an `$sdf_annotate` statement that refers to a nonexistent Standard Delay Format Output File (**.sdo**).

Functional simulation netlists generated for functional simulation are generated correctly.

Workaround

To generate a correct netlist file, modify EDA simulation tool settings to specify generating the netlist for functional simulation, and then run the EDA Netlist Writer.

Antivirus Verification

The Altera Complete Design Suite version 12.0 has been verified virus free using the following software:

AVG Version 2012.0.2169
Virus database version: 2425/1

McAfee VirusScan Enterprise + AntiSpyware Enterprise 8.7i (8.7.0.570)
Scan Engine Version: 5400.1158
DAT Version: 6699.0000

Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Quartus II software version 12.0:

Customer Service Request Numbers Resolved in the Quartus II Software Version 12.0							
10860052	10858417	10857991	10856857	10856479	10855939	10853279	10853226
10849976	10849860	10849261	10848765	10847775	10847631	10844013	10842920
10839512	10836350	10834814	10829266	10818297	10828429	10853189	10849839
10846344	10846902	10846077	10847660	10845195	10843954	10842761	10845935
10842070	10848587	10850509	10853902	10851343	10853088	10851504	10849734
10845908	10844890	10845491	10834076	10845198	10858474	10858470	10842939
10842560	10877182	10866581	10865184	10864762	10864025	10863760	10863402
10863291	10863221	10862374	10861859	10861524	10861367	10861327	10861181
10861156	10861130	10860713	10860370	10860255	10860240	10860086	10859847
10859422	10859402	10859366	10859307	10859161	10858939	10858897	10858765
10858656	10858416	10858378	10858238	10858006	10857997	10857994	10857895
10857813	10857592	10857580	10857552	10857523	10857508	10857348	10857346
10857342	10857228	10856921	10856857	10856718	10856713	10856529	10856464
10856453	10856374	10856362	10856349	10856268	10856248	10856205	10856166
10856093	10856053	10855988	10855985	10855833	10855751	10855747	10855719
10855585	10855558	10855549	10855450	10855409	10855372	10855365	10855364
10855217	10855204	10855187	10854951	10854763	10854666	10854523	10854505
10854456	10854378	10854293	10854291	10854257	10853877	10853838	10853774
10853762	10853756	10853739	10853716	10853658	10853629	10853522	10853384

Customer Service Request Numbers Resolved in the Quartus II Software Version 12.0							
10853357	1085333	110853322	10853252	10853203	10853164	10852827	10852738
10852642	10852392	10852249	10852243	10852240	10852221	10852187	10852184
10852166	10852154	10852044	10852001	10851991	10851972	10851943	10851935
10851907	10851885	10851860	10851832	10851790	10851758	10851555	10851548
10851504	10851487	10851469	10851367	10851366	10851284	10851221	10851136
10851076	10851067	10851034	10850951	10850796	10850754	10850676	10850599
10850551	10850407	10850284	10850279	10850205	10850195	10850186	10850163
10850076	10850047	10850022	10849976	10849970	10849876	10849813	10849725
10849660	10849643	10849623	10849594	10849514	10849474	10849465	10849288
10849248	10849241	10849087	10849056	10849051	10848969	10848954	10848912
10848902	10848838	10848743	10848732	10848689	10848652	10848639	10848618
10848483	10848481	10848456	10848428	10848349	10848323	10848178	10848144
10848098	10848094	10848072	10847953	10847876	10847712	10847660	10847652
10847598	10847498	10847408	10847355	10847267	10847238	10847216	10847180
10847090	10847085	10847071	10846956	10846908	10846869	10846838	10846692
10846688	10846618	10846561	10846546	10846531	10846528	10846527	10846489
10846434	10846405	10846392	10846338	10846287	10846180	10846173	10846124
10846066	10845962	10845957	10845789	10845720	10845680	10845654	10845621
10845393	10845385	10845354	10845215	10845094	10845035	10845026	10844883
10844528	10844418	10844380	10844217	10844008	10843993	10843761	10843760
10843526	10843285	10843224	10843204	10843138	10843036	10843001	10842996
10842919	10842881	10842854	10842794	10842645	10842588	10842553	10842486
10842395	10842257	10842207	10842195	10842169	10842150	10842053	10842050
10841956	10841940	10841888	10841860	10841716	10841713	10841677	10841666
10841605	10841168	10841004	10840830	10840808	10840637	10840551	10840521
10840442	10840418	10840390	10840258	10840202	10840170	10840046	10839899
10839840	10839801	10839704	10839672	10839396	10839149	10838768	10838722
10838339	10838307	10838265	10838213	10838121	10838062	10838039	10838025
10837387	10837119	10836946	10836917	10836607	10836527	10836484	10835715
10835394	10835247	10834979	10834967	10834103	10832503	10832297	10832290
10831499	10831319	10830504	10829148	10825620	10810620	10799101	—

Software Patches Included in this Release

The Quartus II software version 12.0 includes the following patches released for previous versions of the Quartus II software:

Quartus II Software Version	Patch	Customer Service Request Number
12.0cb	0.03c	10863931
12.0cb	0.03b	10859390
12.0cb	0.02c	—

Quartus II Software Version	Patch	Customer Service Request Number
12.0cb	0.02b	—
12.0cb	0.01c	—
12.0cb	0.01b	10858416
11.1sp2	2.ep29a	—
11.1sp2	2.ep28a	—
11.1sp2	2.dp8i	10852391
11.1sp2	2.dp8h	10861197
11.1sp2	2.dp8f	10857542
11.1sp2	2.dp8e	10846918
11.1sp2	2.dp8d	—
11.1sp2	2.dp8c	10858416
11.1sp2	2.dp8b	10854351
11.1sp2	2.dp8a	10855818
11.1sp2	2.dp8	—
11.1sp2	2.dp7	—
11.1sp2	2.dp6	—
11.1sp2	2.dp3	—
11.1sp2	2.36	10861045
11.1sp2	2.32	10854915
11.1sp2	2.31	10852791
11.1sp2	2.30	10855558
11.1sp2	2.29	10854103
11.1sp2	2.28	10854666
11.1sp2	2.23	10855311
11.1sp2	2.19	10847703
11.1sp2	2.18	10854666
11.1sp2	2.17	10836350
11.1sp2	2.16	10847660
11.1sp2	2.15	10847631
11.1sp2	2.13	10849165
11.1sp2	2.11	10848954
11.1sp2	2.09	10838026

Quartus II Software Version	Patch	Customer Service Request Number
11.1sp2	2.08	—
11.1sp2	2.06	10846030
11.1sp2	2.05	10842491
11.1sp2	2.03	10832496
11.1sp2	2.01	10845656
11.1sp1	1.23	10854257
11.1sp1	1.22	10857580
11.1sp1	1.21	10839149
11.1sp1	1.20	10842758
11.1sp1	1.18	—
11.1sp1	1.17	10847660
11.1sp1	1.16	10842645
11.1sp1	1.15	10845720
11.1sp1	1.14	10836527
11.1sp1	1.12	10832496
11.1sp1	1.10	10843036
11.1fb	0.01a	10823809
11.1	0.24	10849660
11.1	0.22	10834412
11.1	0.21	10841940
11.0sp2	2.03	10823750
11.0sp1	1.41	10844925
11.0sp1	1.32	10826945
11.0sp1	1.27	10831588
11.0sp1	1.19	10822963
11.0	0.47	10865502
11.0	0.45	10825620
11.0	0.43	10830504
11.0	0.32	10822963
11.0	0.16	10802682
10.1sp1	1.46	10806416
10.1sp1	1.105	10854232

Quartus II Software Version	Patch	Customer Service Request Number
10.1sp1	1.104	—
10.1sp1	1.103	10845895
10.0sp1	1.218	10845935
9.1sp2	2.130	10807251
9.1	0.99	10827075

Document Revision History

The following table shows the revision history for this document.

Document Revision History

Date	Version	Changes
June 2012	1.0	Initial release.