The Altera JESD204B IP core is a high-speed point-to-point serial interface intellectual property (IP). The JESD204B IP core has been hardware-tested with a number of selected JESD204B-compliant ADC (analog-to-digital converter) devices.

This report highlights the interoperability of the JESD204B IP core with the ADC12J4000 converter evaluation module (EVM) from Texas Instruments Inc. (TI). The following sections describe the hardware checkout methodology and test results.

Related Information
JESD204B IP Core User Guide

Hardware Requirements

The hardware checkout test requires the following hardware tools:

- Stratix V Advanced Systems Development Kit with 15 V power adaptor
- TI ADC12J4000 EVM with 5 V power adaptor
- Mini-USB cables

Hardware Setup

This test uses a Stratix V Advanced Systems Development Kit with the TI ADC12J4000 daughter card module installed on the development board’s FMC connector.
The ADC12J4000 EVM derives power from the 5 V power adaptor.

The 3.76 GHz ADC device clock is sourced from the LMX2581 frequency synthesizer on the ADC12J4000 EVM.

The LMX2581 supplies 1.88 GHz clock to the LMK04828 clock generator on the ADC12J4000 EVM. The LMK04828 divides the 1.88 GHz input clock and distribute the 235 MHz device clock to the FPGA through the FMC connector.

For subclass 1, the LMK04828 system clock generator generates SYSREF pulses for the JESD204B IP core in the FPGA as well as the ADC12J4000 device.
ADC12J4000 EVM Software Setup

The ADC12J4000 EVM software configures the ADC12J4000 device, LMX2581 frequency synthesizer and LMK04828 clock generator for JESD204B link operation. Setup files for each of the parameter configuration are included in the software installation.

You need to configure the ADC12J4000, LMX2581, and LMK04828 modules with the correct settings and sequence for the JESD204B link to operate at the targeted data rate and JESD204B link parameters. Follow these steps to set up the configuration via the ADC12J4000 EVM graphical user interface (GUI):

1. Configure the FPGA.
2. A number of changes are required in the default setup files of the ADC and LMK04828 devices. These are the setup files used for the various JESD204B modes:
   - LMF=124 mode uses LMK04828_DB16_DDR_P54_Fs_3500Msps.cfg & ADC12J4000_DB16_DDR_P54.cfg
   - LMF=222 mode uses LMK04828_DB8_DDR_P54_Fs_3500Msps.cfg & ADC12J4000_DB8_DDR_P54.cfg
   - LMF=422 mode uses LMK04828_DB4_DDR_P54_Fs_3500Msps.cfg & ADC12J4000_DB4_DDR_P54.cfg
3. Modify the setup files:
   For LMK04828,
0x113 0x11 //set the analog delay properties for the device clock
0x114 0x42 //set the FPGA device clock half step value
0x117 0x04 //set output format HSDS 10mA of the device clock
0x12E 0xF0 //set sysref active in normal mode

SYSREF divider value for various mode:

- For LMF=222,422 (K=32): 0x13A 0x00, 0x13B 0x80 //set the value of SYSREF output divider =128
- For LMF=124 (K=32,16): 0x13A 0x01, 0x13B 0x00 //set the value of SYSREF output divider = 256
- For LMF=222,422 (K=16): 0x13A 0x00, 0x13B 0x40 // set the value of SYSREF output divider = 64
- 0x140 0x00 //power on sysref pulse generator

Set the following programming sequence at the end of the LMK04828 default setup file:

0x143 0x11 //set SYNC_MUX to "Pin" as part of sysref/clock dividers initialize sequence
0x139 0x00 //set SYSREF_Mux to "Normal" as part of sysref/clock dividers initialize sequence
0x143 0x31 //toggle sync_pol bit
0x143 0x11 //toggle sync_pol bit
0x144 0xFF //disable syncing of all clock outputs
0x139 0x03 //continuous SYSREF mode

For ADC12J4000,

- 0x0030 0xF0 // SYSREF receiver and processor on, clear sysref detection, clear dirty capture, DC-coupled SYSREF & Device clock
- 0x0030 0xC0 // SYSREF receiver and processor on, DC-coupled SYSREF & Device clock
- 0x0201 0xFE // Scrambler on, KM1 = 31, DDR, JESD disabled
- 0x0202 0x85 // P54 PLL on, Single-ended SYNC, Long transport layer test mode
- 0x0201 0xFF // Scrambler on, KM1 = 31, DDR, JESD enabled

4. Save the setup files in these two locations:

- <EVM GUI installation folder>\Texas Instruments\ADC12J4000EVM GUI\Configuration Files
- <EVM GUI installation folder>\Texas Instruments\ADC12J4000EVM GUI v1.1\Configuration Files

5. In the User Inputs section of the ADC12J4000 EVM GUI,

a. At the #1. Clock Source drop-down list, select On-board option.
b. At the #2a. On-board Fs Selection drop-down list, select Fs = 3760 Msps.
c. At the #3. Decimation and Serial Data Mode drop-down list,

- Select Decimate-by-16; DDR; P54 for LMF=124 mode
- Select Decimate-by-8; DDR; P54 for LMF=222 mode
- Select Decimate-by-4; DDR; P54 for LMF=422 mode
d. Click the Program Clocks and ADC button.

The following figures shows the software setup GUI for LMF=422 configuration.
Figure 3: ADC12J4000 EVM Software Setup - EVM

ADC12J4000EVM GUI v1.3

1. User Inputs:
   - #1. Clock Source
     - On-board
   - #2. On-board Fs Selection
     - Fs = 3760 Mbps
   - #3. External Fs Selection
     - fs = 12.5 MHz
   - #4. Decimation and Serial Data Mode
     - Decimate-by-4, DDR, F54
   - Program Clocks and ADC

2. Temp Sensor:
   - ADC12J4000 Temp
     - degrees C
   - Ambient Temp
     - degrees C
   - Update Temperatures

START HERE!

This lab is used to control the EVM to program the clocks, basic mode of the ADC12J4000, and read the temperature. Once the EVM is programmed, the other tabs allow the user to configure the ADC12J4000.

1. User Inputs - How to program the EVM clocks and ADC12J4000:
   - #1. Clock Source - the DEVCPL to the ADC may be supplied by the on-board LM2581 or externally by the user. If the on-board clock is selected, choose the Fs at #2a. If the external clock is selected, enter the Fs at #3b.
   - #2a. On-board Fs Selection - The LM2581 will be programmed to provide any of the available sampling clock frequencies to the DEVCPL, as well as provide the clock for distribution via the LM2580 for the JESD204B clocks.
   - #2b. External Fs Selection - The user must provide the external Fs supplied in MHz. The LM2581 will be powered down; see the User Guide for details regarding external clocks requested.
   - #3. Decimation and Serial Data Mode - Choose the decimation mode and serial data mode for the ADC. More options will be added in the future.
   - #4. Program Clocks and ADC - once all modes have been selected, press this button to write selections to the LM2581, LM2580B, and ADC12J4000.

2. Temp Sensor - the temperature for the device and ambient (board) may be read.
Figure 4: ADC12J4000 EVM Software Setup - JESD204B / DDC
Hardware Checkout Methodology

The following section describes the test objectives, procedure, and the passing criteria. The test covers the following areas:

- Receiver data link layer
- Receiver transport layer
- Descrambling
- Deterministic latency (Subclass 1)

Receiver Data Link Layer

This test area covers the test cases for code group synchronization (CGS) and initial frame and lane synchronization.

On link start up, the receiver issues a synchronization request and the transmitter transmits /K/ (K28.5) characters. The SignalTap II Logic Analyzer tool monitors the receiver data link layer operation.
# Code Group Synchronization (CGS)

## Table 1: CGS Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| CGS. 1    | Check whether sync request is deasserted after correct reception of four successive /K/ characters. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
- `jesd204_rx_pcs_data[(L*32)-1:0]`  
- `jesd204_rx_pcs_data_valid[L-1:0]`  
- `jesd204_rx_pcs_kchar_data[(L*4)-1:0]`  
  The following signals in `<ip_variant_name>.v` are tapped:  
- `rx_dev_sync_n`  
- `jesd204_rx_int`  
  The rxlink_clk is used as the SignalTap II sampling clock.  
  Each lane is represented by a 32-bit data bus in the `jesd204_rx_pcs_data` signal. The 32-bit data bus for is divided into four octets. | • /K/ character or K28.5 (0xBC) is observed at each octet of the `jesd204_rx_pcs_data` bus.  
- The `jesd204_rx_pcs_data_valid` signal is asserted to indicate data from the PCS is valid.  
- The `jesd204_rx_pcs_kchar_data` signal is asserted whenever control characters like /K/, /R/, /Q/, or /A/ characters are observed.  
- The `rx_dev_sync_n` signal is deasserted after correct reception of at least four successive /K/ characters.  
- The `jesd204_rx_int` signal is deasserted if there is no error. |
| CGS. 2    | Check full CGS at the receiver after correct reception of another four 8B/10B characters. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
- `jesd204_rx_pcs_errdetect[(L*4)-1:0]`  
- `jesd204_rx_pcs_disperr[(L*4)-1:0]`  
  The following signal in `<ip_variant_name>.v` are tapped:  
- `jesd204_rx_int`  
  The rxlink_clk is used as the SignalTap II sampling clock. | The `jesd204_rx_pcs_errdetect`, `jesd204_rx_pcs_disperr`, and `jesd204_rx_int` signals should not be asserted during CGS phase. |

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(1) Indicates the number of lanes.
### Table 2: Initial Frame and Lane Synchronization Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILA.1</td>
<td>Check whether the initial frame synchronization state machine enters FS_DATA state upon receiving non /K/ characters.</td>
<td>The following signals in <code>&lt;ip_variant_name&gt;_inst_phy.v</code> are tapped:</td>
<td>• /R/ character or K28.0 (0x1C) is observed after the /K/ character at the jesd204_rx_pcs_data bus.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_rx_pcs_data[(L*32)-1:0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_rx_pcs_data_valid[1:0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_rx_pcs_kchar_data[(L*4)-1:0]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The following signals in <code>&lt;ip_variant_name&gt;.v</code> are tapped:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• rx_dev_sync_n</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• jesd204_rx_int</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The rxlink_clk is used as the SignalTap II sampling clock.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Each lane is represented by a 32-bit data bus in the jesd204_rx_pcs_data signal. The 32-bit data bus for is divided into four octets.</td>
<td></td>
</tr>
</tbody>
</table>

---

(2) L indicates the number of lanes.
### Receiver Transport Layer

To check the data integrity of the payload data stream through the RX JESD204B IP core and transport layer, the ADC is configured to output long transport layer test pattern. The ADC is also set to operate with the same configuration as set in the JESD204B IP core. The long transport layer test pattern (as

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<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| ILA.2     | Check the JESD204B configuration parameters from ADC in second multiframe. | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
- `jesd204_rx_pcs_data[(L*32)-1:0]`  
- `jesd204_rx_pcs_data_valid[L-1:0]`  

The following signal in `<ip_variant_name>_inst_phy.v` are tapped:  
- `jesd204_rx_int`

The rxlink_clk is used as the SignalTap II sampling clock.  
The system console accesses the following registers:  
- `ilas_octet0`  
- `ilas_octet1`  
- `ilas_octet2`  
- `ilas_octet3`  
The content of 14 configuration octets in the second multiframe is stored in these 32-bit registers (`ilas_octet0`, `ilas_octet1`, `ilas_octet2`, and `ilas_octet3`). | /R/ character is followed by /Q/ character or K28.4 (0x9C) at the beginning of second multiframe.  
The `jesd204_rx_int` signal is deasserted if there is no error.  
Octets 0–13 read from these registers match with the JESD204B parameters in each test setup. |
| ILA.3     | Check the lane alignment | The following signals in `<ip_variant_name>_inst_phy.v` are tapped:  
- `jesd204_rx_pcs_data[(L*32)-1:0]`  
- `jesd204_rx_pcs_data_valid[L-1:0]`  

The following signals in `<ip_variant_name>_v` are tapped:  
- `rx_somf[3:0]`  
- `dev_lane_aligned`  
- `jesd204_rx_int`

The rxlink_clk is used as the SignalTap II sampling clock. | The `dev_lane_aligned` signal is asserted upon the last /A/ character of the ILAS is received, which is followed by the first data octet.  
The `rx_somf` marks the start of multiframe in user data phase.  
The `jesd204_rx_int` signal is deasserted if there is no error. |
defined in the JESD204B specification section 5.1.6.3) is observed at the data output of the RX transport layer.

The SignalTap II Logic Analyzer tool monitors the operation of the RX transport layer.

Table 3: Long Transport Layer Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>TL.1</td>
<td>Check the transport layer mapping using long transport layer test pattern.</td>
<td>The following signals in altera_jesd204_transport_rx_top.sv are tapped: &lt;ul&gt;&lt;li&gt;jesd204_rx_data_valid&lt;/li&gt;&lt;li&gt;jesd204_rx_dataout[(M<em>N</em>FRAMECLK_DIV)-1:0] (3)&lt;/li&gt;&lt;/ul&gt; The jesd204_rx_int signal in jesd204b_ed.sv is tapped. The rxframe_clk is used as the SignalTap II sampling clock.</td>
<td>• The jesd204_rx_data_valid signal is asserted. • The long transport layer test pattern observed at jesd204_rx_dataout signal is correct • The jesd204_rx_int signal is deasserted.</td>
</tr>
</tbody>
</table>

Descrambling

The data integrity with descrambler turned on is checked at the RX transport layer. The SignalTap II Logic Analyzer tool monitors the operation of the RX transport layer.

Table 4: Descrambler Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCR.1</td>
<td>Check the functionality of the descrambler using long transport layer test pattern.</td>
<td>Enable scrambler at the ADC and descrambler at the RX JESD204B IP core. The signals that are tapped in this test case are similar to test case TL.1</td>
<td>• The jesd204_rx_data_valid signal is asserted. • The long transport layer test pattern observed at the jesd204_rx_dataout signal is correct • The jesd204_rx_int signal is deasserted.</td>
</tr>
</tbody>
</table>

(3) M is the number of converters per device. N is the number of conversion bits per converter. FRAMECLK_DIV is the divider ratio on the frame_clk signal.
Deterministic Latency (Subclass 1)

The LMK04828 system clock generator generates periodic SYSREF pulse for both the ADC12J4000 and JESD204B IP core. The SYSREF pulse restarts the LMF counter and realigns it to the LMFC boundary.

Figure 6: Deterministic Latency Measurement Timing Diagram

The JESD204B IP core and ADC are configured to operate in continuous SYSREF detection mode.

Table 5: Deterministic Latency Test Cases

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| DL.1      | Check the FPGA SYSREF continuous detection. | Check that the FPGA detects the first rising edge of SYSREF pulse and SYSREF period is correct.  
Read the status of csr_sysref_singledet (bit[2]) identifier in the syncn_sysref_ctrl register at address 0x54.  
Read the status of csr_sysref_lmfc_err (bit[1]) identifier in the rx_err0 register at address 0x60. | The value of sysref_singledet identifier should be zero.  
The value of csr_sysref_lmfc_err identifier should be zero. |
| DL.2      | Check the SYSREF capture. | Check that FPGA and ADC capture SYSREF correctly and restart the LMF counter for every reset and power cycle.  
Read the value of rbd_count (bit[10:3]) identifier in the rx_status0 register at address 0x80. | If the SYSREF is captured correctly and the LMF counter restarts, for every reset and power cycle, the rbd_count value should only vary by two integers due to the word alignment. |
### Test Case

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL.3</td>
<td>Check the latency from start of SYNC~ deassertion to the first user data output.</td>
<td>Check that the latency is fixed for every FPGA and ADC reset and power cycle. Record the number of link clocks count from the start of SYNC~ deassertion to the first user data output, which is the assertion of the jesd204_rx_link_valid signal. The deterministic latency measurement block has a counter to measure the link clock count.</td>
<td>Consistent latency from the start of SYNC~ deassertion to the assertion of the jesd204_rx_link_valid signal.</td>
</tr>
</tbody>
</table>

### JESD204B IP Core and ADC Configurations

The JESD204B IP core parameters (L, M and F) in this hardware checkout are natively supported by the ADC12J4000 device. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the ADC12J4000 operating conditions. The hardware checkout testing here implements the JESD204B IP core and ADC with the following parameter configuration.

#### Table 6: Parameter Configuration

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMF</td>
<td>124</td>
</tr>
<tr>
<td>HD</td>
<td>0</td>
</tr>
<tr>
<td>S</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>15</td>
</tr>
<tr>
<td>N’</td>
<td>16</td>
</tr>
<tr>
<td>CS</td>
<td>1</td>
</tr>
<tr>
<td>CF</td>
<td>0</td>
</tr>
<tr>
<td>Decimation Factors (4)</td>
<td>16</td>
</tr>
<tr>
<td>DDR (5)</td>
<td>1</td>
</tr>
</tbody>
</table>

(4) This is not a JESD204B IP core parameter. Refer to the ADC12J4000 datasheet for more details.

(5) Serial line rate. This is not a JESD204B IP core parameter. Refer to the ADC12J4000 datasheet for more details.
### Test Results

The following table contains the possible results and their definition.

**Table 7: Results Definition**

<table>
<thead>
<tr>
<th>Result</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>PASS</td>
<td>The Device Under Test (DUT) was observed to exhibit conformant behavior.</td>
</tr>
<tr>
<td>PASS with comments</td>
<td>The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.</td>
</tr>
<tr>
<td>FAIL</td>
<td>The DUT was observed to exhibit non-conformant behavior.</td>
</tr>
<tr>
<td>Warning</td>
<td>The DUT was observed to exhibit behavior that is not recommended.</td>
</tr>
<tr>
<td>Refer to comments</td>
<td>From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.</td>
</tr>
</tbody>
</table>

---

(6) Enable 5/4 PLL to increase the line rate by 1.25x. This is not a JESD204B IP core parameter. Refer to the ADC12J4000 datasheet for more details.

(7) The device clock is used to clock the transceiver.

(8) The frame clock and link clock is derived from the device clock using an internal PLL.
The following table shows the results for test cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, and SCR.1 with different values of L, M, F, K, SCR, sampling clock, and SYSREF frequencies.

Table 8: Test Results for Test Cases CGS.1, CGS.2, ILA.1, ILA.2, ILA.3, TL.1, and SCR.1

<table>
<thead>
<tr>
<th>Test</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>Subclass</th>
<th>SCR</th>
<th>K</th>
<th>Data Rate (Mbps)</th>
<th>Sampling Clock (MHz)</th>
<th>Link Clock (MHz)</th>
<th>Sysref Pulse Frequency (MHz)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>16</td>
<td>9400</td>
<td>235</td>
<td>235</td>
<td>7.34375</td>
<td>Pass</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>16</td>
<td>9400</td>
<td>235</td>
<td>235</td>
<td>7.34375</td>
<td>Pass</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>32</td>
<td>9400</td>
<td>235</td>
<td>235</td>
<td>7.34375</td>
<td>Pass</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>235</td>
<td>235</td>
<td>7.34375</td>
<td>Pass</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>16</td>
<td>9400</td>
<td>470</td>
<td>235</td>
<td>29.375</td>
<td>Pass</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>16</td>
<td>9400</td>
<td>470</td>
<td>235</td>
<td>29.375</td>
<td>Pass</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>32</td>
<td>9400</td>
<td>470</td>
<td>235</td>
<td>14.6875</td>
<td>Pass</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>470</td>
<td>235</td>
<td>14.6875</td>
<td>Pass</td>
</tr>
<tr>
<td>9</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>16</td>
<td>9400</td>
<td>940</td>
<td>235</td>
<td>29.375</td>
<td>Pass</td>
</tr>
<tr>
<td>10</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>16</td>
<td>9400</td>
<td>940</td>
<td>235</td>
<td>29.375</td>
<td>Pass</td>
</tr>
<tr>
<td>11</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>32</td>
<td>9400</td>
<td>940</td>
<td>235</td>
<td>14.6875</td>
<td>Pass</td>
</tr>
<tr>
<td>12</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>940</td>
<td>235</td>
<td>14.6875</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Table 9: Test Results For Deterministic Latency Test

<table>
<thead>
<tr>
<th>Test</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>Subclass</th>
<th>K</th>
<th>Data Rate (Mbps)</th>
<th>Sampling Clock (MHz)</th>
<th>Link Clock (MHz)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL.1</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>235</td>
<td>235</td>
<td>Pass</td>
</tr>
<tr>
<td>DL.2</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>235</td>
<td>235</td>
<td>Pass</td>
</tr>
<tr>
<td>DL.3</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>235</td>
<td>235</td>
<td>Pass with comments. Link clock observed = 191 with IP core csr_rbd_offset set to 0x04.</td>
</tr>
<tr>
<td>DL.1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>470</td>
<td>235</td>
<td>Pass</td>
</tr>
</tbody>
</table>
### Test Result Comments

In each test case, the RX JESD204B IP core successfully initialize from CGS phase, ILA phase, and until user data phase. The long transport layer test pattern (as defined in the JESD204B specification section 5.1.6.3) is observed at the data output of the RX transport layer.

In the deterministic measurement test case DL.3, the link clock count in the FPGA depends on the board layout. The link clock count may vary by only one link clock when you reset or power cycle the FPGA and ADC. The link clock variation in the deterministic latency measurement is caused by word alignment, where the control characters fall into the next cycle of the data some time after realignment. This makes the duration of ILAS phase longer by one link clock some time after a reset or power cycle.

### AN 733 Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tr>
<td>February 2015</td>
<td>2015.02.09</td>
<td>Initial release.</td>
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<th>M</th>
<th>F</th>
<th>Subclass</th>
<th>K</th>
<th>Data Rate (Mbps)</th>
<th>Sampling Clock (MHz)</th>
<th>Link Clock (MHz)</th>
<th>Result</th>
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<td>2</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>470</td>
<td>235</td>
<td>Pass</td>
</tr>
<tr>
<td>DL.3</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>470</td>
<td>235</td>
<td>Pass with comments. Link clock observed = 111 with IP core csr_rbd_offset set to 0x04.</td>
</tr>
<tr>
<td>DL.1</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>940</td>
<td>235</td>
<td>Pass</td>
</tr>
<tr>
<td>DL.2</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>940</td>
<td>235</td>
<td>Pass</td>
</tr>
<tr>
<td>DL.3</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>9400</td>
<td>940</td>
<td>235</td>
<td>Pass with comments. Link clock observed = 111 with IP core csr_rbd_offset set to 0x04.</td>
</tr>
</tbody>
</table>