1. MAX V Device Family Overview

The MAX® V family of low cost and low power CPLDs offer more density and I/Os per footprint versus other CPLDs. Ranging in density from 40 to 2,210 logic elements (LEs) (32 to 1,700 equivalent macrocells) and up to 271 I/Os, MAX V devices provide programmable solutions for applications such as I/O expansion, bus and protocol bridging, power monitoring and control, FPGA configuration, and analog IC interface.

MAX V devices feature on-chip flash storage, internal oscillator, and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirement.

This chapter contains the following sections:

- “Feature Summary” on page 1–1
- “Integrated Software Platform” on page 1–3
- “Device Pin-Outs” on page 1–3
- “Ordering Information” on page 1–4

Feature Summary

The following list summarizes the MAX V device family features:

- Low-cost, low-power, and non-volatile CPLD architecture
- Instant-on (0.5 ms or less) configuration time
- Standby current as low as 25 µA and fast power-down/reset operation
- Fast propagation delay and clock-to-output times
- Internal oscillator
- Emulated RSDS output support with a data rate of up to 200 Mbps
- Emulated LVDS output support with a data rate of up to 304 Mbps
- Four global clocks with two clocks available per logic array block (LAB)
- User flash memory block up to 8 Kbits for non-volatile storage with up to 1000 read/write cycles
- Single 1.8-V external supply for device core
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)
Feature Summary

- I/Os are fully compliant with the PCI-SIG® PCI Local Bus Specification, revision 2.2 for 3.3-V operation
- Hot-socket compliant
- Built-in JTAG BST circuitry compliant with IEEE Std. 1149.1-1990

Table 1–1 lists the MAX V family features.

<table>
<thead>
<tr>
<th>Table 1–1. MAX V Family Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature</td>
</tr>
<tr>
<td>LEs</td>
</tr>
<tr>
<td>Typical Equivalent Macrocells</td>
</tr>
<tr>
<td>User Flash Memory Size (bits)</td>
</tr>
<tr>
<td>Global Clocks</td>
</tr>
<tr>
<td>Internal Oscillator</td>
</tr>
<tr>
<td>Maximum User I/O pins</td>
</tr>
<tr>
<td>tPD1 (ns)</td>
</tr>
<tr>
<td>fCNT (MHz)</td>
</tr>
<tr>
<td>tSU (ns)</td>
</tr>
<tr>
<td>tCO (ns)</td>
</tr>
</tbody>
</table>

Notes to Table 1–1:

(1) tPD1 represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum global clock frequency, fCNT, is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

MAX V devices accept 1.8 V on their VCCINT pins. The 1.8-V VCCINT external supply powers the device core directly. MAX V devices operate internally at 1.8 V. The supported MultiVolt I/O interface voltage levels (VCCIO) are 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

MAX V devices are available in two speed grades: –4 and –5, with –4 being the fastest. For commercial applications, speed grades –C4 and –C5 are available. For industrial and automotive applications, speed grade –I5 and –A5 are available, respectively. These speed grades represent the overall relative performance, not any specific timing parameter.

For propagation delay timing numbers within each speed grade and density, refer to the DC and Switching Characteristics for MAX V Devices chapter.

MAX V devices are available in space-saving FineLine BGA (FBGA), Micro FineLine BGA (MBGA), plastic enhanced quad flat pack (EQFP), and thin quad flat pack (TQFP) packages (refer to Table 1–2 and Table 1–3). MAX V devices support vertical migration within the same package (for example, you can migrate between the 5M570Z, 5M1270Z, and 5M2210Z devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide...
the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–2. MAX V Packages and User I/O Pins *(Note 1)*

<table>
<thead>
<tr>
<th>Device</th>
<th>64-Pin MBGA</th>
<th>64-Pin EQFP</th>
<th>68-Pin MBGA</th>
<th>100-Pin TQFP</th>
<th>100-Pin MBGA</th>
<th>144-Pin TQFP</th>
<th>256-Pin FBGA</th>
<th>324-Pin FBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>5M40Z</td>
<td>30</td>
<td>54</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>5M80Z</td>
<td>30</td>
<td>54</td>
<td>52</td>
<td>79</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>5M160Z</td>
<td>—</td>
<td>54</td>
<td>52</td>
<td>79</td>
<td>79</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>5M240Z</td>
<td>—</td>
<td>—</td>
<td>52</td>
<td>79</td>
<td>79</td>
<td>114</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>5M570Z</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>74</td>
<td>74</td>
<td>114</td>
<td>159</td>
<td>—</td>
</tr>
<tr>
<td>5M1270Z</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>114</td>
<td>211</td>
<td>271</td>
</tr>
<tr>
<td>5M2210Z</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>203</td>
<td>271</td>
</tr>
</tbody>
</table>

*(Note to Table 1–2):*

1. Device packages under the same arrow sign have vertical migration capability.

Table 1–3. MAX V Package Sizes

<table>
<thead>
<tr>
<th>Package</th>
<th>64-Pin MBGA</th>
<th>64-Pin EQFP</th>
<th>68-Pin MBGA</th>
<th>100-Pin TQFP</th>
<th>100-Pin MBGA</th>
<th>144-Pin TQFP</th>
<th>256-Pin FBGA</th>
<th>324-Pin FBGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch (mm)</td>
<td>0.5</td>
<td>0.4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>20.25</td>
<td>81</td>
<td>25</td>
<td>256</td>
<td>36</td>
<td>484</td>
<td>289</td>
<td>361</td>
</tr>
<tr>
<td>Length × width (mm × mm)</td>
<td>4.5 × 4.5</td>
<td>9 × 9</td>
<td>5 × 5</td>
<td>16 × 16</td>
<td>6 × 6</td>
<td>22 × 22</td>
<td>17 × 17</td>
<td>19 × 19</td>
</tr>
</tbody>
</table>

Integrated Software Platform

The Quartus II software provides an integrated environment for HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and programming of MAX V devices.

For more information about the Quartus II software features, refer to the Quartus II Handbook.

You can debug your MAX V designs using In-System Sources and Probes Editor in the Quartus II software. This feature allows you to easily control any internal signal and provides you with a completely dynamic debugging environment.

For more information about the In-System Sources and Probes Editor, refer to the Design Debugging Using In-System Sources and Probes chapter of the Quartus II Handbook.

Device Pin-Outs

For more information, refer to the MAX V Device Pin-Out Files page.
Ordering Information

Figure 1–1 shows the ordering codes for MAX V devices.

Figure 1–1. MAX V Device Packaging Ordering Information

- **Package Type**
  - T: Thin quad flat pack (TQFP)
  - F: FineLine BGA (FBGA)
  - M: Micro FineLine BGA (MBGA)
  - E: Plastic Enhanced Quad Flat Pack (EQFP)

- **Speed Grade**
  - 4 or 5, with 4 being the fastest

- **Operating Temperature**
  - C: Commercial temperature (T J = 0° C to 85° C)
  - I: Industrial temperature (T J = -40° C to 100° C)
  - A: Automotive temperature (T J = -40° C to 125° C)

- **Device Type**
  - 40Z: 40 Logic Elements
  - 80Z: 80 Logic Elements
  - 160Z: 160 Logic Elements
  - 240Z: 240 Logic Elements
  - 570Z: 570 Logic Elements
  - 1270Z: 1,270 Logic Elements
  - 2210Z: 2,210 Logic Elements

- **Pin Count**
  - Number of pins for a particular package

- **Family Signature**
  - 5M: MAX V

- **Optional Suffix**
  - Indicates specific device options or shipment method
  - N: Lead-free packaging

Table 1–4 lists the revision history for this chapter.

Table 1–4. Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2011</td>
<td>1.2</td>
<td>Updated Figure 1–1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Updated Table 1–3.</td>
</tr>
<tr>
<td>January 2011</td>
<td>1.1</td>
<td>Updated “Feature Summary” section.</td>
</tr>
<tr>
<td>December 2010</td>
<td>1.0</td>
<td>Initial release.</td>
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