Differences in Logic Utilization between Quartus II & Synplify Report Files

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Altera Corporation
101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
https://mysupport.altera.com

Introduction

Logic and resource utilization is an important consideration when selecting a programmable logic device (PLD). Historically, designers have relied on logic utilization reports from synthesis tools for an idea of how much logic their design requires, or how big a device they need. Today's FPGA devices provide a wide variety of advanced features in addition to basic registers and look-up tables. Place-and-route tools such as Altera's Quartus® II software have advanced algorithms to take advantage of these FPGA features, as well as optimization techniques to both increase performance and reduce the amount of logic required for a given design. In addition, designs may contain black boxes, and functions that take advantage of specific device features. Due to these advances, place-and-route software is often the only source for accurate logic utilization reports.

This technical brief describes the differences between the Synplify® Resource Report (**.srr**) file from the Synplicity® Synplify synthesis software and the resource utilization information provided by Altera Quartus II place-and-route software and explains how to interpret the reports from each tool.

There are three main areas where the Quartus II and Synplify reports vary:

- Quartus II register and memory packing, including register-packing into logic elements (LEs), DSP blocks, and I/O elements (IOEs)
- Quartus II netlist optimizations
- Megafunctions and black boxes

Quartus II Register & Memory Packing

The Quartus II Fitter can pack device resources together to reduce device utilization. In many cases these packing optimizations can only be performed during place-and-route, so synthesis results can not predict the amount of logic required in the final device. Because of this, the report from the Synplify software alone should not be used to determine how many logic elements or memory blocks are required for a particular design. The following sections outline how registers can be packed into existing LEs, DSP blocks, or IOEs, and how memory blocks can be packed together.

Register Packing into Logic Elements

The Quartus II Compiler can pack registers and logic into the same LE to save device resources and reduce LE utilization. The **Auto Packed Registers** option in the Compiler automatically implements register packing for appropriate pairs of logic functions. A logic function can be implemented in the same LE as the register that it feeds even if it also feeds other LE. In addition, two unrelated functions can be implemented in the same LE in certain cases, such as a combinatorial logic function and a register with a single data input.

The **Auto Packed Registers** logic option is available when using many of the Altera FPGA device families. The default setting is "Normal" for Stratix™, Stratix GX™, and Cyclone™ devices. Setting the logic option to "Minimize Area" maximizes register packing for an even smaller design implementation.

LE register packing often reduces the LE utilization as compared to the original synthesis netlist. Synthesis software is unable to perform or predict register packing because packing is dependent on device placement and routing.

Register-Packing into DSP Blocks

The DSP blocks available in some Altera FPGA device families have high-speed parallel processing capabilities optimized for DSP applications. These DSP blocks contain multiplication, adder, and accumulator logic as well as input, output, and pipeline registers.

If the design contains a multiplier (`lpm_mult`), multiply-adder (`altmult_add`) or multiply-accumulator (`altmult_accum`) megafunction, or the Synplify software has inferred such a function from the HDL code, the logic will be placed in a DSP block where possible. The Quartus II Compiler may be able to pack additional registers from the Synplify netlist into the registers in the DSP block. As is the case with LE register packing, this packing is controlled by the **Auto Packed Registers** logic option. When registers are packed into DSP blocks, the reported logic usage from the Synplify software may be too high because it counts an LE for each of these registers that are instead implemented in an existing DSP block by the Quartus II software.

Register-Packing into I/O Elements

IOEs consist of a single register or group of registers existing next to an I/O pin in a device. IOEs can help maximize I/O timing performance by permitting fast setup or clock-to-out times between the pin and the register.

The **Optimize I/O cell register placement for timing** Quartus II Compiler setting is turned on by default for some device families. This option directs the Fitter to try to implement registers in IOEs (rather than regular LEs) to meet timing requirements that relate to I/O pins (e.g. t_{SU} and t_{CO}). Where this post-synthesis optimization is being used, the logic estimation from the Synplify software may be incorrect because it counts an LE for each of these registers that are instead implemented in an IOE by the Quartus II software.

Memory Packing

In some cases, the Quartus II software can automatically pack two independent memories into one device memory block if the device is running out of memory. For example, the Quartus II Fitter can pack two single-port logical memories into one dual-port physical RAM block in Stratix devices (either M4K or M-RAM blocks) if the original design uses too much memory for the device. Two logical memories can also be packed into one ESB in APEX II devices. When this memory packing is performed, the overall memory usage for the design as reported by the Quartus II software may be less than reported by your synthesis tool.

Quartus II Netlist Optimizations

The Quartus II software includes netlist optimization options to further optimize your design after synthesis and before place-and-route. These options, turned off by default, can be applied regardless of the synthesis tool used. When turned on, these options often change both the logic utilization and the performance of the design. Depending on your design, some options may have more effect than others.

Netlist optimization features can restructure the data from the Verilog Quartus Mapping (**.vqm**) file (generated by the Synplify software) to optimize for placement and routing. Some of these features use timing information only available after place-and-route, so there is no way to predict the results during synthesis. Some features may decrease logic utilization, and some features may increase total logic utilization to improve the design's performance. The results depend on the original coding of the design, as well as whether the Quartus II project is set to optimize for area or speed.

When using advanced netlist optimization options in the Quartus II software, expect the logic utilization reports from the Synplify software to be inaccurate. The Quartus II netlist optimization features will generally change the logic utilization that comes out of synthesis, so you need to refer to the Quartus II report to determine how much logic was actually used during the compilation.

Megafunctions & Black Boxes

When you use megafunctions or black boxes in your design, the logic utilization reports in the Synplify software may be incorrect because there is incomplete information about the function. This section describes how these functions can affect the Synplify logic utilization report.

Altera provides parameterizable megafunctions that are optimized for Altera device architectures. Megafunctions include the library of parameterized modules (LPM), device-specific embedded megafunctions, intellectual property (IP) available as Altera MegaCore® functions, as well as from Altera Megafunction Partners Program (AMPP) partners. Using megafunctions instead of coding your own logic can save valuable design time. Because these functions are optimized for Altera devices, they can offer more efficient logic synthesis and device implementation. In addition, you need to use megafunctions to access some Altera device-specific features, such as memory, DSP blocks, LVDS drivers, phase-locked loops (PLLs), and double data rate I/O (DDRIO) circuitry.

You can instantiate Altera megafunctions in your HDL design by using the Quartus II MegaWizard Plug-In Manager to parameterize the function and create a wrapper file or by instantiating the function using the port and parameter definition. The Synplify software can also automatically recognize certain types of HDL code and infer the appropriate Altera megafunction. When this inference occurs, the software uses the megafunction code when compiling your design even though you did not specifically instantiate the megafunction. These situations can be reported by the Synplify software in different ways.

When a megafunction wrapper file is instantiated in a design, the function will be treated as a “black box” by the Synplify software because it has no information about the logic inside the function. The Synplify report will indicate that a black box has been used but will not provide any utilization information. If a megafunction is instantiated directly or inferred by the software, there is information for some megafunctions that the Synplify compiler can use to report utilization. Some megafunctions offer an “Auto” option to use dedicated circuitry within the Altera device. In these cases the decision whether to use dedicated circuitry or to use LEs is made during place-and-route, so the synthesis report can not include the appropriate utilization. In many cases you need to use attributes to specify what logic will be utilized in black boxes so that it can be counted in the Synplify report.

There are other situations where the Synplify software may encounter different kinds of black boxes, such as if you are re-using some code from an older design that has already been synthesized. In these cases the synthesis software has no information about the logic required to implement that logic and can not report any utilization unless you have specified the information.

When logic is black-boxed in a design, such as when an Altera megafunction is used, the Synplify report does not contain accurate information about the function unless the logic utilization is specified using attributes or other information within the software. To check the logic utilization of a logic block that is black-boxed in your Synplify design, refer to the results from the Quartus II software after place-and-route has taken place.

Comparing the Synplify & Quartus II Report Files

As discussed in the previous sections, the Synplify report file contains post-synthesis device utilization information, which estimates the amount of logic that will be used in the final design. This section shows where the relevant information is found in the Synplify report file, and how you can compare the information to the final Quartus II report.

The sample design used in the following sections generates different logic utilization results in the Synplify and Quartus II Report Files. Table 1 shows a summary of the results; details are provided in the sections below. You can see how the LE results vary between the Synplify and Quartus II tools, and how options in the Quartus II software can make a big difference in the results for logic elements. The Synplify results do not include any memory utilization because all the memory was instantiated as black boxes in this design.

Table 1. Summary of Results from Synplify and Quartus II Report Files for Sample Design *Note (1)*

	Logic Elements	Memory Bits	M-RAM blocks	M4K Blocks	M512 Blocks	Black Boxes (Logic utilization not included)
Resource Availability in Target Device (EP1S25F1020C5 shown)	25,660	1,944,976	2	138	224	N/A
Synplify Resource Report (SRR) file	25,250	N/A	0	0	0	34
Quartus II Post-Synthesis Report (Includes megafunction black boxes)	27,321	200,704	N/A	N/A	N/A	0
Quartus II Compilation Report ("Auto Packed Registers" logic option set to Normal)	24,368	200,704	0	49	5	0
Quartus II Compilation Report ("Auto Packed Registers" logic option set to Minimize Area)	20,948	200,704	0	49	5	0
Quartus II Compilation Report ("Auto Packed Registers" set to Minimize Area, WYSIWYG primitive resynthesis turned on)	19,866	200,704	0	49	5	0

Note to Table 1:
(1) These results reflect a sample design. Results for different Quartus II software options may vary from design to design.

Synplify Resource Report for Sample Design

Figure 1 shows an excerpt from a Synplify resource report (**.srr**) file for a sample design. This device usage section as shown in the excerpt can be found near the end of the SRR file generated during compilation in the Synplify software.

Figure 1. Logic Utilization Excerpt from Synplify SRR Report File

```
Design view:work.sample_design(verilog)
Selecting part EP1S25F1020C5
@N| The following device usage report estimates place and route data...

I/O ATOMs:       419

Total LUTs:  19032 of 25660 (74%)
Logic resources:  25250 ATOMs of 25660 (98%)
ATOM count by mode:
  normal:       21064
  arithmetic:   4186

DSP Blocks:     0  (0 nine-bit DSP elements).
M-RAMs:         0  (0% of 2)
M4Ks:           0  (0% of 138)
M512s:          0  (0% of 224)

LPM latches:    104
Black-boxes:    34
```

The SRR file reports LE utilization in terms of the ATOMs that are written into the VQM netlist file, along with information for the number of look-up tables (LUTs) and details for other architectural features. An explanation of the information relevant to logic utilization is included below.

In this example, the Synplify file gives an accurate report of the 419 I/O pins in the device:

```
I/O ATOMs:       419
```

The Total LUTs entry in the report indicates the number of combinatorial lookup tables written into the VQM netlist file during synthesis. These LUTs are reported separately but are included in the total number of logic ATOMs that are reported on the next line of the report, in this case, 25,250 LEs. It is important to note that these reports do not include any of the Quartus II packing or netlist optimization features, and do not include any LEs that are implemented from black boxes.

```
Logic resources: 25250 ATOMs of 25660 (98%)
```

The number of DSP block 9-bit elements and different types of Stratix memory are also reported based on megafunctions that are inferred in the Synplify software. Note that no DSP or memory features are reported for this design, and these numbers do not include any black boxes used in the design.

```
DSP Blocks:     0   (0 nine-bit DSP elements).
M-RAMs:         0   (0% of 2)
M4Ks:           0   (0% of 138)
M512s:          0   (0% of 224)

LPM latches:    104
```

The report also indicates the total number of black boxes: 34 in this design. The Synplify software does not report the number of LEs, DSP blocks, or RAM blocks included in the black boxes.

```
Black-boxes:    34
```

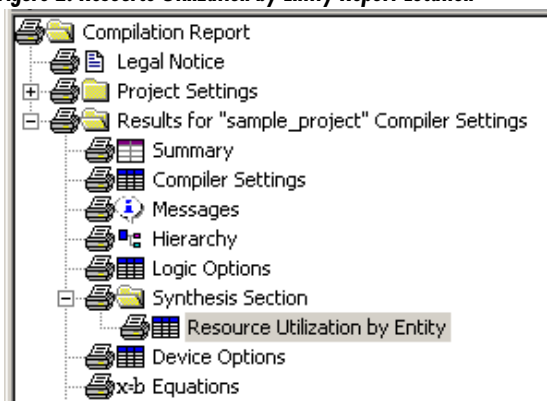
You can use the above entries in the SRR file to check the amount of logic resources used by the Synplify Software when creating the VQM netlist. However, refer to the Quartus II reports shown in the following sections to check the final utilization results for your design.

Quartus II Post-Synthesis Logic Report for Sample Design

When compiling this design in the Quartus II software with the default settings, the results are different from the Synplify post-synthesis report. In the Quartus II post-synthesis report, the black-boxed megafunctions are incorporated into the design, information that is unavailable during Synplify synthesis. The Quartus II software first reports total resource utilization after the Synplify-generated VQM netlist file and all the required Quartus II megafunction files are processed by the software. This report does not include any reductions resulting from Quartus II register or memory packing because packing occurs in the fitter, later in the compilation process. If you use any netlist optimization features, the post-synthesis report may look different because those features do change the "synthesis" stage of the compilation process.

The Quartus II post-synthesis results are indicated in the Resource Utilization by Entity report in the Synthesis Section of the Compilation Report, as shown in Figure 2. You can also get this information from the Compiler Settings File report (**.csf.rpt**) generated by the Quartus II software.

Figure 2. Resource Utilization by Entity Report Location



As shown in the resource utilization report in Figure 3, after the Quartus II software processes VQM file and all the required megafunction libraries, the number of LEs (or logic cells) has increased to 27,321. The report provides the total number of registers in the design, as well as the number of LEs currently using registers only, LUTs only, or both. The Quartus II software also shows the memory usage, the Synplify software does not report any black-boxed memory used in the design.

Figure 3. Resource Utilization by Entity Report *Note (1)*

Resource Utilization by Entity

	Logic Cells	Registers	Memory Bits	DSP Elements	LUT-Only LCs	Register-Only LCs	LUT/Register LCs
1	27321 (112)	16039	200704	0	11282 (112)	6785	9254

Note: to Figure 3

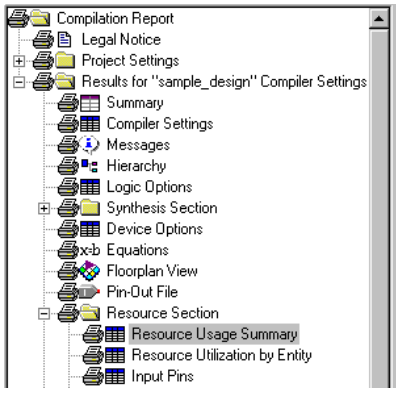
(1) Note that you may need to rearrange the columns in your Quartus II user interface to see the order of columns displayed in the figure.

Once the megafunction black boxes have been accounted for, the LE total of 27,321 would not fit in the target Stratix device which has 25,660 LEs available. Relying on the Synplify report file was not accurate in this case because of the black boxes in the design. See the next section for the results of Quartus II optimizations on the design to make it fit into the target device.

Quartus II Final Logic Report

You can find a summary of the final post-place-and-route results in the Resource Usage Summary section of the Quartus II Compilation Report, as shown in Figure 4. This report includes the results from the register and memory packing performed in the software with the **Auto Packed Registers** logic option set to “normal”.

Figure 4. Quartus II Compilation Report Summary



Resource Usage Summary

	Resource	Usage
1	Logic cells	24,368 / 25,660 (94 %)
2	Registers	16,039 / 27,778 (57 %)
3	User inserted logic cells	0
4	I/O pins	419 / 706 (59 %)
5	Clock pins	6
6	Dedicated input pins	0
7	Global signals	6
8	M512s	5 / 224 (2 %)
9	M4Ks	49 / 138 (35 %)
10	M-RAMs	0 / 2 (0 %)
11	Total memory bits	200,704 / 1,944,576 (10 %)
12	Total RAM block bits	228,672 / 1,944,576 (11 %)
13	DSP block 9-bit elements	0 / 80 (0 %)
14	PLLs	0 / 6 (0 %)

In the Resource Usage Summary you can see that 24,368 LEs are used to implement this design, along with 200,704 memory bits implemented as 5 M512 memory blocks and 49 M4K memory blocks. Register packing is able to reduce LE utilization from 27,321 to 24,368 allowing the design to fit in the target device. Compiling the design with the Auto Packed Register logic option set to "Minimize Area" further reduces the logic element utilization to 20,948 LEs.

Compiling with the Netlist Optimization feature called "Perform WYSIWYG primitive resynthesis" enabled (along with the Auto Packed Register settings described above) further reduces the LE count to 19,866. This feature allows the Quartus II Compiler to partially resynthesize the Synplify netlist to reduce the number of registers from 16,039 to 14,814. Reductions such as this are often due to Quartus II software optimizations of functions that were only recognized as black boxes in the Synplify software.

Conclusion

The Synplify report file provides a report of logic utilization after synthesis. However, synthesis tools can not accurately predict the final device utilization because this information is only available after place-and-route in the Quartus II software. The Quartus II software place-and-route process can reduce your logic utilization by performing register-packing into LEs, DSP blocks, and IOEs, as well as through automatic memory-packing. Quartus II advanced netlist optimizations can also alter the logic used in a design, and megafunctions or black boxes may not be counted at all in your synthesis utilization report.

If resource utilization is an important consideration, do not use the synthesis report provided by the Synplify software to make any decisions regarding your design. Consult the compilation report generated by the Quartus II software for accurate resource utilization statistics.

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