MegaCore IP Library Release Notes and Errata

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Contents

Chapter 7. DDR and DDR2 SDRAM High-Performance Controller

Chapter 8. DDR3 SDRAM High-Performance Controller

Chapter 17. POS-PHY Level 2 and 3 Compiler

Chapter 18. POS-PHY Level 4

Chapter 19. RapidIO

About These Release Notes

These release notes cover versions 8.1 through 9.1 SP2 of the Altera® MegaCore® IP Library. The chapters in these release notes describe the revision history and errata for each product in the MegaCore IP Library.

From v8.0 onwards, this document replaces all individual IP product release notes and errata sheets that Altera previously published.

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

The product errata tables use the following indicators:

- A checkmark "✓" indicates an issue is applicable to that version
- "Fixed" indicates the issue was fixed in that version
- A dash "—" indicates the issue is not applicable to that version

For the most up-to-date errata for this release, refer to the latest version of the *MegaCore IP Library Release Notes* on the Altera website.

For more information about Quartus® II issues, refer to the *Quartus II Software Release Notes*.

These release notes use the following Altera trademarks:

- Arria® devices
- Avalon® interface
- Cyclone® devices
- HardCopy® devices
- MegaCore function
- MegaWizard™ Plug-In
- ModelSim® simulator
- Nios® II processor
- Quartus II software
- SignalTap® II logic analyzer
- Stratix® devices

System Requirements

The MegaCore IP Library is distributed with the Quartus II software and downloadable from the Altera website, www.altera.com.

For system requirements and installation instructions, refer to *Altera Software Installation and Licensing*.

Update Status

The following table shows the chapter update status for these release notes.

Chapter	Date
1. 8B10B Encoder/Decoder	15 November 09
2. ASI	15 November 09
3. CIC	15 May 2010
4. CPRI	1 April 2010
5. CRC Compiler	15 November 09
6. DDR and DDR2 SDRAM Controller Compiler	15 November 09
7. DDR and DDR2 SDRAM High-Performance Controller	15 May 2010
8. DDR3 SDRAM High-Performance Controller	15 May 2010
9. FFT	15 November 2009
10. FIR Compiler	15 May 2010
11. FIR Compiler II	15 February 2010
12. HyperTransport	15 November 2009
13. NCO	15 November 2009
14. Nios II Processor	15 May 2010
15. PCI Compiler	1 April 2010
16. PCI Express Compiler	1 April 2010
17. POS-PHY Level 2 and 3 Compiler	15 November 2009
18. POS-PHY Level 4	15 November 2009
19. RapidIO	1 April 2010
20. QDRII SRAM	15 November 09
21. QDR II and QDR II+ SRAM Controller with UniPHY	15 November 09
22. Reed-Solomon Compiler	15 November 2009
23. RLDRAM II	15 November 09
24. RLDRAM II Controller with UniPHY	15 November 09
25. SDI	1 April 2010
26. SerialLite II	15 November 09
27. Triple Speed Ethernet	15 February 2010
28. UTOPIA Level 2 Master	15 November 2009
29. UTOPIA Level 2 Slave	15 November 2009
30. Video and Image Processing Suite	15 November 2009
31. Viterbi Compiler	15 November 2009

1. 8B10B Encoder/Decoder

Revision History

Table 1–1 shows the revision history for the 8B10B Encoder/Decoder MegaCore function.

For more information about the new features, refer to the *8B10B Encoder/Decoder MegaCore Function User Guide*.

Table 1–1. 8B10B Encoder/Decoder MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX device family.
8.1	November 2008	Maintenance release.

Errata

No known issues in v9.1, 9.0, and 8.1.

Revision History

Table 2–1 shows the revision history for the ASI MegaCore function.

For more information about the new features, refer to the *ASI MegaCore Function User Guide*.

Table 2–1. ASI MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV (soft SERDES) devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Maintenance release.

Errata

Table 2–2 shows the issues that affect the ASI MegaCore function v9.1, v9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the ASI MegaCore function.

Table 2–2. ASI MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Jul 09	Incorrect User Guide on ACDS	—	Fixed	✓	—	—
01 Dec 06	NativeLink Does Not Support Gate-Level Simulation	✓	✓	✓	✓	✓

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *ASI MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the ASI MegaCore function.

NativeLink Does Not Support Gate-Level Simulation

When using the NativeLink simulation example, the gate-level simulation design fails.

Affected Configurations

This issue affects all simulators supported by NativeLink.

Design Impact

This issue only affects simulation and does not affect the design compilation.

Workaround

Perform an RTL simulation of the NativeLink simulation example.

Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.

Revision History

Table 3–1 shows the revision history for the CIC MegaCore function.

For information about the new features, refer to the *CIC MegaCore Function User Guide*.

Table 3–1. CIC MegaCore Function Revision History

Version	Date	Description
9.1 SP2	March 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ Preliminary support for Arria II GX. ■ Added an option to optimize for speed.
8.1	November 2008	■ Full support for Stratix III. ■ Withdrawn support for UNIX.

Errata

Table 3–2 shows the issues that affect the CIC MegaCore function v9.1 SP2, v9.1 SP1, v9.1, v9.0, and v8.1.

Table 3–2. CIC MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		9.1 SP2	9.1 SP1	9.1	9.0	8.1
1 Apr 10	OpenCore Plus Feature Not Supported for Cyclone IV E and Cyclone IV GX Devices	Fixed	✓	—	—	—
15 Mar 09	Error Generating HDL for Decimator with More Than 9 Stages and 11 Interfaces	✓	✓	✓	✓	✓

OpenCore Plus Feature Not Supported for Cyclone IV E and Cyclone IV GX Devices

When uing the OpenCore Plus evaluation feature, the CIC MegaCore function does not generate a functional simulation model for Cyclone IV E and Cyclone IV GX devices.

Affected Configurations

All CIC variations that target a Cyclone IV E device or a Cyclone IV GX device.

Design Impact

This issue has no design impact.

Workaround

To avoid this issue, purchase a license for the CIC MegaCore function.

Solution Status

This issue is fixed in version 9.1 SP2 of the CIC MegaCore function.

Error Generating HDL for Decimator with More Than 9 Stages and 11 Interfaces

An error is issued when you generate HDL after selecting a **Decimator** filter with **Number of Stages** set to more than **9** and **Number of Interface** to more than **11**.

Affected Configurations

Decimator filters with more than 9 stages and more than 11 interfaces.

Design Impact

An error is issued when you generate HDL.

Workaround

If you want more than 9 stages you must select 11 interfaces or fewer. If you want more than 11 interfaces you must choose 9 stages or fewer.

Solution Status

This issue will be fixed in a future version of the CIC MegaCore function.

Revision History

Table 4–1 shows the revision history for the CPRI MegaCore function.

For information about the new features, refer to the *CPRI MegaCore Function User Guide*.

Table 4–1. CPRI MegaCore Function Revision History

Version	Date	Description
9.1 SP2	March 2010	Maintenance release.
9.1 SP1	February 2010	Initial release.

Errata

Table 4–2 shows the issues that affect the CPRI MegaCore function v9.1 SP2. Issues that affect v9.1 SP1 are available in a **readme.txt** file that accompanies the CPRI MegaCore function v9.1 SP1 patch.

Not all issues affect all versions of the CPRI MegaCore function.

Table 4–2. CPRI MegaCore Function Errata

Added or Updated	Issue	Affected Version
		9.1 SP2
01 Apr 10	CPRI Frame Synchronization Machine Unable to Return to XACQ1 from XSYNC1	✓
	Warning Messages from Transceiver During IPFS Model Generation	✓
	MII Interface Description in User Guide Contains Errors	✓
	CPRI MegaCore Function User Guide Unavailable From MegaWizard Interface Info Link	✓
	CPRI MegaCore Function Does Not Support HardCopy IV GX Devices	✓
	MegaWizard Plug-In Manager Does Not Recognize Transceiver Instances	✓
	Setup Time Violations Might Occur in Arria II GX 3072 Mbps Designs	✓
	CPRI MegaCore Function User Guide Does Not Contain Complete Instructions for Running Simulation Testbench	✓

CPRI Frame Synchronization Machine Unable to Return to XACQ1 from XSYNC1

If the CPRI frame synchronization machine is in the XSYNC1 state and does not receive the K28.5 byte, the frame synchronization machine remains in state XSYNC1 instead of moving to state XACQ1 as it should.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

While the core is in the XSYNC1 state, the frame synchronization logic locks up until a K28.5 byte is detected.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

Warning Messages from Transceiver During IPFS Model Generation

While the MegaWizard Plug-In Manager is generating a functional simulation model for the CPRI MegaCore function, several warning messages related to the transceiver are displayed. These messages can be ignored.

Affected Configurations

This Quartus II software issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact. These messages can be safely ignored.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

MII Interface Description in User Guide Contains Errors

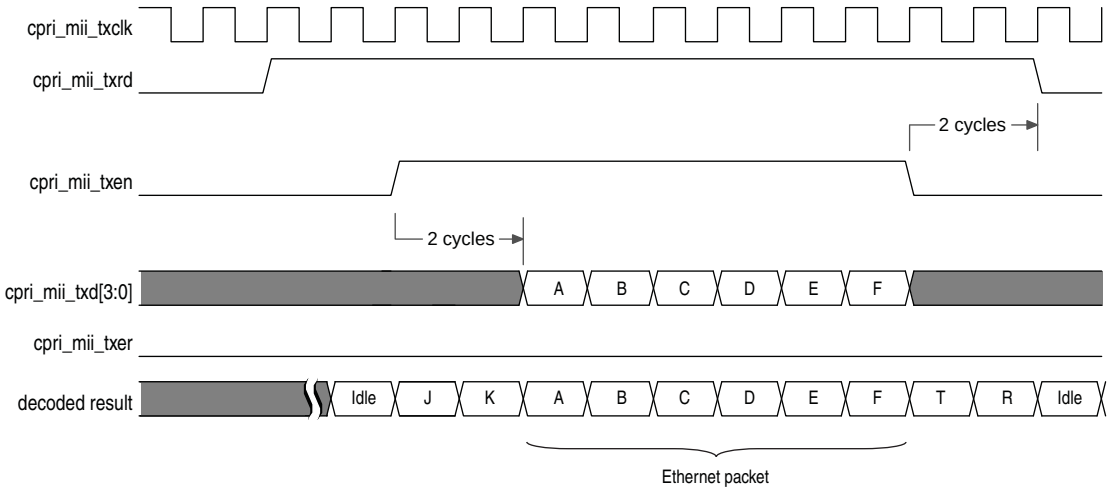
The CPRI MegaCore Function User Guide contains erroneous information about the MII interface. Figure 4-16 and Figure 4-17 in the CPRI MegaCore Function User Guide should be replaced with the figures in this erratum.

In contrast to the description in the CPRI MegaCore Function User Guide, the CPRI MII Interface transmitter inserts start-of-frame only after `cpri_mii_txen` is asserted. During the first two cycles in which `cpri_mii_txen` is asserted, the CPRI MII Interface transmitter inserts the J and K symbols in the buffer of data to be transmitted to the CPRI link, and ignores incoming data on `cpri_mii_txd`.

Typically, the external Ethernet block asserts `cpri_mii_txen` one clock cycle after `cpri_mii_txrd` is asserted. If not, in each clock cycle following that first cycle, while `cpri_mii_txrd` remains asserted but `cpri_mii_txen` is not yet asserted, the CPRI MII Interface transmitter inserts an Idle cycle in the buffer of data to be transmitted to the CPRI link. After `cpri_mii_txen` is asserted following the assertion of `cpri_mii_txrd`, if `cpri_mii_txen` is subsequently deasserted following a cycle in which `cpri_mii_txrd` remains asserted, the CPRI MII Interface transmitter assumes the external Ethernet block has reached end-of-frame, and begins insertion of the T and R nibbles.

Replace Figure 4-16 on page 56 of the CPRI MegaCore Function User Guide with the following Figure 4–1.

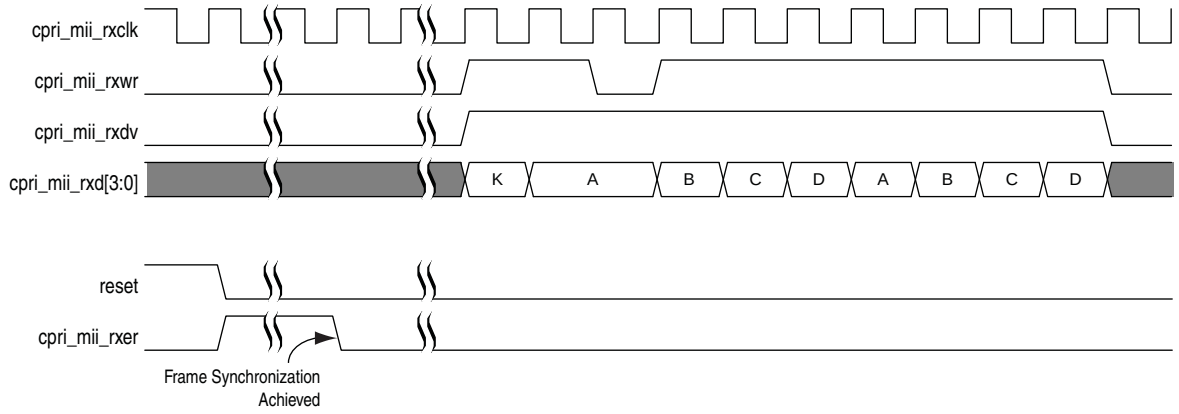
Figure 4–1. Corrected CPRI MII Interface Transmitter Example



Although Figure 4–1 shows `cpri_mii_txrd` asserted continuously during transmission of an Ethernet packet on `cpri_mii_txd`, this is not always the case. The CPRI MII Interface transmitter can deassert `cpri_mii_txrd` while `cpri_mii_txen` is still asserted, to backpressure the external Ethernet block. If this happens, the Ethernet block must deassert `cpri_mii_txen` on the following cycle, to prevent the MII Interface transmitter buffer from overflowing. The `cpri_mii_txen` signal should remain deasserted until the cycle following reassertion of `cpri_mii_txrd`. If `cpri_mii_txen` is not reasserted in the cycle following the reassertion of `cpri_mii_txrd`, then an Idle cyle is inserted in the packet; therefore, the external Ethernet block must reassert `cpri_mii_txen` in the cycle following reassertion of `cpri_mii_txrd`.

The CPRI MII Interface receiver transmits the K nibble to indicate start-of-frame on the MII interface. Replace Figure 4-17 on page 57 of the CPRI MegaCore Function User Guide with the following Figure 4–2.

Figure 4–2. Corrected CPRI MII Interface Receiver Example



The J nibble of the start-of-frame is consumed by the CPRI MegaCore function, and is not transmitted on the MII interface.

The corrections indicated above apply to Figure 4-18 on page 57 of the CPRI MegaCore Function User Guide as well.

Affected Configurations

This issue affects all CPRI MegaCore function variations configured with the MII interface.

Design Impact

Designs that rely on the description of the MII interface in the CPRI MegaCore Function User Guide exhibit data corruption on the MII interface.

Workaround

Use the corrected description in this erratum in designing your external Ethernet block.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore Function User Guide.

CPRI MegaCore Function User Guide Unavailable From MegaWizard Interface Info Link

The Info link to the CPRI MegaCore Function User Guide from the CPRI MegaWizard interface does not work.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact.

Workaround

To view the CPRI MegaCore Function User Guide, open the **ug_cpri.pdf** file in your *<Quartus II v9.1 SP2 IP installation>***/cpri/doc** folder, or click the CPRI MegaCore Function User Guide link on the Altera Literature: User Guides web page.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

CPRI MegaCore Function Does Not Support HardCopy IV GX Devices

The HardCopy IV GX device family is not supported by the current release of the CPRI MegaCore function.

Affected Configurations

This issue affects all CPRI MegaCore function variations that target a HardCopy IV GX device.

Design Impact

CPRI MegaCore function designs that target a HardCopy IV GX device cannot be compiled or simulated.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

MegaWizard Plug-In Manager Does Not Recognize Transceiver Instances

After you generate an instance of the CPRI MegaCore function, its transceiver is not available for editing by the ALTGX MegaWizard interface. The MegaWizard Plug-In Manager does not recognize the transceiver as an existing instance of the ALTGX megafunction.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

The MegaWizard Plug-In Manager does not recognize the CPRI transceiver as an existing instance of the ALTGX megafunction.

Workaround

This issue is caused by a copyright notice at the top of the clear-text version of the ALTGX megafunction HDL code file. You can avoid this issue by editing the clear-text file to remove the copyright notice. To remove the text that causes the problem, perform the following steps:

1. Open the HDL file for your transceiver instance in a text editor.
2. Remove the copyright notice and following blank lines. The first characters in the file should be the following line:

   ```
   --megafunction wizard: %ALTGX%
   ```

3. Save the file. Now you can edit the transceiver instance using the ALTGX MegaWizard interface.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

Setup Time Violations Might Occur in Arria II GX 3072 Mbps Designs

Designs that include a CPRI MegaCore function that runs the CPRI link at 3072 Mbps and targets an Arria II GX device, might exhibit setup time violations.

Affected Configurations

This issue affects some 3072-Mbps CPRI MegaCore functions that target an Arria II GX device.

Design Impact

You might observe hardware failures after you configure the device.

Workaround

To avoid this issue, use the Design Space Explorer for seed sweeping.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

CPRI MegaCore Function User Guide Does Not Contain Complete Instructions for Running Simulation Testbench

The Testbenches chapter of the CPRI MegaCore Function User Guide does not provide adequate details to run the testbench successfully.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact.

Workaround

To run the demonstration testbenches successfully, perform the following steps:

1. Copy the Demonstration Testbench from the Installation Folder.
2. Specify the library file settings by performing one of the following two sets of instructions:
   - If you use the Mentor Graphics ModelSim SE simulator, follow the instructions in Set Up the Library Files for the ModelSim SE Simulator.
   - If you use the Altera ModelSim AE simulator, follow the instructions in Set Up the Library Files for the ModelSim AE Simulator.
3. Edit the .do File.
4. Run the Simulation.

Copy the Demonstration Testbench from the Installation Folder

To run the demonstration testbench successfully, you must copy all the testbench files from <*Quartus II installation directory*>**/ip/altera/cpri/cus_demo_tb** to a new subdirectory of your working directory, called <*working directory*>**/cus_demo_tb**.

Set Up the Library Files for the ModelSim SE Simulator

To run the demonstration testbench using the Mentor Graphics ModelSim SE simulator, perform the following steps:

1. Create a library folder, <*working directory*>**/lib**.

2. Perform one of the following steps:
   - If you are using Verilog HDL models, copy the following files to *<working directory>***/lib**:

```
$QUARTUS_ROOTDIR/eda/sim_lib/altera_mf.v
$QUARTUS_ROOTDIR/eda/sim_lib/arriaii_hssi_atoms.v
$QUARTUS_ROOTDIR/eda/sim_lib/stratixiv_hssi_atoms.v
$QUARTUS_ROOTDIR/eda/sim_lib/220model.v
$QUARTUS_ROOTDIR/eda/sim_lib/sgate.v
```

   - If you are using VHDL models, copy the following files to *<working directory>***/lib**:

```
$QUARTUS_ROOTDIR/eda/sim_lib/altera_mf_components.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/altera_mf.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/220pack.v
$QUARTUS_ROOTDIR/eda/sim_lib/220model.v
$QUARTUS_ROOTDIR/eda/sim_lib/sgate_pack.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/sgate.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/arriaii_hssi_components.v
$QUARTUS_ROOTDIR/eda/sim_lib/arriaii_hssi_atoms.v
$QUARTUS_ROOTDIR/eda/sim_lib/stratixiv_hssi_components.v
$QUARTUS_ROOTDIR/eda/sim_lib/stratixiv_hssi_atoms.v
```

Set Up the Library Files for the ModelSim AE Simulator

Copy the following library files from *<Quartus II installation directory>***/modelsim_ase/altera/vhdl** to your testbench directory *<working directory>*:

- **altera**
- **altera_mf**
- **arriaii_hssi**
- **stratixiv_hssi**
- **sgate**

Edit the .do File

Edit the appropriate ModelSim **.do** file for your CPRI MegaCore function variation. and your choice of HDL. The VHDL files are **compile.do** and **compile_mii.do**, and the Verilog HDL files are **compile_verilog.do** and **compile_mii_verilog.do**.

Perform the following edits, depending on your ModelSim version and HDL:

- To prepare to simulate with ModelSim AE, perform the following edits:
  - Comment out all `vlib` commands, except for `vlib -unix work`
  - Comment out all `vmap` commands.
  - Comment out all Quartus II library `vcom` commands.
  - Change all instances of `src/cpri_top_level.vho` to `../cpri_top_level.vho`.
  - Change all instances of `test/tb_altera_cpri.vhd` to `tb_altera_cpri.vhd`.

- To prepare to simulate Verilog HDL or VHDL files with ModelSim SE, perform the following edits:
  - Change all instances of `src/cpri_top_level.vho` to `../cpri_top_level.vho`.
  - Change all instances of `test/tb_altera_cpri.vhd` to `tb_altera_cpri.vhd`.
- To prepare to simulate Verilog HDL files with ModelSim SE, perform the following edits:
  - Change all instances of `src/cpri_top_level.vo` to `../cpri_top_level.vo`.
  - Change all instances of `test/tb_altera_cpri.vhd` to `tb_altera_cpri.vhd`.

Run the Simulation

To compile and run the simulation, perform the following steps:

1. Depending on your CPRI MegaCore function variation and your HDL, identify the correct .**do** file, <*my_variation*>**.do**. The following files are available: **compile.do** (VHDL), **compile_verilog.do**, **compile_mii.do** (VHDL), and **compile_mii_verilog.do**.
2. To compile the design variation, type the following command:

   ```
   do <my_variation>.do ↵
   ```

3. To simulate the testbench, type the following command:

   ```
   run -all ↵
   ```

The appropriate waveform display file, **wave.do** or **wave_mii.do**, runs and displays the waveforms for a predetermined set of signals automatically.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

5. CRC Compiler

Revision History

Table 5–1 shows the revision history for the CRC Compiler.

For more information about the new features, refer to the *CRC Compiler User Guide*.

Table 5–1. CRC Compiler Revision History

Version	Date	Description
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX device family.
8.1	November 2008	Maintenance release.

Errata

Table 5–2 shows the issues that affect the CRC Compiler v9.1, v9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the CRC Compiler.

Table 5–2. CRC Compiler Errata

Added or Updated	Issue	Affected Version				
		9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Jul 09	Incorrect User Guide on ACDS	—	Fixed	✓	—	—
01 Dec 06	Testbench Directory Generated When You Create a Simulation Model	✓	✓	✓	✓	✓

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *CRC Compiler User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the CRC Compiler.

Testbench Directory Generated When You Create a Simulation Model

When you create a simulation model, the CRC compiler automatically creates a **testbench** directory in the project directory for you. If you follow the **Running the Testbench Example** steps in the *CRC Compiler User Guide* to create the generator and checker files, another **testbench** directory is created as a subdirectory of the initial **testbench** directory, resulting in the following directory structure:

c:\altera\projects\crc_project\testbench\testbench

when the initial directory is

c:\altera\projects\crc_project\testbench

Affected Configuration

All CRC MegaCore function variations are affected.

Design Impact

This issue has no design impact.

Workaround

The **testbench** subdirectory (**testbench\testbench**) of the initial **c:\altera\projects\crc_project\testbench** directory may be deleted.

Solution Status

No change is planned currently.

6. DDR and DDR2 SDRAM Controller Compiler

Revision History

Table 6–1 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.

For more information about the new features, refer to the *DDR and DDR2 SDRAM Controller Compiler User Guide*.

Table 6–1. DDR and DDR2 SDRAM Controller Compiler Revision History

Version	Date	Description
9.1	November 2009	Maintenance release.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	November 2008	Maintenance release.

Errata

Table 6–2 shows the issues that affect the DDR and DDR2 SDRAM Controller Compiler v9.1, v9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controller Compiler.

Table 6–2. DDR and DDR2 SDRAM Controller Compiler Errata

Added or Updated	Issue	Affected Version				
		9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Jul 09	Incorrect User Guide on ACDS	—	Fixed	✓	—	—
15 Mar 09	DDR and DDR2 SDRAM Controllers Verilog HDL Design Does Not Work	—	—	—	Fixed	✓
	"Cannot Find Source Node" Error During Post-Compile Timing Analysis	—	—	—	Fixed	✓
01 Nov 08	VHDL Package Declaration Error When Upgrading the MegaCore Function	—	—	—	—	Fixed
15 Jul 08	Read Requests Are Sometimes Discarded	—	—	—	—	—
15 Oct 07	Error: Can't Find the Clock Output Pins. Stop.	✓	✓	✓	✓	✓
01 Jul 07	ODT Launches Off System Clock	✓	✓	✓	✓	✓
01 Jun 06	Error Message When Recompiling a Project	✓	✓	✓	✓	✓
	Pin Planner HDL Syntax Error	✓	✓	✓	✓	✓

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *DDR and DDR2 SDRAM Controller Compiler User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the DDR and DDR2 SDRAM Compiler.

DDR and DDR2 SDRAM Controllers Verilog HDL Design Does Not Work

If you generate a Verilog HDL instance of the DDR or DDR2 SDRAM Controller version 8.1, the design will not work in hardware or simulation.

Affected Configurations

This issue affects all Verilog HDL instances of the **Insert extra pipeline registers in datapath** option enabled. The VHDL designs are not affected.

Design Impact

Your design will not work in hardware or simulation.

Workaround

If you require a Verilog HDL instance of the DDR or DDR2 SDRAM Controller, you can use one of the following workarounds:

- Continue to use your existing version 8.0 instance. There are no functional changes between versions 8.0 and 8.1 of the DDR or DDR2 SDRAM Controller, so you are not required to upgrade.
- If you choose to upgrade to version 8.1 or if you do not have a version 8.0 instance, edit the <*variation name*>**_auk_ddr_sdram.v** file to change all instances of the line:

  ```
  else if (0)
  ```

  to

  ```
  else if (1)
  ```

Solution Status

This issue is fixed in version 9.0 of the DDR and DDR2 SDRAM Controller Compiler.

"Cannot Find Source Node" Error During Post-Compile Timing Analysis

The post-compile timing script may report the following error:

```
Cannot find source node
'<variation>:<variation>_ddr_sdram|...|<variation>_auk_ddr_datapath:dd
r_io|<variation>_auk_ddr_dqs_group\g_datapath:0:g_ddr_io|dq_enable_res
et[0]'
```

Affected Configurations

Some Stratix II and Stratix II GX designs.

Design Impact

You cannot successfully complete the post-compile timing analysis.

Workaround

Add an `"Auto Shift Register Replacement"` constraint to the following node in your Quartus II project using the Assignment editor, and set the value to **Off**.

```
<variation>:<variation>_ddr_sdram|<variation>_auk_ddr_sdram:<va
riation>_auk_ddr_sdram_inst|<variation>_auk_ddr_datapath:ddr_io
```

Solution Status

This issue is fixed in version 9.0 of the DDR and DDR2 SDRAM Controller Compiler.

VHDL Package Declaration Error When Upgrading the MegaCore Function

If you upgrade an existing custom variation of the MegaCore function, the following error may occur:

```
Error (10624): VHDL Package Declaration error at
auk_ddr_tb_functions.vhd(23): package "auk_ddr_tb_functions" already
exists in the work library
```

IP Toolbench adds files to your Quartus II project when you generate your custom variation. When you upgrade your MegaCore function, the same files from the previous and current versions are present in the same Quartus II project, which causes a VHDL error.

Affected Configurations

This issue affects all designs that were created in a previous version of the MegaCore function.

Workaround

From your Quartus II project, remove the Device Design Files that were added by the earlier version of the MegaCore function. These files can be identified by the files' directory names.

Design Impact

You cannot compile your Quartus II project until you remove the duplicate files.

Solution Status

This issue is fixed in version 8.1 of the DDR and DDR2 SDRAM Controller Compiler.

Read Requests Are Sometimes Discarded

Some read requests on the local interface may be discarded and not sent to the memory, particularly the first read to a bank that has not yet been activated.

Affected Configurations

All configurations are affected.

Design Impact

Your design may fail to operate correctly.

Workaround

Regenerate your controller instance in the latest version of the DDR and DDR2 SDRAM Controller Compiler.

Solution Status

This issue is fixed in version 8.0 SP1 of the DDR and DDR2 SDRAM Controller Compiler.

Error: Can't Find the Clock Output Pins. Stop.

The post-compile timing script reports the following error:

```
'Couldn't find the clock output pins. Stop.'
```

Affected Configurations

This issue affects designs using the DDR SDRAM controller, when the PLL counters have been reordered or the clocks for the DDR SDRAM interface are not on global clocks. This issue may occur automatically in the Fitter if there is pressure on global clock resources.

Design Impact

The design fails.

Workaround

Make the following two assignments:

```
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst Preserve PLL Counter Order
On
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst|altpll:altpll_component|_c
lk3* Global Signal Global Clock
```

Replace the file names of the PLL with those in your DDR SDRAM controller design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

ODT Launches Off System Clock

In designs with a separate address and command clock, the ODT output launches from the system clock, not from this address and command clock.

Affected Configurations

This issue affects the following configurations:

- DDR2 SDRAM controller (not DDR SDRAM)
- ODT is turned on
- CAS latency is set to three
- The design uses a separate address and command clock and not the default system clock

Design Impact

This issue has no design impact.

Workaround

Use a CAS latency of four, which means one extra cycle of read latency, or use the DDR2 SDRAM High-Performance controller, which uses the ALTMEMPHY megafunction to transfer all the address and command outputs to the correct clock.

Solution Status

This issue will never be fixed.

Error Message When Recompiling a Project

If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

```
Error: DDR timing cannot be verified until project has been successfully compiled.
```

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.

Affected Configurations

This issue affects all configurations.

Design Impact

The timing script does not verify your design.

Workaround

Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

Solution Status

This issue will never be fixed.

Pin Planner HDL Syntax Error

There is an HDL syntax error in Pin Planner-generated top-level design files that contain a DDR or DDR2 SDRAM Controller variation.

Affected Configurations

Pin Planner-generated top-level design files that use a design that contains a DDR or DDR2 SDRAM Controller variation.

Design Impact

If you import the DDR or DDR2 SDRAM Controller Pin Planner file into Pin Planner and then generate a top-level design file for your design, it contains an HDL syntax error and does not compile in the Quartus II software. You cannot use this top -level design file for IO Assignment Analysis.

Workaround

Use the IP Toolbench top-level example design and automatically assigned constraints to verify your pin and IO assignments.

Solution Status

This issue will never be fixed.

7. DDR and DDR2 SDRAM High-Performance Controller

Revision History

Table 7–1 shows the revision history for the DDR and DDR2 SDRAM High-Performance Controller MegaCore function.

For more information about the new features, refer to the *DDR and DDR2 SDRAM High-Performance Controller and ALTMEMPHY IP User Guide*.

Table 7–1. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Revision History

Version	Date	Description
9.1 SP2	April 2010	Maintenance release.
9.1 SP1	February 2010	Preliminary support for Cyclone IV E devices.
9.1	November 2009	■ New controller architecture added. ■ Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ Preliminary support for Arria II GX devices. ■ Optional support for Altera PHY interface (AFI) Controller-PHY Interface. ■ Optional multiple controller clock sharing in an SOPC Builder-generated design.
8.1	November 2008	■ Reduced controller latency and improved efficiency. ■ Improved example top-level design. ■ Support for multiple synchronous controllers in an SOPC Builder-generated design.

Errata

Table 7–2 shows the issues that affect the DDR and DDR2 SDRAM High-Performance Controllers v9.1 SP2, 9.1 SP1, 9.1, 9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the DDR and DDR2 SDRAM High-Performance Controllers.

Table 7–2. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version						
		9.1 SP2	9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 May 10	Cyclone III Speed Grade Support for Full-Rate DDR2 SDRAM Memory Specification	✓	✓	✓	—	—	—	—
	DQS and DQSn Signals Generate Extra Pulse	✓	✓	✓	✓	✓	✓	✓
	Wrong or Corrupted Data on Reads In Multi-Chip Designs	✓	✓	✓	✓	✓	✓	✓
	Wrong or Corrupted Data on Reads In Single-Chip Designs	Fixed	✓	✓	✓	✓	✓	✓
01 Apr 10	Postamble Calibration Scheme in Sequencer Violates Timing	✓	✓	✓	—	—	—	—
	CSR Address 0×005 and 0×006 Contents Cannot be Accessed	✓	✓	✓	—	—	—	—
	Half-Rate Clock Not Connected When Clock Sharing is Enabled	✓	✓	✓	—	—	—	—
	Simulation Fails When Power-Down Mode Issued Before Read Operation	—	—	Fixed	✓	✓	✓	—
15 Feb 10	Wrong Default Value	✓	✓	—	—	—	—	—
	csr_waitrequest Signal Exhibits “X” in Simulation	✓	✓	✓	—	—	—	—
15 Nov 09	Timing Violation In Half-Rate Bridge Enabled Designs	✓	✓	✓	—	—	—	—
	Generate Simulation Model Option Gets Disabled	✓	✓	✓	—	—	—	—
	DDR Controller Designs in AFI Mode with Memory Burst Length of 2 Fail in Simulation	✓	✓	✓	✓	✓	✓	✓
	Designs with Eight Chip Selects Fail Compilation	✓	✓	✓	✓	✓	✓	✓
	DDR2 Controller Designs with ODT Setting and Registered DIMM Options Enabled Cannot Be Generated	—	—	Fixed	✓	✓	✓	—
	Simulation Fails When test_incomplete_writes Signal is Asserted	—	—	Fixed	✓	✓	✓	✓
	DDR2 Full Rate Controller Designs with Error Correction Coding (ECC) Fail to Meet Timing	—	—	Fixed	✓	✓	✓	—
01 Sept 09	Intermittent Read Failure After Calibration	—	—	—	—	—	Fixed	✓
01 Jul 09	Incorrect User Guide on ACDS	—	—	—	Fixed	✓	—	—
15 May 09	DDR2 Full Rate Controller Designs in AFI Mode Do Not Meet Specified Maximum Supported Frequency (F_{max})	—	—	—	—	Fixed	✓	—
15 Mar 09	Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	✓	✓	✓	✓	✓	✓	✓
	Incorrect Controller Latency Information in User Guide	—	—	—	—	—	Fixed	✓
01 Dec 08	SOPC Builder Does Not Recognize Decimal Points	✓	✓	✓	✓	✓	✓	✓

Table 7–2. DDR and DDR2 SDRAM High-Performance Controller MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version						
		9.1 SP2	9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 May 08	RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected	✓	✓	✓	✓	✓	✓	✓
	Gate Level Simulation Fails	✓	✓	✓	✓	✓	✓	✓
	VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected	✓	✓	✓	✓	✓	✓	✓
	Memory Presets Contain Some Incorrect Memory Timing Parameters	✓	✓	✓	✓	✓	✓	✓
15 Oct 07	Mimic Path Incorrectly Placed	✓	✓	✓	✓	✓	✓	✓
01 Dec 06	Simulating with the NCSim Software	✓	✓	✓	✓	✓	✓	✓
	Simulating with the VCS Simulator	✓	✓	✓	✓	✓	✓	✓

Cyclone III Speed Grade Support for Full-Rate DDR2 SDRAM Memory Specification

The maximum clock rate for Cyclone III speed grades supporting full-rate DDR2 SDRAM on column I/Os are downgraded for version 9.1 and later. The maximum clock rate is downgraded because the Quartus II tool is unable to achieve push-button placement at the faster clock rates with DDR2 SDRAM high-performance controller II (HPC II).

Table 7–3 shows the downgraded specifications for the Quartus II software version 9.1.

Table 7–3. Full-Rate DDR2 SDRAM Support for Cyclone III Devices

Memory Standard	Device	Speed Grade	Maximum Full-Rate Clock Rate (MHz)
			Column I/O (Single Chip Select)
DDR2 SDRAM	Cyclone III	C6	167 *(1)*
		C7	150 *(2)*
		C8, I7, A7	150 *(1)*

Notes to Table 7–3:

(1) You need 267-MHz memory component speed grade when using class I I/O standard and 333-MHz memory component speed grade when using class II I/O standard.

(2) You need 200-MHz memory component speed grade.

Affected Configurations

This issue affects all designs that use full-rate DDR2 SDRAM with HPC II architecture and target the Cyclone III devices. If you are using DDR2 SDRAM with HPC architecture, you are not affected by this downgrade.

Design Impact

There is no design impact.

Workaround

To achieve higher clock rates, refer to the solution provided at http://www/support/kdb/solutions/rd05112010_783.html.

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controllers.

DQS and DQSn Signals Generate Extra Pulse

The DQS and DQSn signals generate an extra pulse after a write for designs that use the half-rate DDR or DDR2 SDRAM with HPC architecture.

Because the controller asserts the DM pin high after the write burst, the extra pulse does not cause any incorrect data to be written into the memory.

Affected Configurations

This issue affects all designs that use half-rate DDR or DDR2 SDRAM with HPC architecture and target Arria II GX, Stratix III, or Stratix IV devices.

Design Impact

If your board is not using DM pins, incorrect data may be written into the memory.

Workaround

Use the HPC II architecture instead.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Wrong or Corrupted Data on Reads In Multi-Chip Designs

Certain traffic patterns in multi-chip designs using DDR2 SDRAM high-performance controllers may cause writes to fail, making reads return unexpected data.

Affected Configurations

This issue affects all multi-chip designs that use the DDR2 SDRAM HPC or HPC II architecture with close read to write transactions.

Design Impact

The data written is corrupted.

Workaround

Modify the system to push write transactions away from read transaction.

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controllers.

Wrong or Corrupted Data on Reads In Single-Chip Designs

Certain traffic patterns in single-chip designs using DDR2 SDRAM high-performance controllers may cause writes to fail, making reads return unexpected data.

Affected Configurations

This issue affects all single-chip designs that use the DDR2 SDRAM HPC or HPC II architecture with close read to write transactions.

Design Impact

The data written is corrupted.

Workaround

There are two possible ways to work around this issue:

1. Modify the system to push write transactions away from read transactions.
2. Modify the PHY to introduce an additional clock cycle when switching from read to write, by performing the following steps:
   a. Open the <*variation name*>**_alt_mem_phy_seq.vhd** file, found in the folder with the memory IP.
   b. Search for the instantiation of constant `DEFAULT_OCT_EXTEND`
   c. Change the value from 5 to 3.
   d. Recompile the project.

Solution Status

This issue is fixed in version 9.1 SP2 of the DDR2 SDRAM High-Performance Controllers.

Postamble Calibration Scheme in Sequencer Violates Timing

For DDR memory interfaces with low frequency, the postamble calibration scheme in the sequencer violates the refresh memory timing parameter, breaching the JEDEC specifications.

Affected Configurations

This issue affects all designs with DDR SDRAM controller using the following frequencies and devices:

- Frequency between 110 and 120 MHz for Arria II GX devices.
- Frequency between 100 and 110 MHz for Stratix II devices.
- Frequency below 133 MHz frequency for Stratix III and Stratix IV devices.

Design Impact

Your design fails to simulate.

Workaround

Reduce the initial postamble latency by performing the following steps:

1. Open <*variation name*>**_phy_alt_mem_phy.v** file.
2. Search for the `POSTAMBLE_INITIAL_LAT` parameter.
3. Subtract a few cycles off from the current value.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM High-Performance Controllers.

CSR Address 0×005 and 0×006 Contents Cannot be Accessed

Designs that use the DDR or DDR2 HPC II architecture with the **Enable configuration and status register interface** option turned on, cannot access the CSR address 0×005 and 0×006 contents.

Affected Configurations

This issue affects all designs that use the DDR or DDR3 high-performance controller II architecture with the **Enable configuration and status register interface** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To access the CSR address 0×005 and 0×006 contents, perform the following steps:

1. Open <*variation name*>**_controller_phy.v** file.
2. Search for the following debug ports under the <variation *name*>`_phy` instantiation.
   - `dbg_clk` (Clock)
   - `dbg_addr` (Address)
   - `dbg_cs` (Chip select)
   - `dbg_waitrequest` (Wait request)
   - `dbg_wr` (Write request)
   - `dbg_wr_data` (Write data)
   - `dbg_rd` (Read request)
   - `dbg_dr_data` (Read data)
3. Export these ports into <*variation name*>**_example.v** file.
4. Use the Avalon-MM protocol to access the CSR address 0×005 and 0×006 contents through the debug ports.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Half-Rate Clock Not Connected When Clock Sharing is Enabled

If you generate a DDR or DDR2 controller with the **High Performance Controller II** and **Multiple controller clock sharing** options enabled in SOPC Builder, the half-rate clock is not connected.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Multiple controller clock sharing** option enabled in SOPC Builder.

Design Impact

The internal half-rate bridge for the sharing PLL controller does not function.

Workaround

To connect the half-rate clock, perform the following steps:

1. Edit the sharing PLL controller top-level file to include the half-rate clock input port as in the following example:

- Verilog HDL

```
module <variation name> (

sys_clk_in,
sys_half_clk_in,
soft_reset_n,

input sys_clk_in;
input    sys_half_clk_in;
input soft_reset_n;

.sys_clk_in(sys_clk_in),
.sys_half_clk_in(sys_half_clk_in),
.soft_reset_n(soft_reset_n),
```

- VHDL

```
ENTITY <variation name_master> IS
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;
```

```
COMPONENT <variation name>_controller_phy
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;

sys_clk_in  =>  sys_clk_in,
sys_half_clk_in => sys_half_clk_in,
aux_full_rate_clk  =>  aux_full_rate_clk,
```

2. Edit the SOPC top-level file to connect the half-rate clock from the source to the sharing controller as in the following example:

- Verilog HDL

```
<variation name> the_ <variation name>
(

.soft_reset_n (clk_0_reset_n),
.sys_half_clk_in     ( <variation
name_master>_aux_half_rate_clk_out),
.sys_clk_in   (<variation name_master>_phy_clk_out)
```

- VHDL

```
component <variation name> is
port (
-- inputs:

signal soft_reset_n : IN STD_LOGIC;
signal sys_half_clk_in : IN STD_LOGIC;
signal sys_clk_in : IN STD_LOGIC;

the_<variation name> : <variation name>
port map(

soft_reset_n => clk_0_reset_n,
sys_half_clk_in => out_clk_<variation name_master>_aux_half_rate_clk,
sys_clk_in => internal_<variation name_master>_phy_clk_out
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Simulation Fails When Power-Down Mode Issued Before Read Operation

When you enable power-down mode before performing any read operation, simulation fails.

Affected Configurations

This issue affects all designs that use the DDR2 SDRAM with high-performance controller I architecture, and the **Enable power down controls** option turned on.

Design Impact

Your design fails to simulate.

Workaround

Perform at least one read operation before requesting power down.

Solution Status

This issue is fixed in version 9.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Wrong Default Value

If you generate the core targeting a Cyclone IV E device with the high-performance controller architecture, without creating a new project first , the MegaWizard Plug-In Manager selects the default speed grade and clock frequency values that are not supported. If you generate the core, "`The given combination of PLL input and output cannot be synthesized.`" error message appears.

Affected Configurations

This issue affects all designs that use the high-performance controller architecture targeting Cyclone IV E devices .

Design Impact

Your system cannot be generated.

Workaround

Create a new project and select the device first before generating the core. Make sure to specify the speed grade to a value higher that 8, and the clock frequency to a value higher that 200 MHz.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

csr_waitrequest Signal Exhibits "X" in Simulation

If you generate a DDR or DDR2 controller with the **High Performance Controller II** and **Configuration and Status Register Interface** options enabled, the `csr_waitrequest` signal exhibits 'X' in simulation.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Configuration and Status Register Interface** option enabled.

Design Impact

Your design fails to simulate.

Workaround

Remove the `csr_waitrequest` signal connection from your design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Timing Violation In Half-Rate Bridge Enabled Designs

Timing violation occurs during TimeQuest timing analysis for designs that use the high-performance controller II architecture with the **Enable Half Rate Bridge** option turned on.

Affected Configurations

This issue affects all designs that use the high-performance II controller architecture with the **Enable Half Rate Bridge** option turned on.

Design Impact

Timing violation occurs during compilation in the TimeQuest timing analyzer.

Workaround

Open the **altera_avalon_half_rate_bridge_constraints.sdc** file in your project directory, and edit the `slow_clock` variable and add `derive_pll_clocks`.

- Full-rate design

```
derive_pll_clocks
set slow_clk "*|altpll_component|auto_generated|pll1|clk[1]"
```

- Half-rate design

```
derive_pll_clocks
set slow_clk "*|altpll_component|auto_generated|pll1|clk[0]"
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Generate Simulation Model Option Gets Disabled

The **Generate simulation model** option gets disabled after every generation.

Affected Configurations

This issue affects all configurations.

Design Impact

The simulation model for your design is not generated for the second time.

Workaround

Turn on the **Generate simulation model** option each time you want to generate a simulation model.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

DDR Controller Designs in AFI Mode with Memory Burst Length of 2 Fail in Simulation

Designs that use the full-rate DDR SDRAM high-performance controller in AFI mode with a memory burst length of 2 fail to simulate.

Affected Configurations

This issue affects all designs that use DDR SDRAM high-performance controller in full-rate mode with a memory burst length of 2.

Design Impact

As the generated memory model does not support memory burst length of 2, your design fails to simulate.

Workaround

Use a vendor memory model instead.

Solution Status

This issue will not be fixed in a future version of the DDR SDRAM High-Performance Controller.

Designs with Eight Chip Selects Fail Compilation

Designs that use eight chip selects with the high-performance controller architecture fails to compile.

Affected Configurations

This issue affects all designs that use eight chip selects with the high-performance controller architecture.

Design Impact

Your design fails to compile.

Workaround

In the MegaWizard interface, select **High Performance Controller II** as your controller architecture.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

DDR2 Controller Designs with ODT Setting and Registered DIMM Options Enabled Cannot Be Generated

Designs that use DDR2 SDRAM high-performance controllers with **Memory on-die termination (ODT) setting** and **Registered DIMM** option for **Memory format** turned on cannot be generated using the MegaWizard interface.

Affected Configurations

This issue affects all designs with DDR2 SDRAM high-performance controllers that have the **Memory on-die termination (ODT) setting** and **Registered DIMM** options turned on.

Design Impact

Your design cannot be generated in the MegaWizard interface.

Workaround

Perform the following steps to generate the DDR2 SDRAM High-Performance Controller MegaCore in the Quartus II software:

1. Generate a top variant file in the MegaWizard interface with valid options, for example, `RDIMM, ODT disabled, CL 5`.
2. After generating, modify the top variant file to the option that you want. In this case, change the value of ODT to a value that you prefer.

   Change the following code:

   ```
   // Retrieval info: <PRIVATE name = "mem_odt" value="Disabled"
   type="STRING" enable="1" />
   ```

   to:

   ```
   // Retrieval info: <PRIVATE name = "mem_odt" value="50"
   type="STRING" enable="1" />
   ```

3. Type the following command in the terminal:

   `qmegawiz –silent` *<variant file name>*

If you want to generate the core with a simulation model, type:

```
qmegawiz -silent OPTIONAL_FILES=SIM_NETLIST
INTENDED_DEVICE_FAMILY=<family name>  <variant file name>
```

For example, if you are using a Stratix III device and your variant file name is **ddr2hp.v**, your command should look like the following:

```
qmegawiz -silent OPTIONAL_FILES=SIM_NETLIST
INTENDED_DEVICE_FAMILY=stratixiii ddr2hp.v
```

Solution Status

This issue is fixed in version 9.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Simulation Fails When test_incomplete_writes Signal is Asserted

Simulation for DDR and DDR2 SDRAM high-performance controllers fails when `test_incomplete_writes` signal is asserted.

Affected Configurations

This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers with the `MAX_ROW` parameter set to 8191.

Design Impact

Your design fails to simulate at test incomplete writes mode when the `test_incomplete_writes` signal is asserted.

Workaround

Replace the `reached_max_address` assignment code in the example driver with the following assignment code:

- Verilog HDL

```
assign reached_max_address = ((test_dm_pin_mode | test_addr_pin_mode) & (row_addr ==
MAX_ROW_PIN)) || ((test_seq_addr_mode | test_incomplete_writes_mode) & (col_addr ==
(max_col_value)) & (row_addr == MAX_ROW) & (bank_addr == MAX_BANK) & (cs_addr ==
MAX_CHIPSEL));
```

- VHDL

```
reached_max_address <= ((((test_dm_pin_mode OR test_addr_pin_mode)) AND
to_std_logic(((row_addr = MAX_ROW_PIN))))) OR (((((((test_seq_addr_mode OR
test_incomplete_writes_mode)) AND to_std_logic(((col_addr = (max_col_value))))) AND
to_std_logic(((row_addr = MAX_ROW)))) AND to_std_logic(((bank_addr = MAX_BANK)))) AND
to_std_logic(((std_logic'(cs_addr) = std_logic'(MAX_CHIPSEL))))));
```

Solution Status

This issue is fixed in version 9.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

DDR2 Full Rate Controller Designs with Error Correction Coding (ECC) Fail to Meet Timing

Some designs with DDR2 SDRAM high-performance controllers at 200MHz that target Stratix II devices do not meet timing on the ECC path at 200MHz.

Affected Configurations

This issue affects some designs that use DDR2 SDRAM high-performance controllers that have the **Enable error detection and correction logic** option turned on, targeting Stratix II devices.

Design Impact

Your design may not meet timing at 200MHz.

Workaround

Add registers for `local_rdata_valid` and `local_rdata` signals at the user logic.

Solution Status

This issue is fixed in version 9.1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Intermittent Read Failure After Calibration

The ALTMEMPHY megafunction leads to intermittent read failure after calibration.

Affected Configurations

This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers (versions 8.1 and previous) in full-rate mode and DQS-based capture.

Design Impact

Your design may fail in hardware at low frequency.

Workaround

Apply the patch provided at http://www.altera.com/support/kdb/solutions/rd12182008_673.html, and recompile your design.

Solution Status

This issue is fixed in version 9.0 of the DDR and DDR2 SDRAM High-Performance Controllers.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *DDR and DDR2 SDRAM High-Performance Controller MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the DDR and DDR2 SDRAM High-Performance Controller.

DDR2 Full Rate Controller Designs in AFI Mode Do Not Meet Specified Maximum Supported Frequency (F_{max})

Some designs with the full-rate DDR2 SDRAM high-performance controllers in AFI mode do not meet the specified F_{max}.

Affected Configurations

This issue affects designs that use full-rate DDR and DDR2 SDRAM high-performance controllers in AFI mode running maximum frequency, targeting Arria II GX, Cyclone III, and Stratix II devices. Designs that target Arria GX, Stratix III, and Stratix IV are not affected.

Design Impact

Your design does not meet the required F_{max} in Timing Analysis.

Workaround

Use the non-AFI mode instead.

Solution Status

This issue is fixed in version 9.0 SP1 of the DDR and DDR2 SDRAM High-Performance Controllers.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR or DDR2 SDRAM high-performance controllers do not work with the **Enable error detection and correction logic** option enabled.

Affected Configurations

This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers that have the **Enable error detection and correction logic** option turned on.

Design Impact

Your design does not work properly in both simulation and hardware after the subsequent reset.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Incorrect Controller Latency Information in User Guide

The controller latency information in Tables C1 to C9 in the *DDR and DDR2 SDRAM High-Performance Controllers User Guide* 8.1 is incorrect.

The correct controller latency for DDR and DDR2 SDRAM high-performance controllers is five for half-rate controller and four for full-rate controller.

Solution Status

This issue is fixed in version 9.0 of the *DDR and DDR2 SDRAM High-Performance Controllers User Guide*.

SOPC Builder Does Not Recognize Decimal Points

If you assign the PLL clock with a value with decimals, SOPC Builder takes only the whole number and does not recognize the value after the decimal point. When you generate the system, the "`The PLL reference clock of` <*value*> `does not match the clock frequency input to refclk`" error message appears.

Affected Configurations

This issue affects all designs that have a PLL clock value with decimals.

Design Impact

Your system cannot be generated.

Workaround

Ignore the error message, and generate the system by holding down the Ctrl key on the keyboard while clicking **Generate** in SOPC Builder.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected

The example testbench RTL simulation may not simulate correctly when a dedicated memory clock phase is selected because clock net delay between the PLL and the clock output pins is not modelled in the RTL.

Affected Configurations

This issue affects designs that enable the **Use dedicated PLL outputs to drive memory clocks** option and set a value for the **Dedicated memory clock phase** parameter.

Design Impact

The design does not simulate correctly.

Workaround

Add MEM_CLK_DELAY to clk_to_ram signal at example top-level testbench, to compensate for the on-chip clock net delay to mem_dqs which is not present in the RTL simulation.

```
parameter DED_MEM_CLK = 1;
parameter real DED_MEM_CLK_PHASE = <value for dedicated memory clock
phase>
parameter real mem_clk_ratio = ((360.0DED_MEM_CLK_PHASE)/360.0);
parameter MEM_CLK_DELAY = mem_clk_ratio*CLOCK_TICK_IN_PS * (DED_MEM_CLK
? 1 : 0);
wire clk_to_ram0, clk_to_ram1, clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram2 = clk_to_sdram[0];
assign #(MEM_CLK_DELAY/4.0) clk_to_ram1 = clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram0 = clk_to_ram1;
assign #((MEM_CLK_DELAY/4.0)) clk_to_ram = clk_to_ram0;
//Replace testbench clk_to_ram assignment by adding MEM_CLK_DELAY
//assign clk_to_ram = clk_to_sdram[0];
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Gate Level Simulation Fails

Gate level simulation of the example design and example testbench fails when **Use differential DQS** is enabled in the DDR2 High-Performance Controller.

Affected Configurations

This issue affects DDR2 SDRAM High-Performance Controller designs in Stratix III and Stratix IV devices that have the **Use differential DQS** option enabled.

Design Impact

Gate level simulation of the example design does not behave correctly.

Workaround

You can use the following options:

1. To connect dqs_n example top-level design:

   ```
   - .mem_dqsn(mem_dqsn)
   ```

2. To connect dqs_n in memory model:

   ```
   -.DQSN mem_dqsn[index])
   ```

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected

VHDL generated sequencer block for CAS latency 2.0 and 2.5 designs using DDR SDRAM High-Performance Controller results in simulation failure. The issue is due to delta cycle delays on a clock net.

Affected Configurations

This issue affects DDR SDRAM High-Performance Controller CAS latency 2.0 and 2.5 designs.

Design Impact

This issue only affects simulation on VHDL and does not affect the functionality of the design.

Workaround

To workaround this issue, follow these steps:

1. Open the <*variation_name*>**_phy.vho** file in the project directory.
2. Search for the `altsyncram` instantiation for the postamble block (this can be done by searching for `" altsyncram"` —note the white space). This should be the `altsyncram` component with a label that includes the word `"postamble"`.
3. Search for the signal that is attached to the clock1 port to find the point in the design where this signal is assigned to (in a test case, this is on line 4043).

```
wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variat
ion_name>_phy_alt_mem_phy_sii_inst_<variation_name>phy_alt_mem_phy_pos
tamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_cloc
k1
```

4. Change the assignment as shown. The signal inside not(..) should be the same as the signal on clock0 port of a second instance of the `altsyncram` component which is associated to the read datapath (with `"read_dp"` in the label).

```
wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variat
ion_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_po
stamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clo
ck1 <= not
(wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<varia
tion_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_c
lk_reset_sii_clk_<variation_name>_phy_alt_mem_phy_pll_sii_pll_19462_c4
);
```

This step removes a delta delay for simulation but leaves the code unchanged. The right side of the assignment above is taken as the right side of the assignment to the signal which is previously assigned to the `"wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1"` signal.

5. If the <*variation_name*>**_phy** component is recompiled in your simulator, the design should now pass.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM High-Performance Controller.

Memory Presets Contain Some Incorrect Memory Timing Parameters

The memory presets contain incorrect data for the `tDSa` and `tDHa` memory timing parameters.

Affected Configurations

This issue affects all configurations.

Design Impact

Timing analysis results for write and address/command paths may be incorrect.

Workaround

Make sure that the memory timing parameters in the MegaWizard Plug-In Manager match the datasheet of the target memory device. The output edge rate and the use of single-ended versus differential DQS may affect certain memory parameters.

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM High-Performance Controller.

Mimic Path Incorrectly Placed

The Quartus II software may fail to place the mimic path correctly. The report timing script then indicates a timing setup failure on the mimic path.

Affected Configurations

This issue affects all designs.

Design Impact

Your design may fail.

Workaround

Manually edit the following parameter in the auto-generated Synopsis design constraint (**.sdc**) script to correct the timing analysis:

```
mimic_shift
```

Add a value of at least the worst case failed slack to the value already stated in the Synopsis design constraint file.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Simulating with the NCSim Software

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Set the `-relax` switch for all calls to the VHDL analyzer.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

Simulating with the VCS Simulator

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

The following workarounds exist.

VHDL

Change the following code.

- In file <*variation name*>**_example_driver.vhd**, change all `when` statements between lines 333 and 503 from `when std_logic_vector'("<bit_pattern>")` to `when "<bit_pattern>"`.
- In file **testbench**<*example name*>**_tb**, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0')`.

Verilog HDL

No changes are necessary. Calls to the Verilog analyzer sets the `+v2k` switch to enable Verilog 2000 constructs.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM High-Performance Controllers.

8. DDR3 SDRAM High-Performance Controller

Revision History

Table 8–1 shows the revision history for the DDR3 SDRAM High-Performance Controller MegaCore function.

For more information about the new features, refer to the *DDR3 SDRAM High-Performance Controller and ALTMEMPHY IP User Guide*.

Table 8–1. DDR3 SDRAM High-Performance Controller MegaCore Function Revision History

Version	Date	Description
9.1 SP2	April 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	■ New controller architecture added. ■ Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ Preliminary support for Arria II GX devices. ■ Full support for Stratix III devices.
8.1	November 2008	■ Reduced controller latency and improved efficiency. ■ Improved example top-level design. ■ Support for multiple synchronous controllers in an SOPC Builder-generated design.

Errata

Table 8–2 shows the issues that affect the DDR3 SDRAM High-Performance Controller v9.1 SP2, 9.1 SP1, 9.1, 9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Table 8–2. DDR3 SDRAM High-Performance Controller MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version						
		9.1 SP2	9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 May 10	Wrong or Corrupted Data on Reads In Multi-Chip Designs	✓	✓	✓	✓	✓	✓	✓
	Wrong or Corrupted Data on Reads In Single-Chip Designs	Fixed	✓	✓	✓	✓	✓	✓
01 Apr 10	CSR Address 0×005 and 0×006 Contents Cannot be Accessed	✓	✓	✓	—	—	—	—
	Memory Timing Violation During Activate Read Auto-Precharge to Refresh/Activate	✓	✓	✓	—	—	—	—
	Half-Rate Clock Not Connected When Clock Sharing is Enabled	✓	✓	✓	—	—	—	—

Table 8–2. DDR3 SDRAM High-Performance Controller MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version						
		9.1 SP2	9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 Feb 10	csr_waitrequest Signal Exhibits “X” in Simulation	✓	✓	✓	—	—	—	—
15 Nov 09	Timing Violation In Half-Rate Bridge Enabled Designs	✓	✓	✓	—	—	—	—
	Generate Simulation Model Option Gets Disabled	✓	✓	✓	—	—	—	—
	Designs with Eight Chip Selects Fail Compilation	✓	✓	✓	✓	✓	✓	✓
	Unable to Perform Partial-Write After Read in Designs with Error Correction Coding (ECC)	—	—	Fixed	✓	✓	✓	✓
	Simulation Fails When test_incomplete_writes Signal is Asserted	—	—	Fixed	✓	✓	✓	✓
	Different Read Data Orders	—	—	Fixed	✓	✓	✓	✓
01 Jul 09	Address Mirroring Not Supported By Memory Simulation Model	✓	✓	✓	✓	—	—	—
	Incorrect User Guide on ACDS	—	—	—	Fixed	✓	—	—
15 Mar 09	Memory Preset Parameters Do Not Get Updated	✓	✓	✓	✓	✓	✓	—
	Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	✓	✓	✓	✓	✓	✓	✓
	Incorrect Controller Latency Information in User Guide	—	—	—	—	—	Fixed	✓

Wrong or Corrupted Data on Reads In Multi-Chip Designs

Certain traffic patterns in multi-chip designs using DDR3 SDRAM high-performance controllers may cause writes to fail, making reads return unexpected data.

Affected Configurations

This issue affects all multi-chip designs that use the HPC or HPC II architecture with close read to write transactions.

Design Impact

The data written is corrupted.

Workaround

Modify the system to push write transactions away from read transaction.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Wrong or Corrupted Data on Reads In Single-Chip Designs

Certain traffic patterns in single-chip designs using DDR3 SDRAM high-performance controllers may cause writes to fail making reads return unexpected data.

Affected Configurations

This issue affects all single-chip designs that use the HPC or HPC II architecture with close read to write transactions.

Design Impact

The data written is corrupted.

Workaround

There are two possible ways to work around this issue:

1. Modify the system to push write transactions away from read transactions.
2. Modify the PHY to introduce an additional clock cycle when switching from read to write, by performing the following steps:
   a. Open the <*variation name*>**_alt_mem_phy_seq.vhd** file, found in the folder with the memory IP.
   b. Search for the instantiation of constant `DEFAULT_OCT_EXTEND`
   c. Change the value from 5 to 3.
   d. Recompile the project.

Solution Status

This issue is fixed in version 9.1 SP2 of the DDR3 SDRAM High-Performance Controllers.

CSR Address 0×005 and 0×006 Contents Cannot be Accessed

Designs that use the high-performance controller II architecture with the **Enable configuration and status register interface** option turned on, cannot access the CSR address 0×005 and 0×006 contents.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Enable configuration and status register interface** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

There is no workaround available for designs that use the DDR3 high-performance controllers with levelling (DIMM).

For designs that use the DDR3 high-performance controllers without levelling (discrete device only), perform the following steps to access the CSR address 0×005 and 0×006 contents:

1. Open <*variation name*>**_controller_phy.v** file.
2. Search for the following debug ports under the <variation *name*>`_phy` instantiation.

- dbg_clk (Clock)
- dbg_addr (Address)
- dbg_cs (Chip select)
- dbg_waitrequest (Wait request)
- dbg_wr (Write request)
- dbg_wr_data (Write data)
- dbg_rd (Read request)
- dbg_dr_data (Read data)

3. Export these ports into <*variation name*>**_example.v** file.
4. Use the Avalon-MM protocol to access the CSR address 0×005 and 0×006 contents through the debug ports.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Memory Timing Violation During Activate Read Auto-Precharge to Refresh/Activate

Memory timing violation occurs during the activate to read precharge

Affected Configurations

This issue affects all designs that use the high-performance controller architecture.

Design Impact

Your design may fail to simulate.

Workaround

For designs targeting 1066 specification and running with 533 MHz speed, increase one control clock cycle of the timing parameters **tRP** and **tRCD**, so that the tRC for the controller is greater than the tRC for the memory model.

For designs targeting 1066 specification and running with 400 MHz speed, increase one control clock cycle of the timing parameter **tRP**, so that the tRC for the controller is greater than the tRC for the memory model.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Half-Rate Clock Not Connected When Clock Sharing is Enabled

If you generate a DDR3 controller with the **High Performance Controller II** and **Multiple controller clock sharing** options enabled in SOPC Builder, the half-rate clock is not connected.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Multiple controller clock sharing** option enabled in SOPC Builder.

Design Impact

The internal half-rate bridge for the sharing PLL controller does not function.

Workaround

To connect the half-rate clock, perform the following steps:

1. Edit the sharing PLL controller top-level file to include the half-rate clock input port as in the following example:

- Verilog HDL

```
module <variation name> (

sys_clk_in,
sys_half_clk_in,
soft_reset_n,
input sys_clk_in;
input    sys_half_clk_in;
input soft_reset_n;

.sys_clk_in(sys_clk_in),
.sys_half_clk_in(sys_half_clk_in),
.soft_reset_n(soft_reset_n),
```

- VHDL

```
ENTITY <variation name_master> IS
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;

COMPONENT <variation name>_controller_phy
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;
sys_clk_in  =>  sys_clk_in,
sys_half_clk_in => sys_half_clk_in,
aux_full_rate_clk  =>  aux_full_rate_clk,
```

2. Edit the SOPC top-level file to connect the half-rate clock from the source to the sharing controller as in the following example:

- Verilog HDL

```
<variation name> the_ <variation name>
(

.soft_reset_n (clk_0_reset_n),
.sys_half_clk_in     ( <variation name_master>_aux_half_rate_clk_out),
.sys_clk_in   (<variation name_master>_phy_clk_out)
```

- VHDL

```
component <variation name> is
port (
-- inputs:
signal soft_reset_n : IN STD_LOGIC;
signal sys_half_clk_in : IN STD_LOGIC;
signal sys_clk_in : IN STD_LOGIC;

the_<variation name> : <variation name>
port map(

soft_reset_n => clk_0_reset_n,
sys_half_clk_in => out_clk_<variation name_master>_aux_half_rate_clk,
sys_clk_in => internal_<variation name_master>_phy_clk_out
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

csr_waitrequest Signal Exhibits "X" in Simulation

If you generate a DDR3 controller with the **High Performance Controller II** and **Configuration and Status Register Interface** options enabled, the `csr_waitrequest` signal exhibits 'X' in simulation.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Configuration and Status Register Interface** option enabled.

Design Impact

Your design fails to simulate.

Workaround

Remove the `csr_waitrequest` signal connection from your design.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Timing Violation In Half-Rate Bridge Enabled Designs

Timing violation occurs during TimeQuest timing analysis for designs that use the high-performance controller II architecture with the **Enable Half Rate Bridge** option turned on using SOPC Builder.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Enable Half Rate Bridge** option turned on.

Design Impact

Timing violation occurs during compilation in the TimeQuest timing analyzer.

Workaround

Open the **altera_avalon_half_rate_bridge_constraints.sdc** file in your project directory, and add `derive_pll_clocks` above the `slow_clock` variable.

```
derive_pll_clocks
set slow_clk "*|altpll_component|auto_generated|pll1|clk[0]"
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Generate Simulation Model Option Gets Disabled

The **Generate simulation model** option gets disabled after every generation.

Affected Configurations

This issue affects all configurations.

Design Impact

The simulation model for your design is not generated for the second time.

Workaround

Turn on the **Generate simulation model** option each time you want to generate a simulation model.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Designs with Eight Chip Selects Fail Compilation

Designs that use eight chip selects with the high-performance controller architecture fails to compile.

Affected Configurations

This issue affects all designs that use eight chip selects with the high-performance controller architecture

Design Impact

Your design fails to compile.

Workaround

In the MegaWizard interface, select **High Performance Controller II** as your controller architecture.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controller.

Unable to Perform Partial-Write After Read in Designs with Error Correction Coding (ECC)

A read followed by a partial-write is incorrectly implemented as a read followed by a full-write.

Affected Configurations

This issue affects all DDR3 SDRAM high-performance controller designs that have the **Enable error detection and correction logic** option turned on.

Design Impact

You are unable to perform a partial-write. A partial-write after a read is interpreted as a full-write.

Workaround

Apply the patch provided at http://www.altera.com/support/kdb/solutions/rd08042009_327.html, and recompile your design.

Solution Status

This issue is fixed in version 9.1 of the DDR3 SDRAM High-Performance Controller.

Simulation Fails When test_incomplete_writes Signal is Asserted

Simulation for DDR3 SDRAM high-performance controller fails when `test_incomplete_writes` signal is asserted.

Affected Configurations

This issue affects all designs that use DDR3 SDRAM high-performance controllers with the MAX_ROW parameter set to 8191.

Design Impact

Your design fails to simulate at test incomplete writes mode when the test_incomplete_writes signal is asserted.

Workaround

Replace the reached_max_address assignment code in the example driver with the following assignment code:

- Verilog HDL

```
assign reached_max_address = ((test_dm_pin_mode | test_addr_pin_mode) & (row_addr ==
MAX_ROW_PIN)) || ((test_seq_addr_mode | test_incomplete_writes_mode) & (col_addr ==
(max_col_value)) & (row_addr == MAX_ROW) & (bank_addr == MAX_BANK) & (cs_addr ==
MAX_CHIPSEL));
```

- VHDL

```
reached_max_address <= ((((test_dm_pin_mode OR test_addr_pin_mode)) AND
to_std_logic(((row_addr = MAX_ROW_PIN))))) OR (((((((test_seq_addr_mode OR
test_incomplete_writes_mode)) AND to_std_logic(((col_addr = (max_col_value))))) AND
to_std_logic(((row_addr = MAX_ROW)))) AND to_std_logic(((bank_addr = MAX_BANK)))) AND
to_std_logic(((std_logic'(cs_addr) = std_logic'(MAX_CHIPSEL))))));
```

Solution Status

This issue is fixed in version 9.1 of the DDR3 SDRAM High-Performance Controller.

Different Read Data Orders

A write followed by a read to an odd local address gives a different read data sequence.

Affected Configurations

This issue affects all DDR3 SDRAM high-performance controller designs that read from an odd local address when the local size is 2.

Design Impact

The read data sequence does not appear in your expected order when you read from an odd local address. The DDR3 SDRAM high-performance controller only works in an even starting local address when the local size is 2.

Workaround

Write and read to an even starting address to make sure the read data sequence is the same as the write data.

Solution Status

This issue is fixed in version 9.1 of the DDR3 SDRAM High-Performance Controller.

Address Mirroring Not Supported By Memory Simulation Model

The default memory simulation model does not support address mirroring. When you generate your design in the example testbench with the address mirroring parameter enabled, your simulation fails. To simulate successfully, you must replace the current memory simulation model with a vendor memory model and mirror the address bits in the <*variation name*>**_example_top_tb.v** or **.vhd** file.

Affected Configurations

This issue affects the multiple chip selects DDR3 DIMM which require mirrored address bits.

Design Impact

The default memory simulation model does not support DDR3 DIMM multiple chip selects mirrored address bits. Your design fails to simulate.

Workaround

Use the vendor memory model and mirror the address bits in the example top for target chip selects by doing the following:

1. Regenerate the DDR3 testbench. After generating, in the top variant file, <*variation name*>**.v** or **.vhd**, look for the following code:

```
//Retrieval info: <PRIVATE name = “use_generated_memory_model”
value=”true” type=”STRING” enable=”1”/>
```

   and change to:

```
//Retrieval info: <PRIVATE name = “use_generated_memory_model”
value=”false” type=”STRING” enable=”1”/>
```

2. Download the vendor memory model.
3. For the chip selects that require address mirroring, edit the <*variation name*>**_example_top_tb.v** or **.vhd** file by performing the following:
   a. Add the following lines:

```
wire[gMEM_ADDR_BITS - 1:0] a_reversed;
wire[gMEM_BANK_BITS - 1:0] ba_reversed;
assign a_reversed[2:0] = a_delayed[2:0];
assign a_reversed[3] = a_delayed[4];
assign a_reversed[4] = a_delayed[3];
assign a_reversed[5] = a_delayed[6];
assign a_reversed[6] = a_delayed[5];
assign a_reversed[7] = a_delayed[8];
assign a_reversed[8] = a_delayed[7];
assign a_reversed[gMEM_ADDR_BITS - 1:9] = a_delayed[gMEM_ADDR_BITS -
1:9];
assign ba_reversed[0] = ba_delayed[1];
assign ba_reversed[1] = ba_delayed[0];
```

```
assign ba_reversed[gMEM_BANK_BITS - 1:2] = ba_delayed[gMEM_BANK_BITS
- 1:2];
```

b. Locate the following lines:

```
.ba (ba_delayed),
.addr (a_delayed[14-1: 0]),
```

and change to:

```
.ba (ba_reversed),
.addr (a_reversed),
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controller.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *DDR3 SDRAM High-Performance Controller MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the DDR3 SDRAM High-Performance Controller.

Memory Preset Parameters Do Not Get Updated

Some memory presets are changed in version 9.0 of the DDR3 SDRAM High-Performance Controller. If you migrate your existing design from version 8.1 to 9.0, your memory preset paramaters do not get updated in version 9.0.

Affected Configurations

This issue affects all designs that are migrated to version 9.0.

Design Impact

The memory preset paramaters in your design do not get updated in version 9.0, even if you regenerate the MegaCore function.

Workaround

In the MegaWizard GUI, choose any random memory presets, and then reselect your original presets (remember to redo any modifications to the preset such as DQ width, CAS latency, and so on). Click **Finish** to regenerate the MegaCore function.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controller.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR3 SDRAM high-performance controllers do not work with the **Enable error detection and correction logic** option enabled.

Affected Configurations

This issue affects all designs that use DDR3 SDRAM high-performance controllers that have the **Enable error detection and correction logic** option turned on.

Design Impact

Your design does not work properly in both simulation and hardware after the subsequent reset.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM High-Performance Controllers.

Incorrect Controller Latency Information in User Guide

The controller latency information in Tables B2 and B3 in the *DDR3 SDRAM High-Performance Controller User Guide* 8.1 is incorrect.

The correct controller latency for DDR3 SDRAM high-performance controller is five.

Solution Status

This issue is fixed in version 9.0 of the *DDR3 SDRAM High-Performance Controller User Guide*.

Revision History

Table 9–1 shows the revision history for the FFT MegaCore function.

For more information about the new features, refer to the *FFT MegaCore Function User Guide*.

Table 9–1. FFT MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Full support for Stratix III devices.

Errata

Table 9–2 shows the issues that affect the FFT MegaCore function v9.1, v9.0, and 8.1.

Not all issues affect all versions of the FFT MegaCore function.

Table 9–2. FFT MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
15 Mar 09	Example Design Fails Compilation	✓	✓	—
01 Oct 07	Floating-Point FFT Produces Non-Zero Output	—	Fixed	✓
01 Dec 06	Simulation Errors—Synopsys VCS	✓	✓	✓
	Simulation Errors—Incorrect Results	✓	✓	✓
	Simulation Errors—MATLAB Model Mismatch	✓	✓	✓

Example Design Fails Compilation

The example top-level VHDL design with bit-reversal module (variable streaming FFT) cannot run compilation.

Affected Configurations

This issue affects variable streaming FFT designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Floating-Point FFT Produces Non-Zero Output

When a DC signal is input to a floating-point variable streaming configuration of the FFT, the output is an impulse response, where bin 0 contains the magnitude of the impulse response and the other bins should be 0. The value in bin 0 is correct. However, non-zero values are encountered in the other bins. These values have a magnitude in the range of 10 to 39. More specifically, the exponent is zero, and the mantissa contains a non-zero number. The IEEE754 floating point specification refers to a number with a zero exponent and non-zero mantissa as denormalized. The floating point FFT does not support denormalized numbers, therefore any number with a zero exponent can be considered to have a zero mantissa.

Under these conditions, the MATLAB simulation model also produces output with a zero exponent and non-zero mantissa. However, the value of the mantissa does not match the value in simulation.

Affected Configurations

This issue affects all floating point variable streaming configurations of the FFT.

Design Impact

The design compiles but gives incorrect results under some circumstances. The MATLAB simulation model does not match the simulation results.

Workaround

The mantissa bits should be zeroed if the exponent is zero.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—Synopsys VCS

When you use NativeLink to perform an RTL simulation using the generated Verilog HDL testbench in the VCS simulator, you see the following error:

```
Error: VCS: Error-[V2KS] Verilog 2000 IEEE 1364-2000 syntax used. Please
compile with +v2k
Error: VCS:     to support this construct
Error: VCS:     operator '**' .
```

Affected Configurations

This issue affects all Verilog HDL configurations.

Design Impact

There is no design impact; the design compiles correctly.

Workaround

In the Verilog HDL testbench <*variation name*>**_tb.v,** replace the power of operator '**' with the calculated value. Alternatively, compile with the +v2k option in the VCS simulator.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—Incorrect Results

When the input is defined as *N* bit wide, the permissible input range is from $-2^{N-1}+1$ to $2^{N-1}-1$. If the input contains the value -2^{N-1}, the HDL output is incorrect, and does not match the MATLAB simulation result.

Affected Configurations

This issue affects all configurations.

Design Impact

The design compiles but gives incorrect results.

Workaround

If you expect your input signal to contain the value -2^{N-1}, you should add a block in front of the FFT, which maps the value -2^{N-1} to $-2^{N-1}+1$.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—MATLAB Model Mismatch

For one particular FFT parameter combination, the HDL output does not match the MATLAB simulation results (for some frames of data).

HDL simulation results are scaled down by a factor of two compared to the MATLAB simulation results. The exponent value produced by the HDL simulation is one less than the output of the MATLAB simulations. When the exponent is taken into account, the MATLAB and the HDL version may differ by one LSB.

Affected Configurations

This issue affects the following parameter combination:

- Transform length: 64
- I/O data flow: burst architecture
- FFT engine architecture: quad output
- Number of parallel engines: 2

Design Impact

There is no design impact; the design compiles and operates correctly.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

10. FIR Compiler

Revision History

Table 10–1 shows the revision history for the FIR Compiler.

For information about the new features, refer to the *FIR Compiler User Guide*.

Table 10–1. FIR Compiler Revision History

Version	Date	Description
9.1 SP2	March 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	■ Full support for Stratix III devices. ■ Withdrawn support for UNIX.

Errata

Table 10–2 shows the issues that affect the FIR Compiler v9.1 SP2, v9.1 SP1, v9.1, v9.0, and v8.1.

Not all issues affect all versions of the FIR Compiler.

Table 10–2. FIR Compiler Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version				
		9.1 SP2	9.1 SP1	9.1	9.0	8.1
15 May 10	FIR Compiler Functional Simulation Model Is Not Generated	✓	✓	✓	—	—
1 Apr 10	FIR Compiler Does Not Support OpenCore Plus for Cyclone IV E Devices	Fixed	✓	—	—	—
15 Nov 09	Cannot Select M9K Data or Coefficient Storage When Device Family is Cyclone III	—	—	Fixed	✓	✓
15 Jun 09	Simulation Fails for the Coefficient Reloadable Filters	✓	✓	✓	✓	✓
15 Mar 09	Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional	✓	✓	✓	✓	✓
	Bit Serial Filter With 32-Bit Coefficients Does Not Work	—	—	—	Fixed	✓
	Half-Band Decimator and Symmetric Interpolator Do Not Support Unsigned Type	—	—	—	Fixed	✓
	Signed Binary Fraction Results in Output Bit Width Mismatch	—	—	—	Fixed	✓
	Incorrect Screenshot in the User Guide	—	—	—	Fixed	✓

Table 10–2. FIR Compiler Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version				
		9.1 SP2	9.1 SP1	9.1	9.0	8.1
01 Oct 08	Block Memory Incorrectly Used When Logic Storage Selected	✓	✓	✓	✓	✓
01 Oct 07	Simulation Result Incorrect Using MCV Interpolation Filters	✓	✓	✓	✓	✓
01 May 07	Reloadable Coefficient Filters Fail for Some MCV Filters	✓	✓	✓	✓	✓
01 Dec 06	Quartus II Simulation Vector File Not Generated	✓	✓	✓	✓	✓

FIR Compiler Functional Simulation Model Is Not Generated

When you try to generate a FIR Compiler functional simulation model, one of the following two error messages appears:

"Cannot run program
"*<Quartus II IP installation>*\fir_compiler\lib\ip_toolbench\netlist_writer.exe"
(in directory *<project directory>* create process error=14001
this application has failed to start because the application configuration is incorrect"

or

"IP Functional Simulation Model Creation Failed. The following error was returned: Error: Node instance "fircore" instantiates undefined entity "*<instance_name>*_st" File ..."

and the functional simulation model is not generated.

Affected Configurations

All FIR Compiler variations.

Design Impact

FIR Compiler simulation model is not generated.

Workaround

To avoid this problem, perform the following steps:

1. Download the appropriate version of Microsoft Visual C++ 2008 SP1 Redistributable Package — (×86) for a 32-bit machine or (×64) for 64-bit Windows XP.
2. Double-click on the **vcredisk_x86.exe** or **vcredisk_x64.exe** file you downloaded.
3. Follow the instructions.


If you are prompted to uninstall or repair, click **Repair**.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

FIR Compiler Does Not Support OpenCore Plus for Cyclone IV E Devices

When using the OpenCore Plus evaluation feature, the FIR Compiler does not generate a functional simulation model for Cyclone IV E devices.

Affected Configurations

All FIR Compiler variations that target a Cyclone IV E device.

Design Impact

This issue has no design impact.

Workaround

To avoid this issue, purchase a license for the FIR Compiler.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Cannot Select M9K Data or Coefficient Storage When Device Family is Cyclone III

If you try to set **M9K** for **Data Storage** or **Coefficient Storage** when the **Device Family** is set to **Cyclone III**, an error message reports incorrectly that Cyclone III does not support M9K memory.

Affected Configurations

All FIR Compiler variations that target a Cyclone III device.

Design Impact

You cannot select **M9K** for **Data Storage**.

Workaround

Change the **Device Family** to **Stratix III**, select **M9K** for **Data Storage (**or **Coefficient Storage)**, then change the **Device Family** back to **Cyclone III**.

Solution Status

This issue is fixed in version 9.1 of the FIR Compiler.

Simulation Fails for the Coefficient Reloadable Filters

The reloadable coefficient filters might not produce the right output if you use the IP functional simulation models for simulation.

Affected Configurations

This issue affects the reloadable coefficient filters.

Design Impact

The produced output does not match the expected output.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional

Incorrect results when **Structure** is set to **Distributed Arithmetic: Multi-Bit Serial Filter** or the **Rate Specification** is set to **Interpolation**, and **Signed Binary Fractional** is specified for the data type.

Affected Configurations

Configurations that have a signed binary fractional data type with either a multi-bit structure or an interpolation filter rate specification.

Design Impact

The output data is incorrect.

Workaround

Avoid using a multi-bit serial structure or an interpolation filter rate specification with signed binary fractional data types.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Bit Serial Filter With 32-Bit Coefficients Does Not Work

The generated netlist may be incorrect if the maximum coefficient width is 32.

Affected Configurations

All distributed arithmetic based architectures (fully serial, multi-bit serial, and fully parallel).

Design Impact

The generated netlist is incorrect.

Workaround

Limit the input precision to 31 bits and change the coefficient storage to logic cells. Alternatively, you can use a multicycle variable architecture which gives correct results for 32-bit coefficients.

Solution Status

This issue is fixed in version 9.0 of the FIR Compiler.

Half-Band Decimator and Symmetric Interpolator Do Not Support Unsigned Type

The half-band decimator and symmetric interpolator filters do not support unsigned input data type.

Affected Configurations

This issue affects half-band decimator and symmetric interpolator filter architectures.

Design Impact

The FIR filter produces incorrect results.

Workaround

The half-band decimator and symmetric interpolator filter architectures require signed input data types. To use unsigned data, design the filter with input ports 1-bit larger than the original value and connect the MSB bit of the `ast_sink_data` input port to `0`.

Solution Status

This issue is fixed in version 9.0 of the FIR Compiler.

Signed Binary Fraction Results in Output Bit Width Mismatch

For signed binary fraction data types, some FIR filter variations fail Quartus II compilation and simulation model generation.

Affected Configurations

This issue affects all configurations with signed binary fraction data types.

Design Impact

Compilation fails in the Quartus II software.

Workaround

This issue is related to a user interface issue. In some cases, when you reopen the variation file using IP Toolbench and regenerate the filter, the issue is resolved. If it still fails compilation, use one of the other data types (Signed Binary or Unsigned Binary).

Solution Status

This issue is fixed in version 9.0 of the FIR Compiler.

Incorrect Screenshot in the User Guide

The IP Toolbench screenshot in Figure 2-3 of the user guide is out-of-date and shows the **Display Symbol** option although this feature is no longer supported.

Solution Status

This issue is fixed in version 9.0 of the *FIR Compiler User Guide*.

Block Memory Incorrectly Used When Logic Storage Selected

For some instances of the FIR Compiler MegaCore function, if you select logic-based storage for data and coefficients, it is possible that the results of synthesis may include some block memory.

Affected Configurations

Configurations with FIR storage set to logic elements.

Design Impact

An unwanted block memory is used.

Workaround

Turn off **Auto Shift Register Replacement** in the Quartus II **More Analysis and Synthesis Settings** dialog box. This dialog box can be accessed by clicking **More Settings** in the **Analysis & Synthesis Settings** page of the **Settings** dialog box accessed from the Assignments menu in the Quartus II software.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Simulation Result Incorrect Using MCV Interpolation Filters

Some multicycle variable interpolation filters with high interpolation factors may generate incorrect output.

Affected Configurations

This issue affects MCV interpolation filters with high interpolation factors and forced non-symmetric implementation where the pipelining level is set to greater than 1 for higher f_{MAX}.

Design Impact

The produced output does not match the expected output.

Workaround

Change the pipelining level to 1. This change may result in lower f_{MAX} but the filter output will match the expected output.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Reloadable Coefficient Filters Fail for Some MCV Filters

Some reloadable coefficient filters with multicycle variable architecture do not produce the right output when a new set of coefficients is reloaded.

Affected Configurations

This error is observed in some of the reloadable coefficient MCV filters.

Design Impact

The produced output does not match the expected output when the new coefficient set is reloaded.

Workaround

There are two separate problems which may cause this failure. If your target device is **Cyclone III**, change the device to **Stratix II** or **Stratix III** in the FIR Compiler GUI and regenerate the filter. (Your device selection in the Quartus II project should stay the same.) If the coefficient storage is set to logic cells, change to a block memory (such as **M512**, **M9K**, or **Auto**).

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Quartus II Simulation Vector File Not Generated

FIR Compiler does not create a vector file for Quartus II simulation.

Affected Configurations

This issue affects all configurations.

Design Impact

The design can be compiled, but there is no automatically generated vector file testbench available to simulate the design in the Quartus II software.

Workaround

Use NativeLink to simulate the VHDL testbench instead.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

11. FIR Compiler II

Revision History

Table 11–1 shows the revision history for the FIR Compiler II.

For information about the new features, refer to the *FIR Compiler II User Guide*.

Table 11–1. FIR Compiler II Revision History

Version	Date	Description
9.1 SP1	January 2010	First release.

Errata

Table 11–2 shows the issues that affect the FIR Compiler II v9.1 SP1.

Not all issues affect all versions of the FIR Compiler II.

Table 11–2. FIR Compiler II Errata

Added or Updated	Issue	Affected Version
		9.1 SP1
15 Feb 2010	NativeLink Fails with Verilog Top-Level File	✓
	Simulation Fails with Single-Language Simulator	✓
	M144K Memories Output X's in the ModelSim-Altera Software	✓
	Incorrect Testbench Result When Interpolation Factor Is Greater Than The TDM Factor	✓
	Incorrect Results for a Decimation Configuration	✓
	Incorrect Results Might Be Produced When Input Bit Width is Greater Than 17 bits.	✓
	NativeLink Fails with Riviera-Pro/Active-HDL Simulator	✓
	Simulation fails with the NCSim/Riviera-Pro/ActiveHDL Simulator	✓
	Compiler Does Not Create a Block Symbol File	✓

NativeLink Fails with Verilog Top-Level File

When NativeLink is used to run EDA RTL simulations for verilog top-level file, the simulation fails with the following error message:

```
# ** Error: (vlog-7) Failed to open design unit file "test.vo"
in read mode.
# No such file or directory. (errno = ENOENT)
```

Affected Configurations

This issue affects simulation with Verilog top-level file.

Design Impact

The design does not simulate.

Workaround

Replace the following portion of the generated <*variation*>**.v** file to a single-line code before performing Nativelink simulation:

Remove the following lines:

```
// IPFS_FILES : test.vo
// RELATED_FILES: stratix_components.vhd,
altera_avalon_sc_fifo.v,
auk_dspip_avalon_streaming_controller_hpfir.vhd,
auk_dspip_avalon_streaming_sink_hpfir.vhd,
auk_dspip_avalon_streaming_source_hpfir.vhd,
auk_dspip_math_pkg_hpfir.vhd, auk_dspip_lib_pkg_hpfir.vhd,
test_rtl.vhd, test_rtl_safe_path_flat.vhd, test_ast.vhd, test.v
```

Add the following line:

```
// IPFS_FILES : NONE
```

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Simulation Fails with Single-Language Simulator

When the ModelSim® AE or any single-language simulator is used, the simulation fails because FIR Compiler II is written in both Verilog and VHDL.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Use the `quartus_map` API at the command line to create a simulation model by typing the following command:

```
quartus_map <variant file name> --simgen --
simgen_parameter="CBX_HDL_LANGUAGE=<language>"
language : VHDL / VERILOG
```

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

M144K Memories Output X's in the ModelSim-Altera Software

The simulation fails if the M-RAM memory threshold is set inappropriately.

Affected Configurations

This issue affects all configurations if the M-RAM threshold is set to a small value.

Design Impact

The simulation fails due to the output X's produced by the M144K memories.

Workaround

Set the M-RAM threshold to the default value (for example, set the value to 1000000)

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Incorrect Testbench Result When Interpolation Factor Is Greater Than The TDM Factor

The testbench produces incorrect results when the filter is configured with interpolation factor greater than the TDM factor (the ratio of the clock rate to the sample rate).

Affected Configurations

This issue affects configurations with interpolation factor greater than the TDM factor.

Design Impact

There is no design impact. This is a testbench issue.

Workaround

Set the interpolation factor equals or lesser than the TDM factor.

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Incorrect Results for a Decimation Configuration

Incorrect results are produced when the filter is configured as decimation type with certain parameters.

Affected Configurations

This issue affects the following parameter combination:

- Decimation Factor: 2
- Coefficient Bit Width: 8
- Symmetry Mode: Non Symmetry

Design Impact

The output data is incorrect.

Workaround

Use different coefficient bit width or symmetry mode when you use decimation by two configuration.

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Incorrect Results Might Be Produced When Input Bit Width is Greater Than 17 bits.

Incorrect results might be produced when you set the input bit width other than 1–17 bits.

Affected Configurations

Configurations with input bit width greater than 17 bits.

Design Impact

The output data is incorrect.

Workaround

Set the input bit width within 1–17 bits.

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

NativeLink Fails with Riviera-Pro/Active-HDL Simulator

When NativeLink is used to run simulations in Riviera-Pro or Active-HDL software, the simulation fails with the following error message:

For Riviera-Pro simulator,

```
ACOM: Error: COMP96_0001: Cannot find source file <project
directory>/NONE
```

For Active-HDL simulator,

```
Design: Error: File "<project directory>/NONE" does not exist or
does not have READ permission
```

```
Error: Cannot find library 'work' in the Design Browser
```

Affected Configurations

The design does not simulate.

Design Impact

The output data is incorrect.

Workaround

1. For Riviera-Pro simulator, remove the following line from the **.do** file in *<project directory\simulation\rivierapro>*:

   ```
   acom -93 -dbg <project directory>/NONE
   ```

   For Active-HDL simulator, remove the following line from the **.do** file in *<project directory\simulation\activehdl>*:

   ```
   addfile -c -auto <project directory>/NONE
   ```

2. Locate the following line:

   ```
   asim +access +r -t 1ps -L test -L work -L altera -L lpm -L
   sgate -L altera_mf -L cycloneiii work.<testbench name>
   ```

   and change to:

   ```
   asim +access +r -t 1ps -L test -L altera -L lpm -L sgate -L
   altera_mf -L cycloneiii <testbench name>
   ```

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Simulation fails with the NCSim/Riviera-Pro/ActiveHDL Simulator

When you run design simulations with NCSim/Riviera-Pro/ActiveHDL, the simulations might fail with the following error message on the respective softwares.

```
Verilog module/VHDL port width mismatch -
ALTERA_AVALON_SC_FIFO.OUT_EMPTY. (NCSIM). Length of connection (0)
does not match the length of port "out_empty" (2) on instance.
(Riviera-Pro)

Fatal Error: ELAB2_0051 auk_dspip_avalon_streaming_sink_hpfir.vhd
(525): Length of connection (0) does not match the length of port
"out_empty" (2) on instance (Active-HDL)
```

Affected Configurations

This issue affects configurations with `PHYSCHANIN = 1`.

Design Impact

The design does not simulate.

Workaround

Remove the following lines from **auk_dspip_avalon_streaming_sink_hpfir.vhd**:

```
signal out_empty : OUT STD_LOGIC_VECTOR
(log2_ceil(DATA_PORT_COUNT)-1 DOWNTO 0);

out_empty => open,
```

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Compiler Does Not Create a Block Symbol File

The FIR Compiler II does not automatically create a Block Symbol File (**.bsf**) for the MegaCore function.

Affected Configurations

This issue affects all FIR Compiler II MegaCore function variations.

Design Impact

There is no design impact.

Workaround

In the Quartus II software, open *<variation_name>.<v|vhd>*. From the File menu, select **Create/Update** and then click **Create Symbol Files for Current File** to generate the **.bsf** file. Alternatively, use the `quartus_map` API at the command line to create the symbol file, by typing the following command:

```
quartus_map --generate_symbol=<variation_name>.<v|vhd>
```

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

12. HyperTransport

Revision History

Table 12–1 shows the revision history for the HyperTransport MegaCore function.

For more information about new features, refer to the *HyperTransport MegaCore Function User Guide*.

Table 12–1. HyperTransport MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	■ Maintenance release
9.0	March 2009	■ Maintenance release
8.1	November 2008	■ Maintenance release

Obsolescence Notice

CAUTION

The HyperTransport MegaCore function is scheduled for product obsolescence and discontinued support as described in PDN0906. Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's Intellectual Property website.

Errata

No known issues affect the HyperTransport MegaCore function in v9.1, v9.0, or v8.1.

Revision History

Table 13–1 shows the revision history for the NCO MegaCore function.

For information about the new features, refer to the *NCO MegaCore Function User Guide*.

Table 13–1. NCO MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices ■ Added frequency hopping feature. ■ Removed frequency hopping design example. ■ Withdrawn support for HardCopy family of devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ Preliminary support for Arria II GX. ■ Added frequency hopping design example.
8.1	November 2008	■ Full support for Stratix III. ■ Withdrawn support for UNIX.

Errata

Table 13–2 shows the issues that affect the NCO MegaCore function v9.1, v9.0, and v8.1.

Not all issues affect all versions of the NCO MegaCore function.

Table 13–2. NCO MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
15 Nov 09	Cannot Implement Multiplier-Based Architecture using Multipliers for Arria II GX	Fixed	✓	—
	Resource Estimate Displays LEs Instead of ALUTs for Arria II GX	Fixed	✓	—
15 Mar 09	Warning Message Displayed Twice	✓	✓	—
01 Oct 07	Mismatches Between Multiplier-Based MATLAB and RTL Models	✓	✓	✓
01 May 07	Mismatches Between the MATLAB and RTL Models	✓	✓	✓

Cannot Implement Multiplier-Based Architecture using Multipliers for Arria II GX

You cannot implement a multiplier-based architecture using dedicated multipliers for the Arria II GX device family.

Affected Configurations

Multiplier-based architectures with the target device family set to Arria II GX.

Design Impact

You cannot select the **Use Dedicated Multipliers** option in the **Implementation** tab of the **Parameter Setting** dialog box when the target device family is set to Arria II GX.

Workaround

None.

Solution Status

This issue is fixed in version 9.1 of the NCO MegaCore function.

Resource Estimate Displays LEs Instead of ALUTs for Arria II GX

The **Resource Estimate** tab of the **Parameter Setting** dialog box displays LEs instead ALUTs for the Arria II GX device family.

Affected Configurations

Multiplier-based architectures with the target device family set to Arria II GX.

Design Impact

None.

Workaround

None.

Solution Status

This issue is fixed in version 9.1 of the NCO MegaCore function.

Warning Message Displayed Twice

If you change the **Clock Rate** units to **mHz** in the **Parameter Setting** dialog box a warning message is displayed. After closing the warning message, if you then click on both the **Clock Rate** and the **Desired Output Frequency** boxes, two separate warning messages with the same content are displayed.

Affected Configurations

All configurations.

Design Impact

None.

Workaround

Close both of the warning messages.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Mismatches Between Multiplier-Based MATLAB and RTL Models

For the multiplier-based architecture with throughput = 1 (output every clock cycle), there can be mismatches between the outputs of the MATLAB model and the RTL design for values of magnitude precision. These mismatches seem to be rounding errors for very large values.

Affected Configurations

Multiplier-based architecture with throughput = 1 of the NCO MegaCore function.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is small in both absolute and relative terms. For example, the MATLAB model calculates -536,870,910, whereas the RTL calculates -536,870,911.

Workaround

The RTL design works correctly, but comparison between the MATLAB model and the RTL cannot be done automatically.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Mismatches Between the MATLAB and RTL Models

For the multiplier-based architecture with throughput = ½ (output every 2nd clock cycle), and for the serial CORDIC architecture, there can be mismatches between the outputs of the MATLAB model and the RTL for certain parameter combinations. These mismatches occur because some initial output values are not covered by either the MATLAB model or the RTL design, while the other values match.

Affected Configurations

Multiplier-based architecture with halved throughput and serial CORDIC architectures of the NCO MegaCore function.

Design Impact

Automatic comparison of the output values from the MATLAB model and RTL design during testing may show mismatches.

Workaround

The RTL design works correctly, but comparison between MATLAB model and RTL cannot be done automatically.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

14. Nios II Processor

Revision History

Table 14–1 shows the revision history for the Nios® II Processor MegaCore function.

For more information about the new features, refer to the *Nios II Processor Reference Handbook*. For information about new features and errata in the Nios II Embedded Design Suite, refer to the *Nios II Embedded Design Suite Release Notes and Errata*.

Table 14–1. Nios II Processor Revision History

Version	Date	Description
9.1 SP2	March 2010	Maintenance release
9.1 SP1	January 2010	Maintenance release
9.1	November 2009	■ External Interrupt Controller (EIC) Support ■ The EIC interface—Enables the processor to connect to an EIC ■ Support for multiple register sets (shadow register sets) ■ New fields in status registers: `IL` (Current Interrupt Level), `CRS` (Current register set index), `PRS` (Previous register set index), and `NMI` (nonmaskable interrupt active) ■ Shadow status register (`sstatus`) added ■ New instructions, `rdprs` and `wrprs`, support moving a register value between register sets ■ Status register field names simplified—All status registers use the following field names where implemented: `RSIE`, `NMI`, `PRS`, `CRS`, `IL`, `IH`, `EH`, `U`, and `PIE`. Register-specific field names, such as `EPIE`, are discontinued. This is a documentation change, and has no impact on the Nios II hardware or software.
9.0	March 2009	The `eret` instruction supports returning to different register set. This change is fully compatible with earlier versions of the Nios II processor core and software tools.
8.1	November 2008	Maintenance release

Errata

Table 14–2 shows the issues that affect the Nios II Processor in versions 8.1 through 9.1 SP2.

Not all issues affect all versions of the Nios II Processor.

Table 14–2. Nios II Processor Errata

Added or Updated	Issue	Affected Version				
		9.1 SP2	9.1 SP1	9.1	9.0	8.1
15 May 10	Cannot Implement Multiplier as DSP Block in Cyclone IV Devices	Fixed	✓	✓	—	—
15 Feb 10	HardCopy III and HardCopy IV Support Incorrectly Stated	✓	✓	✓	—	—
15 Nov 09	Design Assistant Error on Clock Signal Source in HardCopy Designs	✓	✓	✓	✓	—
	Hardware Breakpoints Not Supported with Nios II MMU and MPU	—	—	—	Fixed	✓
	Nios II Ports Created Incorrectly	✓	✓	✓	✓	✓
15 Oct 07	Errors Adding Custom Instruction to the Nios II Processor	✓	✓	✓	✓	✓

Cannot Implement Multiplier as DSP Block in Cyclone IV Devices

In the Nios II MegaWizard interface in SOPC Builder, if **Hardware Multiply** is set to **DSP Block**, and the SOPC Builder system is the top-level entity in the Quartus II design, Quartus II compilation fails with an error similar to the following:

```
The design contains 4 blocks of type "Embedded multiplier block" but the
selected device EP4Cxx does not support such blocks
```

DSP Block is an invalid option for **Hardware Multiply** on the Cyclone IV device family.

Affected Configurations

Nios II systems targeting the Cyclone IV device family

Design Impact

On Cyclone IV devices, you must use embedded multipliers to implement hardware multiply.

Workaround

Use embedded multipliers to implement hardware multiply in Cyclone IV designs.

Alternatively, upgrade to v. 9.1 SP2 or later.

Solution Status

Fixed in v. 9.1 SP2

HardCopy III and HardCopy IV Support Incorrectly Stated

In "Device Family Support" in the *Nios II Core Implementation Details* chapter of the *Nios II Processor Reference Handbook*, the "Device Family Support" table incorrectly lists full support for the HardCopy® IV GX and HardCopy III/IV E device families. The Nios II processor provides preliminary support for these device families.

Solution Status

This issue will be fixed in a future release of the *Nios II Processor Reference Handbook*.

Design Assistant Error on Clock Signal Source in HardCopy Designs

When you run the Quartus® II Design Assistant on a HardCopy III or HardCopy IV design, the following error message might appear:

```
Rule C106: Clock signal source should not drive registers that are \
    triggered by different clock edges ; clk ;
```

This error occurs if your HardCopy III or HardCopy IV design incorporates a Nios II/s processor core with a logic element (LE)-based multiplier. Only Stratix® designs can be converted for HardCopy III or HardCopy IV devices. In a Stratix design, it is preferable to implement the multiplier in a DSP block, which provides better performance than an LE-based multiplier.

Affected Configurations

HardCopy III and HardCopy IV designs incorporating the Nios II/s processor core with an LE-based multiplier.

Design Impact

You cannot compile a HardCopy III or HardCopy IV design incorporating the Nios II/s processor core with an LE-based multiplier.

Workaround

Implement the Nios II multiplier with DSP blocks when targeting a HardCopy III or HardCopy IV device.

Solution Status

This issue will be fixed in a future release of the Nios II processor core.

Hardware Breakpoints Not Supported with Nios II MMU and MPU

Enabling the MMU and MPU sets the Nios II instruction and data address to 32 bits. The JTAG debug core, however, leaves the address equal to the size of the Nios II instruction and data master address signals. Because of this address size mismatch, data breakpoints cannot be set on a virtual address when using the MMU, or set on an address outside the address space when using the MPU.

Affected Configurations

Nios II systems with the MMU or MPU enabled.

Workaround

There is no workaround available at this time.

Solution Status

Fixed in v. 9.0

Nios II Ports Created Incorrectly

A threading issue between SOPC Builder and the Nios II MegaWizard™ interface occasionally causes HDL file analysis to fail. This creates all ports as std_logic input with width 1.

Affected Configurations

Nios II processor systems with custom instructions.

Design Impact

Design fails to run in ModelSim®.

Workaround

After adding your custom instruction, close and relaunch SOPC Builder.

Solution Status

Not fixed

Errors Adding Custom Instruction to the Nios II Processor

You might get spurious errors after adding custom instruction slave ports through the Nios II MegaWizard interface.

Affected Configurations

Any Nios II system featuring custom instructions.

Design Impact

No design impact. The error messages are benign.

Workaround

Save your system in SOPC Builder. Close and then relaunch SOPC Builder.

15. PCI Compiler

Revision History

Table 15–1 shows the revision history for the PCI Compiler.

For more information about the new features, refer to the *PCI Compiler User Guide*.

Table 15–1. PCI Compiler Revision History

Version	Date	Description
9.1 SP2	April 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Maintenance release.

Errata

Table 15–2 shows the issues that affect the PCI Compiler v9.1 SP2, 9.1 SP1, 9.1, 9.0 SP2, v9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the PCI Compiler.

Table 15–2. PCI Compiler MegaCore Function Errata

Added or Updated	Issue	Affected Version						
		9.1 SP2	9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Apr 10	Configuration Write to Invalid Address Repeats Continuosly	✓	✓	✓	✓	✓	✓	—
15 Nov 09	Designs With Cyclone III LS Devices Fail to Meet Timing	✓	✓	✓	—	—	—	—
01 Jul 09	Incorrect User Guide on ACDS	—	—	—	Fixed	✓	—	—
15 May 09	F1152 Packages for HardCopy III and HardCopy IV-E Not Supported	✓	✓	✓	✓	✓	—	—
	Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported	✓	✓	✓	✓	✓	—	—
15 Mar 09	Designs With Stratix III Devices Fail to Meet Timing	—	—	—	—	—	Fixed	✓
01 Nov 08	Designs With Stratix IV Devices Fail to Meet Timing	✓	✓	✓	✓	✓	✓	✓

Configuration Write to Invalid Address Repeats Continuosly

A configuration write to an invalid configuration space address causes PCI Compiler to attempt continuous writes, and prevents further PCI reads or writes.

Affected Configuration

All PCI Compiler configurations.

Design Impact

The PCI Compiler continuously repeats the configuration write and does not proceed to the next operation.

Workaround

Make sure that you do not to write to an invalid configuration space address.

Solution Status

This issue will not be fixed.

Designs With Cyclone III LS Devices Fail to Meet Timing

Timing fails when using Cyclone III LS devices with any core combination at 66 MHz.

Affected Configuration

All PCI Compiler designs targeting the Cyclone III LS device family with C8 speed grade, and all PCI Compiler designs targeting the EP3CLS150 or EP3CLS200 devices with C7 speed grade.

Design Impact

The PCI Compiler designs with some Cyclone III LS devices may not meet timing requirements.

Workaround

None.

Solution Status

This issue will not be fixed.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *PCI Compiler User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the PCI Compiler.

F1152 Packages for HardCopy III and HardCopy IV-E Not Supported

PCI Compiler does not support F1152 packages for HardCopy III and HardCopy IV-E.

Affected Configuration

All PCI Compiler configurations using the F1152 packages for HardCopy III and HardCopy IV-E.

Design Impact

The PCI Compiler designs with F1152 packages for HardCopy III and HardCopy IV-E fail to compile.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the PCI Compiler.

Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported

PCI Compiler does not support wirebond packages for HardCopy III and HardCopy IV-E.

Affected Configuration

All PCI Compiler configurations using the wirebond packages for HardCopy III and HardCopy IV-E.

Design Impact

The PCI Compiler designs with wirebond packages for HardCopy III and HardCopy IV-E fail to compile.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the PCI Compiler.

Designs With Stratix III Devices Fail to Meet Timing

Timing fails when using Stratix III devices with any core combination at 66 MHz.

Affected Configuration

All PCI Compiler designs targeting the Stratix III EP3SL340 device family with the slowest speed grade, C4.

Design Impact

The PCI Compiler designs with some Stratix III devices may fail to meet timing.

Workaround

None.

Solution Status

This issue is fixed in version 9.0 of the PCI Compiler.

Designs With Stratix IV Devices Fail to Meet Timing

Timing fails when using Stratix IV devices with any core combination at 66 MHz.

Affected Configuration

All PCI Compiler designs targeting the Stratix IV devices with the slowest speed grade, C4.

Design Impact

The PCI Compiler designs with some Stratix IV devices may fail to meet timing.

Workaround

None.

Solution Status

This issue will not be fixed.

16. PCI Express Compiler

Revision History

Table 16–1 shows the revision history for the PCI Express Compiler.

For complete information about the new features, refer to the *PCI Express Compiler User Guide*.

Table 16–1. PCI Express Compiler Revision History

Version	Date	Description
9.1 SP2	April 2010	■ Maintenance release.
9.1 SP1	February 2010	■ Introduces device support for ×2 PCI Express hard IP in Cyclone® IV GX devices. ■ Adds support for 125 MHz reference clock (in addition to the 100 MHz input reference clock) for Gen1 for Arria® II GX, Cyclone IV GX, HardCopy® IV GX and Stratix® IV GX devices.
9.1	November 2009	■ Introduces device support for the ×1 and ×4 PCI Express hard IP in Cyclone IV GX devices. ■ Support for the Gen1 and Gen2 PCI Express ×1, ×4, and ×8 hard IP MegaCore Function in HardCopy IV GX devices. ■ Support for the Gen1 PCI Express ×1 and ×4 soft IP MegaCore Function in HardCopy IV GX devices. ■ Ability to configure many more parameters of the ALTGX transceiver directly from the PCI Express MegaWizard™ Plug-In Manager interface.
9.0 SP2	July 2009	■ Maintenance release.
9.0 SP1	May 2009	■ Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ Major release. Introduces preliminary support for the Gen1 PCI Express protocol in Arria II GX devices in both the soft and hard IP implementations. ■ Introduces Gen2 support for the PCI Express protocol in a hard IP implementation for Stratix IV GX devices. ■ Introduces support for the Avalon Memory-Mapped (Avalon-MM) interface for the hard IP implementation in SOPC Builder. ■ Introduces reconfiguration block for the hard IP implementation to dynamically update read-only configuration space registers. ■ Provides enhancements to the Altera-provided design example.

Table 16–1. PCI Express Compiler Revision History

Version	Date	Description
8.1	November 2008	■ Major release. Introduces full support for root port designs in the Stratix IV GX devices and full support for endpoint or root port Gen2 ×8 designs in the Stratix IV GX devices. ■ Existing 8.0 PCI Express MegaCore functions targeting Stratix IV GX devices must be regenerated with the PCI Express 8.1 Compiler prior to compilation in the Quartus II software 8.1 or higher. ■ The pinout of the 8.1 variant has changed. When regenerating an 8.0 PCI Express variant with version 8.1 of the PCI Express Compiler, there are two differences in the application signal interface: ▪ There is a new input pin, `gxb_powerdown`. The transceiver calibration module uses `gxb_powerdown` in Stratix II GX, Stratix IV GX, and Arria GX devices. It must be grounded if unused. ▪ The input pin, `aer_msi`, which is only used for the root port variants, has been removed from the top-level of endpoint designs that use the hard IP implementation.

Errata

Table 16–2 shows the issues that affect the PCI Express Compiler in 9.1 SP2, 9.1 SP1, v9.1, v9.0 SP2, v9.0 SP1, v9.0, and v8.1.

Not all issues affect all versions of the PCI Express Compiler.

Table 16–2. PCI Express Compiler Errata (Part 1 of 4)

Added or Updated	Issue	Affected Versions					
		9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Apr 10	MSI Requests not Supported in Completer Only Mode	✓	✓	✓	✓	✓	✓
	Incorrect <variation>_serdes.v(hd) File Produced When Editing an Older PCI Express Variation File	✓	✓	—	—	—	—
15 Feb 10	refclk Cannot Be Used to Generate reconfig_clk	✓	✓	—	—	—	—
	Connecting r2c_err0 or r2c_err1 Output Ports to Your Application Causes Quartus II Compilation to Fail	✓	—	—	—	—	—
	Compilation Fails when Working Directory Name Has a Space	Fixed	✓	—	—	—	—
	MSI-X Capability Structure Not Working in Hardware	Fixed	✓	✓	✓	✓	✓
	PCI Express Compiler User Guide, Version 9.1 Error in Table 1-4, Hard IP Configurations	Fixed	✓	—	—	—	—

Table 16–2. PCI Express Compiler Errata (Part 2 of 4)

Added or Updated	Issue	Affected Versions					
		9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 Nov 09	Timing Analysis for Cyclone IV GX ×1 Variants	✓	✓	—	—	—	—
	Possible Deadlock when Using Back-to-Back Root Port and Endpoint Designs	—	Fixed	✓	✓	✓	✓
	The Upper BAR Address Is Set Incorrectly for 64-Bit BAR	—	Fixed	✓	✓	✓	✓
	×4 and ×8 PCI Express MegaCore Functions Might Downtrain	—	Fixed	✓	✓	✓	✓
	OpenCore Plus Evaluation Not Working for Soft IP Implementation in Arria II GX	—	Fixed	✓	—	—	—
	PCI Express Soft IP MegaCore Function Does Not Train to L0	—	Fixed	✓	✓	—	—
15 Nov 09	The tx_cred Signal Indicates Incorrect Non-Posted Credits Available in Hard IP Implementation	—	Fixed	✓	✓	✓	✓
	When Using the Avalon-MM interface, Disabling the Master Bus Does Not Stop Requests	—	Fixed	✓	✓	✓	✓
	An Error Might Occur in Logging a Poisoned TLP	—	Fixed	✓	✓	✓	✓
	PCI Express Compiler User Guide Provides Incorrect Speed Grade Information for Gen1	—	Fixed	✓	✓	✓	—
	Description of the Completion Side Band Signals and Error Handling in the PCI Express Compiler User Guide is Incomplete	—	Fixed	✓	✓	✓	✓
	The Receive Direction Transaction Layer Routing Rules are Incomplete in PCI Express Compiler User Guide	—	Fixed	✓	✓	✓	✓
	Gate-Level Simulation Fails for Hard IP Variations	—	Fixed	✓	✓	✓	—
	Incorrect Link Training for Stratix IV GX ES Gen2 ×8 Hard IP Implementation	—	Fixed	✓	✓	✓	✓
	Timing Closure for Chaining DMA Design Example Gen1×8 in Stratix IV C3 and C4 Speed Grades	—	Fixed	✓	✓	✓	✓
	The Description of cfg_devcsr[31:0] in the PCI Express Compiler User Guide is Incorrect	—	Fixed	✓	✓	✓	✓
	Compiler Does Not Create a Block Symbol File	—	Fixed	✓	✓	✓	✓
01 Jul 09	Hard IP Implementation Returns 0x00 when the Interrupt Pin Register Is Read	—	—	Fixed	✓	✓	✓
	The tx_cred Signal Indicates Incorrect Non-Posted Credits Available for the Soft IP Implementation	—	—	Fixed	✓	✓	✓
	Base Address Register (BAR) Expansion ROM Not Working Correctly	—	—	Fixed	✓	✓	✓
15 May 09	A ×1 or ×4 Soft IP Variation Might Incorrectly Issue a NAK	—	—	—	Fixed	✓	✓
	The ×8 Soft IP Implementation of PCI Express MegaCore Function Only Supports 4 KByte Expansion ROM BAR	—	—	—	Fixed	✓	✓

Table 16–2. PCI Express Compiler Errata (Part 3 of 4)

Added or Updated	Issue	Affected Versions					
		9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
	You Cannot Use the MegaWizard Plug-In Manager to Edit the SERDES in the Hard IP Implementation of the PCI Express MegaCore Function	—	—	—	Fixed	✓	
15 Mar 09	Guidelines for Passing the PCI Express Electrical Gold Test on the v2.0 Compliance Base Board (CBB)	—	✓	✓	✓	✓	—
	Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0	—	✓	✓	✓	✓	✓
	Endpoints Using the Soft IP Implementation Incorrectly Handle CfgRd0	—	—	—	—	Fixed	✓
	The Hard IP Implementation of the PCI Express Compiler May Be Unable to Exit the Disable State at the Gen2 Rate	—	—	Fixed	✓	✓	—
15 Mar 09	Adding Two PCI Express Components to an SOPC Builder System May Cause a System Error	✓	✓	✓	✓	✓	✓
	License File for Soft IP Implementation of the PCI Express Compiler Does Not Work	—	—	—	—	Fixed	✓
	EDA Netlist Writer Does Not Write Netlist for Hard IP Implementation of PCI Express	—	—	—	—	Fixed	✓
	Stratix IV Projects with Pin Assignments Specified Using the Pin Planner May Fail Quartus II Compilation	—	—	—	—	Fixed	✓
	Simulation Fails when Using ModelSim AE for Stratix II GX MegaCore Functions with the Avalon-ST or Descriptor/Data Interfaces	—	—	—	—	Fixed	✓
	The Chaining DMA Design Example May Issue DMA Write Requests that Violate the 4 KByte Boundary Rule in the VHDL Version	—	—	—	—	Fixed	✓
	Design Example in Hardware Might Require the RC Slave Module	—	—	—	—	Fixed	✓
	Root Port BFM in Version 8.1 of the PCI Express Testbench is not Backwards Compatible	—	—	—	—	Fixed	✓
01 Nov 08	Incorrect Connection of SOPC Builder Interrupt Sources to PCI Express Components	✓	✓	✓	✓	✓	✓
	PCI Express Avalon-MM Tx Interface Deadlocks on a Read Request	—	—	—	—	—	Fixed
	Unable to Compile the Example Design Successfully in Quartus II when using ECRC Forwarding	—	—	—	—	—	Fixed
15 Aug 08	Chaining DMA Design Example Forwards Tx ECRC with Incorrect Alignment	—	—	—	—	—	Fixed

Table 16–2. PCI Express Compiler Errata (Part 4 of 4)

Added or Updated	Issue	Affected Versions					
		9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 Jul 08	User Guide Incorrectly Documents the Number of Address Pages	—	—	—	—	—	Fixed
	User Guide Incorrectly Documents rx_st_data and tx_st_data in 128-Bit Mode	—	—	—	—	—	Fixed
	Address Translation Update Can Corrupt Outstanding Reads for MegaCore Functions Created in SOPC Builder	—	—	—	—	Fixed	✓
	User Guide, Version 8.0 Swapped Descriptions of cpl_err[4] and cpl_err[5]	—	—	—	—	—	Fixed
15 May 08	MegaWizard Interface Displays Incorrect Values	—	—	—	—	—	Fixed

MSI Requests not Supported in Completer Only Mode

When you configure the PCI Express MegaCore function in **Completer Only** mode, if an MSI is sent by asserting an interrupt, any subsequent reads returns all zeros.

Affected Configuration

This issue affects variants that use the Avalon-MM interface and select **Completer Only** mode on the **Avalon Configuration** tab.

Workaround

Configure your MegaCore function in **Requester/Completer** mode.

Solution Status

This issue will be fixed in a future version of the PCI Express MegaCore function.

Incorrect <variation>_serdes.v(hd) File Produced When Editing an Older PCI Express Variation File

If you use PCI Express Compiler version 9.1 or later to edit a PCI Express Compiler variation that was created with Quartus II version 9.0 SP2 or earlier, a corrupted **<*variation*>_serdes.v** (or **<*variation*>_serdes.vhd**) file is created. This corrupt file leads to errors when trying to simulate or compile the PCI Express variation.

Workaround

Before editing the variation with the newer PCI Express Compile version, delete the **<*variation*>_serdes.v** (or **<*variation*>_serdes.vhd**) file. If you had modified any settings in the SERDES file, re-enter them in PCI Express Compiler using the **Configure Transceiver Block** button on the **System Settings** tab.

Solution Status

This issue will not be fixed in a future version of PCI Express Compiler.

refclk Cannot Be Used to Generate reconfig_clk

Due to changes to the dynamic reconfiguration IP, you can no longer use the `refclk` pin directly or indirectly to generate the reconfiguration clock (`reconfig_clk`). The example design generated by PCI Express Compiler in the affected versions incorrectly uses the `refclk`.

Affected Configurations

This issue affects implementations of the PCI Express MegaCore function in Stratix IV GX/GT and Arria II GX devices.

Workaround

There are two solutions to this issue:

- Use a free running clock from a non-transceiver IO clock pin that is stable at device power up.
- Use a GPLL to generate the `reconfig_clk` sourced from an IO clock pin.

For more information refer to *Altera Solution rd12172009_302*.

Solution Status

A future version of PCI Express Compiler will be changed to generate an example design that uses a different clock.

Connecting r2c_err0 or r2c_err1 Output Ports to Your Application Causes Quartus II Compilation to Fail

Adding the speed negotiation signals, `r2c_err0` and `r2c_err1`, to your PCI Express MegaCore function causes Quartus II compilation to fail.

Affected Configurations

This issue affects PCI Express designs in Stratix IV GX, HardCopy IV GX, and Arria II GX devices.

Workaround

Leave the output signals, `r2c_err0` and `r2c_err1`, unconnected.

Solution Status

This issue will be fixed in a future version of the Quartus II Compiler.

Compilation Fails when Working Directory Name Has a Space

Compilation of the PCI Express Compiler MegaCore function fails if the working directory name includes a space.

Affected Configurations

This issue affects all versions of the PCI Express MegaCore function that are compiled using version 9.1 of the Quartus II software.

Workaround

Do not include spaces in the working directory name.

Solution Status

This issue is fixed in version 9.1 SP1 of the Quartus II software.

MSI-X Capability Structure Not Working in Hardware

The MSI-X capability structure simulates correctly but is incorrect in the actual hardware for hard IP implementations of the PCI Express MegaCore function.

Affected Configurations

This is an Assembler issue that affects all hard IP PCI Express MegaCore functions in Stratix IV GX, Arria II GX and Cyclone IV GX devices.

Workaround

The workaround is to download and install Quartus II 9.1 software patch described in the following solution.

http:/www.altera.com/support/kdb/solutions/rd11172009_89.html

Solution Status

This issue is fixed in version 9.1 SP1 of the Quartus II software.

PCI Express Compiler User Guide, Version 9.1 Error in Table 1-4, Hard IP Configurations

Table 1-4 in the *PCI Express Compiler User Guide* breaks across two pages. The Avalon-ST heading is erroneously repeated on the second page; however, the Avalon-MM applies to the devices listed on the second page of this table. The correct table is given below.

Table 16–3. PCI Express Hard IP Configurations for the PCI Express Compiler in 9.1 (Part 1 of 2)

Device	Link Rate (Gbps)	×1	×4	×8
Avalon Streaming (Avalon-ST) Interface using MegaWizard Plug-In Manager Design Flow				
Stratix IV GX	2.5	yes	yes	yes
	5.0	yes	yes	yes
Arria II GX	2.5	yes	yes	yes *(1)*
	5.0	no	no	no
Cyclone IV GX	2.5	yes	yes	no
	5.0	no	no	no
HardCopy IV GX	2.5	yes	yes	yes
	5.0	yes	yes	yes
Avalon-MM Interface using SOPC Builder Design Flow				
Stratix IV GX	2.5	yes	yes	no
	5.0	yes	no	no

Table 16–3. PCI Express Hard IP Configurations for the PCI Express Compiler in 9.1 (Part 2 of 2)

Device	Link Rate (Gbps)	×1	×4	×8
Arria II GX	2.5	yes	yes	no
	5.0	no	no	no
Cyclone IV GX	2.5	yes	yes	no
	5.0	no	no	no

Note to Table 16–3:

(1) The ×8 support uses a 128-bit bus at 125 MHz.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue will be fixed in version 91. SP1 of the *PCI Express Compiler User Guide*.

Timing Analysis for Cyclone IV GX ×1 Variants

The Quartus II software does not perform timing analysis for the FPGA fabric in Cyclone IV GX ×1 variants; consequently, variants that would fail timing analysis are not identified.

Affected Configurations

This issue affects ×1 variants in the Cyclone IV GX device.

Workaround

You can manually create the required clock constraint. Example 16–1 provides the equation for this constraint. In this equation <*n*> is 8.000 for a 125 MHz application clock and 16 for a 62.5 MHz application clock.

Example 16–1. Clock Constraint for

```
# create_clock -name {core_clk_out} -period <n> -waveform { 0.000 8.000 } [get_nets
{*altpcie_hip_pipen1b_inst | core_clk_out~clkctrl}]
```

Solution Status

This issue will be fixed in a future release of the Quartus II software.

Possible Deadlock when Using Back-to-Back Root Port and Endpoint Designs

In Gen2 PCI Express designs that create a back-to-back connection between a hard IP root port to a hard IP endpoint, neither device transmits data to establish the link, resulting in a deadlock.

Affected Configurations:

This issue affects a back-to-back link between a Gen2 ×4 and Gen2 ×8 root port and endpoint designs that use the recommended reset circuitry for the Gen2 hard IP implementation. The recommended circuitry holds the PCI Express MegaCore function in reset until successful reception of a correct pattern on each lane. (The recommended reset circuitry is implemented in programmable logic and is not part of the hard IP implementation.)

Workaround

To prevent deadlock, you can temporarily force one end of the link into compliance mode until the other end completes its reset cycle.

Solution Status

This issue is fixed in version 9.1 of the PCI Express MegaCore function.

The Upper BAR Address Is Set Incorrectly for 64-Bit BAR

When using a 64-bit BAR, the upper BAR address is set incorrectly, preventing the operating system from correctly configuring a 64-bit address.

Affected Configurations:

This issue affects PCI Express MegaCore functions that use a 64-bit BAR in Arria II GX and Stratix IV GX devices.

Workaround

If possible, use a 32-bit BAR or update your design to use the PCI Express compiler version 9.1.

Solution Status

This issue is fixed in the Quartus II software, release 9.1.

×4 and ×8 PCI Express MegaCore Functions Might Downtrain

The ×4 and ×8 variants of PCI Express MegaCore function in Arria II GX and Stratix IV GX devices might downtrain. Downtraining is caused by miscommunication of the reset signals between the PCI Express MegaCore function and ALTGX transceiver.

Affected Configurations:

This issue affects ×4 and ×8 PCI Express MegaCore functions in Arria II GX and Stratix IV GX devices.

Workaround

The workaround is to download the Quartus II 9.1 software.

Solution Status

This issue is fixed in the Quartus II software, release 9.1.

OpenCore Plus Evaluation Not Working for Soft IP Implementation in Arria II GX

OpenCore Plus Evaluation does not work for the PCI Express soft IP MegaCore function in 9.0 SP2 for the Arria II GX device.

Affected Configurations

This issue affects the soft IP implementation of the PCI Express MegaCore function for the Arria II GX device.

Workaround

There is no workaround other than buying a license for the PCI Express MegaCore function or targeting a different device.

Solution Status

This issue is fixed in the Quartus II software, release 9.1.

PCI Express Soft IP MegaCore Function Does Not Train to L0

The PCI Express soft IP MegaCore function does not train to L0s for Arria II GX and Stratix IV GX.

Affected Configurations

This issue affects the soft IP implementation of the PCI Express MegaCore function in Arria II GX and Stratix IV GX devices in the Quartus II 9.0 SP1 release.

Workaround

On the **Protocol Settings** page of the ALTGX Megawizard interface, do not turn on **Enable low latency synchronous PCI Express (PIPE)**.

Solution Status

This issue is fixed in version 9.1 of the Quartus II software.

The tx_cred Signal Indicates Incorrect Non-Posted Credits Available in Hard IP Implementation

For the Avalon Streaming (Avalon-ST) interface the `tx_cred` bus fields that indicate the available non-posted data credits (`tx_cred[20:18]`) and non-posted header credits (`tx_cred[17:15]`) can falsely indicate zero available credits when there really are credits available.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function.

Workaround

You can disregard the `tx_cred` signal for non-posted header/data. The PCI Express Megacore function always does an accurate check of the available Tx credits available before starting transmission of a transaction layer packet (TLP) in order to obey the flow control protocol. If transmission of a TLP is held due to a lack of credits, the `tx_st_ready` signal will be deasserted.

Solution Status

This issue is fixed version 9.1 of the PCI Express MegaCore function.

When Using the Avalon-MM interface, Disabling the Master Bus Does Not Stop Requests

For PCI Express MegaCore functions using the Avalon-MM interface, clearing the bus master enable bit (bit 2 of the type 0 configuration space register at address 0x4), does not prevent the SOPC Builder endpoint from issuing upstream transactions.

Affected Configurations

This issue affects PCI Express MegaCore functions that use the Avalon-MM interface.

Workaround

Do not allow the software application to disable the master bus.

Solution Status

This issue is fixed in a version 9.1 of the PCI Express MegaCore function.

An Error Might Occur in Logging a Poisoned TLP

When there is a poisoned TLP and automatic error reporting (AER) is enabled and the error is not masked, an error can occur in logging the poisoned TLP into the header log of the AER capability structure. The error occurs if there is an additional incoming packet immediately behind the poisoned TLP. When the error occurs, the TLP header long will be corrupt.

Affected Configurations

This issue affects all variants of the PCI Express MegaCore function when AER is enabled.

Workaround

You can mask the poisoned TLP error type so that it is not included in the error log. Alternatively, you can ignore the poisoned TLP errors that are logged.

Solution Status

This issue is fixed in the release 9.1 of the PCI Express MegaCore function.

PCI Express Compiler User Guide Provides Incorrect Speed Grade Information for Gen1

Version 9.0 of the *PCI Express Compiler User Guide* incorrectly states that the Stratix IV GX hard IP Gen1 PCI Express MegaCore function is not available in the –4 speed grade; however, the PCI Express MegaCore function is available in the –4 speed grade for Gen1 variants.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 9.1 of the *PCI Express Compiler User Guide*.

Description of the Completion Side Band Signals and Error Handling in the PCI Express Compiler User Guide is Incomplete

The descriptions of the `cpl_err` signals in "Completion Side Band Signals" on page 5–34 is incomplete. In addition, the definition of completer abort in Table4-36 on page 4-54 specifies the wrong bit of the `cpl_err` vector. This error is reported on `cpl_error`. The complete and corrected descriptions are given below.

Transaction Layer

Table 16–4 describes errors detected by the transaction layer.

Table 16–4. Errors Detected by the Transaction Layer (Part 1 of 3)

Error	Type	Description
Poisoned TLP received	Uncorrectable (non-fatal)	This error occurs if a received transaction layer packet has the EP poison bit set. The received TLP is presented passed to the application and the application layer logic must take application appropriate action in response to the poisoned TLP. In PCI Express 1.1, this error is treated as an advisory error.
ECRC check failed *(1)*	Uncorrectable (non-fatal)	This error is caused by an ECRC check failing despite the fact that the transaction layer packet is not malformed and the LCRC check is valid. The MegaCore function handles this transaction layer packet automatically. If the TLP is a non-posted request, the MegaCore function generates a completion with completer abort status. In all cases the TLP is deleted in the MegaCore function and not presented to the application layer.

Table 16–4. Errors Detected by the Transaction Layer (Part 2 of 3)

Error	Type	Description
Unsupported request	Uncorrectable (non-fatal)	This error occurs whenever a component receives any of the following unsupported requests: ■ Completion transaction for which the requester ID does not match the bus/device. ■ Unsupported message. ■ A type 1 configuration request transaction layer packet for the TLP from the PCIe link. ■ A locked memory read (MEMRDLK) on native endpoint. ■ A locked completion transaction. ■ A 64-bit memory transaction in which the 32 MSBs of an address are set to 0. ■ A memory or I/O transaction for which there is no BAR match. ■ A poisoned configuration write request (CfgWr0) If the TLP is a non-posted request, the MegaCore function generates a completion with unsupported request status. In all cases the TLP is deleted in the MegaCore function and not presented to the application layer.
Completion timeout	Uncorrectable (non-fatal)	This error occurs when a request originating from the application layer does not generate a corresponding completion transaction layer packet within the established time. It is the responsibility of the application layer logic to provide the completion timeout mechanism. The completion timeout should be reported from the transaction layer using the `cpl_err[0]` signal.
Completer abort *(1)*	Uncorrectable (non-fatal)	The application layer reports this error using the `cpl_err[2]`signal when it aborts receipt of a transaction layer packet.
Unexpected completion	Uncorrectable (non-fatal)	This error is caused by an unexpected completion transaction. The MegaCore function handles the following conditions: ■ The requester ID in the completion packet does not match the configured ID of the endpoint. ■ The completion packet has an invalid tag number. (Typically, the tag used in the completion packet exceeds the number of tags specified.) ■ The completion packet has a tag that does not match an outstanding request. ■ The completion packet for a request that was to I/O or configuration space has a length greater than 1 dword. ■ The completion status is Configuration Retry Status (CRS) in response to a request that was not to configuration space. In all of the above cases, the TLP is not presented to the application layer; the MegaCore function deletes it. Other unexpected completion conditions can be detected by the application layer and reported through the use of the `cpl_err[2]` signal. For example, the application layer can report cases where the total length of the received successful completions do not match the original read request length.

Table 16–4. Errors Detected by the Transaction Layer (Part 3 of 3)

Error	Type	Description
Receiver overflow *(1)*	Uncorrectable (fatal)	This error occurs when a component receives a transaction layer packet that violates the FC credits allocated for this type of transaction layer packet. In all cases the MegaCore function deletes the TLP and it is not presented to the application layer.
Flow control protocol error (FCPE) *(1)*	Uncorrectable (fatal)	This error occurs when a component does not receive update flow control credits within the 200 Ωs limit.
Malformed TLP	Uncorrectable (fatal)	This error is caused by any of the following conditions: ■ The data payload of a received transaction layer packet exceeds the maximum payload size. ■ The TD field is asserted but no transaction layer packet digest exists, or a transaction layer packet digest exists but the TD bit of the PCI Express request header packet is not asserted. ■ A transaction layer packet violates a byte enable rule. The MegaCore function checks for this violation, which is considered optional by the PCI Express specifications. ■ A transaction layer packet in which the type and length fields do not correspond with the total length of the transaction layer packet. ■ A transaction layer packet in which the combination of format and type is not specified by the PCI Express specification. ■ A request specifies an address/length combination that causes a memory space access to exceed a 4 KByte boundary. The MegaCore function checks for this violation, which is considered optional by the PCI Express specification. ■ Messages, such as Assert_INTx, power management, error signaling, unlock, and Set_Slot_power_limit, must be transmitted across the default traffic class.
Malformed TLP (cont)	Uncorrectable (fatal)	■ A transaction layer packet that uses an uninitialized virtual channel. The MegaCore function deletes the malformed TLP; it is not presented to the application layer.

Note to Table 16–4:

(1) Considered optional by the *PCI Express Base Specification Revision 1.0a, 1.1 or 2.0*.

Completion Side Band Signals

Table 16–5 describes the signals that comprise the completion side band for the Avalon-ST interface. The MegaCore function provides a completion error interface that the application can use to report errors, such as programming model errors, to it. When the application detects an error, it can assert the appropriate cpl_err bit to tell the MegaCore function what kind of error to log. The MegaCore function sets the appropriate status bits for the error in the configuration space, and automatically sends error messages in accordance with the *PCI Express Base Specification*. Note that the application is responsible for sending the completion with the appropriate completion status value for non-posted requests. Refer to "Error Handling" on page 4-53 for information on errors that are automatically detected and handled by the MegaCore Function.

Table 16–5. Completion Signals for Avalon-ST (Part 1 of 2)

Signal	I/O	Description
cpl_err[6:0]	I	Completion error. This signal reports completion errors to the configuration space. When an error occurs, the appropriate signal is asserted for one cycle. ■ cpl_err[0]: Completion timeout error with recovery. This signal should be asserted when a master-like interface has performed a non-posted request that never receives a corresponding completion transaction after the 50 ms timeout period when the error is correctable. The MegaCore function automatically generates an advisory error message that is sent to the root complex. ■ cpl_err[1]: Completion timeout error without recovery. This signal should be asserted when a master-like interface has performed a non-posted request that never receives a corresponding completion transaction after the 50 ms time-out period when the error is not correctable. The MegaCore function automatically generates a non-advisory error message that is sent to the root complex. ■ cpl_err[2]:Completer abort error. The application asserts this signal to respond to a posted or non-posted request with a completer abort (CA) completion. In the case of a non-posted request, the application generates and sends a completion packet with completer abort (CA) status to the requestor and then asserts this error signal to the MegaCore function. The MegaCore function automatically sets the error status bits in the configuration space register and sends error messages in accordance with the *PCI Express Base Specification*.
		■ cpl_err[3]:Unexpected completion error. This signal must be asserted when an application layer master block detects an unexpected completion transaction. Many cases of unexpected completions are detected and reported internally by the transaction layer of the MegaCore function. For a list of these cases, refer to "Errors Detected by the Transaction Layer" on page 4-54. ■ cpl_err[4]: Unsupported request error for posted TLP. The application asserts this signal to treat a posted request as an unsupported request (UR). The MegaCore function automatically sets the error status bits in the configuration space register and sends error messages in accordance with the *PCI Express Base Specification*. Many cases of unsupported requests are detected and reported internally by the transaction layer of the MegaCore function. For a list of these cases, refer to "Errors Detected by the Transaction Layer" on page 4-54. ■ cpl_err[5]: Unsupported request error for non-posted TLP. The application asserts this signal to respond to a non-posted request with an unsupported request (UR) completion. In this case, the application sends a completion packet with the unsupported request status back to the requestor, and asserts this error signal to the MegaCore function. The MegaCore automatically sets the error status bits in the configuration space register and sends error messages in accordance with the *PCI Express Base Specification*. Many cases of unsupported requests are detected and reported internally by the transaction layer of the MegaCore function. For a list of these cases, refer to "Errors Detected by the Transaction Layer" on page 4-54.

Table 16–5. Completion Signals for Avalon-ST (Part 2 of 2)

Signal	I/O	Description
		■ cpl_err[6]: Log header. When asserted, logs err_desc_func0 header. Used in both the soft IP and hard IP implementation of the MegaCore function that use the Avalon-ST interface. When asserted, the TLP header is logged in the AER header log register if it is the first error detected. When used, this signal should be asserted at the same time as the corresponding cpl_err error bit (2, 3, 4, or 5). In the soft IP implementation, the application presents the TLP header to the MegaCore function on the err_desc_func0 bus. In the hard IP implementation, the application presents the header to the MegaCore function by writing the following values to 4 LMI registers before asserting cpl_err[6]: →lmi_addr: 12'h81C, lmi_din: err_desc_func0[127:96] →lmi_addr: 12'h820, lmi_din: err_desc_func0[95:64] →lmi_addr: 12'h824, lmi_din: err_desc_func0[63:32] →lmi_addr: 12'h828, lmi_din: err_desc_func0[31:0] Refer to the *LMI Signals—HARD IP Implementation* in the *PCI Express Compiler User Guide* for more information about LMI signalling. For the ×8 soft IP, only bits [3:1] of cpl_err are available. For the ×1, ×4 soft IP implementation and all widths of the hard IP implementation, all bits are available.
err_desc_func0 [127:0]	I	TLP Header corresponding to a cpl_err. Logged by the MegaCore function when cpl_err[6] is asserted. This signal is only available for the ×1 and ×4 soft IP implementation. In the hard IP implementation, this information can be written to the AER header log register through the LMI interface. If AER is not implemented in your variation this signal bus should be tied to a constant value, for example all 0's.
cpl_pending	I	Completion pending. The application layer must assert this signal when a master block is waiting for completion, for example, when a transaction is pending. If this signal is asserted and low power mode is requested, the MegaCore function waits for the deassertion of this signal before transitioning into low-power state.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 9.1 of the *PCI Express Compiler User Guide*.

The Receive Direction Transaction Layer Routing Rules are Incomplete in PCI Express Compiler User Guide

The *Transaction Layer Routing Rules* given for the *receive direction* in the *PCI Express Compiler User Guide* are incomplete. The complete text is given below.

In the receive direction (from the PCI Express link), memory and I/O requests that match the defined base address register (BAR) contents and vendor-defined messages with or without data route to the receive interface. The application layer logic processes the requests and generates the read completions, if needed.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 9.1 of the *PCI Express Compiler User Guide*.

Gate-Level Simulation Fails for Hard IP Variations

Due to simulation model issues running a post-compilation gate-level simulation of the PCI Express hard IP MegaCore function variations fails, stating incorrectly that the link does not train.

Affected Configurations

This issue affects the hard IP implementation of PCI Express MegaCore functions in the 9.0 release.

Workaround

Use the IP Functional Simulation models for simulation.

Solution Status

This issue is fixed in version 9.1 of the Quartus II software.

Incorrect Link Training for Stratix IV GX ES Gen2 ×8 Hard IP Implementation

The current clock distribution architecture in the Stratix IV GX ES silicon SERDES block could yield excessive inter-quad clock skew which prevents the link from training to Gen2 ×8. The link may train to Gen2 ×4.

For more details on the inter-quad clock skew issue, refer to the "PCI Express Gen2 ×8 functional mode with hard IP using CMU PLL or ATX PLL" heading in the "×8 and ×N Clock Line Timing Issue for Transceivers" section in the *Stratix IV GX ES Errata Sheet*.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express Compiler in Stratix IV GX ES devices.

Workaround

The following possible workarounds are available:

- Replace you ES Device with production devices.

- Contact Altera Support for additional possible work arounds.

Solution Status

This issue is fixed in Stratix IV GX production devices.

Timing Closure for Chaining DMA Design Example Gen1×8 in Stratix IV C3 and C4 Speed Grades

When compiling the PCI Express Gen1 ×8 chaining DMA design example for the C3 and C4 speed grades of the Stratix IV family, the design fails to meet timing requirements.

Affected Configurations

This issue affects the C3 and C4 speed grades of the Stratix IV device family.

Workaround

Add the constraints in Example 16–2 to your Quartus II Settings File (**.qsf**) if you are compiling the chaining DMA design example for 250 MHz operation in the slower speed grades of the Stratix IV family.

Example 16–2. Constraints for C3 and C4 Speed Grade for Stratix IV Family

```
set_global_assignment -name OPTIMIZATION_TECHNIQUE SPEED
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC ON
set_global_assignment -name PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION ON
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC_FOR_AREA ON
set_instance_assignment -name DUPLICATE_ATOM srst_duplicate -from
"top_example_chaining_pipen1b:core|srst" -to
"top_example_chaining_pipen1b:core|top:epmap"
set_instance_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS OFF -to
"top_example_chaining_pipen1b:core|srst"
set_instance_assignment -name PRESERVE_REGISTER ON -to
"top_example_chaining_pipen1b:core|altpcierd_example_app_chaining:app|srst"
set_instance_assignment -name PRESERVE_REGISTER ON -to
"top_example_chaining_pipen1b:core|crst"
set_instance_assignment -name PRESERVE_REGISTER ON -to
"top_example_chaining_pipen1b:core|srst"
```

Solution Status

This issue is fixed in version 9.1 of the Quartus II software.

The Description of cfg_devcsr[31:0] in the PCI Express Compiler User Guide is Incorrect

Table 5-17 of the *PCI Express Compiler User Guide* incorrectly states that `cfg_devcsr[31:16]` is the device control field and `cfg_devcsr[15:0]` is the device status field. The opposite is true. `cfg_devcsr[31:16]` is the device status field and `cfg_devcsr[15:0]` is the device control field.

Affected Configurations

This issue affects versions 8.1 and 9.0 of the *PCI Express Compiler User Guide*.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 9.1 of the *PCI Express Compiler User Guide*.

Compiler Does Not Create a Block Symbol File

The PCI Express Compiler does not automatically create a Block Symbol File (**.bsf**) for the PCI Express MegaCore function.

Affected Configurations

This issue affects all PCI Express MegaCore function variations in 8.0.

Workaround

You can use the Quartus II Block Editor to manually create a **.bsf** for the variation. Alternatively, you can use the `quartus_map` API at the command line to create a symbol, by typing the following command:

`quartus_map --generate_symbol=`*<variation_name>*`.`*<v|vhd>* *<quartus II project name>*

Solution Status

This is fixed in version 9.1 of the Quartus II software.

Hard IP Implementation Returns 0x00 when the Interrupt Pin Register Is Read

For hard IP implementations of the PCI Express MegaCore function, when software reads the configuration space interrupt pin register, offset 0x3d, a value of 0x00 is returned instead of 0x01 which indicates legacy interrupt INTA is used by this function.

Affected Configurations

This issue affects hard IP implementations of the PCI Express compiler in the Stratix IV and Arria II GX device families.

Workaround

If possible, software should ignore the value returned with the interrupt pin register is read and assume a value of 0x01 instead. Alternatively, the register value can be altered by using the PCI Express reconfiguration block. Refer to the "PCI Express Reconfiguration Block" section of the *PCI Express Compiler User Guide*. Specifically, as noted in Table 4-9, the interrupt pin register value is set by bits [3:1] at address 0x97 of the PCI Express reconfiguration block.

Solution Status

This issue is fixed in version 9.0 SP2 of the Quartus II software.

The tx_cred Signal Indicates Incorrect Non-Posted Credits Available for the Soft IP Implementation

For the Avalon Streaming (Avalon-ST) interface the `tx_cred` bus fields that indicate the available non-posted data credits (`tx_cred[20:18]`) and non-posted header credits (`tx_cred[17:15]`) can falsely indicate zero available credits when there really are credits available.

Affected Configurations

This issue affects the soft IP implementation that uses the Avalon-ST interface.

Workaround

You can disregard the `tx_cred` signal for non-posted header/data. The PCI Express Megacore function always does an accurate check of the available Tx credits available before starting transmission of a transaction layer packet (TLP) in order to obey the flow control protocol. If transmission of a TLP is held due to a lack of credits, the `tx_st_ready` signal will be deasserted.

Solution Status

This issue is fixed for the soft IP implementation in Quartus II Release 9.0 SP2.

Base Address Register (BAR) Expansion ROM Not Working Correctly

The BAR Expansion ROM is not working correctly in hardware for the hard IP implementation of the PCI Express MegaCore function in the Stratix IV GX and Arria II GX devices.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function in Stratix IV GX and Arria II GX devices.

Workaround

There is no workaround for this issue.

Solution Status

This issue is fixed for the soft IP implementation in Quartus II Release 9.0 SP2.

A ×1 or ×4 Soft IP Variation Might Incorrectly Issue a NAK

In some unusual circumstances, a ×1 soft IP implementation of the PCI Express MegaCore function or a ×4 soft IP implementation used in a ×1 slot or it might incorrectly issue a NAK to a valid TLP which has no LCRC error or framing error.

Affected Configurations

This issue affects the ×1 soft IP implementation of the PCI Express MegaCore function or a ×4 MegaCore function is plugged into a ×1 slot.

Workaround

There is no workaround.

Resolution

This issue is fixed in Release 9.0 SP1 of the PCI Express Compiler.

The ×8 Soft IP Implementation of PCI Express MegaCore Function Only Supports 4 KByte Expansion ROM BAR

The ×8 soft IP implementation of the PCI Express MegaCore function only supports a 4 KByte expansion ROM BAR; however, the MegaWizard Plug-In Manager erroneously allows the selection of all **BAR Size** options.

Affected Configurations

This issue affects the ×8 soft IP implementation of the PCI Express Compiler in all versions of the Quartus II software.

Workaround

There are three possible workarounds for this issue:

- Restrict the Expansion BAR size to 4 KBytes.
- Change from a ×8 to a ×4 configuration.
- Change to the ×8 hard IP implementation of the PCI Express MegaCore function which is available in Stratix IV GX and Arria II GX devices.

Solution Status

This issue is fixed in version 9.0 SP1 of the PCI Express Compiler.

You Cannot Use the MegaWizard Plug-In Manager to Edit the SERDES in the Hard IP Implementation of the PCI Express MegaCore Function

For the hard IP implementation of the PCI Express Compiler, you cannot edit the SERDES variant using the ALTGX MegaWizard Plug-In Manager.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express Compiler in version 9.0 of the Quartus II software.

Workaround

You can launch the ALTGX MegaWizard Plug-In Manager interface from the command line using the command given in Example 16–3. Be sure that the **Use Auxiliary Transmitter (ATX) PLL** option on the **PLL/Ports** page is turned off.

Example 16–3. Command to Edit the SERDES Variant for

```
qmegawiz IP_MODE=PCIE_HIP_8   -
wiz_override="gxb_analog_power=auto,tx_analog_power=auto,elec_idle_infer_enable=false,
tx_allow_polarity_inversion=false,rx_cdrctrl_enable=true,rateswitchbaseclock,
hip_tx_clkout,tx_pipemargin,tx_pipedeemph,rx_elecidleinfersel,fixedclk,rateswitch,
reconfig_dprio_mode=1,reconfig_clk,reconfig_fromgxb,reconfig_togxb,enable_0ppm=false,
rx_use_double_data_mode=false,tx_use_double_data_mode=false,rx_channel_width=8,
tx_channel_width=8,rx_dwidth_factor=1,tx_dwidth_factor=1,rx_dataout,tx_datain,
tx_ctrlenable,rx_ctrldetect,rx_patterndetect,rx_syncstatus" OPTIONAL_FILES="NONE"
intended_device_family="stratixiv" starting_channel_number=0 <var>_serdes.v
```

Solution Status

This issue is fixed in Release 9.0 SP1.

Guidelines for Passing the PCI Express Electrical Gold Test on the v2.0 Compliance Base Board (CBB)

The PCI Express electrical gold test requires the CBB v2.0 to measure the eye diagram on the transmit side of the serial transceiver at Gen1 and Gen2 rates. To run this test when using the hard IP implementation of the PCI Express Compiler, the Link Training and Status State Machine (LTSSM) must enter several polling compliance states, including: Gen1, Gen2–3.5dB, and Gen2–6dB. Altera recommends using an external hardware apparatus, such as a push-button switch, to trigger these LTSSM state changes. The push-button switch drives the `testin[5]` signal of the PCI Express MegaCore function. For more information about this signal, refer to *Appendix B. Test Port Interface Signals* in the *PCI Express Compiler User Guide*.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express Compiler when performing compliance testing.

Workaround

You can use a push-button switch to trigger the required LTSSM state changes.

Solution Status

The current suggested solution of using a push-button switch to trigger the required state changes was successful at the PCI Sig during Workshop 65. This information will be included in a future version of the *PCI Express Compiler User Guide*.

Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0

The hard IP implementation of the PCI Express endpoint incorrectly handles Type0 Configuration Reads (`CfgRd0`) when the `CfgRd0` TLPs Bus or Device Number does not match the endpoint's current Bus and Device Number. The endpoint issues an unsupported request due to the mismatch. Section 7.1.3 of the *PCI Express Base Specification 1.1 or 2.0* states that, "Devices must respond to all Type 0 Configuration Read Requests, regardless of the Device Number specified in the Request."

Affected Configurations

This issue affects the hard IP implementation of the PCI Express endpoint in Stratix IV GX ES devices.

Workaround

Do not issue a `CfgRd0` with mismatched bus/device numbers.

Solution Status

This issue will be fixed in a future version of the hard IP implementation of the PCI Express Compiler.

Endpoints Using the Soft IP Implementation Incorrectly Handle CfgRd0

The soft IP implementation of the PCI Express endpoint incorrectly handles Type0 Configuration Reads (`CfgRd0`) when the `CfgRd0` TLP's Bus or Device Number does not match the endpoint's current Bus and Device Number. The endpoint issues an unsupported request due to the mismatch. Section 7.1.3 of the *PCI Express Base Specification 1.1 or 2.0* states that, "Devices must respond to all Type 0 Configuration Read Requests, regardless of the Device Number specified in the Request."

Affected Configurations

This issue affects the ×1 and ×4 variants of the soft IP implementation of the PCI Express endpoint in the 8.1 release of the PCI Express Compiler.

Workaround

Do not issue a `CfgRd0` with mismatched bus/device numbers.

Solution Status

This issue is fixed in version 9.0 of the soft IP implementation of the PCI Express Compiler.

The Hard IP Implementation of the PCI Express Compiler May Be Unable to Exit the Disable State at the Gen2 Rate

The hard IP implementation of the PCI Express Compiler may be unable to exit the disable state after entering the disable state at the Gen2 rate.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express Compiler when operating at the Gen2 rate.

Workaround

You can avoid this issue using either of the following workarounds:

- Make sure that you enter the disable state at the Gen1 rate.

- Program your application to detect entry to the Link Training and Status State Machine (LTSSM) disable state and then assert the hard IP reset (assertion of `crst`, `srst`, and `npor`) forcing the LTSSM to transition to the detect state. In this case, note that the LTSSM goes to detect state and eventually to the polling compliance state where the Tx line is no longer in idle state. Altera uses this workaround for the design example generated by the PCI Express Compiler.

Solution Status

This issue will be documented in a future version of the *PCI Express Compiler User Guide*.

Adding Two PCI Express Components to an SOPC Builder System May Cause a System Error

Adding two or more additional PCI Express components to an SOPC Builder system may cause a Java stack overflow error (`StackOverFlowError`).

Affected Configurations

This issue may affect SOPC Builder systems to which you add two or more PCI Express components consecutively.

Workaround

If you encounter this error, save your SOPC Builder system and exit SOPC Builder. Restart SOPC builder and load the saved **.sopc** file. You can now edit all instances of the PCI Express module.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

License File for Soft IP Implementation of the PCI Express Compiler Does Not Work

The license file for the soft IP version of the PCI Express Compiler in 8.1 does not work.

Affected Configurations

This issue affects soft IP implementations of the PCI Express MegaCore function in version 8.1 of the Quartus II software.

Workaround

The workaround is to download and install the Quartus II 8.1 software patch contained in the following **.zip** file:

ftp://ftp.altera.com/outgoing/download/kdb/rd11242008_128and588.zip

Solution Status

This issue is fixed in version 9.0 of the Quartus II software.

EDA Netlist Writer Does Not Write Netlist for Hard IP Implementation of PCI Express

The Quartus II EDA Netlist Writer does not write a Stratix IV GX functional simulation netlist for the hard IP implementation of the PCI Express MegaCore function because a license file has not be en specified. However, the hard IP implementation does not require a license.

Affected Configurations

This issue affects hard IP implementations of the PCI Express MegaCore function in version 8.1 of the Quartus II software.

Workaround

The workaround is to download and install Quartus II 8.1 software patch contained in the following **.zip** file:

ftp://ftp.altera.com/outgoing/download/kdb/rd11242008_128and588.zip

Solution Status

This issue is fixed in version 9.0 of the Quartus II software.

Stratix IV Projects with Pin Assignments Specified Using the Pin Planner May Fail Quartus II Compilation

If you specify pin assignments using the Pin Planner for Stratix IV projects, Quartus II compilation fails.

Affected Configurations

This issue affects PCI Express MegaCore functions that target the Stratix IV family.

Workaround

Change the definition for the I/O standard for the transceivers from 1.2 V PCML to 1.4 V PCML.

Solution Status

This issue is fixed in version 9.0 of the Quartus II software.

Simulation Fails when Using ModelSim AE for Stratix II GX MegaCore Functions with the Avalon-ST or Descriptor/Data Interfaces

If you simulate PCI Express MegaCore functions that use the Avalon-ST or descriptor/data interface and target Stratix II GX devices using ModelSim® AE, you get a compilation error.

Affected Configurations

This issue affects PCI Express MegaCore functions written in Verilog HDL that use the Avalon-ST or descriptor/data interface and target a Stratix II GX device.

Workaround

In the **<*variation_name*>_examples/chaining_dma/testbench/sim_filelist** file, modify the line specifying <*variation_name*>**_serdes.v** to specify <*variation_name*>**_serdes.vo**.

Solution Status

This issue is fixed in version 9.0 of the Quartus II software.

The Chaining DMA Design Example May Issue DMA Write Requests that Violate the 4 KByte Boundary Rule in the VHDL Version

The VHDL version of the chaining DMA design example may issue DMA writes that violate the 4 KByte boundary. If a request crosses the 4 KByte boundary, the DMA data is thrown away. Because there is no data checking in the version 8.1 test driver, the simulation does not fail.

Affected Configurations

This issue affects the VHDL version of the chaining DMA design example for 8.1.

Workaround

You can modify the test driver, **altpcietb_bfm_driver_chaining.vhd**, so that the write DMA does not transfer data across 4 KByte addresses.

Solution Status

This issue is fixed in version 9.0 of the PCI Express Compiler design example.

Design Example in Hardware Might Require the RC Slave Module

The default configuration of the Altera-provided design example described in the *Testbench* chapter of the *PCI Express Compiler User Guide* does not instantiate the RC Slave module. The RC Slave module acknowledges message TLPs and zero-length memory read TLPs from the root complex. Typically, commercial BIOS's issue message TLPs; therefore, if you do not instantiate the RC Slave module in this design example, your hardware system may stall indefinitely.

Affected Configurations

This issue affects designs that use the PCI Express Development Kit and are recompiling the hardware design example with the 7.2 or 8.0 version of the PCI Express Compiler.

Workaround

Enable the RC Slave module when connecting to a commercial PCI Express platform.

Solution Status

This issue is fixed in version 9.0 of the PCI Express Compiler.

Root Port BFM in Version 8.1 of the PCI Express Testbench is not Backwards Compatible

Testbenches for PCI Express MegaCore functions generated in version 8.0 or earlier of the Quartus II software fail in version 8.1 of the Quartus II software.

Affected Configurations

This issue affects existing PCI Express MegaCore functions generated using version 8.0 or earlier of the PCI Express Compiler if you have upgraded to Quartus II 8.1 and want to regenerate the testbench using the Quartus II 8.1 software.

Workaround

If your design targets the Stratix IV family, you must regenerate your PCI Express MegaCore function using version 8.1 of the PCI Express Compiler.

If your design targets other device families, a workaround is to modify the **runtb.do** file in the testbench directory. Edit all lines that contain `stratixiv` to point to version 8.0 of the Altera MegaCore IP Library.

- Example 16–4 shows the original and modified version for VHDL.

Example 16–4. Modifications for runtb.do—VHDL

```
# This is the original line that uses the _ROOTDIR variable
vcom -work stratixiv_pcie_hip
$env(QUARTUS_ROOTDIR)/eda/sim_lib/stratixiv_pcie_hip_components.vhd

# This edited version points to version 8.0 of the Altera IP library
vcom -work stratixiv_pcie_hip
c:/altera/80/quartus/eda/sim_lib/stratixiv_pcie_hip_components.vhd
```

- Example Example 16–5 shows the original and edited versions for Verilog HDL.

Example 16–5. Modifications for runtb.do—Verilog HDL

```
# This is the original line that uses the QUARTUS_ROOTDIR variable
vlog -work stratixiv_hssi $env(QUARTUS_ROOTDIR)/eda/sim_lib/stratixiv_hssi_atoms.v

#This edited version points to version 8.0 of the Altera IP Library
vlog -work stratixiv_hssi c:/altera/80/quartus/eda/sim_lib/stratixiv_hssi_atoms.v
```

Solution Status

This issue is the result of incompatibilities between the high-speed serial interface (HSSI) design for version 8.1 of the Quartus II software and earlier versions. These incompatibilities cannot be resolved.

Incorrect Connection of SOPC Builder Interrupt Sources to PCI Express Components

In SOPC Builder systems containing a PCI Express component which masters interrupt senders on the other side of an Avalon-MM pipeline bridge or clock-crossing bridge, interrupt sources are not correctly wired to the PCI express component.

Affected Configurations

This issue affects PCI Express Compiler instances used in SOPC Builder systems containing an Avalon-MM pipeline bridge or clock-crossing bridge.

Workaround

Ensure that there is not an Avalon-MM pipeline bridge or clock-crossing bridge master between the PCI Express Rx master port and its slaves which produce interrupts.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

PCI Express Avalon-MM Tx Interface Deadlocks on a Read Request

When the Rx completion buffer is almost fully allocated, a new read might be sent even if there is not enough space in the buffer to store the read data. When this new read is sent, the read credit counter rolls over erroneously indicating that buffer space is available and the buffer overflows. Eventually, the Avalon Tx interface deadlocks on a read request because the wait request signal is asserted.

Affected Versions

This issue affects versions 8.0 of the PCI Express Compiler and earlier that use the SOPC Builder design flow.

Workaround

There is no workaround for this issue; however, it is fixed in version 8.1 of the PCI Express Compiler.

Solution Status

This issue is fixed in version 8.1 of the PCI Express Compiler.

Unable to Compile the Example Design Successfully in Quartus II when using ECRC Forwarding

For Stratix IV PCI Express variations that enable ECRC forwarding, compilation of the example design may fail because the included version of the CRC Compiler variation is not enabled for the Stratix IV device family.

Affected Configurations

This issue occurs in version 8.0 of the PCI Express Compiler if you do not have a license for the 8.0 CRC Compiler and you are creating a Stratix IV variant of the PCI Express MegaCore function that uses ECRC forwarding.

Workaround

You can complete the following these steps to edit the CRC Compiler variation created in your design example directory to update it to 8.0:

1. Open the Quartus II project that contains the design example.
2. Launch MegaWizard Plug-In Manager from the Tools menu.
3. Select **Edit an existing custom megafunction variation**.
4. Click **Next**.

5. Select **atpcierd_rx_ecrc_64.v** or **.vhd** or **atpcierd_rx_ecrc_128.v** if using Avalon-ST 128.
6. In the **Megafunction name** list, select **CRC Compiler 8.0**.
7. Click **Next**.
8. Click **Next**.
9. Click **Finish**.
10. Repeat steps 5–9 for **atpcierd_tx_ecrc_64.v** or **.vhd** or **atpcierd_tx_ecrc_128.v** if using Avalon-ST 128.

Solution Status

This is fixed in version 8.1 of the PCI Express Compiler.

Chaining DMA Design Example Forwards Tx ECRC with Incorrect Alignment

The chaining DMA design example incorrectly aligns the Tx ECRC, appending the ECRC to the dword immediately following the header regardless of address alignment, when the TLP does not include a payload data. The alignment is incorrect in two cases:

- With four dword headers, non-qword aligned addressing, and no payload data
- With three dword header, qword aligned addressing, and no payload data

For packets with payload, the ECRC should be appended to the end as an extra dword of payload. For packets without payload, the ECRC field should follow address alignment as if it were a one dword payload.

Affected Configurations

This issue effects the chaining DMA design example, not variants of the PCI Express MegaCore function.

Workaround

The out-of-the-box simulation example does not cause a simulation failure. If you have modified the simulation to use four dword headers, then you must modify the chaining DMA example code to correct the alignment.

Solution Status

This issue is fixed in version 8.1 of the PCI Express Compiler.

User Guide Incorrectly Documents the Number of Address Pages

Table 3-6 of the *PCI Express Compiler User Guide* incorrectly states the choices for the **Number of address pages**. The correct number of pages available is 2^n from 1–512.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 8.1 of the *PCI Express Compiler User Guide*.

User Guide Incorrectly Documents rx_st_data and tx_st_data in 128-Bit Mode

In 128-bit mode, the qwords in the timing diagrams are swapped. The correct order for Rx or Tx data[127:0] is {H3, H2, H1, H0}. The *PCI Express Compiler User Guide* shows data[127:0] as {H1, H0, H3, H2}. In addition, the `rx_st_empty0` and `tx_st_empty0` signals indicate that the TLP ends in the *lower* words of data. The corrected diagrams and text are given here.

Figure 16–1shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for TLPs with a three dword header and qword aligned addresses.

Figure 16–1. 128-Bit Avalon-ST rx_st_data0 Cycle Definition for 3-DWord Header TLPs with QWord Aligned Addresses

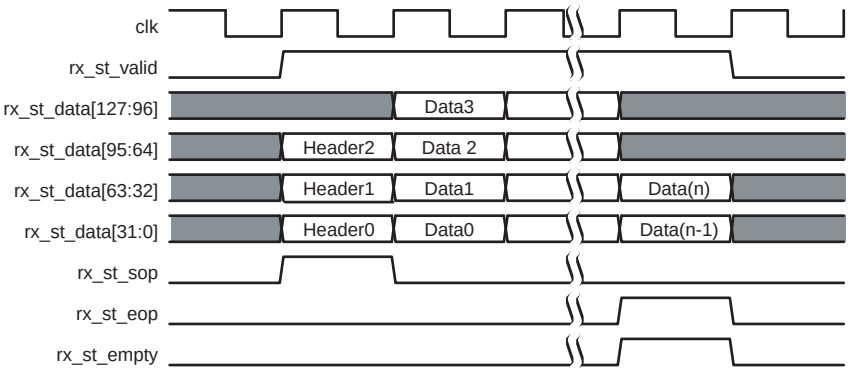


Figure 16–2 shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for TLPs with a 3 dword header and non-qword aligned addresses.

Figure 16–2. 128-Bit Avalon-ST rx_st_data0 Cycle Definition for 3-DWord Header TLPs with non-QWord Aligned Addresses

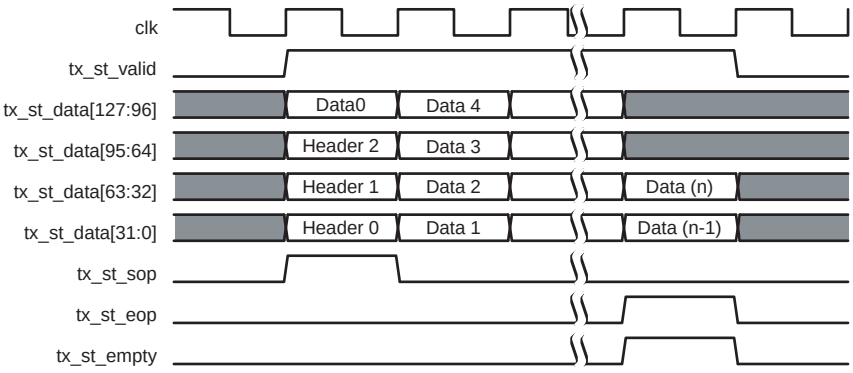


Figure 16–3 shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for a four dword header with non-qword aligned addresses. In this example, `rx_st_empty` is low because the data ends in the upper 64 bits of `rx_st_data`.

Figure 16–3. 128-Bit Avalon-ST rx_st Cycle Definition for 4-DWord Header TLPs with non-QWord Aligned Addresses

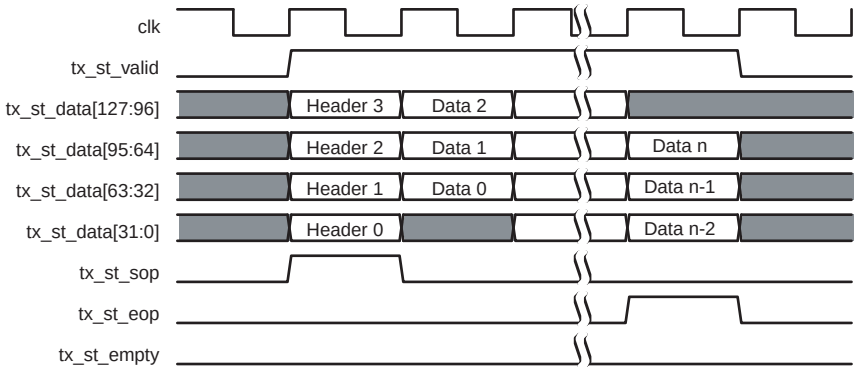


Figure 16–4 shows the mapping of 128-bit Avalon-ST Rx packets to PCI Express TLPs for a four dword header with qword aligned addresses.

Figure 16–4. 128-Bit Avalon-ST rx_st Cycle Definition for 4-DWord Header TLPs with QWord Aligned Addresses

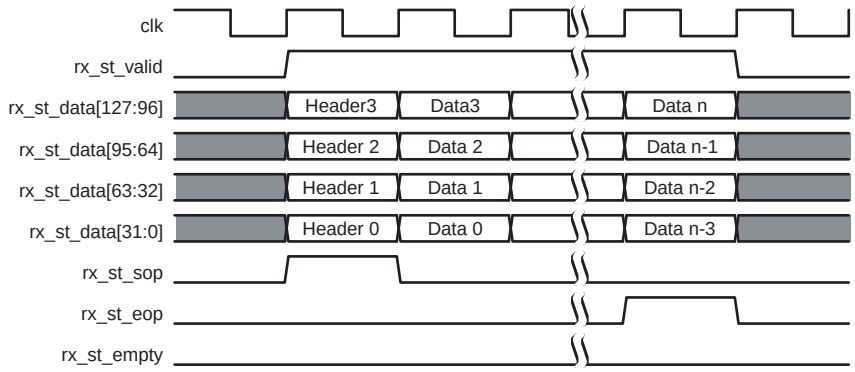


Figure 16–5 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a three dword header with qword aligned addresses.

Figure 16–5. 128-Bit Avalon-ST tx_st_data Cycle Definition for 3-DWord Header TLPs with QWord Aligned Addresses

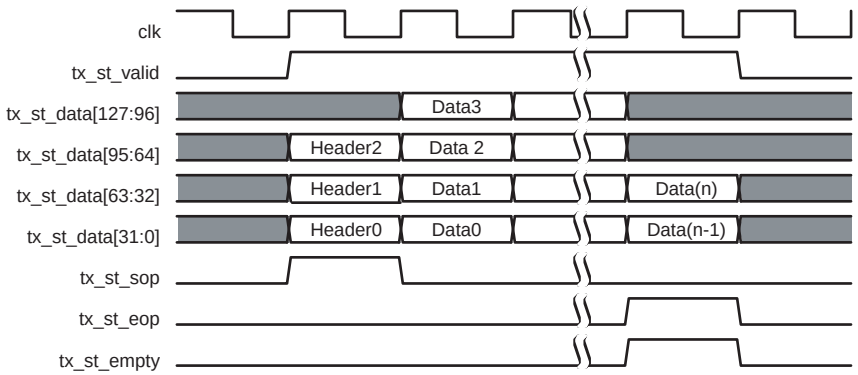


Figure 16–6 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a 3 dword header with non-qword aligned addresses.

Figure 16–6. 128-Bit Avalon-ST tx_st_data Cycle Definition for 3-DWord Header TLPs with non-QWord Aligned Addresses

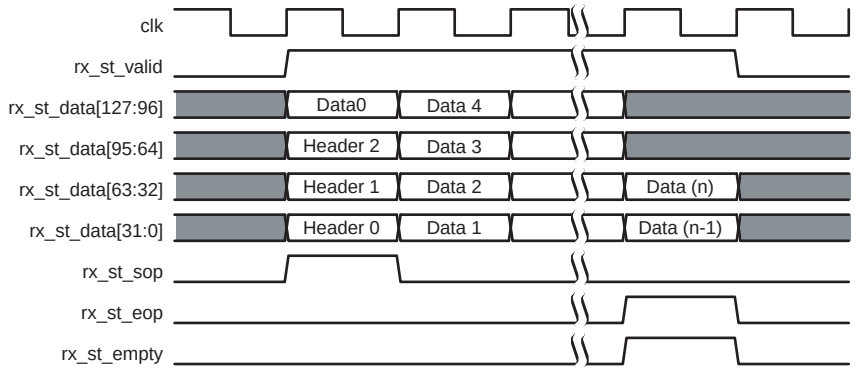
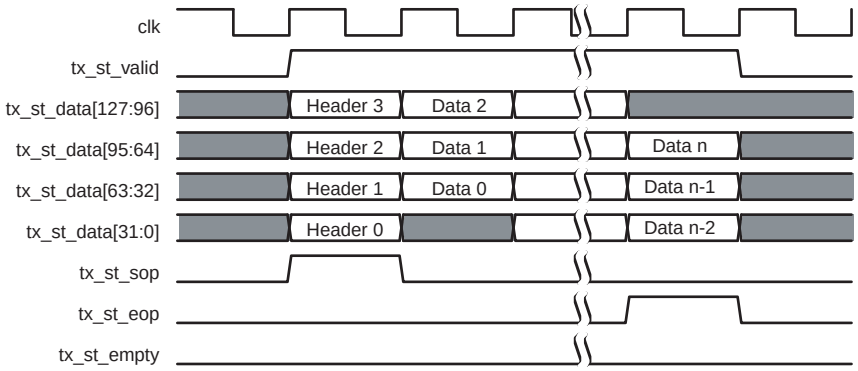


Figure 16–7 shows the mapping of 128-bit Avalon-ST Tx packets to PCI Express TLPs for a four dword header TLP with non-qword aligned addresses. In this example, `tx_st_empty` is low because the data ends in the upper 64 bits of `tx_st_data`.

Figure 16–7. 128-Bit Avalon-ST tx_st_data Cycle Definition for 4-DWord Header TLPs with non-QWord Aligned Addresses



Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 8.1 of the *PCI Express Compiler User Guide*.

Address Translation Update Can Corrupt Outstanding Reads for MegaCore Functions Created in SOPC Builder

When an Avalon-MM master sends a request larger than the PCI Express **Maximum payload size** to the Tx slave port, the MegaCore function converts this large request into multiple PCIe requests of smaller size, depending on address boundaries and size. For each smaller payload packet sent, the address translation table is accessed to generate the address field of the packet. This process takes a number of clock cycles, and during that time, if the translation table entry is altered, the subsequent smaller request packets have the wrong address.

For write requests, it is safe to change the entry associated with a DMA after the last data is accepted for write. For read requests, it is safe to change the table entry after the first data for a DMA is returned. You should rotate among multiple entries in the Avalon-MM to PCIe address translation table in order to support more than one outstanding read request.

Affected Configurations

This issue affects PCI Express applications created in SOPC Builder.

Workaround

You must use the address translation tables as described in this errata.

Solution Status

This issue is version 9.0 of the *PCI Express Compiler User Guide*.

User Guide, Version 8.0 Swapped Descriptions of cpl_err[4] and cpl_err[5]

The descriptions of `cpl_err[4]` and `cpl_err[5]` are reversed in the *PCI Express Compiler User Guide*, version 8.0. Table 16–6 gives correct descriptions.

Table 16–6. Completion Interface Signals for Avalon-ST

Signal	I/O	Description
cpl_err[5:4]	I	Completion error. This signal reports completion errors to the configuration space. ■ `cpl_err[5]`: Unsupported request error for non-posted TLP. Used in soft IP Avalon-ST interface and the hard IP implementation. ■ `cpl_err[4]`: Unsupported request error for posted TLP. Used in soft IP Avalon-ST interface and the hard IP implementation.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This error is fixed version 8.1 of the *PCI Express Compiler User Guide.*

MegaWizard Interface Displays Incorrect Values

PCI Express MegaWizard Interface displays incorrect values for the Credit Display Table of Buffer Setup Page when the hard IP Implementation is selected. The displayed Rx Buffer Space Allocation (per VC) table displays incorrect values for the hard IP implementation of the PCI Express MegaCore function. Table 16–7 lists the correct values. The **Desired performance for received requests** setting has no effect. The credit allocations for the hard IP implementation are set to the values indicated in Table 16–7.

Table 16–7. Rx Buffer Space Allocation (per VC) Hard IP Implementation

Credit Type	Number of Credits	Space Used (in Bytes)
Without ECRC Forwarding		
Posted header credit	50	800
Posted data credit	360	5760
Non-posted header credit	54	864
Completion header credit	112	1792
Completion data credit	448	7168
Total header credits	216	—
Rx buffer size	—	16384
With ECRC Forwarding		
Posted header credit	50	1200
Posted data credit	336	5375
Non-posted header credit	54	1296
Completion header credit	112	1792
Completion data credit	420	6720
Total header credits	216	—
Rx buffer size	—	16384

Affected Configurations

The Rx Buffer Space Allocation information is incorrect for the hard IP implementation of the PCI Express MegaCore function which is available in Stratix IV GX devices.

Workaround

Refer to Table 16–7 for the correct values for Rx buffer space allocation.

Solution Status

This issue is fixed in version 8.1 of the PCI Express Compiler.

17. POS-PHY Level 2 and 3 Compiler

Revision History

Table 17–1 shows the revision history for the POS-PHY Level 2 and 3 Compiler.

For more information about the new features, refer to the *POS-PHY Level 2 and 3 Compiler User Guide*.

Table 17–1. POS-PHY Level 2 and 3 Compiler Revision History

Version	Date	Description
9.1	November 2009	Maintenance release.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Full support for Stratix III devices.

Obsolescence Notice

CAUTION

The POS-PHY Level 2 and 3 Compiler is scheduled for product obsolescence and discontinued support as described in PDN0906. Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's Intellectual Property website.

Errata

Table 17–2 shows the issues that affect the POS-PHY Level 2 and 3 Compiler v9.1, v9.0, and 8.1.

Not all issues affect all versions of the POS-PHY Level 2 and 3 Compiler.

Table 17–2. POS-PHY Level 2 and 3 Compiler Errata

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
01 Oct 07	Compilation Error in NativeLink VHDL Flow for NCSim	✓	✓	✓
01 Dec 06	IP Toolbench Incorrect Behavior	✓	✓	✓
	Errors with Pin Planner Top-Level File	✓	✓	✓

Compilation Error in NativeLink VHDL Flow for NCSim

There is a compilation error because of an error in the file declaration format.

Affected Configurations

This issue affects NCSim simulation for the VHDL flow.

Design Impact

NCSim simulation does not work for the VHDL flow.

Workaround

The incorrect declaration lines are not required and can be commented out:

- Edit the **\sim_lib\testbench\vhdl\auk_pac_mtx_ref_tb.vhd** file and comment out lines 128 and 461.
- Edit the **\sim_lib\testbench\vhdl\auk_pac_mrx_ref_tb.vhd** file and comment out lines 130 and 474.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.

IP Toolbench Incorrect Behavior

In the IP Toolbench Parameterize window, after you click **Finish**, if you click **Parameterize** to review your settings, the options show incorrect behavior.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

When you click **Finish**, ensure you close IP Toolbench (which cancels any changes) or click **Generate**. You can view the Parameterize window again by reopening IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.

Errors with Pin Planner Top-Level File

When you compile a Quartus II Pin Planner-generated top-level file you receive errors.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not compile.

Workaround

Do not use Pin Planner with the POS-PHY Level 2 and 3 Compiler.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 2 and 3 Compiler.

18. POS-PHY Level 4

Revision History

Table 18–1 shows the revision history for the POS-PHY Level 4 MegaCore function.

For more information about the new features, refer to the *POS-PHY Level 4 MegaCore Function User Guide*.

Table 18–1. POS-PHY Level 4 MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Maintenance release.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Full support for Stratix III devices.

Errata

The following sections addresses known errata and documentation issues for the POS-PHY Level 4 MegaCore function. Errata are functional defects or errors, which may cause the POS-PHY Level 4 MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 18–2 shows the issues that affect the POS-PHY Level 4 MegaCore function v9.1, 9.0, and 8.1.

Not all issues affect all versions of the POS-PHY Level MegaCore function.

Table 18–2. POS-PHY Level 4 MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
15 Nov 09	Generation Appears to Fail	Fixed	✓	—
	Demonstration Testbench Fails	Fixed	✓	—
	Valid Range of Full Threshold High is Incorrect	Fixed	✓	✓
01 Sep 08	Incorrect Description of DIP-4 Out of Service Indication in User Guide	✓	✓	✓
15 May 08	Errors when Editing Transmitters v7.2 or Earlier in v8.0	✓	✓	✓
	Transmitter Sends Extra Idles with Burst Limit Enable	—	—	Fixed
	Missing Constraint	—	—	Fixed
	Training Interval is Greater than Specified	✓	✓	✓

Table 18–2. POS-PHY Level 4 MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
01 May 07	Irrelevant Signals: err_ry_msop* & err_ry_meop*	✓	✓	✓
	Warning Message: Pin “err_rd_dpa” Stuck at GND	✓	✓	✓
	IP Toolbench Error After Changing the Device Family	✓	✓	✓
	IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices	✓	✓	✓
	IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted	✓	✓	✓

Generation Appears to Fail

Some transmitter variants take a long time to generate and appear to have failed to generate.

Affected Configurations

Transmitters with embedded addressing, a high number of ports, an Atlantic interface width greater than the data path width, using the **Lite Transmitter** option, or a data path width of 32 bits, may take a long time to generate.

Workaround

Some generation may take over 20 minutes to generate.

Design Impact

There is no design impact.

Solution Status

This issue is fixed in version 9.1 of the POS-PHY Level 4 MegaCore function.

Demonstration Testbench Fails

The demonstration testbench may fail with the following error message:

```
Core Failed to Train
```

Affected Configurations

Receiver configurations with DPA enabled, in Arria II GX devices

Workaround

This issue has no workaround.

Design Impact

There is no design impact.

Solution Status

This issue is fixed in version 9.1 of the POS-PHY Level 4 MegaCore function.

Incorrect Description of DIP-4 Out of Service Indication in User Guide

The following paragraph is incorrect in the *DIP-4 Out of Service* section in the *POS-PHY Level 4 MegaCore Function User Guide*:

> If the receiver is in service (the `stat_rd_dip4_oos` is low) and one or more DIP-4 errors are detected (up to 8 in 128-bit mode) in the current `rdint_clk` cycle, the bad counter is incremented. If the bad counter reaches the bad_level threshold, the receiver goes out of service by asserting the `stat_rd_dip4_oos` signal. If all of the DIP-4s received in the current cycle are good, the bad counter is cleared. If no control words are received, nothing happens.

The following paragraph is correct:

> If the receiver is in service (the `stat_rd_dip4_oos` is low) and one or more DIP-4 errors are detected (up to 8 in 128-bit mode) in the current `rdint_clk` cycle, the bad counter is incremented. If the bad counter reaches the bad_level threshold, the receiver goes out of service by asserting the `stat_rd_dip4_oos` signal. If any of the DIP-4s received in the current cycle are good, the bad counter is cleared. So if both good and bad DIP-4s are received in the current cycle the bad counter is also cleared. If no control words are received, nothing happens.

In particular, the following sentence has the incorrect "all" replaced by the correct "any":

> If any of the DIP-4s received in the current cycle are good, the bad counter is cleared.

In addition, the following paragraph in the *Receiver Options* section is incorrect in a similar way:

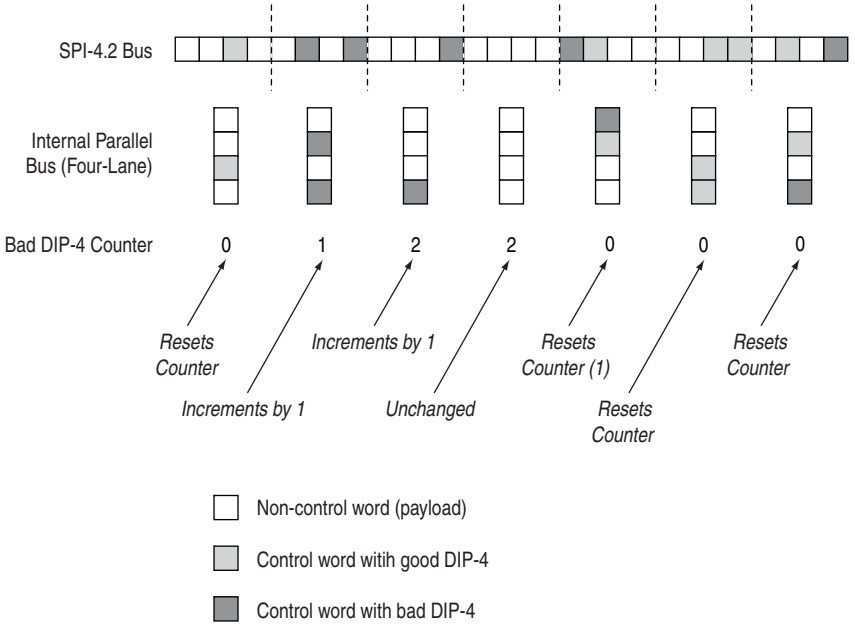
> If the `stat_rd_dip4_oos` signal is low, and any of the DIP-4s in the control words received in the current clock cycle (up to 8 in 128-bit mode) are errored, the bad counter is incremented by 1; otherwise it is reset to 0. If the bad counter reaches the `bad_level` threshold, the `stat_rd_dip4_oos` flag is asserted. A `bad_level` of 0 is invalid.

The following paragraph is correct:

> If the `stat_rd_dip4_oos` signal is low, and all of the DIP-4s in the control words received in the current clock cycle (up to 8 in 128-bit mode) are errored, the bad counter is incremented by 1; otherwise it is reset to 0. If the bad counter reaches the `bad_level` threshold, the `stat_rd_dip4_oos` flag is asserted. A `bad_level` of 0 is invalid.

Figure 18–1 shows an example of the DIP-4 counter, where the receiver is in service state and bad threshold is 3.

Figure 18–1. DIP-4 Counter *(Note 1)*



Note to Figure 18–1:

(1) Receiving a good and a bad DIP-4 in the same parallel cycle resets the counter (does not increment it), so that OOS does not trigger.

Affected Configurations

This issue affects all receiver configurations.

Design Impact

The core may need to receive more control word DIP-4 errors than the **DIP-4 Bad Threshold** parameter set in the wizard for `stat_rd_dip4_oos` to go high.

Solution Status

This issue will be fixed in a future version of the *POS-PHY Level 4 MegaCore Function User Guide*.

Valid Range of Full Threshold High is Incorrect

The valid range of the full threshold high (FTH) is dependent on many parameters such as the width of the internal bus. When changing the width of the bus, the wizard may allow the FTH out of the acceptable range and so you end up with an incorrect or non-existent choice for the FTH.

Affected Configurations

This issue affects transmitters.

Design Impact

There is no design impact.

Workaround

To work around the issue, if you change the bus width, for example the Atlantic data width, ensure you modify the FTH value on the **Protocol Parameters tab of the wizard**.

Solution Status

This issue is fixed in version 9.1 of the POS-PHY Level 4 MegaCore function.

Errors when Editing Transmitters v7.2 or Earlier in v8.0

If you edit a v7.2 or earlier 64 or 128-bit transmitter MegaCore variation in the v8.0 MegaWizard Plug-In, the PLL input frequency is set to 1 MHz, which is incorrect.

Affected Configurations

This issue affects 64- and 128-bit transmitters.

Design Impact

There is no design impact.

Workaround

To work around the issue, follow these steps:

1. Click in the **LVDS Data Rate** dialog box.
2. Press **Enter**.

The PLL input frequency parameter resets to the correct value—data rate divided by deserialization factor.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Transmitter Sends Extra Idles with Burst Limit Enable

The POS-PHY Level 4 MegaCore function transmitter sends up to four control words between two bursts when you turn on **Burst Limit Enable**.

Affected Configurations

This issue affects transmitters with a 32-bit data-path width when you turn on **Burst Limit Enable**.

Design Impact

There design bandwidth is decreased.

Workaround

In the <*variation name*>**tx_core.v** file, change the `TXLITE` parameter from 0 to 1.

```
parameter TXLITE = 1;
```

Solution Status

This issue is fixed in version 8.1 of the POS-PHY Level 4 MegaCore function.

Missing Constraint

In designs targeting Stratix III and Stratix IV devices, the `derive_clock_uncertainty` Synopsis design constraint (SDC) for TimeQuest is missing.

Affected Configurations

This issue affects all Stratix III and Stratix IV designs.

Design Impact

There is no design impact.

Workaround

Add the `derive_clock_uncertainty` SDC for Stratix III and Stratix IV device designs.

Solution Status

This issue is fixed in version 8.1 of the POS-PHY Level 4 MegaCore function.

Training Interval is Greater than Specified

In corner cases, for example with datapath is 256 and a high number of ports and low burst length (`BURSTLEN`), the maximum training interval (`MaxT`) is greater than you specify.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

Add (or subtract) another `BURSTLEN` to calculation, so `MaxT` is `SET_MaxT` + 2 × `BURSTLEN`.

Solution Status

This issue will never be fixed.

Irrelevant Signals: err_ry_msop* & err_ry_meop*

After generation, the MegaCore function may include the following irrelevant output signals, which you can safely ignore:

- `err_ry_msop*`
- `err_ry_meop*`

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Warning Message: Pin “err_rd_dpa” Stuck at GND

During compilation, the Quartus II software issues the following warning, which you can safely ignore:

```
Pin "err_rd_dpa" Stuck at GND
```

Affected Configurations

This issue affects all non-Stratix GX receivers with dynamic phase alignment (DPA) enabled.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

The Calendar Length Value Cannot Equal 256

If the transmitter’s status interpretation mode is set to pessimistic, the programmable calendar length support parameter must be less than the maximum number of ports (< 256), unless the asymmetric port support parameter is enabled.

Affected Configurations

This issue affects all transmitter variations of the MegaCore function that use the pessimistic mode for status interpretation, and that do not have the asymmetric port support parameter enabled.

Design Impact

The status first-in first-out (FIFO) buffer may lock up. The scheduler in individual buffers variations of the MegaCore function may also lock up.

Workaround

If you turn on the programmable calendar length support in your variation, make sure that you set the calendar length value—via a pin or the Avalon Memory-Mapped (Avalon-MM) register—to less than the maximum calendar length (that is, 256); unless asymmetric port support is enabled, in which case you select the maximum calendar length in IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Error After Changing the Device Family

If you change the device family when editing an existing custom megafunction variation (POS-PHY Level 4 MegaCore function variation) without first changing the device family in the Quartus II project, an error may occur when generating the MegaCore function. This results in a MegaCore function generation error message.

This issue also applies when creating a new custom megafunction variation, if you use a different device family to that specified in the Quartus II project.

Affected Configurations

This issue can affect all configurations.

Design Impact

You may not be able to generate a MegaCore function.

Workaround

Before using the MegaWizard Plug-In Manager to create or edit a POS-PHY Level 4 custom megafunction variation, make sure that a Quartus II project exists and that the required device family is set in the project. To set the device family, in the Quartus II software, on the Assignments menu click **Device**.

When using the MegaWizard Plug-In Manager to create or edit the megafunction variation, set the device family to be the same as the device family set in the Quartus II project. You can set the device family in the **Basic Parameters** tab when parameterizing the MegaCore function.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices

If you select **HardCopy Stratix** in the MegaWizard Plug-In Manager and you turn on **Generate Simulation Model** and generate a MegaCore function variation, IP Toolbench fails with an error.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot generate an IP functional simulation model.

Workaround

Select the Stratix family in the MegaWizard Plug-In Manager.

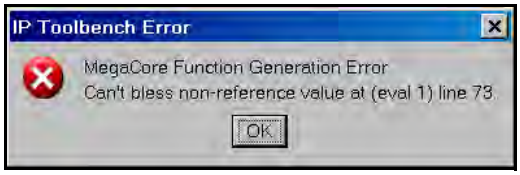
Solution Status

This issue will never be fixed.

IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted

By clicking the IP Toolbench **Generate** button, you start generating a POS-PHY Level 4 MegaCore function variation. If, during generation, you click the **Cancel** button (Generation window) and click the IP Toolbench **Generate** button again to restart the generation, IP Toolbench fails and produces the following error message:

Figure 18–2. IP Toolbench Generation Error Message



Affected Configurations

This issue affects all variations of the MegaCore function.

Design Impact

IP Toolbench does not generate any files.

Workaround

To cancel a generation and avoid this error, follow these steps:

1. Click the **Cancel** button in the Generation window.
2. Close IP Toolbench by clicking the × in the upper right corner.
3. Relaunch IP Toolbench from the MegaWizard Plug-In Manager (Tools menu).

Refer to the Getting Started chapter of the *POS-PHY Level 4 MegaCore Function User Guide* for instructions on using IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Revision History

Table 19–1 shows the revision history for the RapidIO MegaCore function.

For more information about the new features, refer to the *RapidIO MegaCore Function User Guide*.

Table 19–1. RapidIO MegaCore Function Revision History

Version	Date	Description
9.1 SP1	February 2010	Maintenance release
9.1	November 2009	■ Preliminary support for HardCopy IV GX and Cyclone III LS devices ■ Support for 5.0 Gbaud data rate ■ Support for order preservation between I/O write requests and DOORBELL requests ■ NWRITE_R completion indication ■ Post-reset ackID synchronization ■ Transceiver configuration using full transceiver MegaWizard interface
9.0 SP2	July 2009	Maintenance release
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices
9.0	March 2009	■ Preliminary support for Arria II GX devices ■ Support for outgoing multicast-event symbol generation ■ Support for 16-bit device ID
8.1	November 2008	■ Full support for Stratix III devices ■ Support for incoming muticast transactions ■ Support to enable or disable destination ID checking ■ Support to set transceiver starting channel number ■ Requirement to configure a dynamic reconfiguration block with any Stratix IV transceivers, to enable offset cancellation

Errata

Table 19–2 shows the issues that affect the RapidIO MegaCore function v9.1 SP1, v9.1, v9.0 SP2, v9.0 SP1, v9.0, and v8.1.

Not all issues affect all versions of the RapidIO MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

For SOPC Builder errata, which might affect the RapidIO MegaCore function and other SOPC Builder components, refer to the *Quartus II Software Release Notes*.

Table 19–2. RapidIO MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version					
		9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
1 Apr 10	Doorbell Response Packets are not Sent if Master Enable Bit is not Set	✓	✓	✓	✓	✓	✓
	Certain Changes Made in the RapidIO MegaWizard Interface are Ignored	✓	—	—	—	—	—
	Changes Made to the Reference Clock in the ALTGX MegaWizard Interface are Ignored	✓	✓	—	—	—	—
15 Feb 10	A link-request reset-device Sequence Can Be Ignored	✓	✓	✓	✓	✓	✓
	Avalon-ST Pass-Through Interface gen_rx_valid Signal Remains Asserted on Non-Ready Cycles	—	Fixed	✓	✓	✓	✓
	Starting Channel Number Resets When SOPC Builder is Closed	Fixed	✓	—	—	—	—
	Reception of a Small Packet Can Cause Counter Overflow in the Transport Layer Module	Fixed	✓	—	—	—	—
	Response Packet is Sent for Request Packet with Reserved Transaction Type	—	Fixed	✓	✓	✓	✓
15 Nov 09	Specific Variation With Transaction Ordering Enabled Requires Additional Logical Layer Modules	✓	✓	—	—	—	—
	Some Variations Do Not Meet Timing Requirements	✓	✓	—	—	—	—
	Some Variations With High Reference Clock Frequency Generate Critical Timing Warnings	✓	✓	✓	—	—	—
	Errored NREAD Response Can Have Wrong Transaction ID	—	Fixed	✓	✓	✓	✓
	Reception of Six or More Consecutive Control Symbols Can Cause Some of the Received Control Symbols To Be Lost	—	Fixed	✓	✓	✓	✓
	Error Response Packet Can Be Sent Twice if the io_m_rd_readerror Signal is Asserted	—	Fixed	✓	✓	✓	✓
	User Guide Description of Direction of io_s_rd_read Signal is Incorrect	—	Fixed	✓	✓	✓	✓
	SOPC Builder Testbench May Fail on 1× Stratix GX Variations at 1.25 GBaud	—	Fixed	✓	✓	—	—
	Migration of Existing RapidIO MegaCore Function May Generate Warning Message	—	Fixed	✓	✓	✓	✓
	Receipt of a Write Request for 5, 6, or 7 Bytes by the I/O Master Causes an Invalid Avalon-MM Burst Transaction	—	Fixed	✓	✓	✓	✓
	Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets	—	Fixed	✓	✓	✓	✓
01 Jul 09	Stratix III Device Support Level is Reported as Preliminary	—	—	Fixed	✓	✓	—
15 May 09	Transport Layer Can Drop Outgoing Packets if Physical Layer Transmit Buffer Fills	—	—	—	Fixed	✓	✓
	Testbench Fails on Some Stratix GX Variations	—	—	—	Fixed	✓	✓
	Some Variations With Reference Clock Frequency 390.625 MHz do Not Meet Timing	—	—	—	Fixed	✓	✓

Table 19–2. RapidIO MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version					
		9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 Mar 09	SourceID Can Be Incorrectly Set to Zero in NWRITE_R Response Packets	—	—	—	—	Fixed	✓
	A Cancelled Packet Can Be Processed As a Normal Packet	—	—	—	—	Fixed	✓
	Asserting io_m_wr_waitrequest During a Burst Transfer When io_m_wr_write is Not Asserted Can Cause Deadlock	—	—	—	—	Fixed	✓
	Four Back-to-Back Short Incoming Packets Can Cause Miscalculation of the Following Packet Sizes	—	—	—	—	Fixed	✓
	An Errored Incoming Packet Can Cause Miscalculation of the Following Packet Sizes	—	—	—	—	Fixed	✓
	Timeout Logic Can Incorrectly Extend Doorbell Transaction Timeout Period	—	—	—	—	Fixed	✓
	Doorbell Transaction Can Be Transmitted With Invalid Transaction ID	—	—	—	—	Fixed	✓
	User Guide Description of Default Value of EF_ID Field in PHEAD0 Register is Incorrect	—	—	—	—	Fixed	✓
	SOPC Builder Systems May Have Incorrectly Clocked Reset or Incorrect Calibration Clock Driver	—	—	—	—	Fixed	✓
01 Nov 08	Stratix IV Simulations May Fail With ModelSim 6.3g Compiler Optimizations Enabled	✓	✓	✓	✓	✓	✓

Doorbell Response Packets are not Sent if Master Enable Bit is not Set

If the Master Enable (ENA) bit of the `Port General Control` CSR (offset 0x13C) is not set, the Doorbell module does not send `DOORBELL` responses. The Doorbell module checks this signal before sending out any packets, including response packets.

Affected Configurations

All RapidIO variations that instantiate a Doorbell module.

Design Impact

All Doorbell requests sent to the RapidIO MegaCore function while the Master Enable bit is not set, receive no response and eventually time out.

Workaround

Ensure that the the Master Enable (ENA) bit of the `Port General Control` CSR (offset 0x13C) is set.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Certain Changes Made in the RapidIO MegaWizard Interface are Ignored

If you modify the data rate, reference clock frequency, or 1×/4× setting in an existing RapidIO MegaCore function using the RapidIO MegaWizard interface, and then generate the RapidIO MegaCore function, the transceiver is generated with the previous data rate, reference clock frequency, and 1×/4× setting. The change does not propogate to the ALTGX megafunction.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target.

Design Impact

The RapidIO MegaCore function data rate, reference clock frequency, and 1×/4× setting cannot be modified using the RapidIO MegaWizard interface.

Workaround

To change the data rate, reference clock frequency, or 1×/4× setting of an existing RapidIO MegaCore function, remove the existing RapidIO MegaCore function from your design, including deletion of its <*variation*>**_riophy_gxb.v** file, and then create a new RapidIO MegaCore function to replace it.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Changes Made to the Reference Clock in the ALTGX MegaWizard Interface are Ignored

If you modify the reference clock frequency using the ALTGX MegaWizard interface, and then generate the RapidIO MegaCore function, the RapidIO MegaCore function is generated with the previous reference clock frequency.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target, except variations that target a Stratix GX device.

Design Impact

The RapidIO MegaCore function reference clock frequency cannot be set using the ALTGX MegaWizard interface.

Workaround

To avoid this issue in the RapidIO MegaCore function v9.1, set the reference clock frequency in the RapidIO MegaWizard interface. In the RapidIO MegaCore function v9.1 SP1, that solution is not available, and you must create a new RapidIO MegaCore function instead.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

A link-request reset-device Sequence Can Be Ignored

If the third and fourth received `link-request` control symbols with `cmd` set to `reset-device` are separated by other incoming symbols such as a status control symbol or the IDLE sequence, the count of received `link-request reset-device` control symbols resets to zero, instead of triggering a device reset, with 50% probability.

Affected Configurations

All 4× RapidIO variations.

Design Impact

The RapidIO MegaCore function does not reset as expected.

Workaround

Send an additional four `link-request` control symbols with `cmd` set to `reset-device`.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Avalon-ST Pass-Through Interface gen_rx_valid Signal Remains Asserted on Non-Ready Cycles

The `gen_rx_valid` output signal of the receive-side Avalon-ST pass-through interface remains asserted on non-ready cycles. The Avalon-ST interface specification requires that the valid signal be deasserted on non-ready cycles.

Affected Configurations

All RapidIO variations that instantiate the Avalon-ST pass-through interface.

Design Impact

User logic that relies on the `gen_rx_valid` signal being asserted only on ready cycles might sample the receive side pass-through signals when they are not valid.

Workaround

Ignore the `gen_rx_valid` signal on non-ready cycles.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function.

Starting Channel Number Resets When SOPC Builder is Closed

If you regenerate an existing system in SOPC Builder, and that system includes a RapidIO MegaCore function with a non-default (non-zero) starting channel number, and you do not edit the RapidIO MegaCore function by configuring the transceiver to reset the starting channel number explicitly before you regenerate the SOPC Builder system, the RapidIO MegaCore function is generated with the default starting channel number 0.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target, except variations that target an Arria GX or a Stratix GX device.

Design Impact

The RapidIO MegaCore function starting channel number must be reset manually whenever you reopen your design in SOPC Builder, before you regenerate the SOPC Builder system.

Workaround

To reset the starting channel number for the transceiver in your RapidIO MegaCore function, after you open SOPC Builder and before you regenerate your SOPC Builder system, perform one of the following actions:

- In a text editor, open the file <*RapidIO instance_name*>**_riophy_gxb.v**, set the value of `starting_channel_number`, and save the file.
- Open the RapidIO MegaCore function in the SOPC Builder system by double-clicking the MegaCore function name, click **Configure Transceiver**, set the starting channel value to the desired value, and click **Finish**.

Solution Status

This issue is fixed in version 9.1 SP1 of the RapidIO MegaCore function.

Reception of a Small Packet Can Cause Counter Overflow in the Transport Layer Module

The reception of a 64-bit packet, such a response packet with 8-bit device IDs and without data, from the Physical layer, immediately after another packet, can cause the Transport layer packet counter to overflow and roll over to zero.

Affected Configurations

All RapidIO ×4 variations with 8-bit device IDs that implement a Transport layer and can receive 64-bit long packets.

Design Impact

If the counter rolls over to zero, the Rx buffer in the Transport layer appears empty until a new packet arrives. The empty indication may cause a temporary interruption in the transfer of a packet from the Transport layer to a Logical layer module. When the following packet arrives in the Transport layer, the packet-size information transmitted to the Logical layer modules is not synchronized correctly with the packet boundaries. The resulting erroneous packet sizes could cause Input/Output Avalon-MM Logical layer modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible events.

Workaround

To avoid this issue, perform the following workaround to modify the Transport layer counter behavior:

1. Generate the RapidIO MegaCore function using the MegaWizard interface.

2. In a text editor, open the generated Transport layer RTL file, <*variation_name*>**_transport.v**.
3. To increase the size of the counter, replace

```
reg [1:0] pktcnt, _Fpktcnt;
```

with

```
reg [2:0] pktcnt, _Fpktcnt;
```

4. To modify the Transport layer functionality to ensure it recognizes the counter value 4, perform one of the following actions to add `|| (pktcnt == 3'h4)` to the relevant condition:
   - If your RapidIO variation runs at 3.125 GBaud per lane or slower, replace

```
if ((valid_data && srceop && (pktcnt == 2'h2 || just_got_eop)) ||
       (pktcnt == 2'h2 && (inc_pktcnt || inc_pktcnt_dly))      ||
       (pktcnt == 2'h3 && !(dec_pktcnt && !inc_pktcnt && !inc_pktcnt_dly))
) begin
```

   with

```
if ((valid_data && srceop && (pktcnt == 2'h2 || just_got_eop)) ||
       (pktcnt == 2'h2 && (inc_pktcnt || inc_pktcnt_dly))      ||
       (pktcnt == 2'h3 && !(dec_pktcnt && !inc_pktcnt && !inc_pktcnt_dly))
       || (pktcnt == 3'h4)
) begin
```

   - If your RapidIO variation runs at 5.0 GBaud per lane, replace

```
if ((valid_data && srceop && (pktcnt_eq_2 || just_got_eop)) ||
       (pktcnt_eq_2 && pktcnt_flag1)                       ||
       (pktcnt_eq_3 && !(dec_pktcnt && pktcnt_flag2))
) begin
```

   with

```
if ((valid_data && srceop && (pktcnt_eq_2 || just_got_eop)) ||
       (pktcnt_eq_2 && pktcnt_flag1)                       ||
       (pktcnt_eq_3 && !(dec_pktcnt && pktcnt_flag2))
       || (pktcnt == 3'h4)
) begin
```

5. Save your changes and exit the text editor.

You can now compile and simulate your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status

This issue is fixed in version 9.1 SP1 of the RapidIO MegaCore function.

Response Packet is Sent for Request Packet with Reserved Transaction Type

If the RapidIO MegaCore function receives a Type 2 (request class) Input/Output request packet with a reserved transaction type, the Input/Output Avalon-MM master Logical layer module generates an ERROR response packet.

Affected Configurations

All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

The link partner receives a potentially unexpected response packet, which may cause it to incorrectly detect an error in the RapidIO MegaCore function.

Workaround

Avoid sending Type 2 request packets with a reserved transaction type to the RapidIO MegaCore function.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Specific Variation With Transaction Ordering Enabled Requires Additional Logical Layer Modules

Specific RapidIO variations with transaction ordering enabled (**Prevent doorbell messages from passing write transactions** is turned on in the RapidIO MegaWizard interface) require that the variation implement at least one of an Input/Output Avalon-MM master Logical layer module, or the receive functionality of the Doorbell module.

Affected Configurations

RapidIO ×4 variations at 5.0 GBaud, for which you select **Prevent doorbell messages from passing write transactions** in the RapidIO MegaWizard interface, but for which you do not select **Doorbell Rx enable**, that do not implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

A design that contains one of these variations does not operate properly.

Workaround

To avoid this issue, in the RapidIO MegaWizard interface, if you turn on **Prevent doorbell messages from passing write transactions**, you must also specify **Avalon-MM Master and Slave** in the **I/O Logical Layer Interfaces** field, or turn on **Doorbell Rx enable**.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Some Variations Do Not Meet Timing Requirements

Some specific RapidIO MegaCore function variations that use the high-speed transceivers on an Arria II GX or Stratix IV GX device, cause the TimeQuest timing analyzer to issue critical timing warnings. For these variations, by default, the MegaWizard performs an incorrect internal parameter computation for the transceiver.

Affected Configurations

The following configurations have this issue:

- RapidIO ×4 variations at data rate 3.125 GBaud with reference clock frequency 390.625 MHz, that use the high-speed transceivers on an Arria II GX or Stratix IV GX device.
- RapidIO ×1 and ×4 variations at data rate 5.0 GBaud with reference clock frequency 500 MHz, that use the high-speed transceivers on a Stratix IV GX device.

Design Impact

Because these variations do not meet timing requirements, a design that contains one of these variations cannot compile successfully.

Workaround

To avoid this issue, perform the following workaround to regenerate the high-speed transceiver:

1. In the Quartus II software, on the Tools menu, click **MegaWizard Plug-In Manager**.
2. In the MegaWizard Plug-In Manager, turn on **Edit an existing custom megafunction variation**.
3. Click **Next**.
4. In the File name field, select the file <*RapidIO_instance_name*>**_riophy_gxb.v**.
5. Click **Next**.
6. To regenerate the RapidIO MegaCore function high-speed transceiver with the issue resolved, click **Finish**.

   You can now compile your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Some Variations With High Reference Clock Frequency Generate Critical Timing Warnings

RapidIO MegaCore function variations with reference clock frequency higher than 260 MHz that target an Arria II GX or Stratix IV GX device cause the TimeQuest timing analyzer to issue the following critical warning:

```
Critical Warning: Found minimum pulse width or period
violations. See Report Minimum Pulse Width for details.
```

The warning occurs because the reference clock input pin is set to the 2.5 V I/O pin standard by default, and this I/O pin standard requires a minimum pulse width of 3.826 µs, which corresponds to 260 MHz.

Affected Configurations

All RapidIO variations with reference clock frequency higher than 260 MHz that target an Arria II GX or Stratix IV GX device.

Design Impact

Designs that contain any of these RapidIO variations cannot compile with the default I/O standard assignments.

Workaround

To avoid this issue, in the Assignment Editor, assign the reference clock pin to the LVDS I/O standard.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Errored NREAD Response Can Have Wrong Transaction ID

If the RapidIO MegaCore function receives an errored NREAD request, followed immediately by another I/O request, the RapidIO MegaCore function's ERROR response for the errored NREAD request contains the transaction ID of the following I/O request.

Affected Configurations

All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

In all cases, the logical layer modules recover. Specifically, the following actions occur:

- The link partner never receives a response to the errored NREAD response, and eventually the transaction times out. The action of the link partner in response to the timeout should be the same as its reaction to an ERROR response.
- The link partner receives an ERROR response to the following I/O request. If the original request does not require a response, the link partner should ignore the ERROR response. If the original request does require a response, it receives the erroneous ERROR response followed by an unexpected correct response.

Workaround

None known. However, in all cases the logical layer modules recover.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function.

Reception of Six or More Consecutive Control Symbols Can Cause Some of the Received Control Symbols To Be Lost

When six or more consecutive control symbols are received back-to-back with no intervening IDLE or packet data, an internal buffer overflows and some control symbols are lost.

Affected Configurations

All 4× RapidIO variations.

Design Impact

The impact of this sequence of events varies according to the type of control symbol that is lost. Possible effects include: no impact at all, an unexpected link timeout, or the declaration of a fatal error with its side effects, clearing of buffers and resetting of state machines.

Workaround

If possible, avoid sending more than five control symbols back-to-back or use 1× variations.

In practice, this sequence of events has been observed when the RapidIO MegaCore function sends a sequence of read requests to a link partner that does not embed the acknowledgement control symbol `packet-accepted` in the read responses, so that many read request acknowledgement symbols are queued up and then sent consecutively between read responses. To avoid the issue in this particular situation, ensure that only four read requests are outstanding at any time.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function.

Error Response Packet Can Be Sent Twice if the io_m_rd_readerror Signal is Asserted

If the `io_m_rd_readerror` signal is asserted, an error response packet can be sent twice.

Affected configurations

All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design impact

If a read response with ERROR status is transmitted twice, the link partner receives it twice. In that case, the link partner detects an unexpected error response.

Workaround

To avoid this issue, perform one of the following workarounds:

- Do not assert the `io_m_rd_readerror` signal.
- Ensure that reception of an unexpected response packet by the link partner has only benign effects.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function.

User Guide Description of Direction of io_s_rd_read Signal is Incorrect

The Input/Output Avalon-MM slave Logical layer signal `io_s_rd_read` is listed incorrectly in the *RapidIO MegaCore Function User Guide* as an output signal. This read enable signal is an input signal to the Input/Output Avalon-MM slave Logical layer module.

Affected Configurations

All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

Relying on the `io_s_rd_read` read enable signal of an Input/Output Avalon-MM slave Logical layer module to be driven by that module leads to incorrect results.

Workaround

Expect this signal to be an input signal to the Input/Output Avalon-MM slave Logical layer module.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore Function User Guide.

SOPC Builder Testbench May Fail on 1× Stratix GX Variations at 1.25 GBaud

For some 1× RapidIO variations at 1.25 GBaud that use the built-in high-speed transceivers on Stratix GX devices, simulation of the SOPC Builder customer testbench fails, because the testbench dictates a clock frequency that does not match the transceiver clock setting. The problem exists only for the testbench generated for a RapidIO variation with Physical, Transport, and Logical layers.

Affected Configurations

Some 1× RapidIO variations that use the built-in high-speed transceivers on Stratix GX devices.

Design Impact

SOPC Builder system testbench simulation fails for the affected configurations.

Workaround

In the Quartus II project directory, open the file <*RapidIO variation name*>**_hookup.iv** in a text editor, and locate the following code:

```
forever begin
   # <wait time number>;
   clk <= ~clk;
end
```

Replace <*wait time number*> in this code with the value 8.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function.

Migration of Existing RapidIO MegaCore Function May Generate Warning Message

When you migrate your design between device families, you must change the high-speed transceiver types of your RapidIO MegaCore functions to match the new device family. Doing so generates a warning message and does not modify the intended device for the RapidIO MegaCore function as a whole. Modifying the device for the MegaCore function requires that you edit an HDL file.

Affected Configurations

All RapidIO variations.

Design Impact

Changing the high-speed transceiver type of your RapidIO MegaCore function without implementing the workaround causes compilation to fail, because the RapidIO MegaCore function target device and its high-speed transceiver target device are different.

Workaround

To modify the target device for your RapidIO MegaCore function and for its high-speed transceiver, perform the following workaround:

1. In a text editor, open the file <*RapidIO_instance_name*>**.v** or <*RapidIO_instance_name*>**.vhd** for editing.
2. Search for the following two lines in the file:

```
//Retrieval info:<PRIVATE name = "intended_family" value ="<family>"
type="STRING" enable="1" />
```

and

```
//Retrieval info:<PRIVATE name = "phy_selection" value ="<PHY>"
type="STRING" enable="1" />
```

3. In these two lines of code, substitute the new target device family value for <*family*> and <*PHY*> according to Table 19–3.

Table 19–3. New Values for intended_family and phy_selection

New Target Device Family	<*family*> Value	<*PHY*> Value
Arria GX	`Arria GX`	`stratixiigxlite`
Arria II GX	`Arria II GX`	`arriaiigx`
Stratix II GX	`Stratix II GX`	`stratixiigx`
Stratix IV GX	`Stratix IV`	`stratixivgx`

4. Save and close the file.
5. In the Quartus II software, on the Tools menu, click **MegaWizard Plug-In Manager**.
6. In the MegaWizard Plug-In Manager, turn on **Edit an existing custom megafunction variation**.
7. Click **Next**.
8. In the File name field, select the file <*RapidIO_instance_name*>**.v**.

9. Click **Next**.
10. To regenerate the RapidIO MegaCore function and its high-speed transceiver for the new target device family, click **Finish**.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function.

Receipt of a Write Request for 5, 6, or 7 Bytes by the I/O Master Causes an Invalid Avalon-MM Burst Transaction

If a RapidIO Input/Output Avalon-MM master Logical layer module in a 1× (32-bit wide) RapidIO MegaCore variation receives an `NWRITE` or `NWRITE_R` write request for 5, 6, or 7 bytes of data, the module creates an invalid Avalon-MM burst transaction. The module translates the request to a burst with burstcount value 2 but with different byteenable values in the two cycles. The Avalon-MM interface specification requires that a burst have a uniform byteenable value.

Affected Configurations

All RapidIO 1× variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

When this violation of the Avalon-MM interface specification occurs, the behavior of an Avalon-MM slave connected to this Avalon-MM master is undefined.

Workaround

Avoid sending write requests for 5, 6, or 7 bytes in the system, or add a small adapter to translate these two-word bursts to two single-word transfers.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function.

Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets

The RapidIO Input/Output Logical layer Avalon-MM slave can generate an incorrect write request packet if an invalid combination of burstcount, byteenable, and address is applied to the datapath write Avalon-MM slave interface.

Affected Configurations

This issue affects all variations that include the Input/Output logical layer module.

Design Impact

An incorrect write request packet can be sent. This incorrect packet may cause further complications in the attached devices.

Workaround

Avoid using invalid combinations of burstcount, byteenable, and address. The valid combinations are described in the "Avalon-MM Burstcount and Byteenable Encoding in RapidIO Packets" section in the *Functional Description* chapter of the *RapidIO MegaCore Function User Guide*.

Solution Status

This issue is fixed in version 9.1 of the RapidIO MegaCore function. Table 4-14 and Table 4-16 in the *RapidIO MegaCore Function v9.1 User Guide* document the allowed combinations of burstcount, byteenable, and address. Other combinations flag interrupts in the RapidIO MegaCore function.

Stratix III Device Support Level is Reported as Preliminary

The RapidIO MegaCore function v9.0 includes full support for Stratix III devices. However, when you target a design with a RapidIO MegaCore function v9.0 to a Stratix III device in the Quartus II software v9.0, an error message indicates support is preliminary rather than full.

Affected Configurations

All RapidIO variations targeted to a Stratix III device.

Design Impact

None.

Workaround

Ignore the warning message about the support level.

Solution Status

This issue is fixed in version 9.0 SP2 of the RapidIO MegaCore function.

Transport Layer Can Drop Outgoing Packets if Physical Layer Transmit Buffer Fills

If packets are transferred back-to-back from a Logical layer module to the Transport layer—the end-of-packet word of one packet is followed immediately by the start-of-packet word of another packet—and the value of the Physical layer transmit buffer output signal `atxwlevel` becomes 10 in the same cycle in which the end-of-packet word is transferred from the Logical layer to the Transport layer, the following packet is dropped silently.

Affected Configurations

All RapidIO variations that implement a Logical layer module.

Design Impact

Outgoing packets might be lost. The problem has been observed only with packets whose data payload is approximately 80 bytes.

Workaround

To avoid the problem, perform one of the following workarounds:

- Ensure that the Physical layer transmit buffer `atxwlevel` signal value remains greater than 10.
- Ensure a gap of at least one clock cycle between packets from the same Logical layer module to the Transport layer.

Solution Status

This issue is fixed in version 9.0 SP1 of the RapidIO MegaCore function.

Testbench Fails on Some Stratix GX Variations

For some variations that use the built-in high-speed transceivers on Stratix GX devices, simulation of either customer testbench fails, because the testbench dictates a clock frequency that does not match the transceiver clock setting. The problem exists for both the Physical-layer-only testbench and the testbench generated for a RapidIO variation with Physical, Transport, and Logical layers.

Affected Configurations

The following RapidIO variations that use the built-in high-speed transceivers on Stratix GX devices are affected:

- ×1 variation at 3.125 GBaud
- ×4 variation at 1.25 GBaud
- ×4 variation at 3.125 GBaud

Design Impact

Testbench simulation fails for the affected configurations. The problem exists for both the Physical-layer-only testbench and the SOPC Builder system testbench.

Workaround

In the Quartus II project directory, open the file <*RapidIO variation name*>**_hookup.iv** in a text editor, and locate the following code:

```
forever begin
   # <wait time number>;
   clk <= ~clk;
end
```

Replace <*wait time number*> in this code according to Table 19–4:

Table 19–4. Correct <wait time number> Values

Number of Channels	Data Rate (GBaud)	Correct <*wait time number*> Value
1	3.125	3.2
4	1.25	8
4	3.125	3.2

Solution Status

This issue is fixed in version 9.0 SP1 of the RapidIO MegaCore function.

Some Variations With Reference Clock Frequency 390.625 MHz do Not Meet Timing

Some RapidIO MegaCore function variations do not meet timing requirements initially.

Affected Configurations

4× RapidIO variations with reference clock frequency 390.625 MHz that use high-speed transceivers and are targeted to Arria II GX and Stratix IV devices.

Design Impact

Because these variations do not meet timing requirements, a design that contains one of these variations cannot compile successfully.

Workaround

To avoid this issue, perform the following workaround to regenerate the high-speed transceiver:

1. In the Quartus II software, on the Tools menu, click **MegaWizard Plug-In Manager**.
2. In the MegaWizard Plug-In Manager, turn on **Edit an existing custom megafunction variation**.
3. Click **Next**.
4. In the File name field, select the file <*RapidIO_instance_name*>**_riophy_gxb.v**.
5. Click **Next**.
6. On the **Parameter Settings** tabs, click **Next** repeatedly until you reach the **RX Analog** tab.
7. To regenerate the RapidIO MegaCore function high-speed transceiver with the issue resolved, click **Finish**.

   You can now compile your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status

This issue is fixed in version 9.0 SP1 of the RapidIO MegaCore function.

SourceID Can Be Incorrectly Set to Zero in NWRITE_R Response Packets

The `SourceID` field in an `NWRITE_R` response packet might be set to zero instead of being set to the destination ID received in the request packet.

Affected Configurations

All RapidIO variations that implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

If a link partner sends an `NWRITE_R` request and detects an erroneous `SourceID` in the response on the link, it might not recognize the response to the request.

Workaround

To avoid this issue, perform one of the following workarounds:

- Generate NWRITE or SWRITE requests instead of NWRITE_R requests.
- Precede each sequence of NWRITE_R requests to the same destination ID with an NREAD request to that destination ID.
- Program the link partner to accept response packets regardless of their SourceID.

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

A Cancelled Packet Can Be Processed As a Normal Packet

If a packet received over the RapidIO link contains a stomp control symbol, and this packet is immediately followed by a start-of-packet control symbol, the first packet might be processed as if it were not cancelled.

Affected Configurations

All 4× RapidIO variations.

Design Impact

The final two bytes of the cancelled packet are treated as the CRC of the cancelled packet. In most cases, a CRC error is detected, the packet is dropped, and the error recovery process is initiated. In the rare case that the final two bytes form a valid CRC for the packet, the partial packet is processed as if it were not cancelled.

Workaround

None known.

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Asserting io_m_wr_waitrequest During a Burst Transfer When io_m_wr_write is Not Asserted Can Cause Deadlock

If a slave driven by an Avalon-MM I/O master asserts the io_m_wr_waitrequest signal during a burst transfer when io_m_wr_write is not asserted, the Avalon-MM I/O master module will not assert the io_m_wr_write signal until io_m_wr_waitrequest is deasserted. In this case, the Avalon-MM interface deadlocks.

Affected Configurations

All RapidIO variations that implement an Avalon-MM I/O master write interface.

Design Impact

If the slave waits for the assertion of io_m_wr_write before deasserting the io_m_wr_waitrequest signal, and the master waits for the deassertion of io_m_wr_waitrequest before asserting io_m_wr_write, the module deadlocks.

Workaround

Do not assert `io_m_wr_waitrequest` indefinitely, or avoid asserting `io_m_wr_waitrequest` after a burst transfer has started.

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Four Back-to-Back Short Incoming Packets Can Cause Miscalculation of the Following Packet Sizes

If four short packets are transferred back-to-back from the Physical layer to the Transport layer, the size of subsequent packets can be miscalculated. This problem occurs only following a complex sequence of events followed by the receipt of four short back-to-back packets on the RapidIO link, and is therefore unlikely to occur.

Affected Configurations

All 4× RapidIO variations that implement a Transport layer.

Design Impact

If this problem occurs, the resulting erroneous packet sizes can cause Input/Output modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible impacts.

Workaround

To reduce the chance of encountering this issue, you can modify your application to reduce the number of back-to-back packet transfers from the Physical layer to the Transport layer, by preventing received packets from accumulating in the Physical layer Receive buffer.

For example, either of the following two modifications helps to avoid the accumulation of packets in the Physical layer Receive buffer:

- Run the system clock at the nominal clock frequency or higher.
- To decrease the back pressure that occurs when the Avalon-MM wait-request signals are asserted, do not assert these signals.

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

An Errored Incoming Packet Can Cause Miscalculation of the Following Packet Sizes

If a packet marked as errored is transferred from the Physical layer to the Transport layer immediately following a valid packet, with no gap between the end of the first packet and the start of the second packet, the size of subsequent packets can be miscalculated.

Affected Configurations

All RapidIO variations that implement a Transport layer.

Design Impact

Erroneous packet sizes can cause Input/Output modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible impacts.

Workaround

You can modify your application to reduce the chance of encountering this issue, and you can perform a workaround that avoids the issue.

To reduce the chance of encountering this issue, you can modify your application in one or both of the following ways:

- Reduce the bit-error rate to reduce the number of errored packets received by the Transport layer.
- Reduce the number of back-to-back packet transfers from the Physical layer to the Transport layer, by preventing received packets from accumulating in the Physical layer Receive buffer. Either of the following two modifications helps to avoid the accumulation of packets in the Physical layer Receive buffer:
  - Run the system clock at the nominal clock frequency or higher.
  - To decrease the back pressure that occurs when the Avalon-MM wait-request signals are asserted, do not assert these signals.

To avoid the issue, perform the following workaround:

1. Use the MegaWizard interface to specify the parameters of your RapidIO MegaCore function.
2. Perform one of the following steps:
   - In SOPC Builder, click **Generate** to generate the SOPC Builder system.
   - In the MegaWizard Plug-In Manager, click **Finish** to generate the RapidIO MegaCore function.

   The MegaWizard interface generates the Transport layer Verilog HDL file **transport.v**.
3. Open the newly generated **transport.v** file for editing.
4. Replace
   ```
   _Fstart_waddr = waddr ;
   ```
   with
   ```
   _Fstart_waddr = waddr + wren;
   ```

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Timeout Logic Can Incorrectly Extend Doorbell Transaction Timeout Period

When a `DOORBELL` transaction is transmitted, it is assigned a timeout value based on the Port Response Time-Out Control register (offset `0x124`) and a free-running counter. When the counter reaches the timeout value, if the `DOORBELL` transaction has not yet received a response, the transaction times out. In the slowest case, the free-running counter increments every 64 Avalon clock cycles.

If DOORBELL transactions are transmitted fewer than 64 Avalon clock cycles apart, multiple transactions might be assigned the same timeout value. If processing the timeout for the previous DOORBELL transactions with the same timeout value takes too long, a DOORBELL transaction's timeout might not be processed before the counter increments. In this case, the timeout is not recognized until the counter rolls over again to the same value. In addition, the timeout logic processes the pending transactions in FIFO order, and therefore does not examine the remaining pending DOORBELL transactions before the counter rolls over again.

Affected Configurations

All RapidIO variations that implement a Doorbell module.

Design Impact

A DOORBELL transaction might not time out when expected, holding up the timeout queue and preventing the Doorbell module from transmitting new transactions in a timely manner.

Workaround

To avoid this issue, ensure a wait of at least 64 Avalon clock cycles between transmission of DOORBELL transactions.

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Doorbell Transaction Can Be Transmitted With Invalid Transaction ID

A 17th pending DOORBELL transaction can have an invalid transaction ID. After reset, a counter generates 16 transaction IDs for the first 16 DOORBELL transactions. When a Doorbell response packet arrives at the Doorbell module, the transaction ID for the originating transaction is recycled through a FIFO and made available for a new pending DOORBELL transaction. However, a 17th pending DOORBELL transaction may use an underflowed TID FIFO output and be assigned a random value for its transaction ID.

Affected Configurations

All RapidIO variations that implement a Doorbell module.

Design Impact

A DOORBELL transaction can be transmitted with an invalid transaction ID. In this case, its response may not be identified correctly, and the Doorbell module can deadlock.

Workaround

To avoid this issue, ensure that 15 or fewer DOORBELL transactions are pending responses before you transmit the 17th DOORBELL transaction.

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

User Guide Description of Default Value of EF_ID Field in PHEAD0 Register is Incorrect

The default value of the `EF_ID` field in the PHEAD0 register (offset `0x100`), is listed incorrectly in the *RapidIO MegaCore Function User Guide*. The correct value is `0x0001`.

Affected Configurations

All RapidIO variations.

Design Impact

Relying on the default value for the `EF_ID` field in the PHEAD0 register to be the value specified in the *RapidIO MegaCore Function User Guide* leads to incorrect results.

Workaround

Expect the default value `0x0001` in this register field.

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

SOPC Builder Systems May Have Incorrectly Clocked Reset or Incorrect Calibration Clock Driver

A RapidIO transceiver-based system created in SOPC Builder might generate RTL with the source reset clock in the incorrect clock domain, or might connect the calibration clock port incorrectly.

Affected Configurations

All RapidIO variations with high-speed transceivers in SOPC Builder systems with multiple clocks.

Design Impact

If the calibration clock is driven by the wrong clock, transceiver calibration can fail, leading to hardware failures.

If the reset is driven by an incorrect clock, intermittent hardware failures may occur.

Workaround

If your design allows, you can avoid this issue by using a single clock for all components in your SOPC Builder system. However, `cal_blk_clk` runs at a maximum frequency of 125 MHz, and all transceiver-based designs in your system must have the same calibration clock. Therefore, not all designs admit this solution.

If you must implement multiple clocks in your design, perform the following alternate workaround to ensure your design is not impacted by this issue.

To determine whether the clock connections in your design are impacted by this issue, and fix them if needed, perform the following steps:

1. Open your SOPC Builder project.

2. In SOPC Builder, click **Generate**.

   SOPC Builder writes the top-level system file **<***SOPC_system_name***>.v** or **<***SOPC_system_name***>.vhd**, depending on the HDL you use.

3. Click **Exit**.
4. Open the newly generated top-level system **.v** or **.vhd** file for editing.
5. Search for the string `the_rapidio` to locate all your RapidIO MegaCore function instances.
6. For each instance, examine the signal connected to the `cal_blk_clk` port. In Verilog HDL, the relevant code line is similar to the following:

   ```
   .cal_blk_clk (cal_blk_clk),
   ```

7. If the name in parentheses is not that of the calibration clock you want to connect to this port, replace it with your intended calibration clock.
8. For each instance, examine the signal connected to the `reset_n` port. In Verilog HDL, the relevant code line is similar to the following:

   ```
   .reset_n (clk_0_reset_n),
   ```

9. If the clock name in the signal name in parentheses is not that of the clock connected to the Avalon system clock, replace it with the Avalon system clock. The following code line results:

   ```
   .reset_n (<sysclk_name>_reset_n),
   ```

Solution Status

This issue is fixed in version 9.0 of the RapidIO MegaCore function.

Stratix IV Simulations May Fail With ModelSim 6.3g Compiler Optimizations Enabled

Simulation of a RapidIO MegaCore function targeted to a Stratix IV device using ModelSim 6.3g with compiler optimizations enabled, may fail. Compiler optimizations are enabled by default in this version of ModelSim.

Affected Configurations

All RapidIO variations that target a Stratix IV device.

Design Impact

The IP functional simulation model of an affected configuration may produce data errors if simulated using ModelSim 6.3g.

Workaround

To avoid this issue, perform one of the following workarounds:

- Disable the ModelSim compiler optimizations by adding the `-novopt` switch to the `vsim` command, in the *<variant>***_run_modelsim.tcl** script or when you call `vsim` from the command line.
- Use ModelSim 6.4a or later.

Solution Status

The issue is fixed in ModelSim 6.4a.

20. QDRII SRAM

Revision History

Table 20–1 shows the revision history for the QDRII SRAM MegaCore function.

For more information about the new features, refer to the *QDRII SRAM MegaCore Function User Guide*.

Table 20–1. QDRII SRAM MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Maintenance release.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	November 2008	Maintenance release.

Errata

Table 20–2 shows the issues that affect the QDRII SRAM MegaCore functionv9.1, v9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the QDRII SRAM MegaCore function.

Table 20–2. QDRII SRAM MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Jul 09	Incorrect User Guide on ACDS	—	Fixed	✓	—	—
15 May 08	Termination Error When Compiling Design	✓	✓	✓	✓	✓
01 Dec 06	Incorrect IP Toolbench Latency Behavior	✓	✓	✓	✓	✓
01 Nov 06	Simulating with the VCS Simulator	✓	✓	✓	✓	✓
	TimeQuest Timing Analyzer Failure	✓	✓	✓	✓	✓
	PLL Placement	✓	✓	✓	✓	✓
01 Nov 05	Constraints Errors With Companion Devices	✓	✓	✓	✓	✓
	Supported Device Families	✓	✓	✓	✓	✓
	Compilation Error (Stratix II Series & HardCopy II Devices Only)	✓	✓	✓	✓	✓
	Gate-Level Simulation Filenames	✓	✓	✓	✓	✓
	The ModelSim Simulation Script Does Not Support Companion Devices	✓	✓	✓	✓	✓

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *QDRII SRAM MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the QDRII SRAM MegaCore function.

Termination Error When Compiling Design

The Fitter reports the following error: "`Error Bidirectional I/O "cq" uses the parallel termination but does not have dynamic termination control.`"

Affected Configurations

This issue affects designs using the QDRII SRAM Controller.

Design Impact

The design fails to fit.

Workaround

At top-level design, change the pin direction from inout to input for
`- qdrii_cq_<index>; qdrii_cqn_<index>`.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Incorrect IP Toolbench Latency Behavior

When you open the IP Toolbench Parameterize window, you can select any latency for the default **QDRII**, but it only supports 1.5.

Affected Configurations

This issue affects all QDRII SRAM configurations.

Design Impact

IP Toolbench does not generate a variation and gives the following error message:

```
MegaCore Function Generation Error
IP Functional Simulation creation Failed. The following error was
returned:
Error: Top-level design entity
"qdr_auk_qdrii_sram_avalon_controller_ipfs_wrap" is undefined.
```

Workaround

For longer latency, select **QDRII+**.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Simulating with the VCS Simulator

The QDRII SRAM Controller MegaCore function does not support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

There is no workaround for VHDL simulations. For Verilog HDL simulations. Change line 154 in the **qdrii_model.v** file to:

```
begin : f1
```

Also, change line 417 to:

```
begin : f2
```

Solution Status

This issue will not be fixed.

TimeQuest Timing Analyzer Failure

When you use the Quartus II TimeQuest timing analyzer, it reports a recovery issue, because the reset is not in the same clock domain as the system clock.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

Change the reset sequence for the signals clocked on the CQ clock, before you run the TimeQuest timing analyzer.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

PLL Placement

The IP Toolbench-generated example design uses a PLL phase shift of 90°, which can cause the design to fail hold timing analysis. The source synchronous PLL for the read capture should have a location constraint to place it on the same side of the device as the Q pins; otherwise, the source synchronous compensation does not compensate for the expected delays.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails hold timing analysis.

Workaround

The PLL must be located on the same side of the device as the CQ/CQn groups, for the PLL to compensate properly.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Constraints Errors With Companion Devices

When you change the device in your project or add a HardCopy II companion device to a Stratix II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails.

Workaround

Reassign the byte groups for the new device in the constraints editor.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Supported Device Families

The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot compile a design.

Workaround

Ensure you choose a supported device family for the Quartus II project.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Compilation Error (Stratix II Series & HardCopy II Devices Only)

The IP Toolbench Constraints window allows the illegal situation where you can share DQ groups on the top and bottom banks for Stratix II series and HardCopy devices. When you compile your design the Quartus II software issues a no fit error.

Affected Configurations

This issue affects all DQS mode QDRII SRAM controllers on Stratix II series and HardCopy II devices.

Design Impact

When you choose **Start Compilation**, there is an error message and the design does not compile.

Workaround

If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytegroups on either the top or the bottom of the device, but not both.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects <*project name*>**.vho** or .**vo** and <*project name*>**_v** or **_vhd.sdo** files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename <*filename*>**.vho** file to <*project name*>**.vho.**
2. Rename <*filename*>**.sdo** file to <*project name*>**_vhd.sdo**.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename the <*filename*>**.vo** file to <*project name*>**.vo.**
2. Rename the <*filename*>**.sdo** file to <*project name*>**_v.sdo**.
3. In the <*project name*>.**vo** file change the following line to point to the <*project name*>**_v.sdo** file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

The ModelSim Simulation Script Does Not Support Companion Devices

If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

Affected Configurations

This issue affects designs with companion devices.

Design Impact

The simulation script does not run.

Workaround

Edit the ModelSim script to include the correct libraries.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

21. QDR II and QDR II+ SRAM Controller with UniPHY

Revision History

Table 21–1 shows the revision history for the QDR II and QDR II+ SRAM Controller with UniPHY.

For more information about the new features, refer to the *QDR II and QDR II+ SRAM Controller with UniPHY User Guide*.

Table 21–1. QDR II and QDR II+ SRAM Controller with UniPHY Revision History

Version	Date	Description
9.1	November 2009	First release.

Errata

Table 21–2 shows the issues that affect the QDR II and QDR II+ SRAM Controller with UniPHY v9.1.

Not all issues affect all versions of the QDR II and QDR II+ SRAM Controller with UniPHY.

Table 21–2. QDR II and QDR II+ SRAM Controller with UniPHY Errata

Added or Updated	Issue	Affected Version
		9.1
15 Nov 09	UniPHY DQS Clock Buffer Location	✓
	IP Functional Simulation Model	✓
	No Link to User Guide from Wizard	✓
	Incorrect Operation of Waitrequest Signal	✓
	QDR II SRAM Emulated Mode	✓

UniPHY DQS Clock Buffer Location

The DQS clock buffer location for the UniPHY can cause hold time violations when placed suboptimally. The Quartus II software may suboptimally place the DQS clock buffer on a global or dual-regional clock after reentering the FPGA, so that it can be routed to the write side of the read capture FIFO.

Affected Configurations

The issue affects all configurations.

Design Impact

You may see hold time failures on the capture clocks in core logic.

Workaround

Create a location assignment on the buffer to the same edge as the memory interface (for example `EDGE_BOTTOM`).

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

IP Functional Simulation Model

The wizard-generated IP functional simulation model (**.vho**) file for VHDL designs is functionally incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use an IP functional simulation model to simulate your design.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

No Link to User Guide from Wizard

The wizard does not have a link to the *QDR II and II+ SRAM Controller with UniPHY User Guide*.

Affected Configurations

The issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Access the *QDR II and II+ SRAM Controller with UniPHY User Guide* from the Altera website.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Incorrect Operation of Waitrequest Signal

The IP does not correctly assert the Avalon-MM `waitrequest` signal, when the interface is reset.

Affected Configurations

This issue affects designs that try and send Avalon-MM data to the interface while the interface is in reset.

Design Impact

As the interface does not assert `waitrequest` it does not observe Avalon-MM transactions sent to it while reset is asserted.

Workaround

The workaround for this issue is to not send Avalon-MM transactions to the interface while reset is asserted.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

QDR II SRAM Emulated Mode

If you turn on **×36 emulated mode**, you must change the **CQ Width** to 2.

Affected Configurations

The issue affects all ×36 emualated designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

22. Reed-Solomon Compiler

Revision History

Table 22–1 shows the revision history for the Reed-Solomon Compiler.

For more information about the new features, refer to the *Reed-Solomon Compiler User Guide*.

Table 22–1. Reed-Solomon Compiler Revision History

Version	Date	Description
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Full support for Stratix III devices.

Errata

Table 22–2 shows the issues that affect the Reed-Solomon Compiler v9.1, v9.0 SP1, v9.0, and v8.1.

Not all issues affect all versions of the Reed-Solomon Compiler.

Table 22–2. Reed-Solomon Compiler Errata

Added or Updated	Issue	Affected Version			
		9.1	9.0 SP1	9.0	8.1
15 Mar 09	User Guide Link from IP Toolbench is Inactive	—	Fixed	✓	—
01 Nov 08	Verilog HDL Simulation Fails	✓	✓	✓	✓
	RS Decoder Fails When Number of Check Symbols and Symbols are Similar	✓	✓	✓	✓

User Guide Link from IP Toolbench is Inactive

In IP Toolbench, if you click the **Document** tab the link to the *Reed-Solomon Compiler User Guide* is inactive.

Affected Configurations

This issue affects all variable decoder designs.

Design Impact

This issue has no design impact.

Workaround

You can access the current *Reed-Solomon Compiler User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP1 of the Reed-Solomon Compiler.

Verilog HDL Simulation Fails

Running a simulation with the Verilog HDL testbench results in an empty **summary_output.txt** file.

Affected Configurations

This issue affects all Verilog HDL configurations.

Design Impact

You cannot use the **summary_output.txt** file to evaluate the functionality of the design. But you can evaluate the functionality by looking at the simulation waveform.

Workaround

Run the simulation with a VHDL design and use the VHDL testbench.

Solution Status

This issue will be fixed in a future release of the Reed-Solomon Compiler.

RS Decoder Fails When Number of Check Symbols and Symbols are Similar

With the variable decoder, when the **Number of check symbols** and **Symbols per codeword** values are similar, for example, 5 and 6, respectively, the Avalon-ST interface on the source side fails and the `sop` and `eop` overlap.

Affected Configurations

This issue affects all Verilog HDL variable decoder designs.

Design Impact

The design fails simulation.

Workaround

To avoid this issue, create a VHDL design model and use the VHDL testbench.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon Compiler.

23. RLDRAM II

Revision History

Table 23–1 shows the revision history for the RLDRAM II MegaCore function.

For more information about the new features, refer to the *RLDRAM II MegaCore Function User Guide*.

Table 23–1. RLDRAM II MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Maintenance release.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	15 November 2008	Maintenance release.

Errata

Table 23–2 shows the issues that affect the RLDRAM II MegaCore function v9.1, 9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the RLDRAM II MegaCore function.

Table 23–2. RLDRAM II MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 Nov 09	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓	✓	✓
	Hold Timing Violation	✓	✓	✓	✓	✓
01 Jul 09	Incorrect User Guide on ACDS	—	Fixed	✓	—	—
15 Mar 09	RLDRAM II Verilog HDL Design Does Not Work	—	—	—	Fixed	✓
01 Dec 06	NativeLink Fails with the ModelSim Simulator	✓	✓	✓	✓	✓
01 Nov 06	Add an RLDRAM II Controller to a Project with Other Memory Controllers	✓	✓	✓	✓	✓
	Simulating with the NCSim Software	✓	✓	✓	✓	✓
	Simulating with the VCS Simulator	✓	✓	✓	✓	✓
	Multiple Instances of the auk_ddr_functions.vhd File	✓	✓	✓	✓	✓
	Gate-Level Simulation Filenames	✓	✓	✓	✓	✓
	Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)	✓	✓	✓	✓	✓
	Editing the Custom Variation (non-DQS Mode)	✓	✓	✓	✓	✓

The Quartus II Design Assistant Reports Critical Warning

When you compile a design with the RLDRAM II controller, the Quartus II Design Assistant reports design the following warnings:

```
Critical Warning: (High) Rule R101: Combinational logic used as a reset
signal should be synchronized. Found 1 node(s) related to this rule.
```

```
Warning: (Medium) Rule C104: Clock signal source should drive only clock
input ports. Found 2 nodes related to this rule.
```

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Hold Timing Violation

Hold timing violation occurs on the DQS clock reported in fast-corner timing report.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Disable the global clock promotion on `dqs_clk` by adding the following assignment in the Quartus II settings file (**.qsf**):

```
set_instance_assignment -name GLOBAL_SIGNAL OFF -to "<variation
name>_wrapper:<variation
name>|<variation name>_auk_rldramii_datapath:rldramii_io|<variation
name>_auk_rldramii_dqs_group:auk_rldramii_dqs_group_*|dqs_clk[0]"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *RLDRAM II MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the RLDRAM II MegaCore function.

RLDRAM II Verilog HDL Design Does Not Work

If you generate a Verilog HDL instance of the RLDRAM II Controller version 8.1, the design will not work in hardware or simulation.

Affected Configurations

This issue affects all Verilog HDL configurations. VHDL designs are not affected.

Workaround

If you require a Verilog HDL instance of the RLDRAM II Controller MegaCore function, you can use one of the following workarounds:

- Continue to use your existing version 8.0 instance. There are no functional changes between versions 8.0 and 8.1 of the RLDRAM II Controller MegaCore function, so you are not required to upgrade.
- If you choose to update your existing instance or if you do not have a version 8.0 instance, change all instances of the line:

  ```
  else if (0)
  ```

  to

  ```
  else if (1)
  ```

  in the following files:

  - *<variation name>*_**auk_rldramii_addr_cmd_reg.v**
  - *<variation name>*_**auk_rldramii_dqs_group.v**
  - *<variation name>*_**auk_rldramii_pipeline_addr_cmd.v**
  - *<variation name>*_**auk_rldramii_pipeline_qvld.v**
  - *<variation name>*_**auk_rldramii_pipeline_rdata.v**
  - *<variation name>*_**auk_rldramii_pipeline_wdata.v**

  Some files may only require editing if pipeline options are enabled in your RLDRAM II Controller MegaCore variation.

Design Impact

Your design will not work in hardware or simulation.

Solution Status

This issue is fixed in version 9.0 of the RLDRAM II Controller MegaCore function.

NativeLink Fails with the ModelSim Simulator

When using NativeLink to run VHDL gate-level simulations using the ModelSim software, the simulation fails with the following error message:

```
# ** Error: (vcom-19) Failed to access library 'altera' at "altera".
```

Affected Configurations

The issue affects VHDL gate-level simulations.

Design Impact

The design does not simulate.

Workaround

The following lines need to be added to the NativeLink-generated gate-level simulation script:

```
vlib vhdl_libs/altera
vmap altera vhdl_libs/altera
vcom -work altera <Quartus installation
directory>/libraries/vhdl/altera/altera_europa_support_lib.vhd
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Add an RLDRAM II Controller to a Project with Other Memory Controllers

If you try to generate a new RLDRAM II controller in a project that already contains a DDR, DDR2, QDRII, or RLDRAM II controller, the example design gets corrupted and the compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not compile.

Workaround

To workaround this issue, follow these steps:

1. Generate the RLDRAM II controller in a new project and update the required project to instantiate the new RLDRAM II controller.
2. Copy the constraints from the new RLDRAM II project to the target project.

3. Copy the new RLDRAM II design files into the target project directory.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Simulating with the NCSim Software

The RLDRAM II Controller MegaCore function does not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Set the `-relax` switch for all calls to the VHDL or Verilog HDL analyzer.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Simulating with the VCS Simulator

The RLDRAM II Controller MegaCore function does not fully support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

For VHDL simulations, in the <*variation name*>**_example_driver.vhd** file, change all `when` statements from:

```
when std_logic_vector'("<bit_pattern>")
```

to:

```
when "<bit_pattern>"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Multiple Instances of the auk_ddr_functions.vhd File

When a project contains multiple memory MegaCore functions, the Quartus II project has multiple instances of the **auk_ddr_functions.vhd** file (one per MegaCore function).

Affected Configurations

This issue affects all configurations.

Design Impact

The Quartus II project fails during compilation.

Workaround

Remove the **auk_ddr_functions.vhd** file associated with the RLDRAM II controller from the list of files added to the Quartus II project, by choosing **Add/Remove Files from Project** on the Project menu. Keep only the **auk_ddr_functions.vhd** file associated with the DDR or DDR2 SDRAM controller.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause the Quartus II software to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects <*project name*>**.vho** or .**vo** and <*project name*>**_v** or **_vhd.sdo** files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory, follow these steps:

1. Rename <*filename*>**.vho** file to <*project name*>**.vho.**
2. Rename <*filename*>**.sdo** file to <*project name*>**_vhd.sdo**.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory, follow these steps:

1. Rename the <*filename*>**.vo** file to <*project name*>**.vo.**
2. Rename the <*filename*>**.sdo** file to <*project name*>**_v.sdo**.
3. In the <*project name*>.**vo** file, change the following line to point to the <*project name*>**_v.sdo** file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)

Gate-level simulations may not work as expected on HardCopy II devices, because HardCopy II timing is preliminary in the Quartus II software.

Affected Configurations

This issue affects all configurations on HardCopy II devices.

Design Impact

This issue has no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Editing the Custom Variation (non-DQS Mode)

When you generate a non-DQS mode custom variation with large databus widths, you may encounter one of the following characteristics when you try to edit the custom variation:

- IP Toolbench does not reload
- IP Toolbench reloads, but the databus width and constraints are set to the default for the selected RLDRAM II device
- IP Toolbench reloads, but the databus width is set to the default value for the selected RLDRAM II device and the constraints floorplan shows no chosen byte groups

Affected Configurations

This issue affects non-DQS mode designs only.

Design Impact

This issue has no design impact if you implement the workaround.

Workaround

Use one of the following workarounds:

- If IP Toolbench does not reload, you must regenerate a new custom variation and re-enter your parameters

- If IP Toolbench reloads, but the databus width and constraints are set to the default, reselect the databus width and rechoose the byte groups in the constraints floorplan
- If IP Toolbench reloads, but the databus width is set to the default and the constraints floorplan shows no byte groups, reselect the databus width and rechoose the byte groups in the constraints floorplan

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

24. RLDRAM II Controller with UniPHY

Revision History

Table 24–1 shows the revision history for the RLDRAM II Controller with UniPHY.

For more information about the new features, refer to the *RLDRAM II Controller with UniPHY User Guide*.

Table 24–1. RLDRAM II Controller with UniPHY Revision History

Version	Date	Description
9.1	November 2009	First release.

Errata

Table 24–2 shows the issues that affect the RLDRAM II Controller with UniPHY v9.1.

Not all issues affect all versions of the RLDRAM II Controller with UniPHY.

Table 24–2. RLDRAM II Controller with UniPHY Errata

Added or Updated	Issue	Affected Version
		9.1
15 Nov 09	UniPHY DQS Clock Buffer Location	✓
	IP Functional Simulation Model	✓
	No Link to User Guide from Wizard	✓
	Incorrect Operation of Waitrequest Signal	✓
	User Guide States Support for ×72 Devices	✓
	–18 Presets Give Errors	✓
	tQKH Parameter Incorrect	✓

UniPHY DQS Clock Buffer Location

The DQS clock buffer location for the UniPHY can cause hold time violations when placed suboptimally. The Quartus II software may suboptimally place the DQS clock buffer on a global or dual-regional clock after reentering the FPGA, so that it can be routed to the write side of the read capture FIFO.

Affected Configurations

The issue affects all configurations.

Design Impact

You may see hold time failures on the capture clocks in core logic.

Workaround

Create a location assignment on the buffer to the same edge as the memory interface (for example `EDGE_BOTTOM`).

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

IP Functional Simulation Model

The wizard-generated IP functional simulation model (**.vho**) file for VHDL designs is functionally incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use an IP functional simulation model to simulate your design..

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

No Link to User Guide from Wizard

The wizard does not have a link to the *QDR II and II+ SRAM Controller with UniPHY User Guide*.

Affected Configurations

The issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Access the *QDR II and II+ SRAM Controller with UniPHY User Guide* from the Altera website.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Incorrect Operation of Waitrequest Signal

The IP does not correctly assert the Avalon-MM `waitrequest` signal, when the interface is reset.

Affected Configurations

This issue affects designs that try and send Avalon-MM data to the interface while the interface is in reset.

Design Impact

As the interface does not assert `waitrequest` it does not observe Avalon-MM transactions sent to it while reset is asserted.

Workaround

The workaround for this issue is to not send Avalon-MM transactions to the interface while reset is asserted.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

User Guide States Support for ×72 Devices

The states support for multiple devices with a combined interface width of up to ×72, which is incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use multiple devices with a combined interface width of up to ×72.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the *RLDRAM II Controller with UniPHY User Guide*.

–18 Presets Give Errors

If you select any preset with –18 (for example, MT49H64M9-18, MT49H32M18-18, MT49H16M36-18), you see the following error:

```
Error: <variation>: Memory clock frequency must be between 170 MHz
and 500 MHz
```

Affected Configurations

The issue affects all –18 presets.

Design Impact

If you select a 533-MHz component, the FPGA device fails to meet timing.

Workaround

Ensure you change the frequency to a supported frequency.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

tQKH Parameter Incorrect

In the wizard, the t_{QKH} parameter is defined as a "percentage of half of a clock period." However, in the generated timing constraints, the tQKH parameter is used as a "percentage of a full clock period." .

Affected Configurations

The issue affects all configurations.

Design Impact

The read hold margin, as defined in the timing constrants, is too optimistic

Workaround

Manually edit the following two files, to apply the t_{CKH} corrective factor to the equations where t_{QKH} is used:

- <*variaiton name*>**_report_timing.tcl**
- <*variaiton name*>**.sdc**

For example, change:

```
[ expr $tQKH * $tCK ]
```

to:

```
[ expr $tQKH * $tCK * 0.45 ]
```

where: `0.45` is an example value of the t_{CKH} parameter.

☞ You can obtain the t_{CKH} parameter for your memory device from the RLDRAM II datasheet.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Revision History

Table 25–1 shows the revision history for the SDI MegaCore function.

For more information about the new features, refer to the *SDI MegaCore Function User Guide*.

Table 25–1. SDI MegaCore Function Revision History

Version	Date	Description
9.1 SP2	April 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	■ Preliminary support for Cyclone III LS and Cyclone IV (soft SERDES) devices. ■ Dynamic generation of SDC and TCL scripts for all configurations. ■ Example simulation for triple standard cores.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Maintenance release.

Errata

Table 25–2 shows the issues that affect the SDI MegaCore function v9.1 SP2, 9.1 SP1, 9.1, 9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the SDI MegaCore function.

Table 25–2. SDI MegaCore Function Errata

Added or Updated	Issue	Affected Version						
		9.1 SP2	9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Apr 10	Quartus II Fitter Reports Error When Multiple Channels in One Transceiver Quad Use More than One Reference Clock	✓	✓	—	—	—	—	—
15 Nov 09	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓	—	—	—	—
	The Interface Signals Do Not Behave As Expected	—	—	Fixed	✓	✓	✓	—
	Transmitter Line Number (LN) Insertion	—	—	Fixed	✓	✓	✓	✓
01 Jul 09	Incorrect User Guide on ACDS	—	—	—	Fixed	✓	✓	✓
15 Mar 09	Cyclical Redundancy Check (CRC) Error When Receiving 3G-SDI 425M-A Input	—	—	—	—	—	Fixed	✓

Table 25–2. SDI MegaCore Function Errata

Added or Updated	Issue	Affected Version						
		9.1 SP2	9.1 SP1	9.1	9.0 SP2	9.0 SP1	9.0	8.1
01 Nov 08	Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices	✓	✓	✓	✓	✓	✓	✓
15 May 08	NativeLink Fails With ModelSim Simulator	✓	✓	✓	✓	✓	✓	✓
01 Mar 08	Timing Not Met in C5 Speed Grade Stratix II GX Devices	✓	✓	✓	✓	✓	✓	✓

Quartus II Fitter Reports Error When Multiple Channels in One Transceiver Quad Use More than One Reference Clock

The Quartus II Fitter reports an error when multiple channels within one transceiver quad use more than one reference clock in Stratix II GX devices.

For example, four SDI transmitter core is instantiated four times for 4 video channels. These four channels reside within one transceiver quad of a Stratix II GX device. There are two reference clocks connected to this quad—two channels use the first reference clock, and the other two use the second reference clock.

Affected Configurations

This issue affects all designs targeting Stratix II GX devices.

Design Impact

The design cannot be fitted in the device.

Workaround

Apply the quartus variable in the design, by doing the following steps:

1. Create a **quartus.ini** file with content `farm_s2gx_dprio_bypass_pll_number_check=on`.
2. Place the **quartus.ini** file you creatd in your design folder, and compile the design in the Quartus II software version 9.1 SP2.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

The Quartus II Design Assistant Reports Critical Warning

When the **rx_protocol_clk** clock is used, the Quartus II Design Assistant reports the following error:

```
"Critical Warning: (High) Rule D103: Data bits are not
correctly synchronized when transferred between asynchronous
clock domains."
```

This clock is not constrained in the SDC file.

Affected Configurations

This issue affects the dual link SDI in split protocol mode.

Design Impact

The design may fail to function properly on the hardware.

Workaround

Add the following constraints into the SDC file:

```
set rx_protocol_clk_name "rx_protocol_clk[1]"
```

```
create_clock -name $rx_protocol_clk_name -period 13.468 -waveform
{0.000 6.734} [get_ports $rx_protocol_clk_name]
```

Solution Status

This issue will be fixed in a future version of the Quartus II software.

The Interface Signals Do Not Behave As Expected

The interface signals, `rx_xyz`, `xyz_valid`, and `rx_eav`, are asserted at the next word after the actual XYZ word. These interface signals should be asserted to accompany the actual XYZ word.

Affected Configurations

This issue affects the receiver and duplex SDI MegaCore functions.

Design Impact

You cannot rely on these signals to detect the current XYZ word.

Workaround

To detect the current XYZ word, create a counter and count. Three word counts after `rx_trs` is asserted indicates that the current word is XYZ word. Decode `rxdata` for its validity and to indicate that the current TRS is EAV.

Solution Status

This issue is fixed in version 9.1 of the SDI MegaCore function.

Transmitter Line Number (LN) Insertion

The LN insertion feature on the SDI MegaCore transmitter function does not perform correctly. The line information appears on the chroma channel but not on the luma channel.

Affected Configurations

This issue affects the transmitter and duplex MegaCore functions.

Design Impact

The Tektronix WFM700 equipment does not recognize the HD-SDI signal transmitted by the SDI MegaCore transmitter.

Workaround

Connect the LN word to the upper 11 bits of `tx_ln` signal.

For example:

`tx_ln`	[21:0]	Input	HD-SDI: bits 21:11 LN; bits 10:0 LN
			Dual link: bits 21:11 LN link B; bits 10:0 LN link A
			3G-SDI Level A: bits 21:11 LN; bits 10:0 LN
			3G-SDI Level B: bits 21:11 LN link B; bits 10:0 LN link A

Solution Status

This issue is fixed in version 9.1 of the SDI MegaCore function.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *SDI MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the SDI MegaCore function.

Cyclical Redundancy Check (CRC) Error When Receiving 3G-SDI 425M-A Input

The SDI MegaCore function reports CRC error when receiving 3G-SDI 425M-A input. The SDI MegaCore function intermittently outputs corrupted data on the `rxdata` port, and the `rx_status[3]`, `rx_status[4]`, and `rx_ln` bits go to zero.

Affected Configurations

This issue affects all SDI MegaCore triple-rate and 3G-SDI receiver functions.

Design Impact

The `rxdata` port is intermittently corrupted causing CRC error.

Workaround

None.

Solution Status

This issue is fixed in version 9.0 of the SDI MegaCore function.

Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices

The Quartus II Fitter reports an error when you use PLL-generated clock inputs of 67.5 MHz frequency in SDI-SD MegaCore targeting Stratix GX devices.

Affected Configurations

This issue affects all Stratix GX SDI-SD MegaCore functions with PLL-generated clock inputs of 67.5 MHz frequency.

Design Impact

The design cannot be fitted in the device.

Workaround

Set the input clock to 29.7 MHz frequency so that the PLL generates the frequency of the output clock to 74.25 MHz.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

NativeLink Fails With ModelSim Simulator

When using NativeLink to run simulations with the ModelSim simulator, the testbench fails.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate and the testbench reports a failure.

Workaround

Use the ModelSim simulation scripts provided by Altera or carry out the following steps:

1. Edit the NativeLink generated script to command `“vsim -t 100fs”`.
2. Reexecute the script in ModelSim.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Timing Not Met in C5 Speed Grade Stratix II GX Devices

The 3-Gbps and triple rate variants of the SDI MegaCore function may not meet the timing requirements in the C5 speed grade device of the Stratix II GX device family.

Affected Configurations

This issue affects the 3-Gbps and triple-rate SDI MegaCore functions.

Design Impact

Your design does not meet timing requirements.

Workaround

Use either a C4 or C3 speed grade device.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

26. SerialLite II

Revision History

Table 26–1 shows the revision history for the SerialLite II MegaCore function.

For more information about the new features, refer to the *SerialLite II MegaCore Function User Guide*.

Table 26–1. SerialLite II MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Preliminary support for HardCopy IV GX devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Maintenance release.

Errata

Table 26–2 shows the issues that affect the SerialLite II MegaCore v9.1, 9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the SerialLite II MegaCore.

Table 26–2. SerialLite II MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 Nov 09	Designs with Frequency Offset Tolerance Enabled Fail Testbench Simulation	✓	✓	✓	✓	✓
	The Quartus II Design Assistant Reports Critical Warning	✓	—	—	—	—
	Simulating Streaming Mode Design with a Non-Default Reference Clock Frequency Selected	Fixed	✓	✓	✓	✓
	Selecting Non-Default Input Clock Frequency Value for Stratix IV GX Devices	Fixed	✓	✓	✓	—
01 Jul 09	Incorrect User Guide on ACDS	—	Fixed	✓	—	—

Designs with Frequency Offset Tolerance Enabled Fail Testbench Simulation

Designs that have the **Frequency Offset Tolerance** option turned on to either 100 ppm or 300 ppm, using streaming or packet mode with an RX buffer size of zero with a non-default reference clock frequency, may fail the demonstration testbench simulation citing data mismatch errors.

This issue occurs because the utilities for the testbench monitor run at a different clock rate compared to the DUT's receive side's Atlantic clock rate.

Affected Configurations

This issue affects designs with the following settings:

- **Frequency Offset Tolerance** turned on to either 100 ppm or 300 ppm
- Streaming mode or Packet mode with RX buffer size = 0
- Reference clock frequency not equal to (data rate/(TSIZE*10))

Design Impact

There is no design impact. This is a demonstration testbench issue.

Workaround

To simulate the testbench successfully, perform the following steps:

1. Open the generated **<design>_tb.v**.
2. Search for the instantiation of **amon_dat_dut**, and replace the `trefclk` in the clock connection with `tx_coreclock`.

   For example,

   Original line: `.clk (trefclk & reset_done)`

   Replaced line: `.clk(tx_coreclock & reset_done)`
3. Repeat step 2 for **amon_dat_sis**, **amon_pri_dut**, and **amon_pri_sis** (if you have enabled Priority Port).
4. Search for the instantiation of **sbrd_dat_dut_to_sis**, and replace the `trefclk` in the `rclk` connection with `tx_coreclock`:

   For example,

   Original line: `,.rclk (trefclk)`

   Replaced line: `,.rclk (tx_coreclock)`
5. Repeat step 4 for **sbrd_pri_dut_to_sis**, **sbrd_dat_sis_to_dut**, and **sbrd_pri_sis_to_dut**.

Solution Status

This issue will be fixed in a future version of the SerialLite II MegaCore function.

The Quartus II Design Assistant Reports Critical Warning

When you compile a SerialLite II design that targets Stratix GX devices, the Quartus II Design Assistant reports the following error:

```
Critical Warning: (Critical) Rule C101: Gated clock should be
implemented according to the Altera standard scheme. Found 1 node(s)
related to this rule.

    Critical Warning: Node
"<design>_slite2_top|slite2_top_inst|slite2_xcvr:xcvr_inst|altgxb:altg
xb_component|rx_clkout_wire[0]
```

This warning, if targeted to the rx_clkout_wire[0], is erroneously issued by the Quartus II Design Assistant, and is not valid. You can ignore this warning.

Affected Configurations

This issue affects all designs that target Stratix GX devices.

Design Impact

There is no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Simulating Streaming Mode Design with a Non-Default Reference Clock Frequency Selected

If you have selected a streaming mode design together with a non-default reference clock frequency, the IP Functional Simulation model fails to simulate. The default reference clock frequency is defined as (data rate/ (transfer size *10)). Any frequency that is not equal to the formula is non-default.

Affected Configurations

This issue affects all designs that have enabled the **Streaming** data type option with non-default reference clock frequency.

Design Impact

None.

Workaround

To enable the IP Functional Simulation model to simulate successfully, perform the following steps:

1. Open the **<design_name>_tb.v** file.

2. In the following strings, change the value of N to equate N = (1/(data rate/ (transfer size *10))) * 1000000.

```
parameter arclk_period = N;
parameter atclk_period = N;
```

Solution Status

This issue is fixed in version 9.1 of the SerialLite II MegaCore function.

Selecting Non-Default Input Clock Frequency Value for Stratix IV GX Devices

The Quartus II reports an error and fails to compile your design, if you choose the 3,125-Mbps data rate and specify 97.6562-Mhz for input clock frequency.

Affected Configurations

This issue affects all configurations targeting Stratix IV with 3,125-Mbps data rate and 97.6562-Mhz input clock frequency.

Design Impact

The Quartus II software fails to compile your design.

Workaround

To compile your design successfully, perform the following steps:

1. Open the <*variation name*>**_slite2_xcvr.v** file.
2. Locate the string `97.6562`, and replace the string with 97.65625.
3. Recompile your design with the Quartus II software.

Solution Status

This issue is fixed in version 9.1 of the SerialLite II MegaCore function.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *SerialLite II MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the SerialLite MegaCore function.

27. Triple Speed Ethernet

Revision History

Table 27–1 shows the revision history for the Triple Speed Ethernet MegaCore function.

For more information about the new features, refer to the *Triple Speed Ethernet MegaCore Function User Guide*.

Table 27–1. Triple Speed Ethernet MegaCore Function Revision History

Version	Date	Description
9.1 SP1	February 2009	Preliminary support for Cyclone IV E devices
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ Preliminary support for Arria II GX device family. ■ Support for different speeds in multi-port MACs. ■ Option to extend the width of selected statistics counters to 64 bits. ■ Support for 64 Kbyte frame length. ■ Implemented 125-MHz clock enable signals in the physical coding sublayer (PCS) function to replace the internal SGMII clock generator blocks. ■ Added a new field, `disable_rd_timeout` (bit 27), in the `command_config` register. ■ Added a new parameter in the top-level file that specifies the depth of the synchronizer chain.
8.1	November 2008	Support for dynamic reconfiguration.

Errata

Table 27–2 shows the issues that affect the Triple Speed Ethernet MegaCore function v9.1, 9.0 SP2, 9.0 SP1, 9.0, and 8.1.

Not all issues affect all versions of the Triple Speed Ethernet MegaCore function.

Table 27–2. Triple Speed Ethernet MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		9.1	9.0 SP2	9.0 SP1	9.0	8.1
15 Nov 09	Transceiver Instantiation Turns On Dynamic Reconfiguration Mode	✓	✓	✓	✓	✓
	Four-Channel Port Not Supported for MAC PCS Variations Using Stratix IV (GT)	Fixed	✓	✓	✓	✓
	Half-Duplex Collision in MACs	Fixed	✓	✓	✓	✓
	Loopback Module Missing When Generated in SOPC Builder	Fixed	✓	✓	✓	✓
	Half-Duplex Late Collision in MACs Corrupts Next Packets	Fixed	✓	✓	✓	✓
	MACs in Half-Duplex Mode Continue Transmitting Packets	Fixed	✓	✓	✓	✓
	Reconfig_clk Frequency Violates Device Specification	Fixed	✓	✓	✓	✓
	Half-Duplex Collision in MACs Without Internal FIFO Buffers	Fixed	✓	✓	✓	—
	Timing Not Met in Stratix III, Stratix IV, and Arria II GX Devices	Fixed	✓	✓	✓	—
01 Jul 09	Incorrect User Guide on ACDS	—	Fixed	✓	—	—
15 Apr 09	Timing Not Met When System Clock is Set to High Frequency	—	—	—	Fixed	✓
	Half-Duplex Collision in MACs With Internal FIFO Buffers	—	—	Fixed	✓	—
15 Mar 09	Timing Not Met in Cyclone III Devices	✓	✓	✓	✓	—
	Connection Point Validation Fails in SOPC Builder	—	—	—	Fixed	✓
	Intermittent Payload Corruption When 32-Bit Byte Alignment is On	—	—	—	Fixed	✓
	Testbench Compilation Fails When Using Nativelink with ModelSim	—	—	—	Fixed	✓
	Timing Not Met in 12-Port Configurations Targeting Stratix IV Devices	—	—	—	Fixed	✓
15 May 08	Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register	✓	✓	✓	✓	✓
	Non-Compliant Implementation of aAlignmentError Statistics Counter	✓	✓	✓	✓	✓

Transceiver Instantiation Turns On Dynamic Reconfiguration Mode

For designs that target Arria GX or Stratix II GX devices with the **Use transceiver block** and **Enable transceiver dynamic reconfiguration** options turned on, the core does not fit into the same quad with other modules that do not enable the dynamic reconfiguration mode. The transceiver instantiation by the Triple Speed Ethernet enables the dynamic reconfiguration mode even if you choose to turn off the option in the MegaWizard interface.

Affected Configurations

This issue affects all designs that target Arria GX or Stratix II GX devices with the **Use transceiver block** and **Enable transceiver dynamic reconfiguration** options turned on.

Workaround

Edit the following files in the TSE installation directory:

- **altera_tse_gxb_gige_inst.v**

  Change:

  ```
  the_altera_tse_alt2gxb_gige.starting_channel_number =
  STARTING_CHANNEL_NUMBER;
  ```

  to:

  ```
  the_altera_tse_alt2gxb_gige.starting_channel_number =
  STARTING_CHANNEL_NUMBER,
  the_altera_tse_alt2gxb_gige.ENABLE_ALT_RECONFIG =
  ENABLE_ALT_RECONFIG;
  ```

- **altera_tse_alt2gxb_gige.v**

  Change:

  ```
  parameter starting_channel_number = 0;


  alt2gxb_component.reconfig_dprio_mode = 1,
  ```

  to:

  ```
  parameter starting_channel_number = 0;
  parameter ENABLE_ALT_RECONFIG = 1;


  alt2gxb_component.reconfig_dprio_mode = ENABLE_ALT_RECONFIG,
  ```

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Four-Channel Port Not Supported for MAC PCS Variations Using Stratix IV (GT)

Configurations that contain MAC and PCS variations and target Stratix IV GT devices do not support ports with 4 channels.

Affected Configurations

This issue affects all configurations that contain MAC and PCS variations targeting Stratix IV GT devices.

Workaround

Change the number of channels to eight or change the device.

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

Half-Duplex Collision in MACs

Half-duplex collisions that occur during the reception of the first three bytes of the preamble remain undetected in media access control (MAC) functions.

Affected Configurations

This issue affects all configurations that contain 8-bit MAC functions operating in half-duplex mode.

Workaround

None.

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

Loopback Module Missing When Generated in SOPC Builder

The loopback module does not get generated in SOPC Builder using the Windows operating system.

Affected Configurations

This issue affects all configurations generated in SOPC Builder using the Windows operating system.

Workaround

Look for the generate_loopback_module.pl file in the **triple_speed_ethernet\testbench\loopback_modules** directory and edit the following in line 121

Change

```
$OUTPUT_DIRECTORY = "`pwd`";
```

to

```
$OUTPUT_DIRECTORY = ".";
```

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

Half-Duplex Late Collision in MACs Corrupts Next Packets

Half-duplex late collisions in media access control (MAC) functions cause the following errors:

- Late collision that happens 17 bytes before the end of packet (EOP) corrupts the next outgoing packet, and may cause the subsequent packets to underflow.
- MAC continues transmitting packets even when the user logic stops providing packets to the Avalon-ST transmit interface.

Affected Configurations

This issue affects all configurations that contain MACs operating in half-duplex mode.

Workaround

None.

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

MACs in Half-Duplex Mode Continue Transmitting Packets

MACs with internal 8-bit FIFO buffers in half-duplex mode continue transmitting packets even when the user logic stops providing packets to the Avalon-ST transmit interface.

Affected Configurations

This issue affects all configurations that contain MACs with internal 8-bit FIFO buffers operating in half-duplex mode.

Workaround

None.

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

Reconfig_clk Frequency Violates Device Specification

A single clock source drives both the `reconfig_clk` input port of the reconfiguration block and an internal clock, `fixedclk_fast`. Because the internal clock accepts only a frequency of 125 MHz, the clock source is set to the same frequency. This frequency, however, violates the frequency range of the `reconfig_clk` input port specified for the device, which is between 37.5 and 50 MHz.

Affected Configurations

All configurations that use GXB transceivers.

Workaround

Change the internal clock speed to accept a value between 37.5 and 50 MHz by setting `fixedclk_fast` to `0` in **altera_tse_gxb_gige_inst.v**, and set the frequency of the clock source that drives both `reconfig_clk` and `fixedclk_fast` to a value within the same range.

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

Half-Duplex Collision in MACs Without Internal FIFO Buffers

Half-duplex collisions in MAC functions without internal FIFO buffers cause the following errors:

- Retransmission fails if collision happens during the transmission of the preamble, start frame delimiter, and source address.
- Collision that happens after the transmission of 64 bytes of the packet corrupts the next outgoing packet.
- Collision remains undetected if it happens during the reception of the final six bytes of the packet.

Affected Configurations

This issue affects all configurations that contain MACs without internal FIFO buffers operating in half-duplex mode.

Workaround

None.

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

Timing Not Met in Stratix III, Stratix IV, and Arria II GX Devices

Designs that use the default clock resource assignments may not meet timing.

Affected Configuration

This issue may affect Stratix III, Stratix IV, or Arria II GX designs that contain the multi-port **10/100/1000 Mbps Ethernet MAC with 1000BASE-X/SGMII PCS** variation.

Workaround

Assign each instance of `tbi_tx_clk` to the periphery clock by adding the following assignment for each port in the Quartus II settings file (**.qsf**):

```
set_instance_assignment -name GLOBAL_SIGNAL “PERIPHERY CLOCK” -to tbi_tx_clk_0
```

Solution Status

This issue is fixed in version 9.1 of the Triple Speed Ethernet MegaCore function.

Incorrect User Guide on ACDS

The user guide that is on the Altera Complete Design Suite (ACDS) is an out-of-date version.

Affected Configurations

This issue affects no configurations.

Design Impact

There is no design impact.

Workaround

Download the latest *Triple Speed Ethernet MegaCore Function User Guide* from the Altera website.

Solution Status

This issue is fixed in version 9.0 SP2 of the Triple Speed Ethernet MegaCore function.

Timing Not Met When System Clock is Set to High Frequency

Configurations that contain **10/100/1000 Mbps Ethernet MAC only** variations do not meet timing when the system clock is set to a frequency higher than 75 MHz.

Affected Configurations

All configurations that contain **10/100/1000 Mbps Ethernet MAC only** variations.

Workaround

Add the system clock to the following command in the **.sdc** file, as shown:

```
set_clock_groups -exclusive -group
{rx_clk_to_the_triple_speed_ethernet_0} -group
{tx_clk_to_the_triple_speed_ethernet_0} -group {clk}
```

Solution Status

This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Half-Duplex Collision in MACs With Internal FIFO Buffers

Half-duplex collisions that occur during the reception of the final six bytes of the packet remain undetected in MACs with internal FIFO buffers.

Affected Configuration

This issue affects all configurations that contain MACs with internal FIFO buffers operating in half-duplex mode.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Timing Not Met in Cyclone III Devices

Designs targeted to Cyclone III devices may not meet timing when the skew optimization option is turned on by default.

Affected Configuration

This issue may affect variations in designs targeted to Cyclone III devices.

Workaround

Turn off the skew optimization option by adding the following assignment in the Quartus II settings file (**.qsf**):

```
set_global_assignment -name ENABLE_BENEFICIAL_SKEW OPTIMIZATION OFF
```

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Connection Point Validation Fails in SOPC Builder

The connection point validation fails for SOPC Builder systems that contain the MAC block without internal FIFO buffers and the physical coding sublayer (PCS) block with embedded gigabit transceiver block. This variation of the Triple Speed Ethernet MegaCore function contains two unassociated clocks, `rx_afull_clk` and `cal_blk_clk`, but SOPC Builder only allows for one unassociated clock.

Affected Configuration

This issue affects all SOPC Builder systems that contain the **10/100/1000 Ethernet MAC with 1000BASE-X/SGMII PCS** variation with the following options:

- **Use internal FIFO** is turned off.
- **Use transceiver block** and **GXB** are selected.

Workaround

None.

Solution Status

This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Intermittent Payload Corruption When 32-Bit Byte Alignment is On

The payload is occasionally corrupted when 32-bit byte alignment is turned on in MACs without internal FIFO buffers.

Affected Configuration

This issue affects all configurations that contain the core variations **10/100/1000 Mbps Ethernet MAC only** or **10/100/1000 Mbps Ethernet MAC with 1000BASE-X/SMII PCS** with the following options:

- **Use internal FIFO** is turned off
- **Align packet headers to 32-bit boundaries** is turned on

Workaround

None.

Solution Status

This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Testbench Compilation Fails When Using Nativelink with ModelSim

The following error occurs during the testbench compilation when Nativelink is used with ModelSim:

```
# ** Error: (vlog-7) Failed to open design unit file
"D:/altera/81/ip/altera/triple_speed_ethernet/lib/altera_tse_alt2gxb_gige.vo" in read
mode.
# No such file or directory. (errno = ENOENT)
# Error in macro ./tse_run_msim_rtl_verilog.do line 9
```

This error is caused by a wrong extension in the Nativelink Tcl script.

Affected Configuration

This issue affects any configuration with the following characteristics:

- Targets Stratix II GX or Arria GX.
- Contains the **10/100/1000 Ethernet MAC with 1000BASE-X/SGMII PCS** or **1000BASE-X/SGMII PCS** variation.
- Turns on the **Use transceiver block** option.

Workaround

Edit the script **tse_run_msim_rtl_**<*verilog/vhdl*>**.do** and change the extension of **altera_tse_alt2gxb_gige.vo** to **.v**.

Solution Status

This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Timing Not Met in 12-Port Configurations Targeting Stratix IV Devices

Twelve-port configurations that target the Stratix IV device family and implement LVDS I/O do not meet timing.

Affected Configuration

This issue affects only 12-port configurations that target the Stratix IV device family and implement LVDS I/O.

Workaround

None.

Solution Status

This issue is fixed in version 9.0 of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register

The Triple Speed Ethernet MegaCore function sets the `PAGE_RECEIVE` bit in the PCS register `an_expansion` to 1 when a /C/ ordered set is received. This behavior does not comply with the IEEE 802.3 Standard clause 37.

Affected Configuration

This issue affects all configurations that include the PCS function.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of aAlignmentError Statistics Counter

The Triple Speed Ethernet MegaCore function increments the `aAlignmentError` statistics counter when an SFD error is encountered. This behavior does not comply with the IEEE 802.3 Standard clause 5.2.2.1.7.

Affected Configuration

This issue affects all configurations.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

28. UTOPIA Level 2 Master

Revision History

Table 28–1 shows the revision history for the UTOPIA Level 2 Master MegaCore function.

For more information about the new features, refer to the *UTOPIA Level 2 Master MegaCore Function User Guide*.

Table 28–1. UTOPIA Level 2 Master MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	November 2008	Full support for Stratix III devices.

Obsolescence Notice

CAUTION

The UTOPIA Level 2 Master MegaCore function is scheduled for product obsolescence and discontinued support as described in PDN0906. Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's Intellectual Property website.

Errata

Table 28–2 shows the issues that affect the UTOPIA Level 2 Master MegaCore function v9.1, 9.0, and 8.1.

Table 28–2. UTOPIA Level 2 Master MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
15 Nov 09	VHDL Gate Level Simulations Fail in Modelsim 6.5b	✓	—	—

VHDL Gate Level Simulations Fail in Modelsim Version 6.5b

Some VHDL gate level simulations of the UTOPIA Level 2 Master MegaCore function fail in Modelsim version 6.5b.

Affected Configurations

All HDL gate level simulations of the UTOPIA Level 2 Master MegaCore function in Modelsim version 6.5b.

Workaround

Use Modelsim version 6.5c.

Design Impact

There is no design impact.

Solution Status

This issue may be fixed in a later version of the UTOPIA Level 2 Master MegaCore function.

29. UTOPIA Level 2 Slave

Revision History

Table 29–1 shows the revision history for the UTOPIA Level 2 Slave MegaCore function.

For more information about the new features, refer to the *UTOPIA Level 2 Slave MegaCore Function User Guide*.

Table 29–1. UTOPIA Level 2 Slave MegaCore Function Revision History

Version	Date	Description
9.1	November 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	November 2008	Full support for Stratix III devices.

Obsolescence Notice

CAUTION

The UTOPIA Level 2 Slave MegaCore function is scheduled for product obsolescence and discontinued support as described in PDN0906. Therefore, Altera does not recommend use of this IP in new designs. For more information about Altera's current IP offering, refer to Altera's Intellectual Property website.

Errata

There are no issues that affect the UTOPIA Level 2 Slave MegaCore function v9.1, v9.0, and 8.1.

30. Video and Image Processing Suite

Revision History

Table 30–1 shows the revision history of the Video and Image Processing Suite MegaCore functions.

For information about the new features, refer to the *Video and Image Processing Suite User Guide*.

Table 30–1. Video and Image Processing Suite Revision History (Part 1 of 2)

Version	Date	Description
9.1	November 2009	■ Added the following new MegaCore functions: ■ The Frame Reader ■ The Control Synchronizer ■ The Switch MegaCore function ■ The Frame Buffer MegaCore function supports: ■ Controlled frame dropping or repeating to keep the input and output frame rates locked together ■ Triple buffering of interlaced video streams. ■ The ability to discard invalid frames or fields, or both, by repeating the last video frame received. ■ The Clipper, Frame Buffer, and Color Plane Sequencer MegaCore functions now support four channels in parallel. ■ The Deinterlacer MegaCore function supports a new 4:2:2 motion-adaptive mode and an option to align read/write bursts on burst boundaries. ■ The Clocked Video Input and Clocked Video Output MegaCore functions support synchronization signals and have revised control register maps. ■ The Line Buffer Compiler MegaCore function is obsolete. ■ Extended the Avalon-ST Video protocol to improve support for interlaced content. The change is backward compatible.
9.0 SP1	May 2009	■ Preliminary support for HardCopy® III and HardCopy IV E devices.

Table 30–1. Video and Image Processing Suite Revision History (Part 2 of 2)

Version	Date	Description
9.0	March 2009	■ The Deinterlacer MegaCore function supports controlled frame dropping or repeating to keep the input and output frame rates locked together. ■ The Test Pattern Generator MegaCore function can generate a user-specified constant color that can be used as a uniform background. ■ Preliminary support for Arria II GX devices.
8.1	November 2008	■ Added new Test Pattern Generator. ■ The Deinterlacer supports pass-through mode and run-time algorithm switching. ■ The Deinterlacer and Frame Buffer support clock crossing for improved external memory access efficiency. ■ The Clocked Video Input and Clocked Video Output support run-time switching between standard definition (SD) and high definition (HD) video streams. ■ The Color Space Converter supports run-time changing of coefficients. ■ The Gamma Corrector supports parallel data processing for three channels. ■ The 2D FIR Filter supports run-time changing of coefficients. ■ Full support for Stratix III devices. ■ Withdrawn support for UNIX.

Errata

Table 30–2 shows the issues that affect the Video and Image Processing Suite MegaCore functions v9.1, v9.0, and v8.1.

Not all issues affect all versions of the Video and Image Processing Suite MegaCore function.

Table 30–2. Video and Image Processing Suite Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
15 Feb 10	Compilation Errors with the Frame Buffer	✓	—	—
15 Nov 09	Frame Buffer and Deinterlacer are Missing Entry in .sdc File	✓	—	—
	Clocked Video Output Incorrectly Aligns Start of Frame (vid_sof)	✓	—	—
	Scaler: Number of Colour Planes Incorrect	✓	—	—
	Compilation Fails on the Windows Vista Operating System	✓	—	—
01 Jul 09	Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly	✓	✓	—

Table 30–2. Video and Image Processing Suite Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
15 Mar 09	RTL Simulation Reports Errors When Using Verilog HDL	✓	✓	—
	Incorrect Simulation Models Created for Deinterlacer and Frame Buffer	✓	✓	—
	Deinterlacer and Test Pattern Generator May Not Upgrade	✓	✓	—
	The 2D Median Filter Does Not Support 7×7 Filter Size	✓	✓	✓
	Misleading Error Message Issued by Color Plane Sequencer	—	Fixed	✓
	Changing Target Device After Quartus II Compilation Causes Error	—	Fixed	✓
	Active Picture Line Selection Should be Available for Separate Sync Mode	—	Fixed	✓
	v7.2 MegaCore Functions are Not Compatible with v8.x Quartus II	—	—	✓
	Packets Sent to VIP Cores Must Have Non-Empty Payload	✓	✓	✓
15 May 08	SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video	✓	✓	✓
01 Oct 07	Scalar Coefficients Preview Window Cannot be Closed	✓	✓	✓
01 May 07	Precision Must be Set When Using Lanczos Coefficients in Scaler	✓	✓	✓
01 Dec 06	Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector	✓	✓	✓

Compilation Errors with the Frame Buffer

The frame buffer may fail to generate and issues a compilation error when **Discard invalid frames/fields** is turned on.

Affected Configurations

This issue affects configurations that use the **Discard invalid frames/fields** option without turning on either the frame dropping or the support for interlaced fields.

Design Impact

The generation fails and you receive the following compilation errors:

```
Error: IP Generator Error: At end of source: error: expected a "}"
```

```
Error: IP Generator Error:
"C:/altera/91/ip/altera/frame_buffer/lib/vip_vfb_hwfast.hpp", line
756: error: expected "while"
```

Workaround

This issue has no workaround. However, enabling the support for interlaced video may be an acceptable solution for video systems where the frame buffer is only processing progressive frames.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Frame Buffer and Deinterlacer are Missing Entry in .sdc File

The Synopsis Design Constraint **(.sdc)** files that constrain the Deinterlacer, Frame Buffer, Clocked Video Input and Clocked Video Output MegaCore functions have to be added manually to the Quartus II project.

Affected Configurations

All configurations using any of these MegaCore functions.

Design Impact

These **.sdc** files declare false paths that should not be considered during timing analysis. Timing closure for valid critical paths may not be achievable if these files are not included in your project, which results in a nonfunctioning system.

Workaround

Add the **.sdc** files manually from the project settings windows. In the Quartus II software, point to the Project menu and click **Add/Remove Files in Project**. These **.sdc** files are provided with your Quartus II installation and are in the following directory:

<*install_dir*>**\ip**<*megacore_function*>**\lib\alt_vip_**<*tla*>**.sdc**

where:

- <*megacore_function*> is **deinterlacer**, **frame_buffer**, **clocked_video_input**, or **clocked_video_output**
- <*tla*> is an acronym that identifies the MegaCore function

To verify that the **.sdc** files have been correctly added, keep the **Settings** window open and click **Timing Analysis Settings** then **TimeQuest Timing Analyzer** in the tree menu.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Clocked Video Output Incorrectly Aligns Start of Frame (vid_sof)

When frame locking is turned on in the **Clocked Video Output** it attempts to align its start of frame (output by the `vid_sof` signal) to the incoming start of frame signal (the `sof` signal). When this aligment is achieved, the output video is frame locked (the start of frames are aligned) to the input video.

Affected Configurations

Systems enabling the frame locking functionality in the **Clocked Video Output**.

Design Impact

The output video frame lock is out by one cycle.

Workaround

Move the **Clocked Video Output** start of frame one cycle earlier. For example if the start of frame required for **Mode 1** is at sample 10, write 9 into bits 2 to 15 of the `Mode1 SOF Sample` register.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler: Number of Colour Planes Incorrect

The **Scaler: Number of colour planes** should be 1 to 3.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Compilation Fails on the Windows Vista Operating System

On the Windows Vista Operating System, when synthesizing the VIP Suite IP MegaCore functions in the Quartus II software, or generating an IP functional simulation model, compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

For synthesis, you receive the following error:

```
Error: Node instance "scaler" instantiates undefined entity
"alt_vip_scl_GNRA6GTEAK" File: C:/work/testvip/db/scaler_GN.vhd Line:
52
```

For IP functional simulation model generation, you receive the following error:

```
Error:  Simulation model map command failed:
D:\altera\90sp2\quartus/bin/quartus_map scaler --simgen --
simgen_parameter="CBX_HDL_LANGUAGE=VHDL"
```

Workaround

You must run the Quartus II software as adminstrator to enable the VIP Suite IP generation and synthesis to complete successfully. To run Quartus II as adminstrator on the **Start menu**, point to **Programs**, then **Altera**, then right click on **Quartus II** *<version>*. Click **Run as adminstrator**.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly

The Deinterlacer and Frame Buffer MegaCore functions may not work properly when connected to a DDR3 High Performance Memory Controller MegaCore function.

In some configurations and/or with specific input resolutions, the Deinterlacer and Frame Buffer MegaCore functions may issue write and read bursts starting at odd addresses. The DDR3 controller uses wrapping bursts for read accesses and, as a consequence, the wrong data may be read back from memory.

Affected Configurations

Systems connecting the Video and Image Processing MegaCore functions to DDR3 SDRAM memory.

Design Impact

This issue may have unpredictable effects. Typically, the output video will be distorted.

Workaround

There is no workaround. However, increasing the number of samples reserved for non-image data packets in memory may solve the issue and realign the starting addresses of the bursts in specific cases.

To realign the starting addresses, the number of words reserved in memory for a non-image packet should be equal to the full wrapping burst, or a multiple of this value. The number of memory words reserved for a non-image packet in memory can be calculated as follows:

1. Determine the number of beats necessary to stream the longest allowed non-image packet through the Avalon Streaming (Avalon-ST) interface. For example, the number of beats to stream an Avalon-ST Video packet of length 10, is 4 when the number of color samples in parallel is 3, 6 when the number of symbols per beat is 2, and 10 when the number of symbols per beat is 1.

   ```
   number_beats = roundUp((max_length + symbols_per_beat - 1) /
   symbols_per_beat)
   ```

2. Determine the number of words necessary to store the longest allowed non-image packet:

   ```
   number_words = roundUp(number_beats × symbols_per_beat ×
   bits_per_symbol / memory_word_bits)
   ```

By reversing these expressions, you can deduce an adequate value for the maximum number of samples:

```
max_length = (wrapping_burst_size ×
roundDown(memory_word_bits / (symbols_per_beat ×
bits_per_symbol)) × symbols_per_beat) - symbols_per_beat + 1
```

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

RTL Simulation Reports Errors When Using Verilog HDL

EDA RTL simulation started from the Quartus II software reports errors in ModelSim® for designs containing Video and Image Processing Suite MegaCore functions when the output files are in Verilog HDL.

Affected Configurations

Configurations using Native Link to run a Model*Sim* simulation from Verilog HDL.

Design Impact

An error message reports that the altera library cannot be found.

Workaround

Compile the file **db/alt_cusp90_package.vhd** to the altera library. This compilation can be performed by modifying the top-level .**do** script in the **simulation/modelsim** directory.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Incorrect Simulation Models Created for Deinterlacer and Frame Buffer

Incorrect functional simulation models may be created for the Deinterlacer and Frame Buffer MegaCore functions.

Affected Configurations

Configurations that use a different clock domain for the Avalon Memory-Mapped (Avalon-MM) master interfaces.

Design Impact

The IP functional simulation models generated using the MegaWizard™ Plug-in Manager may reset in an incorrect state. This issue may also affect simulation models generated with SOPC Builder.

Workaround

If possible, release the reset signals for the Avalon-MM interface ports before the reset signal for the MegaCore function. Alternatively, repeat the generation until a valid .**vo** or .**vho** file is produced.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Deinterlacer and Test Pattern Generator May Not Upgrade

The Deinterlacer and Test Pattern Generator MegaCore functions may not directly upgrade to v9.0 in SOPC Builder.

Affected Configurations

Quartus II v8.1 designs containing Deinterlacer or Test Pattern Generator MegaCore functions that were originally created in the Quartus II v8.0 software.

Design Impact

SOPC Builder reports an error when it tries to upgrade the MegaCore function if the parameterization has not changed.

Workaround

Open the v8.1 version of your design, make a change to the parameterization of any Deinterlacer or Test Pattern Generator MegaCore functions and apply your change. Change back to the original parameterization, then save the SOPC Builder system.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

The 2D Median Filter Does Not Support 7×7 Filter Size

The 2D Median Filter MegaCore function does not support the 7×7 filter size.

Affected Configurations

Configurations including the 2D Median Filter MegaCore function.

Design Impact

You can select a 7×7 filter size in pre-9.0 versions of the 2D Median Filter MegaCore function but an error message is issued when generating the simulation model.

Workaround

There is no workaround. Do not select the 7×7 filter size.

Solution Status

The 7×7 filter size is not available in version 9.0 or later of the Video and Image Processing Suite. The documentation will be updated in the next version.

Misleading Error Message Issued by Color Plane Sequencer

If you try to enable both ports `din1` and `dout1` in the MegaWizard interface for the Color Plane Sequencer MegaCore function a misleading error message is issued stating that: "`dout0 and dout1 cannot both be enabled`". The message should state "`din1 and dout1 cannot both be enabled`".

Affected Configurations

Pre-9.0 configurations including the Color Plane Sequencer MegaCore function.

Design Impact

None.

Workaround

None needed.

Solution Status

The error message has been updated in v9.0 of the Video and Image Processing Suite.

Changing Target Device After Quartus II Compilation Causes Error

Changing the target device in a family after compilation in the Quartus II software can cause an error with subsequent Quartus II compilations.

Affected Configurations

Any Video and Image Processing Suite MegaCore function when the target device is changed within the same device family.

Design Impact

The generation flow does not correctly recognize the change to the target device. The HDL generation is skipped for subsequent Quartus II compilations, and the following error message is issued when you re-compile:

```
Error (10481): VHDL Use Clause error at  *_GN.vhd: design library
"altera" does not contain primary unit "alt_cusp81_package"
```

Workaround

Remove the **db** directory from the project directory and re-compile in the Quartus II software.

Solution Status

This issue is fixed in v9.0 of the Video and Image Processing Suite.

Active Picture Line Selection Should be Available for Separate Sync Mode

The **Active picture line** selection box should be available when **On separate wires** is selected for **Sync signals**.

Affected Configurations

This issue affects the Clocked Video Output MegaCore function when sync signals on separate wires are selected.

Design Impact

An incorrect active picture line is selected.

Workaround

Select **Embedded in video** to enable the selection box, then switch back to **On separate wires** after specifying the required active picture line. The specified value is used although it is shown dimmed in the selection box.

Solution Status

This issue is fixed in v9.0 of the Video and Image Processing Suite.

v7.2 MegaCore Functions are Not Compatible with v8.x Quartus II

The v7.2 Video and Image Processing Suite MegaCore functions are not compatible with v8.0 or v8.1 of the Quartus II software, SOPC Builder or DSP Builder.

Affected Configurations

All designs including v7.2 Video and Image Processing Suite MegaCore functions.

Design Impact

Errors are issued when you attempt to compile the design.

Workaround

Upgrade the MegaCore functions to v8.0 or v8.1.

Solution Status

This issue will not be fixed. However v8.x MegaCore functions can be used in v9.0 of the Quartus II software.

Packets Sent to VIP Cores Must Have Non-Empty Payload

The packets sent to the Color Space Converter and 2D Median Filter MegaCore functions must have non-empty payload. If a packet is sent with a type but without any further information, the packet processing logic may enter an inconsistent state.

Affected Configurations

Configurations including the Color Space Converter or 2D Median Filter MegaCore functions.

Design Impact

If a packet with an empty payload is received, the MegaCore function may not output correct data until a few non-empty packets have been received.

Workaround

If an empty packet is intended, send one symbol of data with it.

Solution Status

This issue is unlikely to be fixed as there is a simple workaround.

SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video

In SOPC Builder, the Avalon-ST data adapter does not support the Avalon-ST Video protocol. No error message is currently displayed when connecting the components.

Affected Configurations

SOPC Builder configurations that connect an Avalon-ST adapter to a Video and Image Processing MegaCore function.

Design Impact

Connecting any of the Video and Image Processing Suite MegaCore functions to an Avalon-ST data adapter results in a generated system in which the Avalon-ST video protocol is corrupted.

Workaround

To connect Video and Image Processing MegaCore functions which have a different number of planes in parallel, use the Color Plane Sequencer. For example: to convert between 3 colors in parallel (3 symbols per beat) and 3 colors in sequence (1 symbol per beat).

Solution Status

It will not be possible to connect unsupported Avalon-ST adapters in a future version of SOPC Builder and the Video and Image Processing Suite.

Scalar Coefficients Preview Window Cannot be Closed

The Scalar Coefficients Preview window cannot be closed when it is used in SOPC Builder.

Affected Configurations

This issue affects the Scaler MegaCore Function when it is parameterized in the SOPC Builder flow.

Design Impact

This issue does not prevent you from parameterizing the Scalar and therefore has no design impact.

Workaround

The Coefficient Preview window will close when you close the main Scalar parameterization interface.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Precision Must be Set When Using Lanczos Coefficients in Scaler

When configuring the Scaler MegaCore function, you must choose the correct coefficient precision when using Lanczos coefficients.

Affected Configurations

This issue affects configurations of the Scaler MegaCore function using the polyphase algorithm with Lanczos coefficients.

Design Impact

The MegaCore function fails to generate.

Workaround

If you select polyphase mode with Lanczos coefficients, you must set the coefficient precision to be signed with one integer bit. Fraction bits can be set within the full range available in the MegaWizard interface.

Solution Status

The coefficient precision restriction will be enforced in future versions of the Video and Image Processing Suite.

Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector

M4K block write operations may fail for Cyclone II devices with the Alpha Blending Mixer and Gamma Corrector MegaCore functions.

Affected Configurations

This issue affects configurations using Cyclone II devices and the Alpha Blending Mixer or Gamma Corrector MegaCore function.

Design Impact

The following error message is issued:

```
Error: M4K memory block WYSIWYG primitive
"vhdl_gam:vhdl_gam_inst|TTA_X_smem_av:gamma_lut|altsyncram:\ds1:altsyn
cram_component|altsyncram_rvh1:auto_generated|ram_block1a0" utilizes
the dual-port dual-clock mode. However, this mode is not supported in
Cyclone II device family in this version of Quartus II software. Please
refer to the Cyclone II FPGA Family Errata Sheet for more information
on this feature.
```

Workaround

If you are targeting any affected revision (Rev a or b of the 2c35 or Rev a of any other Cyclone II part), set the `CYCLONEII_SAFE_WRITE` variable to `RESTRUCTURE`. This setting causes the Quartus II software to fix the issue at a cost in M4Ks and F_{max}. If you are using a newer revision device, set the `CYCLONEII_SAFE_WRITE` variable to `VERIFIED_SAFE` which turns off the error message.

Solution Status

This issue has been fixed for the latest silicon devices but remains an issue if you are using the earlier silicon.

Refer to the *Cyclone II FPGA Family Errata Sheet* for more information about this issue.

31. Viterbi Compiler

Revision History

Table 31–1 shows the revision history for the Viterbi Compiler.

For more information about the new features, refer to the *Viterbi Compiler User Guide*.

Table 31–1. Viterbi Compiler Revision History

Version	Date	Description
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria® II GX devices.
8.1	November 2008	Full support for Stratix III devices.

Errata

Table 31–2 shows the issues that affect the Viterbi Compiler v9.1, v9.0, and 8.1.

Not all issues affect all versions of the Viterbi Compiler.

Table 31–2. Viterbi Compiler Errata

Added or Updated	Issue	Affected Version		
		9.1	9.0	8.1
15 Nov 09	File Summary Does Not List All Generated Files	Fixed	✓	✓
15 Mar 09	Testbench ber_clear Signal is Not Connected	✓	✓	—
	Gate-Level Simulation Fails	✓	✓	—

File Summary Does Not List All Generated Files

The file summary on the IP Toolbench Generate window does not always list all the generated files.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

In the Parameterize window, when you finish parameterizing your variation, do not click **Finish**, just go to IP Toolbench and click **Generate**.

Solution Status

This issue is fixed in version 9.1 of the Viterbi Compiler.

Testbench ber_clear Signal is Not Connected

The `ber_clear` signal in the generated testbench is not connected correctly.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Viterbi Compiler.

Gate-Level Simulation Fails

The Viterbi Compiler does not support gate-level simulations.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Viterbi Compiler.

How to Contact Altera

For the most up-to-date information about Altera® products, see the following table.

Contact *(Note 1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions that this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, dialog box options, software utility names, and other GUI labels. For example, **\qdesigns** directory, **d:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicates document titles. For example, *AN 519: Stratix IV Design Guidelines.*
Italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicates keyboard keys and menu names. For example, Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. Active-low signals are denoted by suffix `n`. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).

Visual Cue	Meaning
1., 2., 3., and a., b., c., and so on.	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
↵	The angled arrow instructs you to press Enter.
	The feet direct you to more information about a particular topic.