Impact of I/O Settings on Signal Integrity in Stratix III Devices

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Introduction

This application note provides information on the effects of the I/O settings on the quality of the signal. Its main focus is on drive strength and slew rate effects and explains how Altera® defines these two settings for a given I/O, along with ways to choose these based on the specific application for which the Stratix® III device is used.

This application note also covers the impact of multiple topologies, transmission line lengths, and output loads on the output signal and how these features relate to the settings mentioned above. This application note is a technical background document that concludes by providing recommendations on the selection of the I/O settings based on your custom system.

It is important to follow the recommendations described in this document to reduce the signal integrity (SI) effects on your system.

The following are key terms used in this application note:

Definitions of Key Terms Used in this Document:

- **VOL_{Max}/VOH_{Min} (DC):** For a given transmitter, the VOL/VOH (DC) is defined as the maximum and minimum voltage, that is logic state low and high. These voltages are defined for the near-end node.
- **VIL_{Max}/VIH_{Min} (DC):** For a given receiver, the VIL and VIH (DC) is defined such that the final logic state is unambiguously defined, that is once the receiver input has crossed this value, the receiver changes to and maintains the new logic state. These voltages are defined for the far-end node.
- **Signal Integrity (SI):** The quality of a signal being at the correct level, within a certain time interval, at a given node of a system.
- **C_{LOAD}:** This is the input pin capacitance at the receiver, as seen by the driver. If multiple devices are connected at the far-end, C_{LOAD} is the sum of the input pin capacitances of those devices. Modern systems usually have small output loads (2 pF to 5 pF), except for the cases of legacy systems and multiple receivers connected at the output. For these, the load can be in the order of tens of pF. All voltage

measurements in this document are taken at the C_{LOAD} (far-end node), as shown in Figure 1. The far-end node is located at the end of the transmission line.

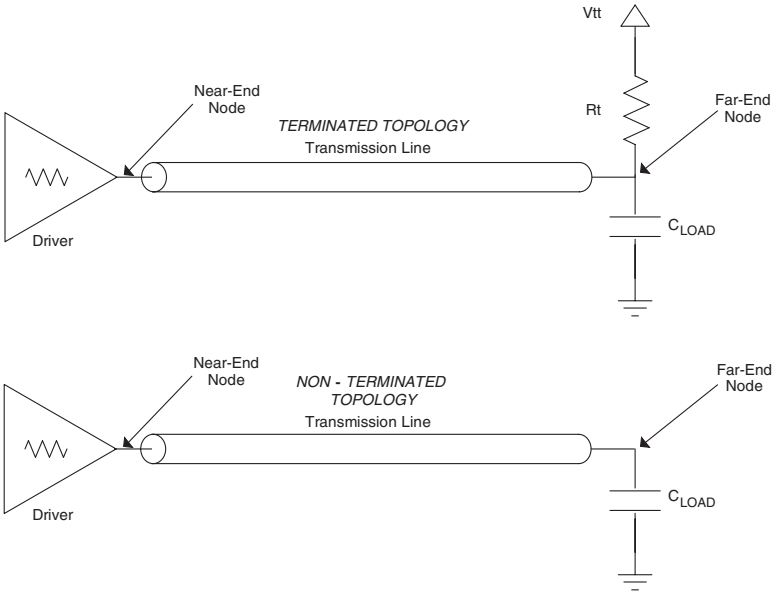
- **Output Signal and Output Node:** In this document, output signal refers to the signal observed at the far-end node; far-end node refers to the node at the end of the transmission line (also called output node). This node is the transmitter's far-end, and the input of the receiver. The far-end node for both topologies (terminated and non-terminated) is shown in Figure 1. All voltage plots in this document show signals observed at the output node. Current plots are observed at the near-end, between the driver's output and the transmission line.

- **Terminated Topology:** In this application note, this is a topology that contains at least one parallel termination resistor. Figure 1 shows a terminated topology. In this document, the drivers used in the terminated topology simulations are HSTL-18 Class I and SSTL-18 Class I.

- **Non-Terminated Topology:** In this application note, this is a topology that does not contain a parallel termination resistor. Figure 1 shows the diagram of a non-terminated topology. In this document, the drivers used in the non-terminated topology simulations are CMOS 2.5 and CMOS 1.8.

- **Rise and Fall Time:** Rise time is the time taken by the signal to go from low-level to high-level (20%-80%) and vice-versa for the fall time.

Figure 1. Terminated and Non-Terminated Topologies Used in this Document



I/O Settings

Drive Strength

The drive strength of a given driver is a measurement of how much current the driver launches on a given load. It can also determine the largest load that can be driven at a certain speed, without affecting the integrity of the transmitted signal. In other words, a stronger driver is able to drive larger loads and longer transmission lines.

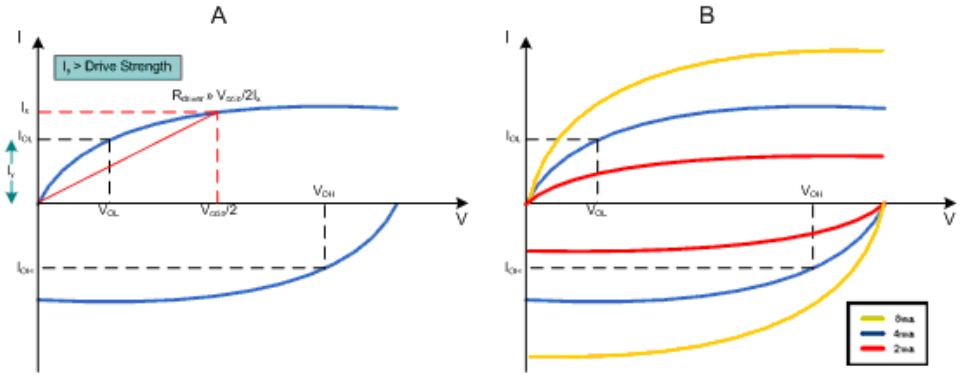
Altera FPGAs offer a variety of drive strengths for each supported I/O standard. The drive strength is specified in mA because it is a measure of how much current the driver supplies to the load. This is why drive strength is also known as current strength.The impedance of the drivers, as well as the I_{OL} and the $I_{OH,}$ vary depending on the drive strength because they are directly related to it. Figure 2 A shows a generic driver's IV curve where the driver's equivalent resistance and the drive strength are graphically identified:

- The driver's equivalent resistance is approximated by dividing the output voltage by the current provided by the driver (I_x) at half the V_{CCIO}. That is, $R_{driver} = (V_{CCIO}/2) / I_x$.

- For a given drive strength, the minimum current provided to the load by the driver when the output voltage is V_{OL} (I_y), is equal to or larger than the drive strength (in mA). For example, a 4 mA driver has I_{OL} greater than or equal to 4 mA.

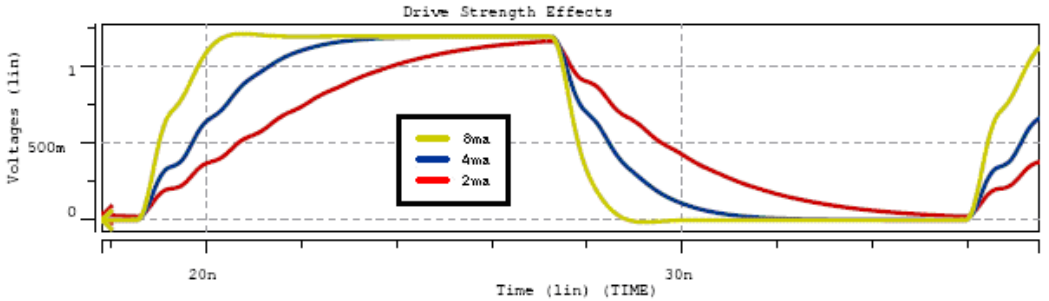
In addition, the instantaneous output impedance of the I/O buffer is equal to the instantaneous voltage divided by the current at that voltage (obtained from the IV curve). A driver with larger drive strength has a different IV curve. Figure 2 B shows a generic graph for three different drive strengths of the same I/O. The yellow curves correspond to the strongest driver while the red curves correspond to the weakest driver. I_{OL} and I_{OH} are larger for the stronger driver. The IV characteristics of a driver vary across PVT.

Figure 2. Generic I-V Curve of a Driver



The output signal edge may be degraded when you use weaker drivers because these drivers source less current to the load for any given voltage. Figure 3 shows an example of the output signal of a driver with three different drive strength settings, under the same conditions (topology, termination, slew rate, transmission line characteristics, and output load). In this example, the driver with 2 mA drive strength is not strong enough to drive the load, the one with 4 mA drive strength is able to drive it but may have timing issues (rise and fall times take approx 40% of the period). The one with 8 mA drive strength has a better output signal.

Figure 3. Drive Strength Effects on the Output Signal



You may wonder why not simply choose the strongest driver, if it is able to drive larger loads and longer transmission lines? The reason is that stronger drivers launch larger currents, and larger currents also imply larger crosstalk, simultaneous switching noise (SSN), and power consumption. A stronger driver might provide a larger noise margin but also generates larger noise. Therefore, choosing the right driver directly affects the quality of your signal. You should choose the minimum drive strength that is able to drive the load connected to the output of the Stratix III device.

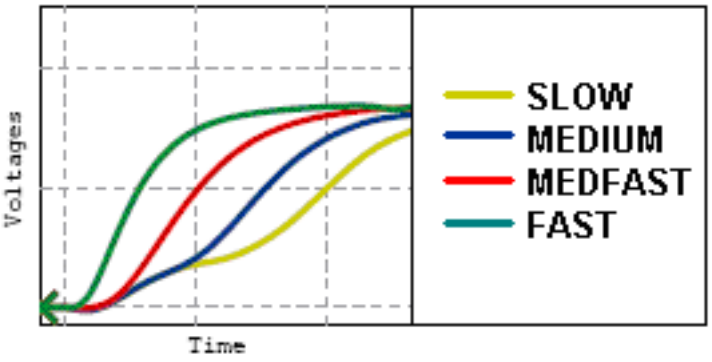
Slew Rate Control

The slew rate control determines the maximum rate of change of the output signal. In other words, it defines how fast the rise and fall times of the output signal are.

Note that the drive strength specifies how much current the driver sources/sinks, while the slew rate specifies how fast it sources/sinks the current. Together, these two settings determine the rise and fall times of the output signal.

Process technologies with smaller feature sizes allow faster clocks, but faster clocks also signify shorter rise and fall times. This means that switching times are reduced even on low frequency signals as the rise and fall times are set by the technology. This reduction of the switching time comes together with larger transient current; consequently, larger switching noise. For a high f_{max} link signal, it might be necessary to have short rise and fall times, but for a low f_{max} link signal, you may reduce the noise by using longer rise and fall times.

Figure 4. Rise Time Effects of the Slew Rate Setting



The slew rate setting allows you to modify the duration of the rise and fall times. There are four different slew rate settings; slow, medium, medfast, and fast. You can choose the one that is optimal for your specific design. Figure 4 shows a rising edge of the output signal under the four settings: slow, medium, medfast, and fast. In this plot you can see how the slope gets reduced for slower settings. This slope decrease is the main reason for the noise reduction. But there is a timing-noise tradeoff in the slew rate selection and it will also depend on the design. This tradeoff will be addressed in the section "Timing Versus Transient Currents".

Effects of I/O Settings on Signal Integrity

So far, each setting has been introduced independently, but in a real design, all of the settings are combined and affect the output signal. Depending on how these settings are combined, as well as the system characteristics, the integrity of the signal may be improved, avoiding overdriving (which may be observed as ringing) or under-driving, both cases leading to potential failures at the receiver.

Under-Driving

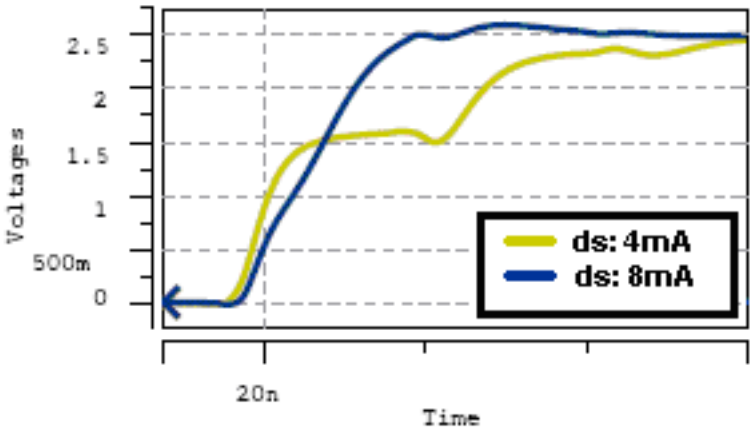
When a driver is not strong enough to drive its output load, it is said to be under-driving. If by the time the output signal is read by the receiver system, it hasn't reached V_{IH} for the case of a low-to-high transition, or V_{IL} for the case of a high to low transition, it results in an incorrect reading. This behavior means the driver is not able to drive that specific load; in other words, it is under-driving.

Given a fixed topology and a PCB already designed with specified transmission line lengths, varying the drive strength can drastically change the results. In some cases it only improves the signal quality (which by itself is a huge advantage) but in other cases it may be the factor

that determines if the system works. The drive strength determines how much current is provided by the driver to the load. If the transmission line is long and/or the load is large, this current might not be sufficient to charge the load to the desired level before the data is read by the receiver, giving way to an incorrect reading. The effect of choosing a weaker driver is worse in non-terminated topologies. This is due not only to the reflections that contribute to the degradation of the signal, but also to the lack of a termination resistor that behaves like a pull-up in the terminated schemes.

Figure 5 shows the output signals of a non-terminated topology, with 4 mA and 8 mA drive strengths. You can see the signal is very weak for the first case (4 mA), while the second (8 mA) drives the signal well.

Figure 5. Drive Strength Effects on a Non-Terminated Topology: Under-Driving



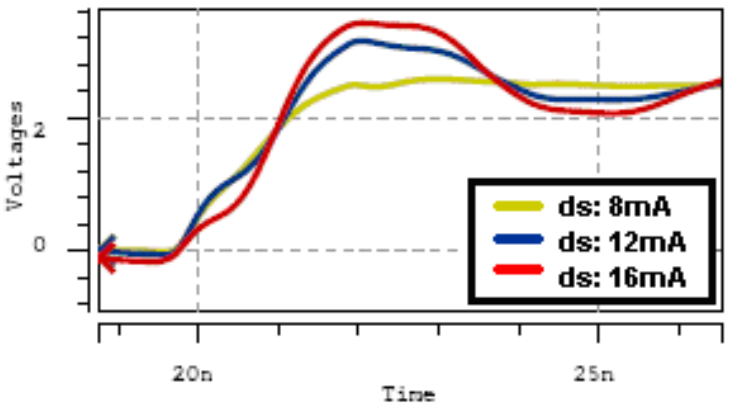
Over-Driving

When a driver is too strong for its output load, and the output signal goes above the high-level or below the low-level it is supposed to reach, the driver is said to be over-driving.

If a PCB has long transmission lines, it is very important to provide enough current to guarantee that the signal reaches the required voltage at the far-end and on time. Furthermore, if the load is large, more current is necessary to charge it faster. However, if the traces are not very long, and the load is small, selecting a strong driver is counter-productive. Too much current not only draws excessive power but also brings larger noise into the picture.

Figure 6 shows an example with 8 mA, 12 mA, and 16 mA drive strengths. In this figure, the effects of the extra current can be seen in two of the curves; the 12 mA drive strength, and the 16 mA drive strength. In these two cases, the output signal goes above the desired level generating ringing.

Figure 6. Drive Strength Effects on a Non-Terminated Topology: Over-Driving



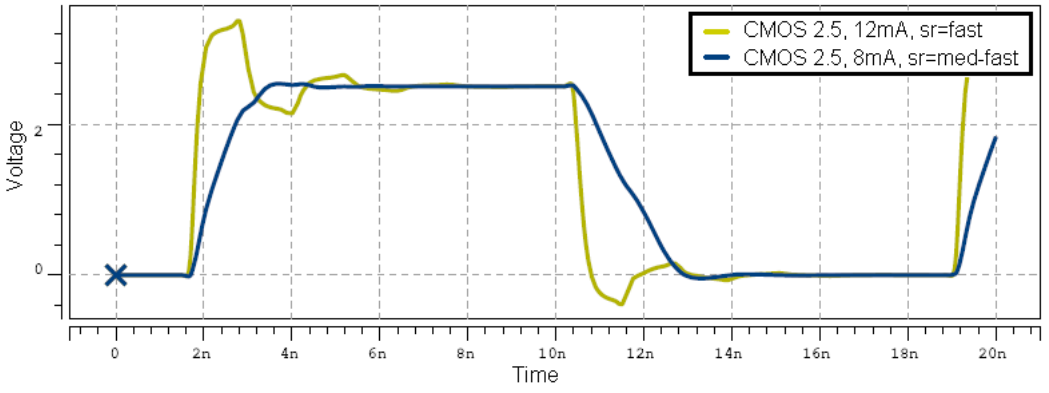
In addition, if a strong driver is combined with a fast slew rate setting, the noise results can be worse.

Figure 7 shows the output signal of a strong driver with a fast slew rate setting and a weaker driver with a medium-fast slew rate setting. The fast slew rate (yellow) exhibits a large ringing, which may exceed the AC specifications, while the medium-fast does not. If you were running at a low speed, simply reducing the slew rate to slow would solve the ringing problem. However, if the speed you are running your system at is high, and the rising and falling time are required to be very short due to timing constraints, the fast slew rate is the setting to choose. To avoid ringing, reduce the drive strength, which in turn reduces the current and the noise.

In this example, the driver was changed from CMOS 2.5 12 mA to CMOS 2.5 8 mA and the slew rate was changed from fast to med-fast. This way the signal reached the high level on time and did not have ringing. You must balance between timing constraints and transient currents that the system tolerates. Shorter rising and falling edges and stronger drivers lead to larger transient currents; slow slew rates and weaker drivers may lead to timing issues by degrading the output edge. You must choose

what is more convenient for your specific system. A more in-depth explanation of this tradeoff is given in the section "Timing Versus Transient Currents" on page 9.

Figure 7. Slew Rate Effects: Over-Driving



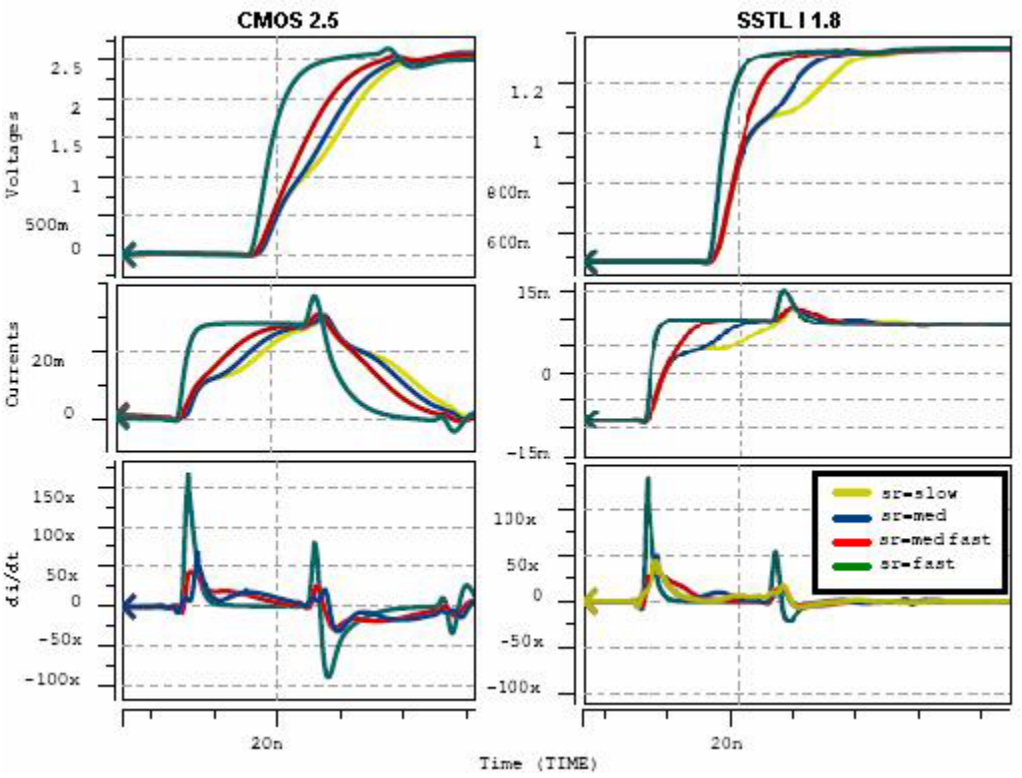
Timing Versus Transient Currents

The four slew rate settings on terminated (SSTLI 1.8) and non-terminated (CMOS 2.5) topologies are shown in Figure 8.

The possibility of choosing the slew rate of a signal is a tremendous advantage in terms of transient currents. Using the fastest slew rate for a given technology is no longer a good idea, because the small feature sizes used in the latest technologies come together with extremely fast edges, hence large transient currents. These currents not only affect the signal on the selected I/O, but also the signals on the surrounding I/Os and the power distribution network, creating noise all over the system. Usually, the non-terminated drivers only source or sink current during the transition; that is, the rising and falling edges of the output signal, while the terminated topologies have a DC current on both states (high and low).

Figure 8 shows the voltage (top), the current (middle), and di/dt (bottom) of a terminated (right) and a non-terminated (left) topology during the low-to-high transition. There is a large current delta at the very beginning of the transition. This current increase happens faster in the driver with a fast slew rate setting (green) and is much more gradual in the driver with a slow slew rate setting (yellow). In other words, the faster the slew rate setting selected, the larger the peak di/dt.

Figure 8. Output Voltage, Near-End Current, and Near-End di/dt Curves During The Rising Edge (1ns/div)



The noise voltage is directly proportional to the current delta. If you want to reduce noise, you will need to look for ways to reduce di/dt. The slow slew rate provides you with the smallest di/dt but the output signal reaches the high level (in this example 1.5 to 2.5 ns) later than the signal with the fast slew rate. If timing is more critical in your design than noise, the fast slew rate is more acceptable. If you are concerned about both, you must balance them and choose one of the intermediate levels. That is the timing-noise tradeoff: the slower the slew rate, the smaller the di/dt and the noise from it, but also the longer the time the signal takes to reach the desired level. Likewise, the faster the slew rate, the shorter the time to reach the appropriate level, but the larger the di/dt and the noise from it.

The current drawn and the di/dt also depend on your topology devices. The second current glitch (the one that happens after the 20 ns line) is larger for the non-terminated topology as a consequence of the

reflections. In this same topology, a third reflection glitch can be seen and few others happen before degrading completely (not shown in Figure 8). These additional current deltas are also an undesired noise source.

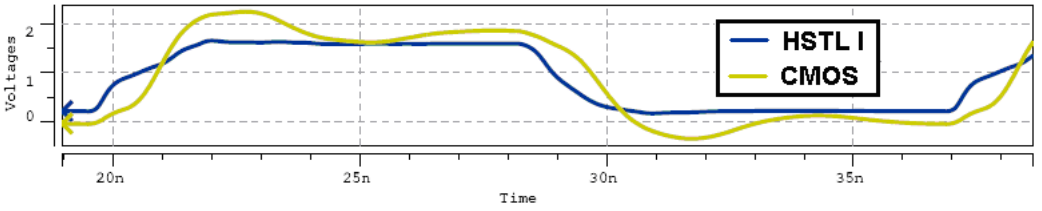
Topologies

Comparison Between Topologies

You must consider the topology used when choosing the I/O settings. The most noticeable difference exists between terminated and non-terminated topologies. Terminated topologies have far fewer reflections than non-terminated topologies. They also have a termination resistor that is also a pull-up, making them less vulnerable to over- and under-driving.

Figure 9 compares a non-terminated topology (CMOS 1.8) with a terminated topology (HSTL-18 Class I) under the same conditions. In this example, the CMOS signal is affected by the reflections while the HSTL signal is not. The terminated topology is superior in controlling reflections. This advantage is important when running fast data rates.

Figure 9. Topologies Comparison: CMOS versus HSTL I



In addition to topology, it is necessary to consider other features, such as the PCB and what is going to be connected at the far-end. The following two sections show examples of transmission line lengths and output loads.

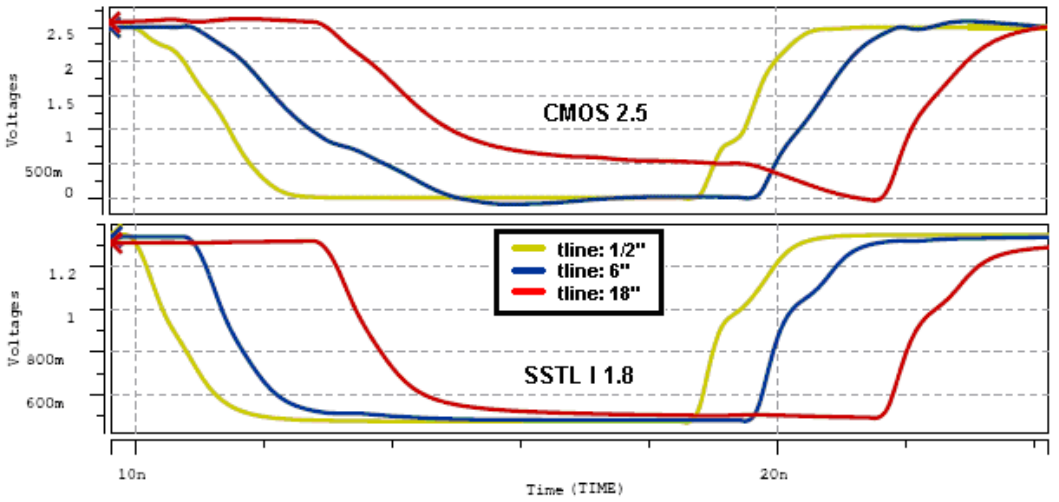
Transmission Line Length

An ideal transmission line does not have losses, but in a real system, the signal is attenuated along the length of the transmission line. The highest frequency components are affected more because the attenuation is frequency dependent. This effect combined with reflections, result in output edge degradation, affecting the quality of the signal.

Figure 10 shows a non-terminated topology (CMOS 2.5) and a terminated topology (SSTL-I 1.8) using short (1/2 inch), intermediate (6 inches) and long (18 inches) transmission lines. The terminated topology is less

affected by the length of the transmission line than the non-terminated one. As a reminder, a long transmission line requires a stronger driver to provide enough current to charge the load to the desired level by the time required. In this example, using a stronger driver for the longer transmission lines improves the shape of the output signals.

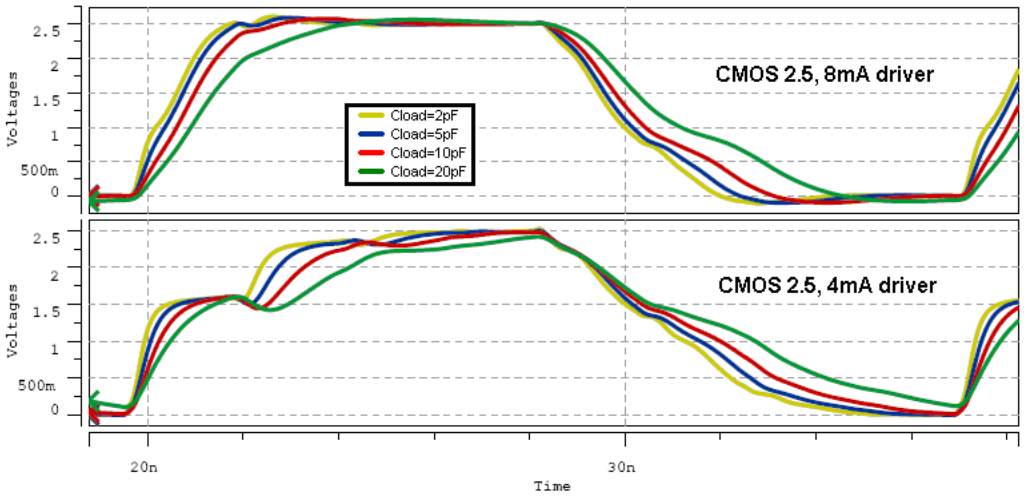
Figure 10. Losses and Reflections on 1/2, 6, and 18 Inches Transmission Lines



Output Load

The larger the load at the far-end, the longer the time to charge and discharge it. This means the rise and fall times are increased when the loads are larger. Figure 11 compares the signal at the output of 2 CMOS drivers for loads from 2 pF up to 20 pF. In this example, the larger the load, the longer the time taken to transition from low to high. The transition time increase is more critical in the weaker driver, which is not able to reach either the high or low level for the largest load. This delay in reaching the high and low level may be decisive for high-speed signals and can be improved by using a stronger driver.

Figure 11. Output Signal for 2 pF, 5 pF, 10 pF and 20 pF Loads



Recommendations

The topology, trace length, load, and design constraints you have, should dictate the I/O settings selections that you make. This application note explained how the settings change your output signal under various configurations. The "How to Choose Settings" section summarizes the main features you should consider when choosing the settings for your design.

How to Choose Settings

- Speed, load, topology, transmission line length, termination, and design specific constraints (noise and timing) are the main areas to consider before choosing the I/O settings.
- Altera recommends using faster slew rate settings only when the speed is high and the timing constraints are critical. Faster slew rates come with larger transient currents and therefore, larger noise.
- Altera recommends stronger drivers for long transmission lines and large loads, principally for non-terminated topologies. Stronger drivers launch more current into the load, consuming more power and generating more noise.
- When timing constraints are tight, consider faster slew rates combined with the right drive strength to avoid under- and over-driving.

- Select the minimum drive strength and the slower slew rate setting where possible.

Design Tradeoff

The design trade-off presented in this application note is between timing constraints and transient currents. You can either reduce the time to reach the desired level or reduce the transient currents but you cannot decrease both at the same time. The best you can do is to balance them according to your design constraints. To reduce the time, you can either use a stronger driver or choose a faster slew rate. To reduce the transient currents you can reduce the slew rate or use a weaker driver.

The other variables analyzed, such as C_{LOAD}, transmission line length, topology, and speed of the signal, are design-dependent and are usually fixed for your design.

Summary

I/O settings play a very important role for the quality of your output signal. You must be careful when deciding what settings you choose and consider the timing and noise tradeoffs. There is no rule-of-thumb that works for every design, but there are recommendations you can follow for your specific constraints. The topology, trace length, load, and the design constraints you have are the areas to consider—these should dictate the I/O settings selections that you make.

Referenced Documents

This application note references the following documents:

- Eric Bogatin, *Signal Integrity Simplified*
- *FPGA Design for Signal and Power Integrity*, DesignCon 2007, Paper by Larry Smith and Hong Shi

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
October 2007 ver. 1.0	Initial release	—

101 Innovation Drive
San Jose, CA 95134
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Technical Support:
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Literature Services:
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