HardCopy IV Device Handbook,

Volume 4: Datasheet

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Contents

Chapter Revision Dates

The chapters in this document, HardCopy IV Device Handbook, Volume 4: Datasheet, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. DC and Switching Characteristics of HardCopy IV Devices
Revised: *December 2011*
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Chapter 2. Extended Temperature Range for HardCopy IV Devices
Revised: *March 2012*
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Section I. HardCopy IV Device Datasheet

This section provides the datasheet for the HardCopy® IV device family. This section includes the following chapter:

- Chapter 1, DC and Switching Characteristics of HardCopy IV Devices
- Chapter 2, Extended Temperature Range for HardCopy IV Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. DC and Switching Characteristics of HardCopy IV Devices

HIV54001-2.1

Electrical Characteristics

This chapter covers the electrical characteristics for HardCopy® IV devices.

Operating Conditions

When implementing HardCopy IV devices in a system, the system rates the devices according to a set of defined parameters. To maintain the highest possible performance and reliability, consider the operating requirements described in this chapter. HardCopy IV devices are not speed binned because HardCopy IV devices function at a target frequency based on timing constraints. Altera offers HardCopy IV devices that support applications in commercial or industrial grade temperatures.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for HardCopy IV devices. Experiments with the device and theoretical modeling of breakdown and damage mechanisms provide these values. These conditions do not imply the functional operation of the device.

Table 1–1 lists the absolute maximum ratings for a HardCopy IV device.

Conditions other than those listed in Table 1–1 and Table 1–3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1. HardCopy IV Device Absolute Maximum Ratings (Part 1 of 2) *(Note 1)*

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	–0.5	1.35	V
V_{CCPT} *(2)*	Power supply for programmable power technology	—	—	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.75	V
V_{CCAUX}	Power supply for temperature sensing diode and POR	–0.5	3.75	V
V_{CCBAT} *(3)*	Battery back-up power supply for design security volatile key register	—	—	V
V_{CCPD}	I/O predriver power supply	–0.5	3.75	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply	–0.5	3.75	V
V_{CCD_PLL}	Phase-locked loop (PLL) digital power supply	–0.5	1.35	V
V_{CCA_PLL}	PLL analog power supply	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.0	V

Table 1–1. HardCopy IV Device Absolute Maximum Ratings (Part 2 of 2) *(Note 1)*

Symbol	Description	Minimum	Maximum	Unit
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	C
T_{STG}	Storage temperature (No bias)	–65	150	C

Notes to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins and not the power supply.
(2) HardCopy IV devices do not require programmable power technology.
(3) HardCopy IV devices do not use this power supply.

Table 1–2 lists the power supply absolute maximum ratings for HardCopy IV GX transceiver.

Table 1–2. HardCopy IV GX Transceiver Power Supply Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	–0.5	3.75	V
V_{CCA_R}	Transceiver high voltage power (right side)	–0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP digital power (right side)	–0.5	1.35	V
V_{CCHIP_R}	Transceiver hard IP digital power (left side)	–0.5	1.35	V
V_{CCR_L}	Receiver power (left side)	–0.5	1.35	V
V_{CCR_R}	Receiver power (right side)	–0.5	1.35	V
V_{CCT_L}	Transmitter power (left side)	–0.5	1.35	V
V_{CCT_R}	Transmitter power (right side)	–0.5	1.35	V
V_{CCL_GXBLn} *(1)*	Transceiver clock power (left side)	–0.5	1.35	V
V_{CCL_GXBRn} *(1)*	Transceiver clock power (right side)	–0.5	1.35	V
V_{CCH_GXBLn} *(1)*	Transmitter output buffer power (left side)	–0.5	1.65	V
V_{CCH_GXBRn} *(1)*	Transmitter output buffer power (right side)	–0.5	1.65	V

Note to Table 1–2:

(1) The V_{CCH} and V_{CCL} powers are per transceiver block.

Maximum Allowed Overshoot or Undershoot Voltage

Table 1–3 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

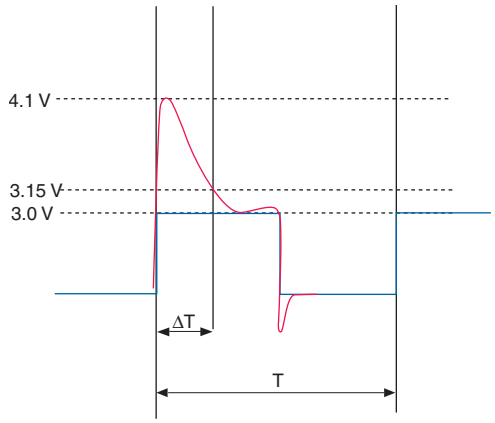
During transitions, input signals may overshoot to the voltage shown in Table 1–3 and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–3. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition	Overshoot Duration as Percentage of High Time	Unit
Vi (AC)	AC input voltage	4.0 V	100.000	%
		4.05 V	79.330	%
		4.1 V	46.270	%
		4.15 V	27.030	%
		4.2 V	15.800	%
		4.25 V	9.240	%
		4.3 V	5.410	%
		4.35 V	3.160	%
		4.4 V	1.850	%
		4.45 V	1.080	%
		4.5 V	0.630	%
		4.55 V	0.370	%
		4.6 V	0.220	%
		4.65 V	0.130	%
		4.7 V	0.074	%
		4.75 V	0.043	%
		4.8 V	0.025	%
		4.85 V	0.015	%

Figure 1–1 shows the methodology to determine overshoot duration. The color red shows the overshoot voltage and is present at the HardCopy IV pin, up to 4.1 V. In Table 1–3, for an overshoot of up to 4.1 V, the percentage of high time for overshoot is greater than 3.15 V can be as high as 46% over an 11.4 year period. The percentage of high time is (Δ T/T) × 100. This 11.4 year period assumes that you turned on the device with 100% I/O toggle rate and 50% duty cycle signal. Lifetimes increase for lower I/O toggle rates and situations in which the device is in an idle state.

Figure 1–1. Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for HardCopy IV devices. Table 1–4 shows the steady-state voltage and current values expected from HardCopy IV devices. All supplies must reach their full-rail values in t_{RAMP} maximum monotonically.

Table 1–4. HardCopy IV Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	—	0.87	0.90	0.93	V
V_{CCPT} *(1)*	Power supply for programmable power technology	—	—	—	—	V
V_{CCAUX}	Power supply for the temperature sensing diode and POR	—	2.375	2.5	2.625	V
V_{CCPD}	I/O predriver (3.0 V) power supply	—	2.85	3	3.15	V
	I/O predriver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V

Table 1–4. HardCopy IV Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_PLL}	PLL digital voltage regulator power supply	—	0.87	0.90	0.93	V
V_{CC_CLKIN}	Differential clock input power supply	—	1.075	1.2	1.325	V
	Differential clock input power supply	—	1.375	1.5	1.625	V
	Differential clock input power supply	—	1.675	1.8	1.925	V
	Differential clock input power supply	—	2.375	2.5	2.625	V
	Differential clock input power supply	—	2.875	3.0	3.125	V
V_{CCBAT} *(2)*	Battery back-up power supply (for design security volatile key register)	—	—	—	—	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial use	0	—	85	°C
		Industrial use	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Normal POR (PORSEL = 0)	0.05	—	100	ms
		Fast POR (PORSEL = 1) *(3)*	0.05	—	4	ms

Notes to Table 1–4:

(1) HardCopy IV devices do not require programmable power technology.
(2) HardCopy IV devices do not require this power supply.
(3) If the PORSEL pin is connected to V_{CC}, all supplies must ramp up in 4 ms.

Table 1–5 shows the transceiver power supply recommended operating conditions.

Table 1–5. HardCopy IV GX Transceiver Power Supply Recommended Operating Conditions (Part 1 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_L}	Transceiver high voltage power (left side)	2.85 or 2.375	3.0 or 2.5 *(3)*	3.15 or 2.625	V
V_{CCA_R}	Transceiver high voltage power (right side)				V
V_{CCHIP_L} *(1)*	Transceiver hard IP digital power (right side)	0.87	0.90	0.93	V
V_{CCHIP_R} *(1)*	Transceiver hard IP digital power (left side)				V
V_{CCR_L}	Receiver power (left side)	1.05	1.1	1.15	V
V_{CCR_R}	Receiver power (right side)				V
V_{CCT_L}	Transmitter power (left side)	1.05	1.1	1.15	V
V_{CCT_R}	Transmitter power (right side)				V

Table 1–5. HardCopy IV GX Transceiver Power Supply Recommended Operating Conditions (Part 2 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCL_GXBLn} *(2)*	Transceiver clock power (left side)	1.05	1.1	1.15	V
V_{CCL_GXBRn} *(2)*	Transceiver clock power (right side)				V
V_{CCH_GXBLn} *(2)*	Transmitter output buffer power (left side)	1.33 or 1.425	1.4 or 1.5 *(4)*	1.47 or 1.575	V
V_{CCH_GXBRn} *(2)*	Transmitter output buffer power (right side)				V

Notes to Table 1–5:

(1) If $V_{CCHIP\_L/R}$ is connected to the same power supply source as V_{cc}, the recommended minimum and maximum operating supply levels are 0.87 V and 0.93 V respectively.

(2) The V_{CCH} and V_{CCL} powers are per transceiver block.

(3) $V_{CCA\_L/R}$ must be connected to a 3.0 V supply if the clock multiplier unit phase-locked loops (CMU PLLs), receiver clock data recovery (CDR), or both are configured at a base data rate > 4.25Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA\_L/R}$ to either 3.0 V or 2.5 V.

(4) For data rates up to 6.5 Gbps, you can connect $V_{CCH\_GXBL/R}$ to either 1.4 V or 1.5 V.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination (OCT) tolerance, and hot socketing specifications.

Supply Current

Standby current is the current the device draws after configuration, with no inputs or outputs toggling and no activity in the device. Because these currents vary with the resources you use, use the Excel-based PowerPlay Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1–6 lists supply current specifications for V_{CC_CLKIN} and V_{CCPGM}. Use the PowerPlay EPE to get supply current estimates for the remaining power supplies.

Table 1–6. Supply Current Specifications for VCC_CLKIN and VCCPGM

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	250	mA
I_{PGM}	V_{CCPGM} current specifications	0	250	mA

I/O Pin Leakage Current

Table 1–7 lists the HardCopy IV I/O pin leakage current specifications.

Table 1–7. HardCopy IV I/O Pin Leakage Current *(Note 1)*, *(2)*

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0_V$ to $V_{CCIOMAX}$	–20	—	20	µA
I_{OZ}	Tristated I/O pin	$V_O = 0_V$ to $V_{CCIOMAX}$	–20	—	20	µA

Notes to Table 1–7:

(1) This value is for normal device operation. The value may vary during power up. This applies for all V_{CCIO} settings (3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 20 mA I/O leakage current limit is applicable when the internal clamping diode is off. You can observe a higher current when the diode is on.

Bus Hold Specifications

Table 1–8 lists the HardCopy IV bus hold specifications

Table 1–8. Bus Hold Parameters

Parameter	Symbol	Condition	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Max	Min	Max	Min	Min	Max	Max	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25.0	—	–30.0	—	–50.0	—	–70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

OCT Specifications

If you enabled OCT calibration, calibration is automatically performed at power up for I/Os connected to the calibration block. Table 1–9 lists the HardCopy IV OCT calibration block accuracy specifications.

Table 1–9. HardCopy IV OCT With Calibration Specification for I/Os *(Note 1)*

Symbol	Description	Conditions	Calibration Accuracy	Unit
25-Ω R_S 3.0/2.5/1.8/1.5/1.2 *(2)*	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0/2.5/1.8/1.5/1.2 V	±8	%
50-Ω R_S 3.0/2.5/1.8/1.5/1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0/2.5/1.8/1.5/1.2 V	±8	%
50-Ω R_T 2.5/1.8/1.5/1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5/1.8/1.5/1.2 V	±10	%
25-Ω, 25-Ω, and 25-Ω R_S 3.0/2.5/1.8/1.5/1.2 *(3)*	Expanded range for internal series termination with calibration (20-Ω, 40-Ω and 60-Ω RS settings)	V_{CCIO} = 3.0/2.5/1.8/1.5/1.2 V	±10	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0/2.5/1.8/1.5/1.2 V	±10	%

Notes to Table 1–9:

(1) OCT calibration accuracy is valid at the time of calibration only.
(2) 25-Ω R_S not supported for 1.5 V and 1.2 V in Row I/O.
(3) 20-Ω R_S not supported for 1.5 V and 1.2 V in Row I/O.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. If the voltage or temperature changes, the termination resistance value varies. Table 1–10 lists the resistance tolerance for HardCopy IV OCT.

Table 1–10. I/O OCT Resistance Tolerance

Symbol	Description	Resistance Tolerance		
		Commercial Max	Industrial Max	Unit
25-Ω RS 3.0/2.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0/2.5 V	±40	%
25-Ω RS 1.8/1.5	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8/1.5 V	±40	%
25-Ω RS 1.2	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	±50	%
50-Ω RS 3.0/2.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0/2.5 V	±40	%
50-Ω RS 1.8/1.5	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8/1.5 V	±40	%
50-Ω RS 1.2	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	%

Table 1–11 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–11 and Equation 1–1 to determine the OCT variation when voltage and temperature vary after power-up calibration.

Equation 1–1. OCT Variation Without Recalibration ***(Note 1)***, ***(2)***, ***(3)***, ***(4)***, ***(5)***, ***(6)***

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 1–1:

(1) R_{OCT} value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1–11. OCT Variation after Power-Up Calibration ***(Note 1)***

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	

Table 1–11. OCT Variation after Power-Up Calibration ***(Note 1)***

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Notes to Table 1–11:

(1) Valid for V_{CCIO} range of ± 5% and a temperature range of 0° to 85°C.

Pin Capacitance

Table 1–12 lists the HardCopy IV device family pin capacitance.

Table 1–12. HardCopy IV Device Capacitance

Symbol	Description	Typical	Unit
C_{IOTB}	Input capacitance on top or bottom I/O pins	5	pF
C_{IOLR}	Input capacitance on left or right I/O pins	5	pF
C_{CLKTB}	Input capacitance on top or bottom dedicated clock input pins	4	pF
C_{CLKLR}	Input capacitance on left or right dedicated clock input pins	4	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output or feedback pins	5	pF
C_{CLK1} C_{CLK3} C_{CLK8} C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Hot Socketing

Table 1–13 lists the hot socketing specification for HardCopy IV devices.

Table 1–13. HardCopy IV Hot Socketing Specifications

Symbol	Description	Maximum
$I_{IIOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA ***(1)***

Note to Table 1–13:

(1) The I/O ramp rate is 10 ns or more. For ramp rate faster than 10 ns, |IIOPIN| = Cdv/dt, in which C is I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 1–14 lists the weak pull-up resistor values for HardCopy IV devices.

Table 1–14. HardCopy IV Internal Weak Pull-Up Resistor *(1)*, *(2)*

Symbol	Parameter	Conditions	Typ	Unit
R_{PU}	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.0 V ± 5% *(3)*	25	kΩ
		V_{CCIO} = 2.5 V ± 5% *(3)*	25	kΩ
		V_{CCIO} = 1.8 V ± 5% *(3)*	25	kΩ
		V_{CCIO} = 1.5 V ± 5% *(3)*	25	kΩ
		V_{CCIO} = 1.2 V ± 5% *(3)*	25	kΩ

Notes to Table 1–14:

(1) All I/O pins have an option to enable weak pull-up except test and JTAG pins.
(2) The internal weak pull-down feature is only available for JTAG TCK pin. The typical value for this internal weak pull-down resistor is around 25k.
(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Table 1–15 through Table 1–20 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by HardCopy IV devices. These tables also show the HardCopy IV device family I/O standard specifications. For an explanation of terms used in Table 1–15 through Table 1–20, refer to the "Glossary" on page 1–35. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

Table 1–15. Single-Ended I/O Standards

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V **LVTTL**	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.3-V **LVCMOS**	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} - 0.2	0.1	–0.1
2.5-V **LVTTL/LVCMOS**	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.2	2.1	0.1	–0.1
								0.4	2	1	–1
								0.7	1.7	2	–2
1.8-V **LVTTL/LVCMOS**	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} - 0.45	2	–2
1.5-V **LVTTL/LVCMOS**	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2-V **LVTTL/LVCMOS**	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
3.0-V **PCI**	2.85	3	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	3.6	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	–0.5
3.0-V **PCI-X**	2.85	3	3.15	—	0.35 * V_{CCIO}	0.5 * V_{CCIO}	—	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	–0.5

For an example of a voltage referenced receiver input waveform and explanation of terms used in Table 1–16, refer to Figure 1–10 on page 1–37.

Table 1–16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	0.47 * V_{CCIO}	V_{REF}	0.53 * V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	V_{CCIO}/2	—

Table 1–17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} - 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	V_{TT} - 0.76	V_{TT} + 0.76	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	V_{TT} - 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} - 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} - 0.25	V_{REF} + 0.25	0.28	V_{CCIO} - 0.28	13.4	–13.4
SSTL-15 Class I	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	–8
SSTL-15 Class II	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	–16
HSTL-18 Class I	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	–8
HSTL-18 Class II	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	–16
HSTL-15 Class I	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	8	–8
HSTL-15 Class II	–0.3	V_{REF} - 0.1	V_{REF} + 0.1	V_{CCIO} + 0.3	V_{REF} - 0.2	V_{REF} + 0.2	0.4	V_{CCIO} - 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} - 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} - 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	–16

For receiver input and transmitter output waveforms and for all differential I/O standards (**LVDS**, **mini-LVDS**, and **RSDS**), refer to Figure 1–5 on page 1–35 and Figure 1–6 on page 1–35. V_{CC_CLKIN} is the power supply for differential column clock input pins. V_{CCPD} is the power supply for row I/Os and all other column I/Os.

Table 1–18. Differential SSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.2	—	V_{CCIO}/2 + 0.2	0.6	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 - 0.125	—	V_{CCIO}/2 + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	V_{CCIO}/2	—	0.4	—	—	V_{CCIO}/2	—

Table 1–19. Differential HSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.8	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.7	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.2	—	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	—

Table 1–20. Differential I/O Standard Specifications *(Note 1)* (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5-V **LVDS** (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.05	*Dmax* ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	*Dmax* > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
2.5-V **LVDS** (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.05	*Dmax* ≤ 700 Mbps	1.8	0.247	—	0.6	1.0	1.25	1.5
						—	1.05	*Dmax* > 700 Mbps	1.55	0.247	—	0.6	1.0	1.25	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1.0	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1.0	1.2	1.5

Table 1–20. Differential I/O Standard Specifications *(Note 1)* (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL	2.375	2.5	2.625	300	—	—	0.6	*Dmax* ≤ 700 Mbps	1.8 *(3)*	—	—	—	—	—	—
	2.375	2.5	2.625	300	—	—	1.0	*Dmax* ≤ 700 Mbps	1.6 *(3)*	—	—	—	—	—	—

Notes to Table 1–20:

(1) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.

(2) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(3) For $D_{MAX} > 700$ Mbps, the minimum input voltage is 0.85 V; the maximum input voltage is 1.75 V. For $F_{MAX} \leq 700$ Mbps, the minimum input voltage is 0.45 V; the maximum input voltage is 1.95 V.

Power Consumption

Altera offers the Excel-based PowerPlay EPE and the Quartus® II PowerPlay Power Analyzer feature to estimate power consumption for your design.

Use the interactive Excel-based PowerPlay EPE before designing your HardCopy IV device to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of your design after placement and routing is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.

For supply current estimates for V_{CCPGM} and V_{CC_CLKIN}, refer to Table 1–6 on page 1–6. Use the PowerPlay EPE and Power Analyzer for current estimates of the remaining power supplies.

For more information about power estimation tools, refer to the PowerPlay Early Power Estimator page on the Altera website and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of HardCopy IV core and periphery blocks for commercial grade devices.

HardCopy IV devices can meet, at minimum, the –3 speed grade of the Stratix® IV devices. Silicon characterization determines the actual performance of the HardCopy IV devices. These characteristics are **Preliminary** or **Final**, as defined in the following:

- **Preliminary**—Created using simulation results, process data, and other known parameters.
- **Final**—Based on actual silicon characterization and testing.

These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

Transceiver Performance Specifications

This section describes transceiver performance specifications. Table 1–21 lists HardCopy IV GX transceiver specifications.

Table 1–21. HardCopy IV GX Transceiver Specifications (Part 1 of 5)

Symbol	Parameter	Min	Typ	Max	Unit
Reference Clock					
Input frequency from REFCLK input pins	—	50	—	672	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	325	MHz
Absolute Vmax for a REFCLK pin	—	—	—	1.6	V
Operational Vmax for a REFCLK pin	—	—	—	1.5	V
Absolute Vmin for a REFCLK pin	—	–0.4	—	—	V
Rise/fall time	—	—	—	0.2	UI
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCI Express	30	—	33	kHz
Spread-spectrum downspread	PCI Express	—	0 to –0.5%	—	—
OCT resistors	—	—	100	—	Ω
VICM (AC coupled)	—	—	1100	—	mV
VICM (DC coupled)	**HCSL** I/O standard for PCI Express reference clock	250	—	550	mV
Rref	—	—	2000 ±1%	—	Ω
Transceiver Clocks					
Calibration block clock frequency	—	10	—	125	MHz
fixedclk clock frequency	PCI Express Receiver Detect	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5 or 37.5 *(2)*	—	50	—
Transceiver block minimum power-down pulse width	—	—	1	—	µs

Table 1–21. HardCopy IV GX Transceiver Specifications (Part 2 of 5)

Symbol	Parameter	Min	Typ	Max	Unit
Receiver					
Data rate (Single width, non-PMA Direct)	—	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	6500	Mbps
Data rate (Single width, PMA Direct)	—	600	—	3250	Mbps
Data rate (Double width, PMA Direct)	—	1000	—	6500	Mbps
Absolute Vmax for a receiver pin *(3)*	—	—	—	1.6	V
Operational Vmax for a receiver pin	—	—	—	1.5	V
Absolute Vmin for receiver pin	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage VID (diff p-p)	VICM = 0.82-V setting	—	—	2.7	V
	VICM = 1.1-V setting *(4)*	—	—	1.6	V
Minimum peak-to-peak differential input voltage VID (diff p-p)	Data Rate = 600 Mbps to 5 Gbps	100	—	—	mV
	Data Rate > 5 Gbps	165	—	—	mV
VICM	VICM = 0.82-V setting	—	820	—	mV
	VICM = 1.1-V setting *(4)*	—	1100	—	mV
Differential OCT resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: –10dB	—	—	—
	XAUI	100 MHz to 2.5 GHz: –10dB	—	—	—
	(OIF) CEI	100 MHz to 4.875 GHz: –8dB 4.875GHz to 10GHz: 16.6 dB/decade slope	—	—	—
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: –6dB	—	—	—
	XAUI	100 MHz to 2.5 GHz: –6dB	—	—	—
	(OIF) CEI	100 MHz to 4.875 GHz: –6dB 4.875GHz to 10GHz: 16.6 dB/decade slope	—	—	—

Table 1–21. HardCopy IV GX Transceiver Specifications (Part 3 of 5)

Symbol	Parameter	Min	Typ	Max	Unit
Programmable PPM detector *(5)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000	—	—	ppm
Run length	—	—	80	—	Ui
Programmable equalization	—	—	—	16	dB
Signal detect/loss threshold	PCI Express (PIPE) Mode	65	—	175	mV
CDR LTR time *(6)*	—	—	—	75	µs
CDR minimum T1b *(7)*	—	15	—	—	µs
LTD lock time *(8)*	—	0	100	4000	ns
Data lock time from `rx_freqlocked` *(9)*	—	—	—	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	7872	`reconfig_clk` cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	dB
	DC Gain Setting = 1	—	3	—	dB
	DC Gain Setting = 2	—	6	—	dB
	DC Gain Setting = 3	—	9	—	dB
	DC Gain Setting = 4	—	12	—	dB
Transmitter					
Data rate (Single width, non-PMA Direct)	—	600	—	3750	Mbps
Data rate (Double width, non-PMA Direct)	—	1000	—	6500	Mbps
Data rate (Single width, PMA Direct) *(10)*	—	600	—	3250	Mbps
Data rate (Double width, PMA Direct) *(10)*	—	1000	—	6500	Mbps
VOCM	0.65-V setting	—	650	—	mV
Differential OCT resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω

Table 1–21. HardCopy IV GX Transceiver Specifications (Part 4 of 5)

Symbol	Parameter	Min	Typ	Max	Unit
Return loss differential mode	PCI Express	50 MHz to 1.25 GHz: –10 dB	—	—	—
	XAUI	312 MHz to 625 MHz: –10 dB 625 MHz to 3.125 GHz: -10 dB/decade slope	—	—	—
	(OIF) CEI	100 MHz to 4.875 GHz: –8 dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope	—	—	—
Return loss common mode	PCI Express	50 MHz to 1.25 GHz: –6 dB	—	—	—
	(OIF) CEI	100 MHz to 4.875 GHz: –6 dB 4.875 GHz to 10 GHz: 16.6 dB/decade slope	—	—	—
Rise time	—	50	—	200	ps
Fall time *(11)*	—	50	—	200	ps
Intra differential pair skew	—	—	—	15	ps
Intra-transceiver block skew ×4 PMA and PCS bonded	XAUI, PCI Express (PIPE) ×4, Basic ×4	—	—	120	ps
Inter-transceiver block skew ×8 PMA and PCS bonded	PCI Express (PIPE) ×8, Basic ×8	—	—	500	ps
Inter-transceiver block skew ×N PMA-Only bonded *(12)*	N < 18 channels located across three transceiver blocks with the source CMU PLL located in the center transceiver block	—	—	400	ps
CMU PLL0 and CMU PLL1					
Supported Data Range	—	600	—	6500	Mbps
CMU PLL lock time from `pll_powerdown` deassertion	—	—	—	100	µs
ATX PLL					
Supported Data Range *(13)*	/L = 1	4800 to 5400 and 6000 to 6375	—	—	Mbps
	/L = 2	2400 to 2700 and 3000 to 3187.5	—	—	Mbps
	/L = 4	1200 to 1350 and 1500 to 1593.75	—	—	Mbps

Table 1–21. HardCopy IV GX Transceiver Specifications (Part 5 of 5)

Symbol	Parameter	Min	Typ	Max	Unit
Transceiver-HCell Logic Interface					
Interface speed (non-PMA Direct)	—	25	—	250	MHz
Interface speed (PMA Direct)	—	50	—	325	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles	—	—	—

Notes to Table 1–21:

(1) The –2X speed grade is the fastest speed grade offered in the following HardCopy IV GX devices: HC4GX15LF780N, HC4GX25LF780N, HC4GX25LF1152N, HC4GX25FF1152N, HC4GX35FF1152N, HC4GX35LF1517N and HC4GX35FF1517N.

(2) The minimum `reconfig_clk` frequency is 2.5 MHz if you configure the transceiver channel in transmitter only mode. The minimum `reconfig_clk` frequency is 37.5 MHz if you configure the transceiver channel in receiver only or receiver and transmitter mode. For more information, refer to *HardCopy IV GX Dynamic Reconfiguration* chapter in volume 3 of the *HardCopy IV Device Handbook*.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) Use the 1.1-V RX VICM setting if the input serial data standard is **LVDS** and the link is DC coupled.

(5) The rate matcher supports only up to ±300 ppm.

(6) The duration for `rx_pll_locked` signal goes high from `rx_analogreset` deassertion. For more information, refer to Figure 1–2 on page 1–19.

(7) The duration for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` signal goes high and before `rx_locktodata` is asserted in manual mode. For more information, refer to Figure 1–2 on page 1–19.

(8) The duration for to recover valid data after the `rx_locktodata` signal is asserted in manual mode. For more information, refer to Figure 1–2 on page 1–19.

(9) The duration for to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. For more information, refer to Figure 1–3 on page 1–19.

(10) A general- purpose PLL (GPLL) may be required to meet PMA-HardCopy fabric interface timing above certain data rates and this requirement is the same as PMA-FPGA fabric interface. For more information, refer to section “Left/Right PLL Requirements in Basic (PMA Direct) Mode” in the *Stratix IV Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

(11) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(12) For applications that require low transmit lane-to-lane skew, use Basic (PMA Direct) xN to achieve PMA-Only bonding across all channels in the link. You can bond all channels on one side of your device by configuring the channels in Basic (PMA-Direct) xN mode. For more information about clocking requirements in Basic (PMA-Direct) xN mode, refer to the “Basic (PMA Direct) Mode Clocking” section in the *Stratix IV Transceiver Clocking* chapter in volume 2 of the *Stratix IV Device Handbook*.

(13) The Quartus II software automatically selects the appropriate /L divider depending upon the configured data rate.

Figure 1–2 shows the lock time parameters in manual mode. Figure 1–3 shows the lock time parameters in automatic mode.

LTD = Lock-To-Data; LTR = Lock-To-Reference

Figure 1–2. Lock Time Parameters for Manual Mode

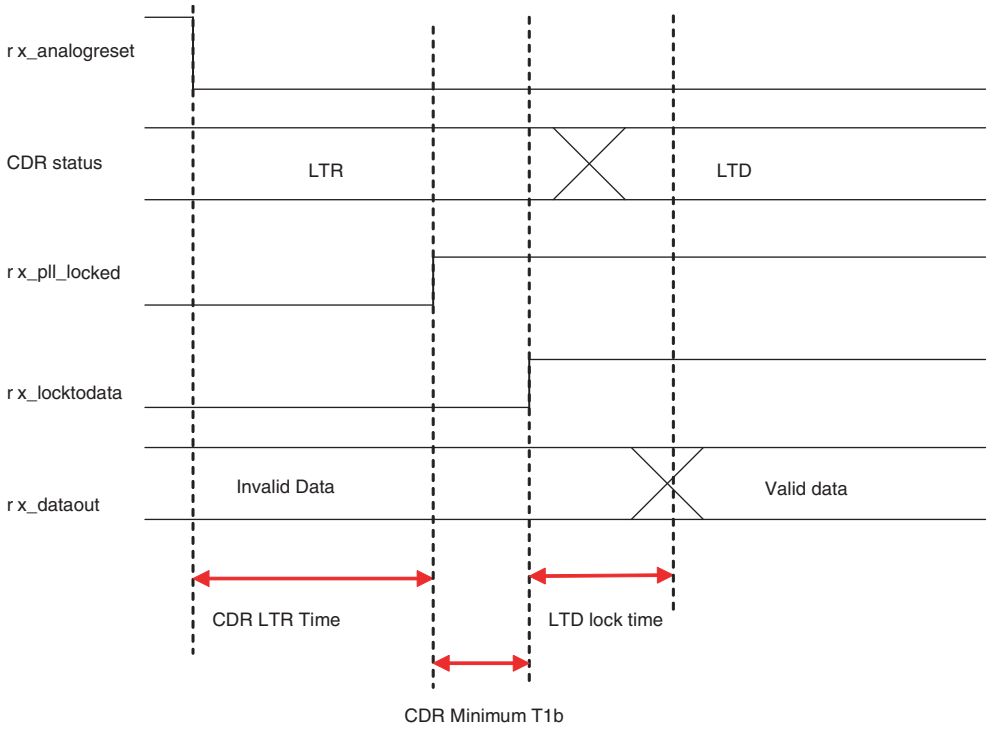


Figure 1–3. Lock Time Parameters for Automatic Mode

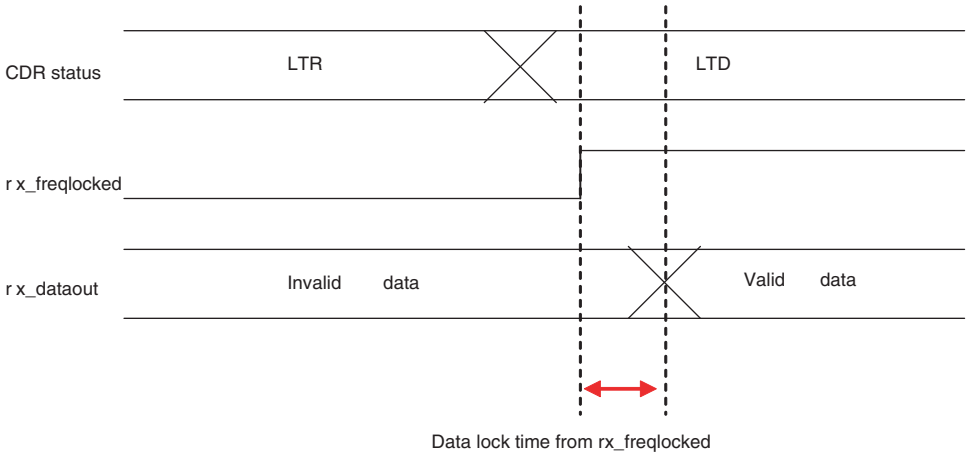


Table 1–22 through Table 1–25 list the typical V_{OD} for various differential termination settings for HardCopy IV GX devices.

Table 1–22. Typical VOD Setting, TX Term = 85 Ω

Symbol	VOD Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	170± 20%	340± 20%	510± 20%	595± 20%	680± 20%	765± 20%	850± 20%	1020± 20%

Table 1–23. Typical VOD Setting, TX Term = 100 Ω

Symbol	VOD Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	200± 20%	400± 20%	600± 20%	700± 20%	800± 20%	900± 20%	1000± 20%	1200± 20%

Table 1–24. Typical VOD Setting, TX Term = 120 Ω

Symbol	VOD Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	240± 20%	480± 20%	600± 20%	720± 20%	840± 20%	960± 20%	1080± 20%	1200± 20%

Table 1–25. Typical VOD Setting, TX Term = 150 Ω

Symbol	VOD Setting (mV)					
	0	1	2	3	4	5
VOD differential peak-to-peak Typical (mV)	300± 20%	600± 20%	900± 20%	1050± 20%	1200± 20%	1350± 20%

Table 1–26 lists typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–26 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

To estimate the pre-emphasis level for your specific data rate and pattern, run simulations using the HardCopy IV high-speed serial interface (HSSI) HSPICE models.

Table 1–26. Transmitter Pre-emphasis Levels for HardCopy IV Devices

Pre-emphasis First Post-Tap Setting	VOD Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	—	0.7	0	0	0	0	0	0
2	—	1	0.3	0	0	0	0	0
3	—	1.5	0.6	0	0	0	0	0
4	—	2	0.7	0.3	0	0	0	0
5	—	2.7	1.2	0.5	0.3	0	0	0
6	—	3.1	1.3	0.8	0.5	0.2	0	0
7	—	3.7	1.8	1.1	0.7	0.4	0.2	0
8	—	4.2	2.1	1.3	0.9	0.6	0.3	0
9	—	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	—	5.4	2.8	1.9	1.4	1	0.7	0.3
11	—	6	3.2	2.2	1.7	1.2	0.9	0.4
12	—	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	—	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	—	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	—	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	—	—	4.9	3.7	2.9	2.2	1.7	0.9
17	—	—	5.3	4	3.1	2.4	1.8	1.1
18	—	—	5.7	4.4	3.4	2.6	2	1.2
19	—	—	6.1	4.7	3.6	2.8	2.2	1.4
20	—	—	6.6	5.1	4	3.1	2.4	1.5
21	—	—	7	5.4	4.3	3.3	2.7	1.7
22	—	—	8	6.1	4.8	3.8	3	2
23	—	—	9	6.8	5.4	4.3	3.4	2.3
24	—	—	10	7.6	6	4.8	3.9	2.6
25	—	—	11.4	8.4	6.8	5.4	4.4	3
26	—	—	12.6	9.4	7.4	5.9	4.9	3.3
27	—	—	—	10.3	8.1	6.4	5.3	3.6
28	—	—	—	11.3	8.8	7.1	5.8	4
29	—	—	—	12.5	9.6	7.7	6.3	4.3
30	—	—	—	—	11.4	9	7.4	—
31	—	—	—	—	12.9	10	8.2	—

Table 1–27 lists HardCopy IV GX transceiver jitter specifications for all supported protocols.

Table 1–27. HardCopy IV GX Transceiver Block Jitter Specification *(Note 1)*, *(2)* (Part 1 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
SONET/SDH Transmit Jitter Generation *(3)*					
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS23	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS23	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS23	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS23	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance *(3)*					
Jitter tolerance at 622.08Mbps	Jitter frequency = 0.03KHz Pattern = PRBS23	> 15	> 15	> 15	UI
	Jitter frequency = 25KHz Pattern = PRBS24	> 1.5	> 1.5	> 1.5	UI
	Jitter frequency = 250KHz Pattern = PRBS25	> 0.15	> 0.15	> 0.15	UI
Jitter tolerance at 2488.32Mbps	Jitter frequency = 0.06KHz Pattern = PRBS23	> 15	> 15	> 15	UI
	Jitter frequency = 100KHz Pattern = PRBS24	> 1.5	> 1.5	> 1.5	UI
	Jitter frequency = 1MHz Pattern = PRBS25	> 0.15	> 0.15	> 0.15	UI
	Jitter frequency = 10MHz Pattern = PRBS26	> 0.15	> 0.15	> 0.15	UI
Fibre Channel Transmit Jitter Generation *(4)*, *(12)*					
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	UI
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	—	—	0.33	UI
Fibre Channel Receiver Jitter Tolerance *(4)*, *(13)*					
Deterministic jitter FC-1	Pattern = CJTPAT		> 0.37		UI
Random jitter FC-1	Pattern = CJTPAT		> 0.31		UI
Sinusoidal jitter FC-1	Fc/25000		> 1.5		UI
	Fc/1667		> 0.1		UI
Deterministic jitter FC-2	Pattern = CJTPAT		> 0.33		UI

Table 1–27. HardCopy IV GX Transceiver Block Jitter Specification *(Note 1)*, *(2)* (Part 2 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
Random jitter FC-2	Pattern = CJTPAT		> 0.29		UI
Sinusoidal jitter FC-2	Fc/25000		> 1.5		UI
	Fc/1667		> 0.1		UI
Deterministic jitter FC-4	Pattern = CJTPAT		> 0.33		UI
Random jitter FC-4	Pattern = CJTPAT		> 0.29		UI
Sinusoidal jitter FC-4	Fc/25000		> 1.5		UI
	Fc/1667		> 0.1		UI
XAUI Transmit Jitter Generation *(5)*					
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	UI
XAUI Receiver Jitter Tolerance *(5)*					
Total jitter	—		> 0.65		UI
Deterministic jitter	—		> 0.37		UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1		UI
PCI Express Transmit Jitter Generation *(6)*					
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	UI
Total jitter at 5 Gbps (Gen2)	Compliance pattern	—	—	—	UI
PCI Express Receiver Jitter Tolerance *(6)*					
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6		UI
Total jitter at 2.5 Gbps (Gen2)	Compliance pattern	—	—	—	UI
Serial RapidIO Transmit Jitter Generation *(7)*					
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	UI
Serial RapidIO Receiver Jitter Tolerance *(7)*					
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.37		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.55		UI

Table 1–27. HardCopy IV GX Transceiver Block Jitter Specification *(Note 1)*, *(2)* (Part 3 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 8.5		UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1		UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1		UI
GIGE Transmit Jitter Generation *(8)*					
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	UI
GIGE Receiver Jitter Tolerance *(8)*					
Deterministic jitter (peak-to-peak)	Pattern = CJPAT		> 0.4		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.66		UI
HiGig Transmit Jitter Generation *(9)*					
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
HiGig Receiver Jitter Tolerance *(9)*					
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
	Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	—	UI

Table 1–27. HardCopy IV GX Transceiver Block Jitter Specification *(Note 1)*, *(2)* (Part 4 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
(OIF) CEI Transmitter Jitter Generation *(10)*					
Total jitter (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS15 BER = 10exp-12	—	—	—	UI
(OIF) CEI Receiver Jitter Tolerance *(10)*					
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-13	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
	Jitter Frequency = 3.82 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
	Jitter Frequency = 20 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 BER = 10exp-12	—	—	—	UI
SDI Transmitter Jitter Generation *(11)*					
Alignment jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.2	—	—	UI
	Data Rate = 2.97 Gbps (3G) Pattern = Color Bar Low-Frequency Roll-Off = 100 KHz	0.3	—	—	UI
SDI Receiver Jitter Tolerance *(11)*					
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 2			UI
	Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 0.3			UI
	Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) Pattern = Single Line Scramble Color Bar	> 0.3			UI

Table 1–27. HardCopy IV GX Transceiver Block Jitter Specification *(Note 1)*, *(2)* (Part 5 of 5)

Symbol/Description	Conditions	Min	Typ	Max	Unit
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 1		UI
	Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 0.2		UI
	Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) Pattern = 75% Color Bar		> 0.2		UI

Notes to Table 1–27:

(1) Dedicated `refclk` pins drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(4) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.1.0.
(5) The jitter number for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(6) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(7) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(8) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(9) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(10) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(11) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(12) The fibre channel transmitter jitter generation numbers are compliant to the specification at δ_T interoperability point.
(13) The fibre channel receiver jitter tolerance numbers are compliant to the specification at δ_R interoperability point.

Core Performance Specifications

This section describes the clock tree, PLL, DSP, TriMatrix, and configuration and JTAG specifications.

Clock Tree Specifications

Table 1–28 lists clock tree performance specifications for the logic array, DSP blocks, and TriMatrix memory blocks for HardCopy IV devices.

Table 1–28. HardCopy IV Clock Tree Performance

Device	Maximum Frequency	Unit
HC4E25	600	MHz
HC4E35	600	MHz

PLL Specifications

Table 1–29 describes the HardCopy IV PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C). For a PLL block diagram, refer to Figure 1–8 on page 1–36.

Table 1–29. HardCopy IV PLL Specifications (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	5	—	717 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	—	—	600	MHz
f_{OUT_EXT}	Output frequency for external clock input (–3 speed grade)	—	—	717 *(2)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chain	—	3.5	—	`scanclk` cycles
$t_{CONFIGPHASE}$	Time required or reconfigure phase shift	—	1	—	`scanclk` cycles
$f_{SCANCLK}$	`scanclk` frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on a reset signal	10	—	—	ns
t_{INCCJ} *(3)*	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} *(4)*	Period jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC} *(4)*	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} *(4)*	Period Jitter for clock output on regular IO ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular IO ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} *(4)*	Cycle-to-cycle jitter for clock output on regular IO ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle jitter for clock output on regular IO ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)

Table 1–29. HardCopy IV PLL Specifications (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CASC\_OUTPJ\_DC}$ *(4)*	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq$ 100 MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs (F_{OUT} < 100 MHz)	—	—	25	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 us	—	—	±10	%

Notes to Table 1–29:

(1) This specification is limited in Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 120 ps.

(4) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–38.

DSP Block Specifications

Table 1–30 describes the HardCopy IV DSP block performance specifications.

Table 1–30. HardCopy IV DSP Block Performance Specifications *(Note 1)*

Mode	Number of Multipliers	Maximum Frequency		Unit
		Flipchip	Wirebond	
9 × 9-bit multiplier (a, c, e, g)	1	345	276	MHz
9 × 9-bit multiplier (b, d, f, h)	1	385	308	MHz
12 × 12-bit multiplier (a, e)	1	345	276	MHz
12 × 12-bit multiplier (b, d, f, h)	1	385	308	MHz
18 × 18-bit multiplier	1	425	340	MHz
36 × 36-bit multiplier	1	345	276	MHz
18 × 18-bit multiply accumulator	4	370	296	MHz
18 × 18-bit multiply adder	4	380	304	MHz
18 × 18-bit multiply adder-signed full precision	2	380	304	MHz
18 × 18-bit multiply adder with loopback *(2)*	2	300	240	MHz
36-bit shift (32 bit data)	1	370	296	MHz
Double mode	1	345	276	MHz

Notes to Table 1–30:

(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.

(2) Maximum is for non-pipelined block with loopback input registers disabled and **Round** and **Saturation** disabled.

TriMatrix Memory Block Specifications

Table 1–31 lists the HardCopy IV TriMatrix memory block specifications.

Table 1–31. HardCopy IV TriMatrix Memory Block Performance Specifications (Part 1 of 2)

Memory	Mode	TriMatrix Memory	Maximum Frequency		Unit
			Flipchip	Wirebond	
MLAB	Single port 16 × 10	1	500	375	MHz
	Simple dual-port 16 × 20	1	500	375	MHz
	ROM 64 × 10	1	500	375	MHz
	ROM 32 × 20	1	500	375	MHz
M9K	Single-port 8K × 1	1	540	405	MHz
	Single-port 4K × 2 or 2K × 4	1	540	405	MHz
	Single-port 1K × 9, 512 × 18, or 256 × 36	1	540	405	MHz
	Simple dual-port, 8K × 1	1	490	368	MHz
	Simple dual-port, 4K × 2 or 2K × 4	1	490	368	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36	1	490	368	MHz
	Simple dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to “Old Data”	1	340	255	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36 with the read-during-write option set to “Old Data”	1	340	255	MHz
	True dual-port, 8K × 1	1	430	323	MHz
	True dual-port, 4K × 2 or 2K × 4	1	430	323	MHz
	True dual-port, 1K × 9 or 512 × 18	1	430	323	MHz
	True dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to “Old Data”	1	335	236	MHz
	True dual-port, 1K × 9 or 512 × 18 with the read-during-write option set to “Old Data”	1	335	236	MHz
	ROM 1P, 8K × 1, 4K × 2, or 2K × 4	1	540	405	MHz

Table 1–31. HardCopy IV TriMatrix Memory Block Performance Specifications (Part 2 of 2)

Memory	Mode	TriMatrix Memory	Maximum Frequency		Unit
			Flipchip	Wirebond	
M9K	ROM 1P, 1K × 9, 512 × 18, or 256 × 36	1	540	405	MHz
	ROM 2P, 8K × 1, 4K × 2, or 2K × 4	1	540	405	MHz
	ROM 2P, 1K × 9, or 512 × 18	1	540	405	MHz
	Min Pulse Width (Clock High Time)	—	800	1067	ps
	Min Pulse Width (Clock Low Time)	—	625	831	ps
M144K	True dual-port 16K × 9 or 8K × 18	1	350	263	MHz
	True dual-port 4K × 36	1	350	263	MHz
	Simple dual-port 16K × 9 or 8K × 18	1	375	281	MHz
	Simple dual-port 4K × 36 or 2K × 72	1	375	281	MHz
	ROM 1 Port	1	450	338	MHz
	ROM 2 Port	1	425	319	MHz
	Single-port 16K × 9 or 8K × 18	1	400	300	MHz
	Single-port 4K × 36	1	400	300	MHz
	True dual-port 16K × 9, 8K × 18, or 4K × 36 with the read-during-write option set to “Old Data”	1	225	169	MHz
	Simple dual-port 16K × 9, 8K × 18, 4K × 36, or 2K × 72 with the read-during-write option set to “Old Data”	1	225	169	MHz
	Simple dual-port 2K × 64 (with ECC)	1	295	221	MHz
	Min Pulse Width (Clock High Time)	—	1382	1843	ps
	Min Pulse Width (Clock Low Time)	—	690	920	ps

JTAG Specification

Table 1–32 lists the JTAG timing parameters and values for HardCopy IV devices. For JTAG timing requirements, refer to the "High-speed I/O Block" row in Table 1–39 on page 1–35.

Table 1–32. HardCopy IV JTAG Timing Parameters and Values

Symbol	Description	Flipchip		Wirebond		Unit
		Min	Max	Min	Max	
t_{JCP}	TCK clock period	30	—	40	—	ns
t_{JCH}	TCK clock high time	14	—	19	—	ns
t_{JCL}	TCK clock low time	14	—	19	—	ns
t_{JPSU_TDI}	TDI JTAG port setup time	1	—	1	—	ns
t_{JPSU_TMS}	TMS JTAG port setup time	3	—	3	—	ns
t_{JPH}	JTAG port hold time	5	—	5	—	ns
t_{JPCO}	JTAG port clock to output	—	14 *(1)*	—	16 *(1)*	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 *(1)*	—	16 *(1)*	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 *(1)*	—	16 *(1)*	ns

Note to Table 1–32:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 15 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 16 ns if it equals 1.8 V.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface, and OCT calibration block specifications.

High-Speed I/O Specification

Table 1–33 shows the high-speed I/O timing for HardCopy IV devices.

Table 1–33. High-Speed I/O Specifications—Preliminary (Part 1 of 2) *(Note 1), (2), (3)*

Symbol	Conditions	FlipChip			Wirebond		
		Min	Typ	Max	Min	Typ	Max
Transmitter							
Dedicated LVDS—f_{HSDR} (data rate)	SERDES factor J = 3 to 10	150	—	1250	150	—	840
	SERDES factor J = 2, uses DDR registers	*(4)*	—	1250	*(4)*	—	840
	SERDES factor J = 1, uses SDR register	*(4)*	—	717	*(4)*	—	450
LVDS_E_3R—$f_{HSDRDPA}$ (data rate)	SERDES factor J =4 to 10	*(4)*	—	1000	*(4)*	—	640
LVDS_E_1R—$f_{HSDRDPA}$ (data rate)		*(4)*	—	200	*(4)*	—	170
t_x Jitter	Total Jitter for data rate, 600 Mbps - 1.6G bps	—	—	160	—	—	160
	Total Jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1

Table 1–33. High-Speed I/O Specifications—Preliminary (Part 2 of 2) ***(Note 1), (2), (3)***

Symbol	Conditions	FlipChip			Wirebond		
		Min	Typ	Max	Min	Typ	Max
t_{DUTY}	Tx output clock duty cycle	45	50	55	45	50	55
t_{RISE} and t_{FALL}	Dedicated LVDS	—	—	200	—	200	—
	LVDS_E_3R	—	—	350	—	350	—
	LVDS_E_1R	—	—	500	—	500	—
TCCS	Dedicated LVDS	—	—	100	—	—	200
	LVDS_E_3R/ LVDS_E_1R	—	—	250	—	—	250
Receiver							
$f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	—	1250	150	—	840
DPA Mode							
DPA run length	—	—	—	10000	—	—	10000
Soft CDR mode							
Soft-CDR PPM tolerance	—	—	—	300	—	—	
Non DPA Mode							
Sampling Window	All differential I/O standards	—	—	300	—	—	400

Notes to Table 1–33:

(1) Numbers are preliminary pending characterization.

(2) When J = 3 to 10, the SERDES block is used.

(3) When J = 1 or 2, the SERDES block is bypassed.

(4) The minimum specification is dependent on the clock source (for example, PLL and clock pin) and the clock routing resource (global, regional, or local) is used.

Table 1–34 lists the DPA lock time specifications for HardCopy IV devices.

Table 1–34. DPA Lock Time Specifications—Preliminary *(Note 1)*, *(2)*, *(3)*

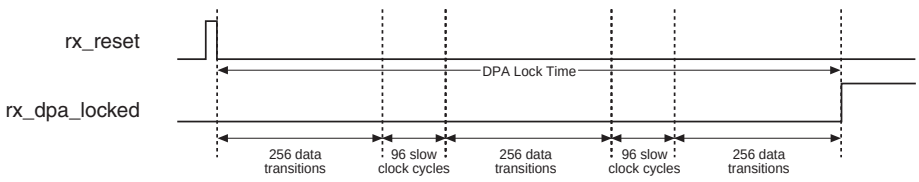
Standard	Training Pattern	Number of Data Transitions in one repetition of training pattern	Number of repetition per 256 data transition *(4)*	Condition	Min	Typ	Max
SPI-4	00000000001111111111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles *(5)*, *(6)*	—	—
Parallel Rapid I/O	00001111	2	128	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles *(5)*, *(6)*	—	—
	10010000	4	64	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles *(5)*, *(6)*	—	—
Misc.	10101010	8	32	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles *(5)*, *(6)*	—	—
	01010101	8	32	without DPA PLL calibration	256 data transitions	—	—
				with DPA PLL calibration	3 × 256 data transitions + 2 × 96 slow clock cycles *(5)*, *(6)*	—	—

Notes to Table 1–34:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in the table applies to both commercial and industrial grade.
(4) This is the number of repetition for the stated training pattern to achieve 256 data transitions.
(5) Slow clock = data rate (MHz)/deserialization factor.
(6) The DPA lock time with **DPA PLL Calibration** enabled is preliminary.

Figure 1–4 shows the DPA lock time specifications with DPA PLL calibration enabled.

Figure 1–4. DPA Lock Time Specification with DPA PLL Calibration Enabled



DLL and DQS Logic Block Specifications

Table 1–35 describes the delay-locked loop (DLL) frequency range specifications for HardCopy IV devices. Table 1–36 shows the average DQS offset delay for setting.

Table 1–35. HardCopy IV DLL Frequency Range Specifications

Frequency Mode	DQS Delay Setting	Number of Delay Chains	f_{MIN} (MHz)	f_{MAX} (MHz)
0	6 bits	16	90	130
1	6 bits	12	120	170
2	6 bits	10	150	210
3	6 bits	8	180	250
4	5 bits	12	240	320
5	5 bits	10	290	380
6	5 bits	8	360	450
7	5 bits	6	430	590

Table 1–36. Average DQS Phase Offset Delay per Setting *(1), (2), (3)*

Minimum	Typical	Maximum	Unit
7	11	15	ps

Notes to Table 1–36:

(1) The valid settings for phase offset are –64 to +63 for frequency modes 0 to 3 and –32 to +31 for frequency modes 4 to 6.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear with a cumulative delay variation of ±20ps for all speed grades.

OCT Calibration Block Specifications

Table 1–37 describes the OCT calibration block specifications for HardCopy IV devices.

Table 1–37. OCT Calibration Block Specifications

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	28	—	Cycles
T_{RS_RT}	Time required to dynamically switch from R_S to R_T	—	2.5	—	ns

Duty Cycle Distortion (DCD) Specifications

Table 1–38 lists the worst case DCD for HardCopy IV devices.

Table 1–38. DCD on HardCopy IV I/O Pins

Symbol	Min	Max	Unit
Output Duty Cycle	45	55	%

I/O Timing

Altera offers the Excel-based I/O Timing spreadsheet and the Quartus II TimeQuest Timing Analyzer to determine I/O timing.

Excel-based I/O Timing spreadsheet provides pin timing performance for each device density and speed grade. Use the data before designing the HardCopy device to get an estimate of the timing budget as part of the link timing analysis. The TimeQuest analyzer provides a more accurate and precise I/O timing data based on the specifics of your design after completing placement and routing.

You can download the Excel-based I/O Timing spreadsheet from the HardCopy IV Devices Literature web page.

Glossary

Table 1–39 shows the glossary for this chapter.

Table 1–39. Glossary Table (Part 1 of 4)

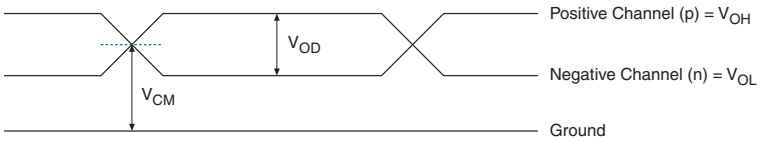
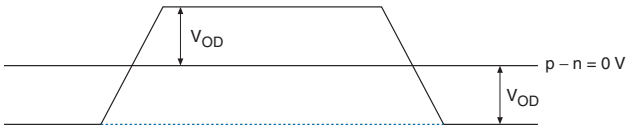
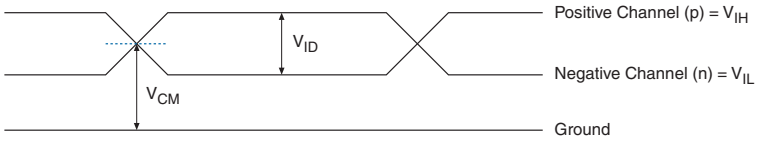
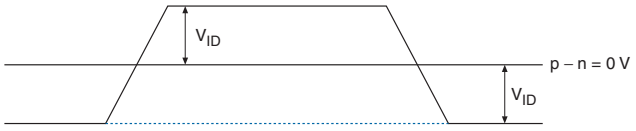
Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—
D	Differential I/O Standards	**Figure 1–5. Receiver Input Waveforms** Single-Ended Waveform  Differential Waveform  **Figure 1–6. Transmitter Output Waveforms** Single-Ended Waveform  Differential Waveform 

Table 1–39. Glossary Table (Part 2 of 4)

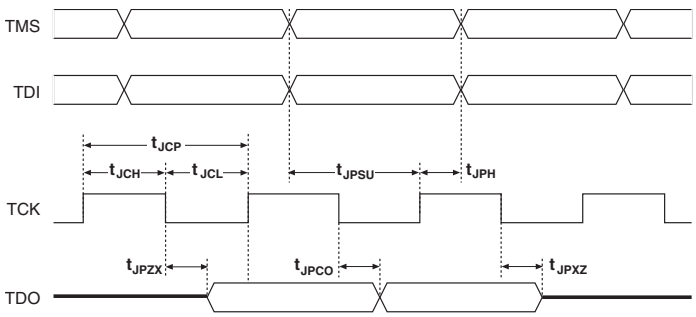
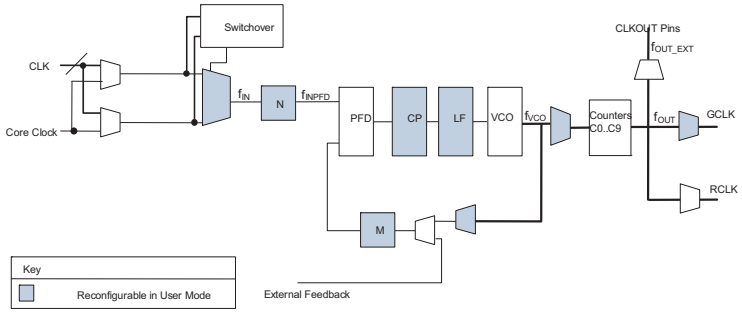
Letter	Subject	Definitions
E	—	—
F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block: Maximum/minimum **LVDS** data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block: Maximum/minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G	—	—
H	—	—
I	—	—
J	J	High-speed I/O block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	**Figure 1–7. JTAG Timing Specifications** 
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	**PLL Specifications**	Figure 1–8 shows the PLL specification parameters: **Figure 1–8. Diagram of PLL Specifications *(1)***  **Note to Figure 1–8:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to HardCopy IV device).

Table 1–39. Glossary Table (Part 3 of 4)

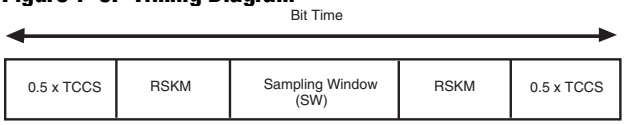
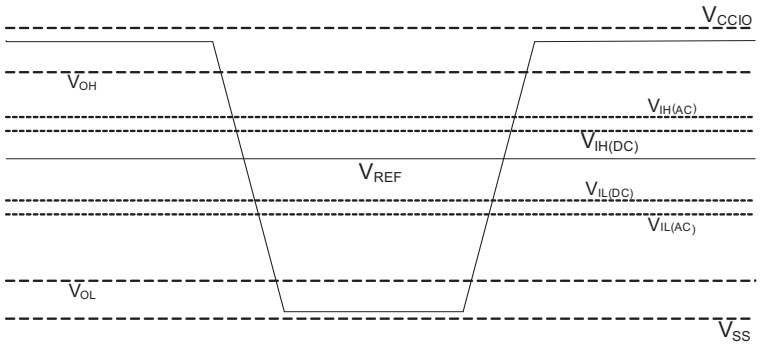
Letter	Subject	Definitions
S	**SW (sampling window)**	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown in Figure 1–9: **Figure 1–9. Timing Diagram** 
	Single-ended voltage referenced I/O standard	The JEDEC standard for **SSTI** and **HSTL** I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown in Figure 1–10: **Figure 1–10. Single-Ended Voltage Referenced I/O Standard** 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{C0} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table).
	t_{DUTY}	High-speed I/O block: Duty cycle on high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_c/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on PLL clock input
	t_{OUTPJ_IO}	Period jitter on general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20-80%)
U	—	—

Table 1–39. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage: Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block: Clock boost factor
X	—	—
Y	—	—
Z	—	—

Document Revision History

Table 1–40 shows the revision history for this chapter.

Table 1–40. Document Revision History

Date	Version	Changes
December 2011	2.1	■ Updated t_{RAMP} PORSEL value in Table 1–4. ■ Updated HardCopy IV I/O pin leakage current value. ■ Added Table 1–8 Bus Hold Specifications ■ Updated Single-Ended SSTL and HSTL I/O Reference Voltage Specifications ■ Updated supply current specifications for V_{CC_CLKIN} and V_{CCPGM} values. ■ Updated JTAG timing parameters values. ■ Updated DSP block performance specification. ■ Updated the TriMatrix memory block performance specifications. ■ Updated DLL frequency range specifications. ■ Updated hot socketing values. ■ Updated device capacitance values. ■ Updated internal weak pull-up resistor values. ■ Updated I/O OCT resistance tolerance values. ■ Updated OCT with calibration specification values. ■ Updated OCT variation after power-up calibration values. ■ Updated PLL specifications values. ■ Updated operating junction temperature value. ■ Minor text edits.
January, 2011	2.0	■ Updated Table 1–5, Table 1–20, Table 1–21, Table 1–22, Table 1–23, Table 1–28, Table 1–30, and Table 1–32. ■ Added Table 1–24. ■ Removed “External Memory Interface Specifications” section. ■ Updated “I/O Timing” section. ■ Made general formatting update.
March, 2010	1.0	Metadata corrected. No changes made to document.
June, 2009	1.0	Initial release.

2. Extended Temperature Range for HardCopy IV Devices

HIV54002-1.0

As part of the Altera® initiative to provide enhanced commercial off-the-shelf (COTS) devices for wider applications, the temperature range for the HardCopy® IV device families has been extended to enable operation across the extended temperature range (–40°C to 125°C). This extension allows design engineers who are working on systems with stringent temperature requirements to benefit from the cost savings by using commercially available HardCopy IV ASICs.

HardCopy IV ASICs are extremely robust and capable of operating across a wide temperature range with excellent reliability. This chapter describes the Altera support for HardCopy IV extended temperature range operation with the appropriate background information. It also explains how to use HardCopy IV devices across the extended temperature range operation, along with any limitations in operation that affect the HardCopy IV datasheet specifications.

These guidelines have been determined through additional characterization of HardCopy IV devices on samples of production silicon across the extended temperature ranges (125°C and –40°C). While characterizations demonstrate correct operation across extended temperatures by design, production testing of industrial grade devices for extended temperature range operation is performed at 100°C.

Extended Temperature Support

Extended temperature operation requires additional timing margin over industrial temperature operation to compensate for the potentially increased variation of f_{MAX} across temperature. For the Stratix® IV FPGA prototype devices, the increased timing margin is achieved by compiling the design using an industrial I4 part and setting the temperature range from –40°C to 125°C in the Quartus® II software. The Quartus II software provides separate timing models at 125°C for slow corner and –40°C for fast corner. By selecting a HardCopy IV companion device and extended temperature range (–40°C min and 125°C max) in the operating temperature condition, the Quartus II software uses the appropriate timing models to ensure that the constraints of extended temperature range operation are met.

The extended temperature range support design flow is the same as that for commercial and industrial devices. Use the Quartus II HardCopy IV Advisor to help guide you through the flow to ensure your design is ready for submission to the Altera HardCopy Design Center.

Table 2–1 lists the HardCopy IV device part numbers that support the extended temperature operation.

Table 2–1. HardCopy IV Extended Temperature Support

HardCopy Family	Device	Package	Extended Temperature Support
HardCopy IV	HC4E25	All	Yes
	HC4E35	All	Yes
	HC4GX15	All	Yes
	HC4GX25	All	Yes
	HC4GX35	All	Yes

Software Support

The HardCopy IV extended temperature grade device models are supported in the following versions of these tools:

- The PowerPlay Early Power Estimator (EPE) or the PowerPlay Power Analyzer software, version 11.1 or later. Download these tools from: www.altera.com/support/devices/estimator/pow-powerplay.html
- The Quartus II software, version 11.1 or later. Download the software from: www.altera.com/products/software/quartus-ii/subscription-edition/qts-se-index.html

Limitations to Datasheet Specifications

This section describes the limitations to the HardCopy IV datasheet specifications when operating HardCopy IV devices at extended temperature range. Characterization results show that HardCopy IV device operation across the extended temperature range is bounded by the industrial grade of the datasheet specifications and any relevant errata, except where noted below.

DSP Block Specifications

Table 2–2 lists the HardCopy IV DSP block performance specifications.

Table 2–2. HardCopy IV DSP Block Performance Specifications (Part 1 of 2) ***(Note 1)***

Mode	Number of Multipliers	Maximum Frequency		Unit
		Flipchip	Wirebond	
9 x 9-bit multiplier (a, c, e, g) *(2)*	1	315	252	MHz
9 x 9-bit multiplier (b, d, f, h) *(2)*	1	375	300	MHz
12 x 12-bit multiplier (a, e) *(3)*	1	315	252	MHz
12 x 12-bit multiplier (b, d, f, h) *(3)*	1	375	300	MHz
18 x 18-bit multiplier	1	400	320	MHz
36 x 36-bit multiplier	1	315	252	MHz
Double mode	1	315	252	MHz
18 x 18-bit multiply accumulator	4	330	264	MHz

Table 2–2. HardCopy IV DSP Block Performance Specifications (Part 2 of 2) *(Note 1)*

Mode	Number of Multipliers	Maximum Frequency		Unit
		Flipchip	Wirebond	
18 x 18-bit multiply adder	4	345	276	MHz
18 x 18-bit multiply adder-signed full precision	2	345	276	MHz
18 x 18-bit multiply adder with loopback *(4)*	2	300	240	MHz
36-bit shift (32-bit data)	1	330	264	MHz

Notes to Table 2–2:

(1) The maximum is for a fully pipelined block with **round** and **saturation** disabled.

(2) The DSP block implements eight independent 9 x 9-bit multipliers using a, b, c, and d for the top half of the DSP block; and e, f, g, and h for the bottom half of the DSP block multipliers.

(3) The DSP block implements six independent 12 x 12-bit multipliers using a, b, and d for the top half of the DSP block; and e, f, and h for the bottom half of the DSP block multipliers.

(4) The maximum for a non-pipelined block with loopback input registers disabled with **round** and **saturation** disabled.

TriMatrix Memory Block Specifications

Table 2–3 lists the HardCopy IV TriMatrix memory block specifications.

Table 2–3. HardCopy IV TriMatrix Memory Block Performance Specifications (Part 1 of 2)

Memory	Mode	TriMatrix Memory	Maximum Frequency		Unit
			Flipchip	Wirebond	
MLAB	Single port 16 × 10	1	450	338	MHz
	Simple dual-port 16 × 20	1	450	338	MHz
	ROM 64 × 10	1	450	338	MHz
	ROM 32 × 20	1	450	338	MHz
M9K	Single-port 8K × 1	1	405	304	MHz
	Single-port 4K × 2 or 2K × 4	1	405	304	MHz
	Single-port 1K × 9, 512 × 18, or 256 × 36	1	460	345	MHz
	Simple dual-port, 8K × 1	1	400	300	MHz
	Simple dual-port, 4K × 2 or 2K × 4	1	400	300	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36	1	400	300	MHz
	Simple dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to “Old Data”	1	265	199	MHz
	Simple dual-port, 1K × 9, 512 × 18, or 256 × 36 with the read-during-write option set to “Old Data”	1	265	199	MHz
	True dual-port, 8K × 1	1	435	326	MHz

Table 2–3. HardCopy IV TriMatrix Memory Block Performance Specifications (Part 2 of 2)

Memory	Mode	TriMatrix Memory	Maximum Frequency		Unit
			Flipchip	Wirebond	
M9K	True dual-port, 4K × 2 or 2K × 4	1	370	278	MHz
	True dual-port, 1K × 9 or 512 × 18	1	370	278	MHz
	True dual-port, 8K × 1, 4K × 2, or 2K × 4 with the read-during-write option set to "Old Data"	1	245	184	MHz
	True dual-port, 1K × 9 or 512 × 18 with the read-during-write option set to "Old Data"	1	245	184	MHz
	ROM 1P, 8K × 1, 4K × 2, or 2K × 4	1	405	304	MHz
	ROM 1P, 1K × 9, 512 × 18, or 256 × 36	1	405	304	MHz
	ROM 2P, 8K × 1, 4K × 2, or 2K × 4	1	405	304	MHz
	ROM 2P, 1K × 9, or 512 × 18	1	405	304	MHz
	Min Pulse Width (Clock High Time)	—	800	1067	ps
	Min Pulse Width (Clock Low Time)	—	625	831	ps
M144K	True dual-port 16K × 9 or 8K × 18	1	310	233	MHz
	True dual-port 4K × 36	1	310	233	MHz
	Simple dual-port 16K × 9 or 8K × 18	1	325	244	MHz
	Simple dual-port 4K × 36 or 2K × 72	1	325	244	MHz
	ROM 1 Port	1	420	315	MHz
	ROM 2 Port	1	380	285	MHz
	Single-port 16K × 9 or 8K × 18	1	350	263	MHz
	Single-port 4K × 36	1	350	263	MHz
	True dual-port 16K × 9, 8K × 18, or 4K × 36 with the read-during-write option set to "Old Data"	1	200	150	MHz
M144K	Simple dual-port 16K × 9, 8K × 18, 4K × 36, or 2K × 72 with the read-during-write option set to "Old Data"	1	200	150	MHz
	Simple dual-port 2K × 64 (with ECC)	1	245	171	MHz
	Min Pulse Width (Clock High Time)	—	1382	1843	ps
	Min Pulse Width (Clock Low Time)	—	690	920	ps

Transceiver Performance Specifications

Transceiver performance is supported up to 3Gbps protocols only.

For additional information about extended temperature support, refer to the *Stratix IV Military Temperature Range Support Technical Brief* and the *HardCopy IV PowerPlay Early Power Estimator*.

Document Revision History

Table 2–4 lists the revision history for this document.

Table 2–4. Document Revision History

Date	Version	Changes
March 2012	1.0	Initial release.

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>*.**pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.