AES3/EBU Reference Design

Version 1.1, February 2005 Application Note

Introduction

The Audio Engineering Society and the European Broadcasting Union developed the AES3/EBU digital audio transmission standard. AES3/EBU is a serial point-to-point interface that carries digital audio data over a standard cable. Audio data is typically in pulse code modulation (PCM) format. The reference design also supports compressed audio and non-audio data transmission. The information sent over the AES3/EBU is (non-return to zero) NRZ coded with the BPM (bi-phase mark code) so clock and data can be recovered on the receive side of the interface.

The AES3/EBU reference design provides both a transmitter and a receiver. The receiver extracts the data and the clock from an incoming AES3/EBU stream and stores the parallel audio data and control bits into a FIFO buffer.

The received information can be extracted from the FIFO buffer for processing, or sent directly to the transmitter. The AES3/EBU nominal data rate is directly related to the source audio sample rate. The receiver's input data rate is set at compile time to a fixed frequency, supporting PCM sample rates up to 192 kHz.

The transmitter takes parallel data from a FIFO buffer, performs serialization, parity bit generation, bi-phase coding, and appends the appropriate X,Y, Z header. It performs null-packet stuffing when no audio data is present in the transmit FIFO buffer. The transmit clock may be derived from an asynchronous source or it may be locked to an extracted receive clock via an external voltage-controlled crystal oscillator (VCXO).

Altera supplies the AES3/EBU reference design as Verilog HDL source code. The reference design includes transmit and receive blocks, testbenches, which allow you to test the Verilog HDL source code, Quartus® II implementation constraints, and demonstrations that run on Altera® Stratix GX and Cyclone Video Demonstration Boards.

For more information on the Stratix GX Video Demonstration Board see the *Stratix GX Video Demonstration Board Data Sheet*; for more information on the Cyclone Video Demonstration Board see the *Cyclone Video Demonstration Board Data Sheet*.

The reference design can also address the Sony/Philips digital interface (S/PDIF), if the electrical interface for S/PDIF is adhered to.

For S/PDIF, some differences exist in the interpretation of the channel status block registers, but the reference design needs no changes for S/PDIF.

This application note includes the following topics:

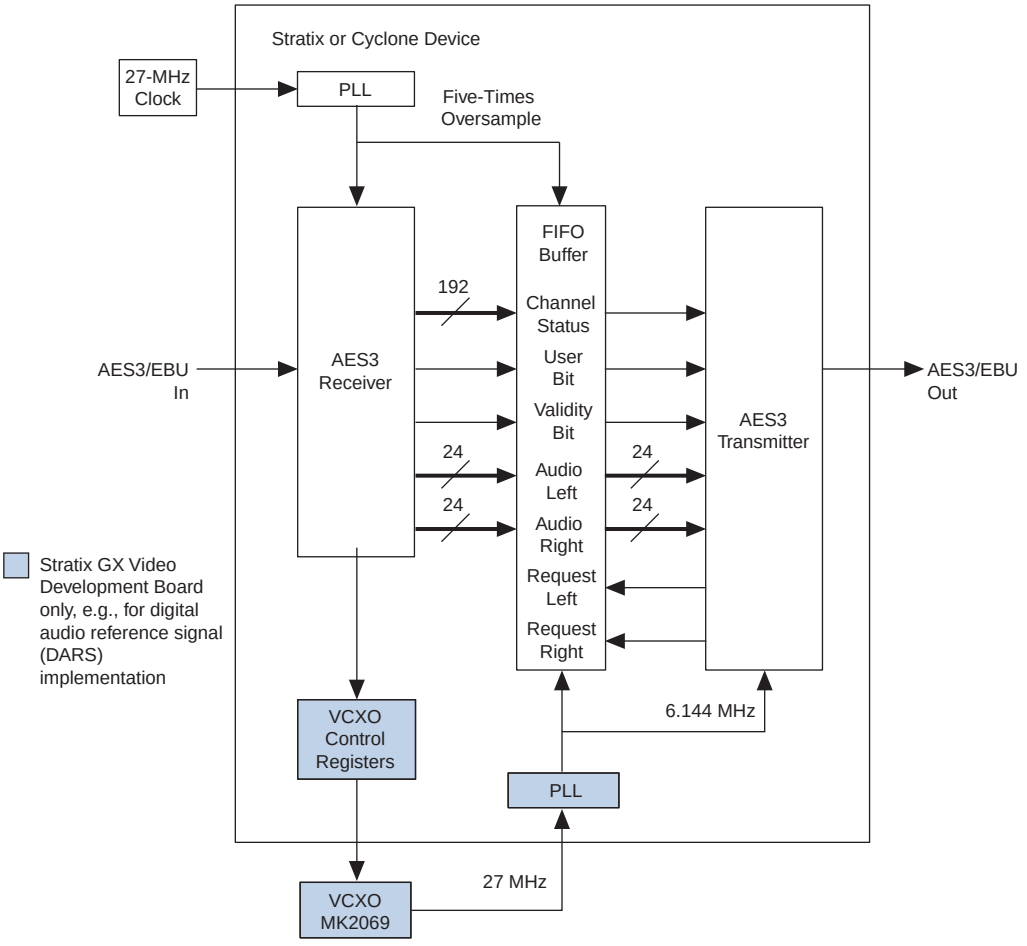
Features

- AES3/EBU transmit and receive functionality
- Control channel status block capture on the receiver
- Control channel status block insertion for the transmitter
- Hardware cyclic redundancy code (CRC) checking on the receiver
- Hardware CRC generation on the transmitter
- S/PDIF compatibility

Functional Description

Figure 1 shows the reference design block diagram.

Figure 1. Block Diagram



The AES3/EBU reference design comprises the following elements:

- AES3/EBU transmitter
- AES3/EBU receiver
- PLL for the system clock (derived from 27 MHz)
- PLL to derive the transmit clock from the VCXO's 27-MHz output, if a lock to the receive clock is needed, (Stratix GX Video Demonstration Board only)

Table 1 shows the reference design signals.

Table 1. Signals

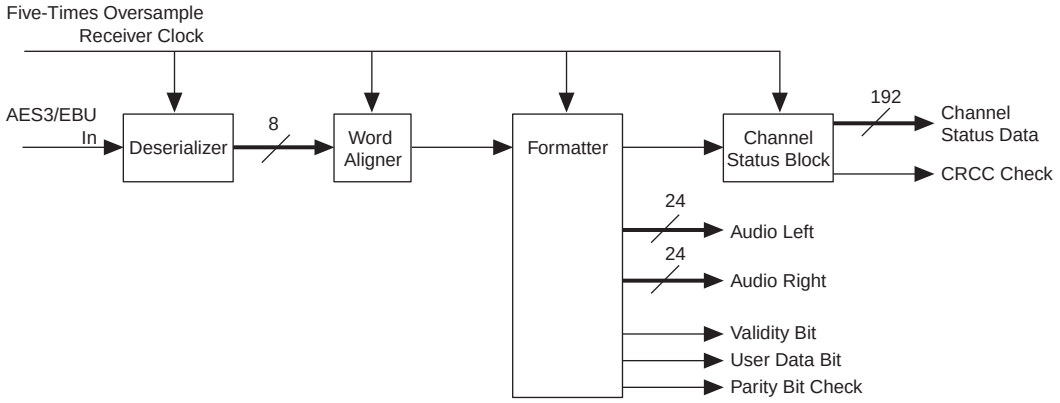
Name	Required	Direction	Description
clk_in	Yes	Input	System clock.
reset_n	Yes	Input	Asynchronous reset (active low).
aes_in	Yes	Input	AES3/EBU input.
aes_out	Yes	Output	AES3/EBU output.
aes_clk_out *(1)*	No	Output	AES3/EBU recovered clock.
mk2064_rv *(1)*	No	Output	Control VCXO divider on the Stratix GX Video Demonstration Board.
mk2064_clrn *(1)*	No	Output	Clear VCXO on the Stratix GX Video Demonstration Board.
mk2064_fv *(1)*	No	Output	Control VCXO divider on the Stratix GX Video Demonstration Board.
mk2064_sv *(1)*	No	Output	Control VCXO divider on the Stratix GX Video Demonstration Board.
mk2064_ld *(1)*	No	Output	Control VCXO on the Stratix GX Video Demonstration Board.
ics660_sel *(1)*	no	Output	Bypass divider on the Stratix GX Video Demonstration Board.
ddr_clk_fb_in *(1)*	No	Input	To access enhanced PLL (re-using DDR PLL on the Stratix GX Video Demonstration Board).
ddr_clk_fb_out *(1)*	No	Output	To access enhanced PLL (re-using DDR PLL on the Stratix GX Video Demonstration Board).
vcxo_out *(1)*	No	Output	To access enhanced PLL (re-using DDR PLL on the Stratix GX Video Demonstration Board).
pll_locked *(1)*	Yes	Output	PLL lock status.
ld_led	Yes	Output	Check status.

Note to Table 1:
(1) Stratix GX Video Demonstration Board demonstration only..

Receiver

Figure 2 shows the receiver.

Figure 2. AES3/EBU Receiver



The receiver comprises the following elements:

- Deserializer
- Word aligner
- Formatter (to re-construct frames)
- Parity check
- CRC check

Table 2 shows the receiver signals.

Table 2. Receiver Signals (Part 1 of 2)

Name	Direction	Description
clk_rx	Input	Five-times oversample receiver clock.
reset_n	Input	Receiver reset (active low).
aes_in	Input	AES3/EBU input.
rxclk_out	Output	Recovered clock output.
channel_left[27:0]	Output	Recovered audio and control signals (left channel).
channel_right[27:0]	Output	Recovered audio and control signals (left channel).
wrusedw[3:0]	Input	FIFO buffer level.
oe	Output	Enables the transmit module when ready.
reset_fifo	Output	Resets FIFO buffer when re-synchronization is in progress.

Table 2. Receiver Signals (Part 2 of 2)

Name	Direction	Description
wreq_sig_a	Output	Write request signal (left channel) for the FIFO buffer.
wreq_sig_b	Output	Write request signal (right channel) for the FIFO buffer.

Deserializer

The serial data stream from the LVDS input buffer is oversampled using a local asynchronous clock and converted into a parallel 8-bit word.

The rxclk_out signal is generated to determine when the 8-bit word is available. Because of the nature of the digital oversampling algorithm, this clock may exhibit a large amount of jitter. In applications that need a low jitter recovered clock, the rxclk_out signal may be fed through an external VCXO to remove the jitter caused by resample block.

In the Stratix GX video demonstration board demonstration, the rxclk_out signal is sent through a VCXO to clean the jitter caused by the oversampling and to allow the transmitter to be locked to the receiver. When the AES3/EBU receiver or transmitter are used independently the system does not require a VCXO.

You can use the output of the VCXO to lock all the AES3/EBU outputs to this AES3/EBU input.

Jitter is usually expressed in unit interval (UI), and in the reference design the UI is calculated using the following equation:

1UI = 1/(48,000 Hz × 2 × 32 bit frame × 2 bit per sample) = 163 ns

The AES3/EBU receiver has been tested against the AES3/EBU standard receiver jitter tolerance mask. The receiver reliably captures data at input jitter levels slightly greater than the maximum specification (see Figure 3).

Figure 3. Receiver Jitter Tolerance

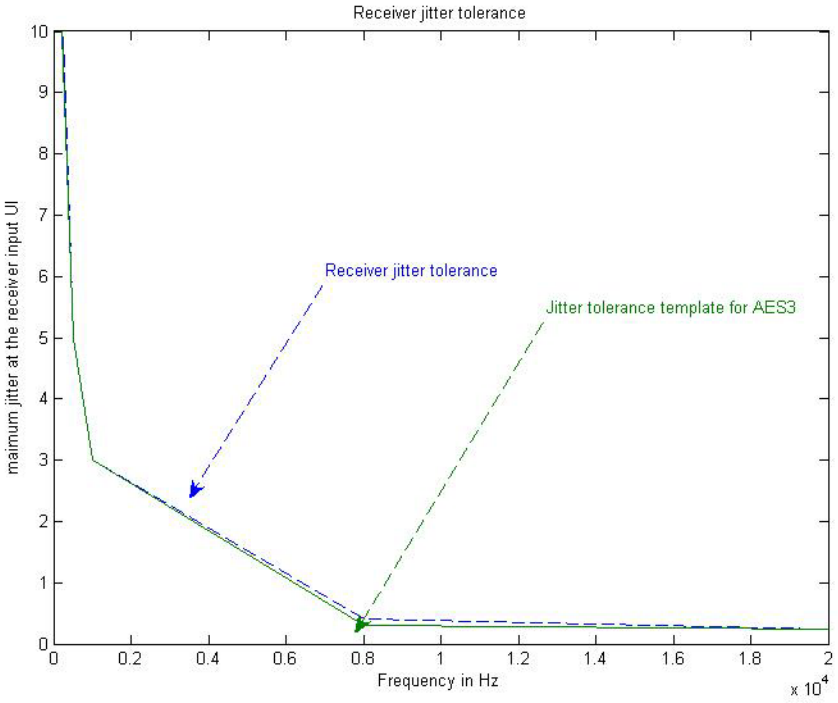
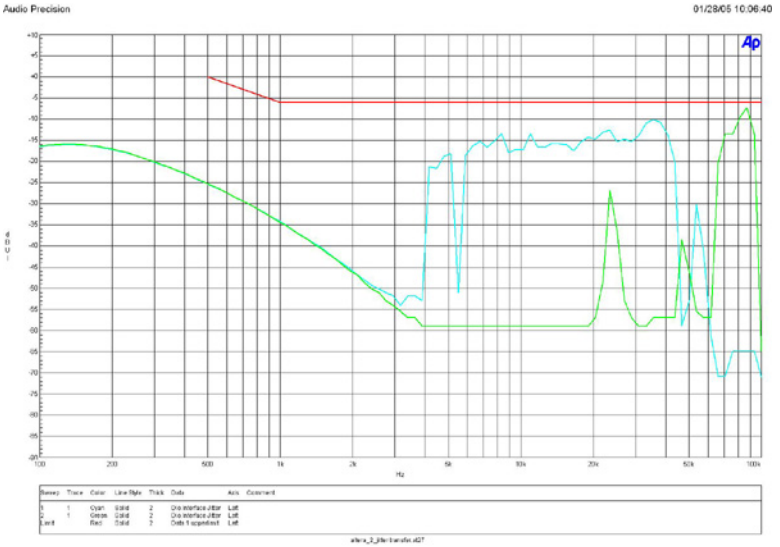


Figure 4 shows the jitter transfer of the complete system (receiver and transmitter) with a VCXO to smooth the recovered receive clock.

Figure 4. Jitter—With the VCXO



The red line shows the jitter transfer mask, and the other two responses are the jitter transfer of the entire system with two different oversampling rates.

The blue response represents the jitter transfer using the five-times oversampling scheme; the green response shows the same jitter transfer but running a 15-times oversampling scheme.

These two cases both pass the jitter transfer mask, and also show the influence of the oversampling frequency on clocking the transmitter.

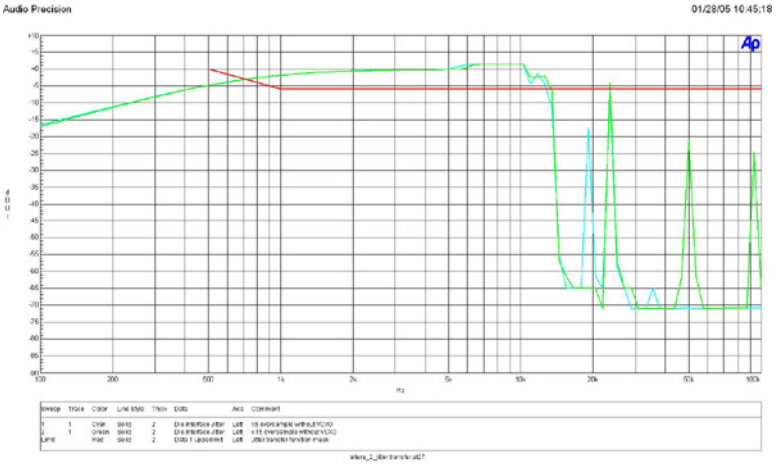
The five times oversampling scheme can be more advantageous because the clocking frequency is lower, but this example shows that higher oversample rates can provide alternative jitter characteristics across the frequency spectrum..

To change the oversampling frequency, you need to change the `SAMPLE_INTERVAL` in the file **aes_rxsample.v**, and change the PLL MegaWizard® Plug-In set -up (**aes_pll.v** for the Sratix GX Video Demonstration Board and **aes_demo_cvdb.v** for the Cyclone Video Demonstration Board)

The jitter transfer function depends on the final application's specific VCXO device.

Figure 5 shows the jitter transfer of the complete system (receiver and transmitter) without a VCXO.

Figure 5. Jitter—Without the VCXO



The red line shows the jitter transfer mask as specified in the standard. The other two responses being the jitter transfer of the entire system in two slightly different configurations.

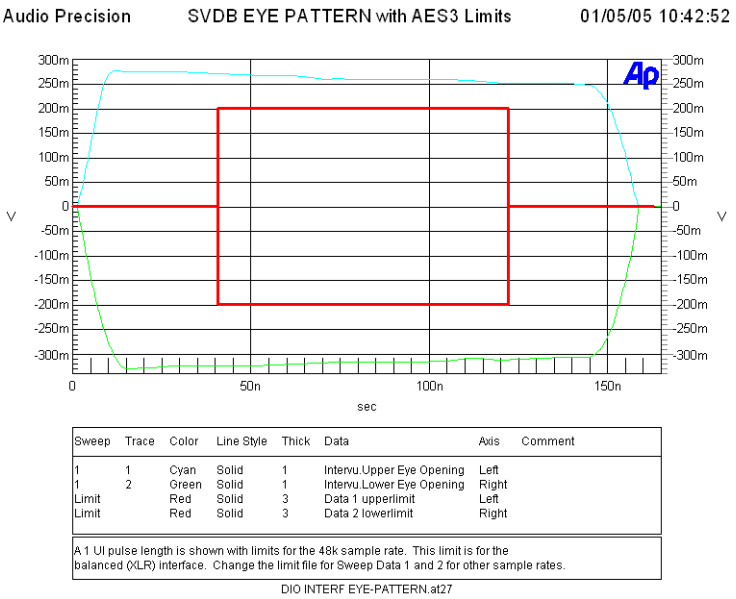
The blue response represents the jitter transfer using the five times over-sampling scheme and the green response shows the same jitter transfer when using a 15-times oversampling scheme. The difference in the two responses illustrates the influence of the oversampling function on the jitter transfer when different oversampling frequencies are used.

In this example, the jitter transfer does not pass the AES3/EBU jitter transfer mask, because the system does not use any jitter filtering mechanism such as a VCXO. This configuration shows the receiver jitter tolerance is met and the audio samples can be received reliably. Only when the system has to retransmit using a recovered receive clock is a jitter attenuation mechanism needed.

For example, for four AES3/EBU inputs, one input can use a VCXO to cancel out most of the jitter for a clean receive clock. The other inputs can use this clean receive clock, as a reference (audio clock) acting like a DARS input for the system.

Figure 6 show the eye diagram with the VCXO; Figure 7 shows the eye diagram without the VCXO.

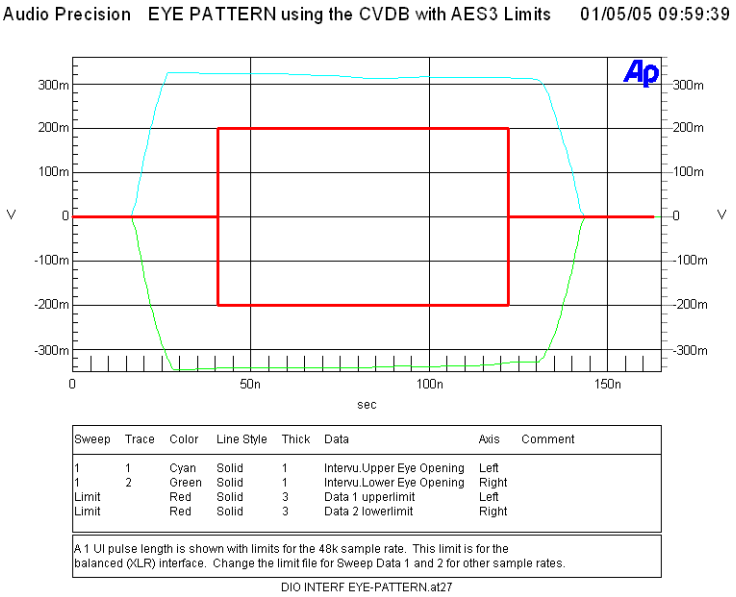
Figure 6. Eye Pattern—With the VCXO *Note (1)*



Note to Figure 6:

(1) The red line shows the AES3 limits; the blue and green lines show the eye pattern.

Figure 7. Eye Pattern—Without the VCXO *Note (1)*



Note to Figure 7:

(1) The red line shows the AES3 limits; the blue and green lines show the eye pattern.

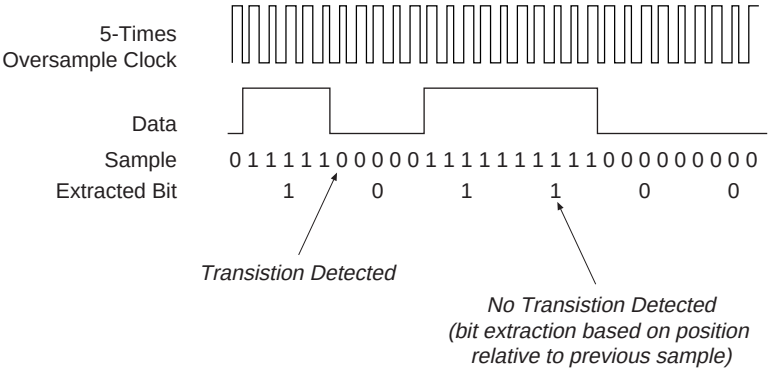
Receive data is oversampled using an internal PLL clock that is set to approximately 5 times the AES3/EBU data rate. For an audio sample rate of 48 kHz, the sample rate is:

5 ×48,000 Hz × 32 bits per channel × 2 channels × 2 (bi-phase coding) = 30.72 MHz

A 5-times oversampling scheme implements data recovery and bit synchronization, which corresponds to a sampling rate of 30.72 MHz. The deserializer provides a fixed frequency sampling of the serial data. Approximately 5 samples are taken for each bit. These samples are accumulated by the deserializer and passed to the oversampling interface in a parallel format. Logic extracts the data from the sets of samples generated by the deserializer. Firstly, the transition points within the received word are determined. These transition points determine the best sample to extract for each data bit. The logic continuously realigns to the transition points in the incoming data, and can therefore adapt to a frequency mismatch between the sampling clock and the incoming data rate. The extracted samples for each data bit are accumulated into a parallel word for processing by the deserializer.

Figure 8 shows the 5-times oversampling scheme.

Figure 8. Oversampling Scheme



Word Aligner

The word aligner scans the incoming data until it finds the Z preamble that indicates the beginning of a status block.

Formatter

The formatter reconstructs the AES3 frame, re-synchronises the channel status block when the AES3 input is un-plugged, and stores the 192 bits of the channel status structure for monitoring. A parity check is also performed on the AES3 input and compared with the parity bit in the AES3 stream. The CRC check is also performed on the channel status structure and compared to the CRC received value.

Channel Status Block

The channel status block accumulates all the control bits as they are received and performs a CRC check on the 191 bits. If the value of the 8-bit CRC register is equal to zero, the CRC signal indicates that all the control bits are correct. You can access channel status bits via a 192-bit output bus

VCXO Control

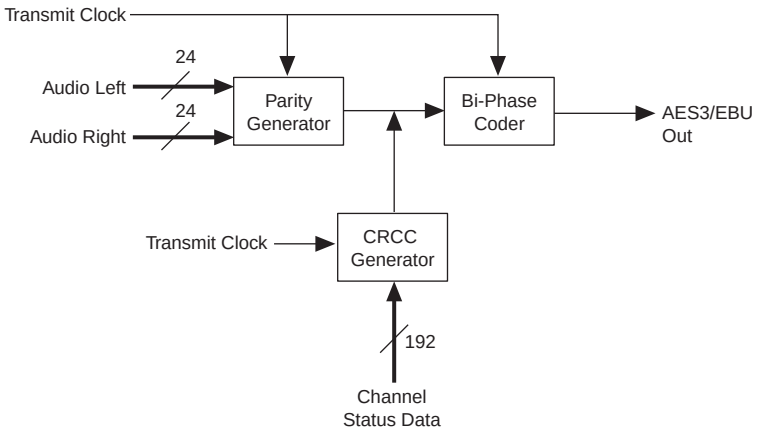
The resample block generates a `rxclk_out` signal that can be fed through an external VCXO to remove the jitter caused by resample block. The VCXO control sets up the correct divider ratio to generate a 27-MHz

output that is fed to a second PLL. Figure 1 on page 3 shows how you connect a system where AES3/EBU transmitters must be synchronized to a digital audio reference signal (DARS) input.

Transmitter

Figure 9 shows the transmitter.

Figure 9. AES/EBU Transmitter



The transmitter comprises the following elements:

- Parity generator
- Bi-phase coder
- CRC generator

Table 3 shows the transmittter signals.

Table 3. Transmitter Signals (Part 1 of 2)

Name	Direction	Description
reset_n	Input	Reset.
aes_clk	Input	Transmit clock (at bit rate).
asb_a[3:0]	Input	Auxilliary sample bit (left channel).
asb_b[3:0]	Input	Auxilliary sample bit (right channel).
asw_a[19:0]	Input	Audio sample word (left channel).
asw_b[19:0]	Input	Audio sample word (right channel).

Table 3. Transmitter Signals (Part 2 of 2)

Name	Direction	Description
vb_a	Input	Validity bit (left channel).
vb_b	Input	Validity bit (right channel).
udb_a	Input	User data bit (left channel).
udb_b	Input	User data bit (right channel).
csb_a	Input	CS bit from FIFO buffer (left channel).
csb_b	Input	CS bit from FIFO buffer (right channel).
csb_reg_a[191:0]	Input	Channel status bit (local) (left channel).
csb_reg_b[191:0]	Input	Channel status bit (local) (right channel).
local_ctrl	Input	When "1" read from FIFO buffer; when "0" read from local_ctrl.
oe	Input	Enables the tranmitter when data is ready.
reg rd_req_a	Ouput	Read request from the FIFO buffer (left channel).
reg rd_req_b	Ouput	Read request from the FIFO buffer (right channel).
reg aes_out	Ouput	AES3/EBU output.
reg Ch_B	Ouput	Channel left or right.

The transmitter has inputs for channel status. These inputs in the reference design are derived directly from the receiver channel status outputs.

Parity Generator

The parity generator calculates the party of the 24-bit audio and the control bit (V, U, C). The result is then inserted as the last bit of the 32 bit word (P bit).

Bi-Phase Coder

The data is combined with a clock signal of twice the bit rate to code a 1 or a 0 with 2 bits. A 1 is coded with following two bits 01 and a 0 is either coded as a 00 or 11.

CRC Generator

The CRC is generated from the first 184 bits of the status channel block structure. The 8-bit result from the CRC calculation is inserted to form the 192-bit status channel block structure.

Testbench

Altera supplies three testbenches with the reference design—**aes_input_tb_cvdb.v**, **aes_input_tb_svdb.v** and **aes_tx_tb_svdb.v**.

The **aes_input_tb_cvdb.v** testbench is a transmitter and receiver for the the Cyclone Video Demonstration Board; the **aes_input_tb_svdb.v** testbench is a similar design for the Stratix GX Video Demonstration Board; the **aes_tx_tb_svdb.v** testbench is for transmit only on the Stratix GX Video Demonstration Board.

The two testbenches (**aes_input_tb_cvdb.v** and **aes_input_tb_svdb.v**) differ in their use of the VCXO. The **aes_input_tb_svdb.v** testbench uses the VCXO to remove jitter from the `rxclk_out` signal before applying it to the transmitter. The **aes_input_tb_cvdb.v** testbench uses the recovered receive clock directly as the transmiter clock without using the VCXO. The transmit jitter in **aes_input_tb_cvdb.v** testbench may not be strictly compliant with the AES3/EBU specification, but depends on the jitter of the input signal.

Electrical Interfaces

You can use the AES3/EBU reference design in two different ways depending on the end application—with a balanced or unbalanced interface.

Balanced Interfaces

The balanced interface is differential, so you must select differential input and output buffers in the Quartus II software. You need an RS-422 line driver and receiver, and a transformer to provide complete electrical isolation.

Unbalanced Interfaces (AES-3ID)

The unbalanced interface uses only one connector, which saves board space. You can use a 75 Ω coaxial cable as a medium, which can run for hundreds of meters.

Both the Cyclone Video Demonstration Board and Stratix GX Video Demonstration Board are re-using the ASI, which provides similar electrical characteristics. The receiver uses a simple transformer followed by a resistor bridge to guarantee the correct bias voltage for the Altera LVDS buffer. For the transmitter, the differential buffer drives the equalizer directly, and its output is electrically isolated through a transformer.

Getting Started

This section involves the following steps:

1. System Requirements
2. Install the Design
3. Simulate using the Testbench
4. Compile the Design
5. Use the Demonstrations

System Requirements

The design requires the following hardware and software:

- Stratix GX or Cyclone Video Demonstration Board
- Digital audio source and sink, e.g., Prism Sound dScope series III, or a DSA-1, or Audio Precision 2700 series.
- PC running the Windows 98/2000/XP software
- Quartus II version 4.2 or higher
- ModelSim-Altera version 5.8c

The precompiled libraries for ModelSim-Altera simulator are available from the Altera website at **https://www.altera.com/support/software/download/service_packs/quartus/dnl-qii30sp2.jsp**.

Install the Design

To install the reference design, run the **.exe** and follow the installation instructions. Figure 10 shows the directory structure.

Figure 10. Directory Structure

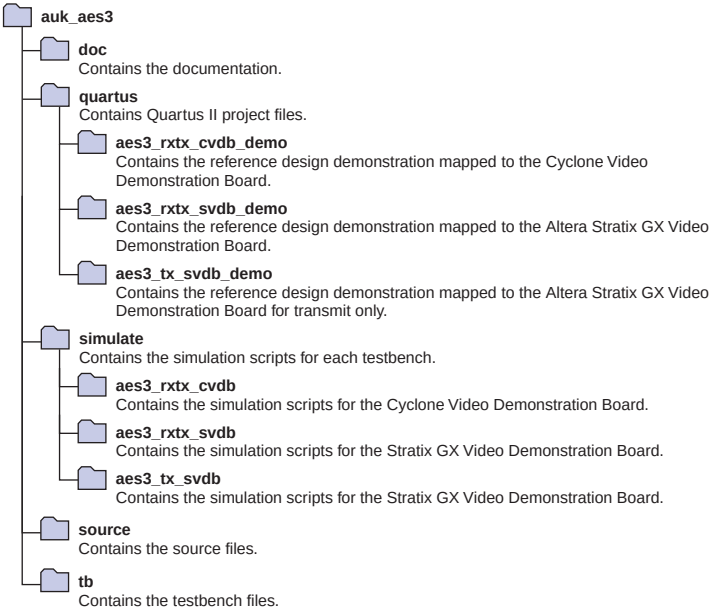


Table 4 shows the Verilog HDL modules.

Table 4. Verilog HDL Modules (Part 1 of 2)

Module	Description
aes_channel_status_block.v	Channel status block, which stores AES control signal and calculates CRC.
aes_demo_cvdb.v	AES3/EBU top-level design file for the Cyclone Video Demonstration Board.
aes_demo_svdb.v	AES3/EBU top-level design file for the Stratix GX Video Demonstration Board.
aes_formatter.v	Formatter, which reconstructs the the frames audio and control.
aes_pll.v	System PLL.
aes_receiver.v	Receiver.
aes_reset.v	Reset control that waits for the PLLs to be locked before starting up.
aes_rxsample.v	Serializer.
aes_tx_phy_fifo.v	Transmitter.

Table 4. Verilog HDL Modules (Part 2 of 2)

Module	Description
aes_vcxo_control.v	Controls the divider inputs of the MK2069 and the divider ics660.
aes_word_aligner.v	Word aligner, which searches for the preamble to synchronize the AES3/EBU input.
fifo.v	FIFO buffer left and right channels.
led.v	Flashing LED.
pll_tx.v	PLL, to clock the AES3/EBU transmiter.
ramp.v	Generates ramp-shape audio sample.

Simulate using the Testbench

The reference design includes three testbenches, **aes3_input_tb_cvdb.v**, **aes3_input_tb_svdb.v** and **aes3_tx_tb_svdb**, and a script for simulating with the ModelSim-Altera simulator. To use any of the testbenches, follow these steps:

For more information on the testbenches, see "Testbench" on page 15.

1. In the ModelSim simulator, choose **Change Directory** (File menu) and choose **auk_aes3\simulate**.
2. Choose **Execute Macro** (Tools menu)**,** choose **aes.do**, and click **OK**.

The waveform viewer displays a selection of signals. The simulation runs automatically and provides a pass or fail indication on completion.

Compile the Design

Quartus II project files are provided for the reference design mapped to the Cyclone video demonstration board and the Stratix GX video demonstration board. The **.qsf** files define the pinout and other compilation directives for the designs. You must compile the designs to produce the device images required for the demonstrations.

To compile any of the demonstration designs, open the relevant project in the Quartus II software and choose **Start Compilation** (Tools menu).

Use the Demonstrations

Figures 10 and 11 shows the demonstration on the Stratix GX or Cyclone Video Demonstration Board.

Figure 11. Demonstration on the Video Demonstration Boards

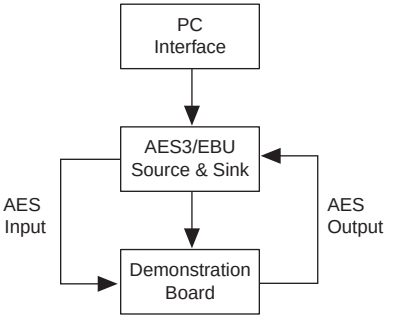
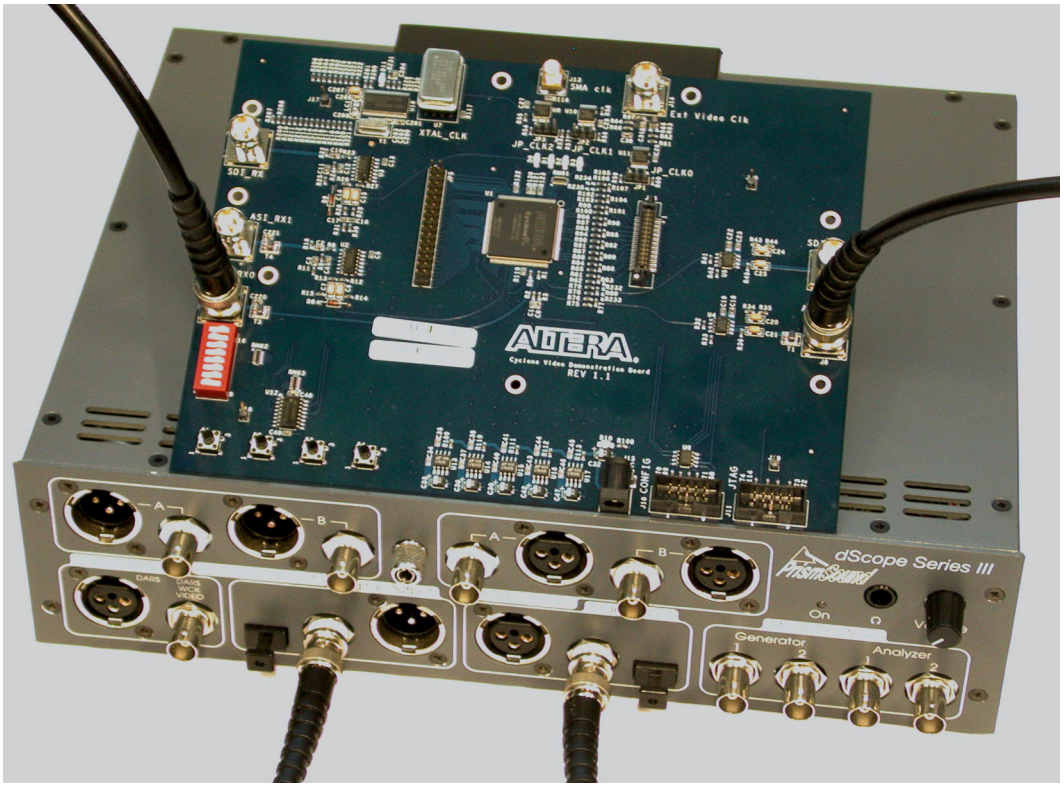


Figure 12. Demonstration Set Up



To set up the demonstration, follow these steps:

1. Connect an audio source and sink, e.g., a Prism Sound dScope series III or a DSA-1, and a USB-Blaster download cable to a Stratix GX or Cyclone Video Demonstration Board (see Table 5).

Table 5. Connections

Connection	Demonstration Board	
	Stratix GX	Cyclone
USB-Blaster™ download cable	JF1	J19
AES3/EBU receive	J33	J1
AES3/EBU transmit	J34	J8

2. Use the Quartus II Programmer to download the demonstration to the demonstration board.

When the demonstration is running correctly the Cyclone Video Demonstration Board LEDs have the following status:

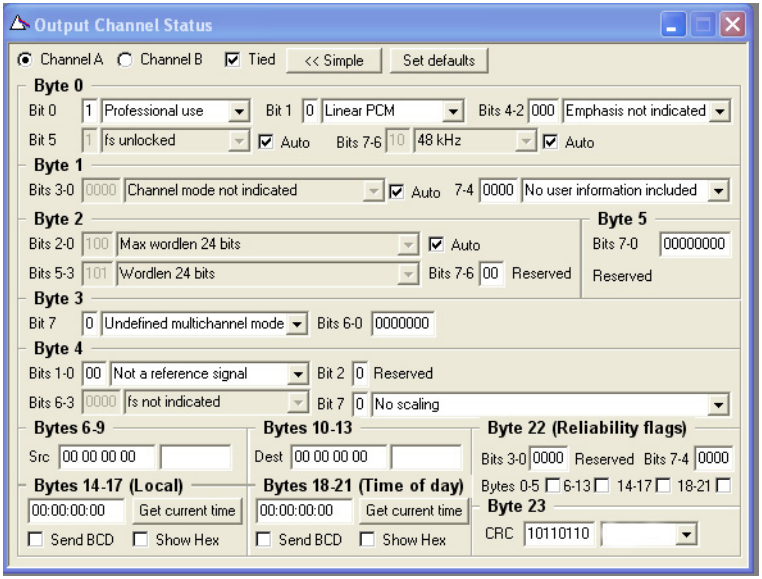
- D0 flashes
- D1 and D2 illuminate
- D2 is off

When the demonstration is running correctly the Stratix GX Video Demonstration Board LEDs have the following status:

- D13 flashes
- D6, D9, D10, D11, and D12 illuminate
- D7 and D8 are off

Figure 13 shows the AES3/EBU output on a Prism Media Products Ltd scope (see Figure 13).

Figure 13. AES3/EBU Output



Resource Usage

Table 6 shows the resource usage.

Table 6. Resource Usage

Module	LEs
Receiver	229
Transmitter	185
Entire reference design on Stratix GX or Cyclone Video Demonstration Board	910

References

The document uses the following references:

- *The AES3-2003 AES recommended practice for digital audio engineering —Serial transmission format for two-channel linearly represented digital audio data (Revision of AES3-1992)*, see www.aes.org/standards/b_pub/aes3-2003.pdf
- *The AES information document for digital audio engineering—Guidelines for the use of the AES3 interface*, see **www.aes.org/standards/b_pub/aes-2id-1996.pdf**
- *The AES recommended practice for digital audio engineering—Synchronization of digital audio equipment in studio operations*, see **www.aes.org/standards/b_pub/aes11-2003.pdf**.

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