Phase-Locked Loop (PLL) Loss of Lock Checklist

Please use the checklist below to assist you to find out the possible causes of PLL loss of lock. These are the common causes for PLL loss of lock. If your answer is “Yes” to the question, please refer to following table for further information and recommended action.

No.	*Checking Item*	*Yes*	*No*
1	Is the jitter and duty cycle on PLL input clock out of the specification?		
2	Is there excessive simultaneous switching noise (SSN) on the clock input of PLL?		
3	Is the VCCA and VCCD power rail out of the specification?		
4	Is your input clock running with any glitches or sudden phase change?		
5	Did you assert the `areset` or `pllena` ports?		
6	Did you reconfigure the PLL?		
7	Is the temperature of Stratix or Cyclone PLL below -20 ^{0}C?		
8	Is the input clock frequency outside the lock range?		
9	Did you disable the phase frequency detector (PFD)?		
10	Did you enable the spread spectrum in your design?		
11	Did a clock switchover occur?		
12	Is the jitter on PLL output clock out of the specification?		
13	Are the RREF pins connected correctly with its own individual resistor to GND?		
14	Are VREF and termination of the I/O standards set correctly?		

15	Did the `permit_cal` signal being disabled in Stratix 10 IOPLL during power-up calibration?		
16	Did you reconfigure Stratix 10 IOPLL in Advanced Mode Reconfiguration?		

If the explanations of these causes do not solve your issue, submit a service request to Intel's technical online support system. Please provide the following information when you submit a service request:

a) Issue description
b) Quartus II software version and patch (if any)
c) Tested unit and the failure rate
d) A simplified design that can exhibit the failure
e) SignalTap II result or scope shots that shows all the control signal (e.g. `areset`, `locked` and etc.), input clock and output clock.

No	Cause/ Explanation	Action
1	***Jitter and duty cycle on PLL input clock is out of specification*** Excess jitter on the PLL input clock can cause the PLL to lose lock.	• Since PLL acts as a low-pass filter, you can use a low bandwidth setting to filter out high frequency jitter from the input clock.
2	***Simultaneous switching noise(SSN)*** Switching noise on the I/Os could affect both the jitter on the input and feedback clock. Switching noise on the inputs is a form of deterministic jitter that is subject to the input jitter specification as shown in the device family data sheet.	• Ensure stand-alone PLL works fine when SSN is not present or minimized: - Reduce drive strength. - Reduce the number of toggling I/Os. • Ensure drive strength is set correctly in the Quartus II assignment editor.
3	***Power supply noise*** Since VCCA powers the voltage controlled oscillator (VCO), noise on this supply could cause the VCO output frequency to fluctuate and cause jitter.	• Use oscilloscope to monitor the VCC power rail with lock signal as triggering signal • A low bandwidth causes the loop to respond slower to the noise being injected by the VCO. In turn, it cannot adjust for this noise and counteract it. A high bandwidth allows the loop to respond quickly to the noise and compensate for it.

4	***Input clock stops/glitches or sudden phase change*** If the reference clock stops, the PLL no longer has a signal to track. If there is a sudden drastic phase change of the input clock, the PLL may not be able to react quickly enough to maintain lock.	• Reset the PLL to ensure the phase relationship between the input and output clocks are maintained. • Recommend the input clock is stable before FPGA enters user mode.
5	***PLL is reset*** Asserting the `areset` or `pllena` port of the PLL causes it to lose lock	• Ensure the `areset` and `pllena` ports are deactivated.
6	***PLL is reconfigured*** Once the `scanwrite` port is asserted, the PLL scan chain is uploaded to actual counters. The PLL loses lock during or after PLL reconfigure the M counter, N counter, or phase shift settings. Changes in post-scale counters do not affect the PLL lock signal.	• The PLL is expected to lose lock if any changes are made to the M counter, N counter or phase shift settings. Otherwise, check the `scandata` bit stream to make sure you did not inadvertently change these settings.
7	***Stratix@ or Cyclone@ at Low Temperature(<-20 ^{0}C)*** For details, see Table 1 in the Stratix FPGA Errata Sheet or Table 4-52 in the DC & Switching Characteristics chapter of the Cyclone Device Handbook.	• This is a known issue.
8	***Input clock frequency goes outside the lock range as reported in the Quartus II PLL summary report file***	• Make sure the input clock frequency stay within the minimum and maximum lock frequency as reported in the Quartus II PLL summary report file.
9	**Phase frequency detector(PFD) is disabled** When the PFD is disabled, the loop no longer tracks changes to the input clock. The PLL output continues to toggle at the last frequency but drifts to a lower frequency over time, causing the output clock phase (and frequency) to drift outside the lock window of the PLL.	• Make sure `pfdena` signal is enabled.
10	***Spread spectrum is enabled in the design*** When the spread spectrum is enabled based on the modulation frequency, the PLL switches between two sets of M, N counter settings, i.e. M1, N1 and M2, N2. The PLL could lose lock due to the spreading of the VCO clock.	• Verify that the output clock is being “spread” properly and that this is just lock circuit marginality.
11	***A clock switchover condition occurs*** PLL is expected to lose lock during a clock switchover condition.	• Reset the PLL to ensure the phase relationship between input and output clocks are maintained.
12	***Jitter on PLL output clock out of specification*** Switching noise due to core or IO toggling is coupling onto the PLL circuitry.	• Move switching IOs and LE's away from the vicinity of the PLL.

13	***Reference resistor (RREF) pins are not connected correctly with its own resistor to GND*** Analog circuitry of PLL might not operate as per expected if the RREF pins are not connected correctly, which will cause PLL unable to lock.	• For FPGA V series and newer FPGA devices, ensure RREF pins are connected to reference resistance that documented in the pin connection guideline of the respective device family.
14	***Voltage reference (VREF) and termination of the I/O standards are not set correctly***	• Ensure the appropriate VREF and termination are used for the different I/O standard.
15	***Unstable reference clock before device configuration of I/OPLL in Stratix 10*** The `permit_cal` signal from I/O PLL IP core is use to gate power up calibration if the reference clock is not stable before device configuration. Unstable reference clock to I/O PLL upon power up calibration may result I/O PLL unable to gain lock.	• In PLL standalone mode, set `permit_cal` = 0 upon power up until the reference clock is stable and operating at the correct frequency. Then, set `permit_cal` = 1 to initiate the power-up calibration. Ensure that the `permit_cal` signal remains high once asserted. • In PLL cascading mode, the `permit_cal` input of the downstream I/O PLL must be connected to the locked output of the upstream I/O PLL.
16	***Advanced Mode Reconfiguration limitations in Stratix 10*** If PLL is configure with wrong PLL setting, wrong bit, or overwrite the whole byte for settings that made up just part of one byte, PLL may lose lock and can cause reliability problems. Besides, recalibration need to be trigger manually after reconfiguration	• Ensure that the configuration setting is a legal value so that the I/O PLL has a legal configuration. • Ensure to trigger recalibration of the PLL after reconfiguration in Advance Mode Reconfiguration.

Revision History

Revision	Date	Description
1.0	12/04/2008	-Initial Release
1.1	07/16/2012	-Included checking item 12. -Updated the requested information before submit service request
1.2	11/18/2015	-Included checking item 13.
1.3	12/28/2017	-Included checking item 14.
1.4	04/25/2019	-Included checking item 15 and 16.