White Paper

FPGA

Top 10 Reasons to Replace Your Microcontroller with a MAX® 10 FPGA

Using MAX® 10 FPGAs and the Nios® V processor can help differentiate products, meet time-to-market schedules, and mitigate processor obsolescence risks.

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Introduction

Microprocessors or microcontrollers (MCUs) are one of the most universal components in digital electronic systems. This need remains strong as Internet of Things (IoT) solutions become increasingly integrated into various aspects of life. Whether designing for the IoT revolution or bleeding edge products that require novel solutions, commercial off-the-shelf (COTS) or system on a module (SoM) board cannot provide the optimal combination of performance, peripherals, form factor, scalability, or life cycle persistence to deliver competitive differentiation and time-to-market needs. When choosing a COTS or SoM processor, designers must compromise on MCUs with fixed functionality by overpaying for features they don't need or over-designing their system to add features the COTS/SoM lacks. With their integrated, fully customizable soft processing capability, FPGA-based solutions enable true flexibility and scalability—addressing custom needs with programmable hardware and software in a single chip.

The Nios® V processor is an FPGA-optimized 32-bit RISC-V Harvard architecture soft-core processor. As the FPGA is programmable, the Nios V processors offer a range of options, allowing designers to select the optimal version for their needs. Moreover, various processor peripheral configurations are available to align with specific requirements, enabling the FPGA to meet the exact needs of any application. In addition, the processor peripheral set is easily configured to meet any application-specific requirement. MAX® 10 FPGA-based solutions, based on the Nios V processors, overcome the limitations of COTS by enabling a unique single-chip embedded system that can be customized for product differentiation and optimization. The innovative architecture of MAX 10 FPGAs and the flexibility of Nios V processors provide an unmatched alternative solution for today's embedded designers.

Attain Instant-On Power and Faster System Boot

Unlike traditional FPGA-based systems that require longer boot times, MAX 10 FPGA's on-die flash enables instant-on capability. System boot and management also benefit from the on-die flash. In traditional FPGA systems with embedded processor technology, whether hard or soft, the FPGA takes a delayed amount of time to power up and configure.

With MAX 10 FPGA's on-die flash, the FPGA powers up instantly (in a few milliseconds) as the first component in the system, allowing the custom FPGA logic to not only completely manage system bring-up but also allowing the Nios V system

to be available at system power-on for software diagnostics or prognostics. This single-chip integration and hardware upgrade capability give embedded designers reduced cost of ownership by eliminating product design defects, product returns, and providing a competitive advantage with customized hardware.

Optimize Performance for AI and Edge Computing

The rapid advancement of artificial intelligence (AI) is revolutionizing industries and driving new capabilities in edge computing, industrial automation, healthcare, and smart infrastructure. AI is expanding beyond data centers and entering embedded and edge devices where real-time performance, low power consumption, and cost efficiency are critical. Standard MCUs often lack the necessary features, speed, scalability, and energy efficiency required by AI workloads.

MAX 10 FPGAs address these challenges with robust DSP capabilities, including up to 144 embedded multiplier blocks, enabling high-performance AI and edge computing solutions. Each block supports 18 × 18-bit or dual 9 × 9-bit multipliers, delivering the computational power needed for demanding AI tasks like real-time signal processing, video analytics, and sensor fusion. With support for DSP IP cores—such as finite impulse response (FIR) filters, fast fourier transform (FFTs), and numerically controlled oscillator (NCOs)—MAX 10 devices provide the flexibility to implement complex AI algorithms efficiently. Additionally, integration with tools like DSP Builder for Altera FPGAs and MATLAB/Simulink simplifies development, ensuring faster time-to-market for AI-driven edge applications. By combining low power consumption, high performance, and scalability, MAX 10 FPGAs are ideal for meeting the evolving demands of AI and edge computing.

Recently, one of Altera's Solution Acceleration Partners, One Ware, demonstrated a combined image processing and AI inferencing solution targeting a MAX 10 FPGA. One Ware demonstrated the capabilities of the Altera MAX 10 FPGA in enabling real-time, low-latency processing for industrial automation and edge computing applications.

The demonstration highlighted how the MAX 10 FPGA's instant-on capability, low power consumption, and integrated flash memory make it ideal for time sensitive industrial systems.

One Ware showcased the FPGA's ability to perform high-speed data acquisition and real-time signal processing, which are critical for applications like predictive maintenance, machine vision, and robotics. The MAX 10 FPGA's compact design and cost efficiency were also emphasized, making it a practical solution for deploying advanced automation and AI at the edge. Overall, the demonstration illustrated how the MAX 10 FPGA empowers industries to achieve faster decision-making, improved system reliability, and scalable edge computing solutions. Register for free access to the technical webinar

Alternatively, MAX 10 FPGA, equipped with the Nios V soft processor, brings AI capability to compact, power-efficient designs by enabling real-time inferencing, edge AI acceleration, and tiny machine learning (tinyML) deployments. By integrating AI tasks into MAX 10 FPGAs, developers can benefit from custom hardware acceleration, deterministic performance, and low-latency execution to process AI models efficiently at the edge without needing a separate AI component. MAX 10 FPGAs provide the intelligence, flexibility, and scalability needed to bring AI to emerging embedded systems.

Ensure Hitless Updates for Continuous Operation

MAX 10 devices also offer a hitless update feature, which provides the capability and flexibility to control the state of the I/O pins during an internal flash image update and subsequent reconfiguration of the device. All I/O pins can remain stable without any disruption throughout the hitless update process. This feature also allows the MAX 10 FPGA to behave as a system controller when monitoring and controlling critical signals without interruption. By leveraging dual configuration images—Active and Update—the FPGA can seamlessly switch between configurations while maintaining continuous operation, ensuring no downtime during updates.

This is particularly critical for mission-critical systems such as board management, telecommunications, industrial automation, and automotive applications. MAX 10 devices support two types of hitless updates. All MAX 10 devices allow hitless updates via external JTAG, ensuring broad compatibility, while the 10M40DD and 10M50DD devices support hitless updates through internal JTAG or I2C/SPI interfaces, enabling greater flexibility for system integration. These options provide designers with the ability to update firmware reliably while maintaining system stability, making MAX 10 FPGAs ideal for applications that require uninterrupted operation.

Manage Power Efficiently with Single and Dual Supply Options

MAX 10 single-supply devices only need either a 3.0- or 3.3-V external power supply. The external power supply serves as an input to the MAX 10 device VCC_ONE and VCCA power pins. This external power supply is then regulated by an internal voltage regulator in the MAX 10 single-supply device to 1.2 V, as reflected in Figure 1. The 1.2-V voltage level is required by core logic operation. For applications demanding higher performance, dual-supply devices utilize 1.2 V for the core and 2.5 V for I/O, peripherals, PLLs, and ADCs. This configuration optimizes power delivery, enhancing performance while reducing power consumption. By leveraging high-efficiency switching power supplies, designers can achieve significant energy savings compared to single-supply devices with internal linear regulators.

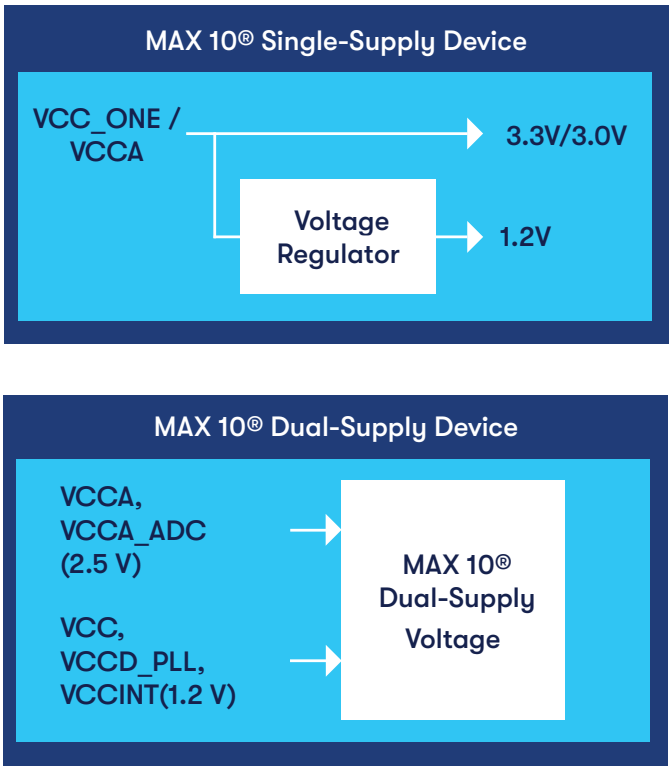

Figure 1. MAX® 10 Power Supply Device Options

Lower Total Cost of Ownership (TCO) and Upgradable Solutions

MAX 10 FPGAs integrate embedded flash directly onto the FPGA die, enabling a true single-chip embedded system with both hardware and software customization. Imagine a CPU with customizable hardware features that can change in real-time, in the field, to match the Quality of Service (QoS) or feature packages licensed by the end customer. Another benefit of this feature is the ability to upgrade a system's microcontroller hardware for changes due to emerging standards, functionality missing in the initial release due to time-to-market pressures, or product upgrades purchased after the initial installation. These scenarios are not physically possible with typical microprocessors but are possible when utilizing Nios V processors with MAX 10 FPGA embedded flash and remote update capability.

The MAX 10 embedded flash contains two FPGA configuration image partitions, as shown in Figure 2; one of these can be used to guarantee failsafe remote updates to the FPGA hardware image. If the remote update or dual-configuration capability is not required, the general-purpose user flash memory (UFM) can be expanded (up to 700 Kilobytes) for additional software code storage space.

The power management controller scheme in MAX 10 FPGAs enables dynamic power reduction by allowing unused design sections to enter sleep mode during operation. This feature, combined with a rapid wake-up time of less than 1 ms, ensures efficient power usage without compromising responsiveness. Key features like I/O power down, global clock gating, and sleep mode are particularly beneficial for applications such as DSLR cameras, where power savings during idle states are critical.

MAX 10 FPGAs also include a soft power management controller as a reference design, featuring a simple finite state machine (FSM) to manage low-power states. Designers can customize this controller to meet specific application requirements, leveraging features like I/O power down and clock gating. All MAX 10 devices support clock gating, while specific models (10M16, 10M25, 10M40, and 10M50) also offer I/O power-down capabilities. These hardware features, combined with the soft power management controller, enable efficient low-power state management during sleep mode. The internal oscillator clocks the power management controller operation. The internal oscillator is routed from flash to the core. The internal oscillator enables the power management controller to detect the wake-up event and the sleep mode event.

With single-supply simplicity, dual-supply flexibility, and advanced power management features, MAX 10 FPGAs empower designers to optimize power efficiency, reduce system complexity, and accelerate time-to-market. These capabilities make MAX 10 FPGAs a reliable and versatile solution for applications ranging from industrial automation to portable devices, ensuring both high performance and energy efficiency.

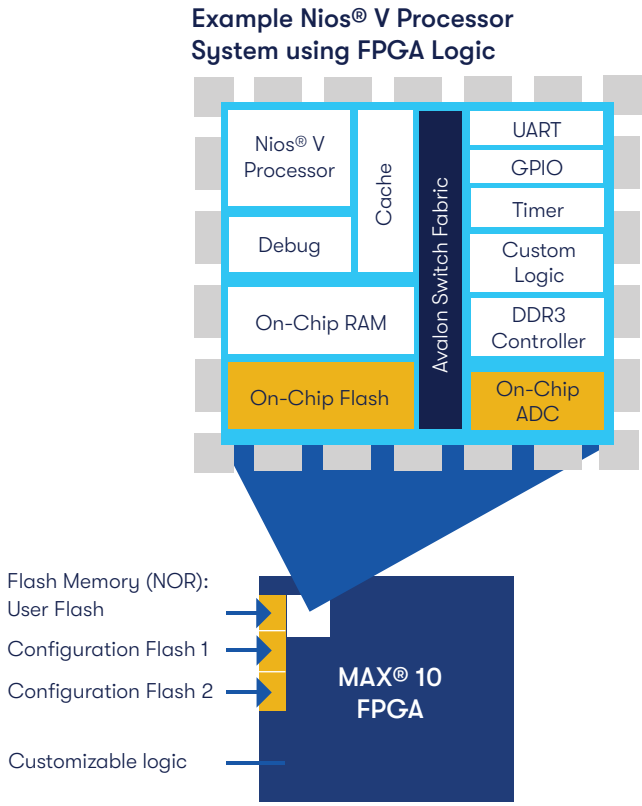

Figure 2. Single-Chip Nios® V Processor Capability with Dual-Configuration Partitions

MAX 10 FPGA integrates up to two 12-bit Successive Approximation Register (SAR) analog-to-digital converter (ADC) blocks with up to 17 input channels, which can be used to measure environmental conditions, manage power-up and power-down sequencing, control motor torque, and more. The 12-bit SAR ADCs include programmable digital interfaces, sample sequence control, hardware averaging, and interrupt thresholds for voltages and device temperature. By using these ADCs in Nios V processor designs, MCUs or external ADCs can be removed from the system BoM to reduce system cost and complexity.

As shown in Figure 3, combined with the MAX 10 FPGA's on-die flash, ADC, PLLs, and Nios V processors reduce board space by up to 50% compared to traditional FPGA solutions with discrete power supplies. The single-supply option, enabled by an on-die regulator, further minimizes board space and complexity by eliminating the need for multiple power rails. This reduction in chip count and PCB size lowers system costs and increases reliability.

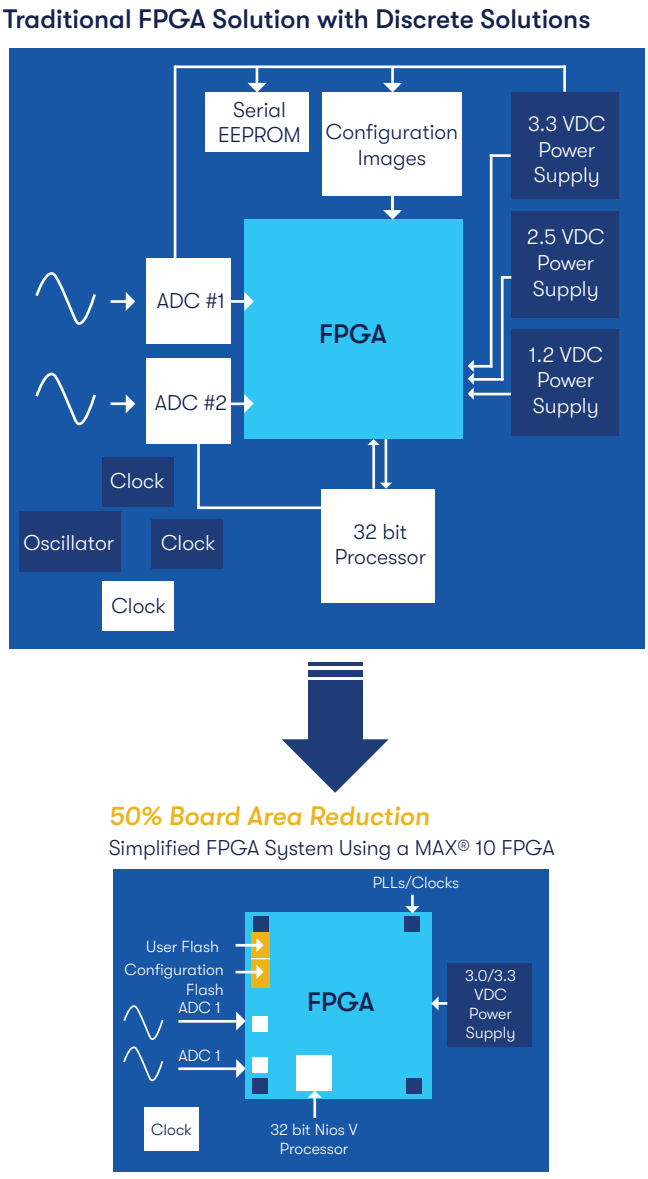

Figure 3. TCO Savings, Board Space, and Reliability: Traditional FPGA vs. MAX® 10 FPGA

MAX 10 FPGAs simplify power management by requiring only a 3.0V or 3.3V external power source. This connects to the VCC_ONE and VCCA power pins, with an on-die regulator converting it to 1.2V for core logic. By using a single power source for both core and I/O voltage (if they match), board complexity and footprint are minimized, and overall system costs are reduced. This single-supply capability enhances reliability by reducing external components and potential failure points, making it ideal for space-constrained applications like portable and embedded systems.

With packaging as small as 3x3 mm², MAX 10 FPGA's single-chip solution offers an exceptionally small configurable FPGA footprint. The variable pitch BGA (VPBGA) packaging maximizes I/O density and optimizes space with up to 485 I/Os in a compact 19x19 mm² package. Its small form factor, LVDS Tunneling Protocol Interface (LTPI) support, and flexible supply options help reduce the bill of materials (BOM) space and costs. The VPBGA package also simplifies routing and lowers board costs.

These compact package sizes allow the MAX 10 FPGA to replace or augment ASICs, ASSPs, and microcontroller units (MCUs) in portable or space-constrained applications. By minimizing external components while maintaining robust FPGA functionality, MAX 10 single-supply FPGAs enable designers to create compact, cost-effective, and high-reliability embedded solutions.

Customize Peripheral Sets for Differentiation

With the perfect fit of CPUs, memory interfaces, and custom peripherals to meet the unique demands of every new design, the Nios V processors offer tremendous flexibility where designers need it. Designers may choose from different Nios V CPU flavors to optimize the processor for performance or size and can even create custom CPU configurations to meet their needs. Customized peripherals in the FPGA can be an embedded system's "secret sauce," allowing any number of general- purpose I/Os (GPIOs), Ethernet MACs, serial interfaces, multiple CPUs, and so on.

Unlike traditional MCUs, MAX® 10 FPGAs also support specialized interfaces such as CSI camera interfaces for image capture, I2S audio interfaces for high-quality audio data transmission, and many more, enabling developers to integrate advanced peripherals that MCUs may lack. Moreover, the flexibility of MAX 10 FPGAs allows for as many universal asynchronous receiver/transmitter (UARTs) as there are available pins, addressing the common resource limitations of MCUs where UARTs are often a scarce resource.

A large library of embedded peripherals is available to plug into your custom system, or designers have the option of creating their entirely unique and custom hardware peripheral blocks using Verilog HDL or VHDL. Assembling the exact set of peripherals necessary for an end system, which are not available in microcontroller-based COTS/SoM products, gives embedded designers a differentiating advantage over their competition by maximizing functional efficiency and engineering costs.

Enhance GPIO Capabilities for Flexibility and Performance

One of the advantages of replacing a MCU with a MAX 10 FPGA is its superior general-purpose I/O capabilities. Unlike MCUs, which typically support only single-ended I/O at a fixed voltage level, MAX 10 FPGAs offer significantly greater flexibility, including support for differential signaling and multiple voltage levels through independent I/O banks. This makes them ideal for applications requiring high-speed communication, noise immunity, and mixed-voltage interfacing.

MAX 10 FPGAs support differential signaling, such as low-voltage differential signaling (LVDS), which improves signal integrity and enables higher data rates compared to the single-ended I/O of MCUs. Differential signaling reduces electromagnetic interference (EMI) and allows reliable communication over longer distances, making it suitable for high-speed data acquisition, video processing, and industrial automation. On top of that, MAX 10 FPGAs feature multiple independent I/O banks, each capable of operating at different voltage levels (e.g., 1.0V, 1.2V, 1.8V, 2.5V, 3.0V, or 3.3V). This eliminates the need for external level shifters, reducing board complexity and component costs in mixed-voltage designs.

Concurrently, MAX 10 FPGAs provide programmable I/O standards, such as LVCMOS, LVTTL, and SSTL, along with adjustable drive strength and on-chip termination (OCT) to optimize signal integrity and power efficiency. These features reduce the need for external components like buffers and termination resistors, resulting in a more compact design and lower overall system costs. With support for high-speed I/O operations up to 720 Mbps, MAX 10 FPGAs outperform traditional MCUs.

Optimize Real-Time Processing

Traditionally, embedded developers have had limited options for accelerating performance near the end of a design cycle, including buying a faster processor or last-minute hand-tuning of assembly subroutines. While both options can be effective, the trade-offs they bring are too large to ignore. MAX 10 FPGAs and Nios V processors provide an entirely new toolbox of performance-enhancing features.

Using custom hardware accelerators, designers can optimize their system performance in a way not possible with standard products. The configurable nature of Nios V processor systems allows designers to create custom components in FPGA logic that can run as a co-processor unit for complex algorithms. These accelerator or co-processing units can run in parallel to the Nios V processor, executing function orders of magnitude faster than software execution. Figure 4 illustrates an example custom accelerator and its relative performance to software-only implementation.

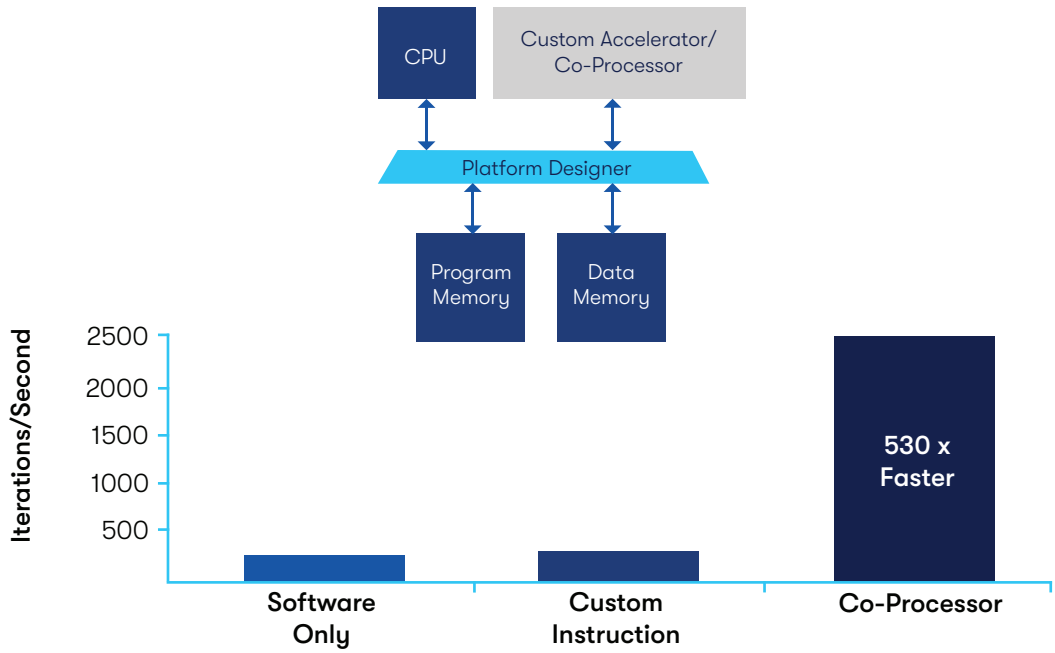

Figure 4. Custom Accelerator Performance Gains

Nios V processors provide many other options for reducing risk in embedded design, as shown in Table 1. When designing with the Nios V embedded processor, designers have access to a portfolio of mature, robust software development tools and software components available from Altera and Nios V ecosystem partners.

Features	Description
Nios V/c (Compact processor core variant)	Compact microcontroller core featuring 32 general-purpose registers, state-machine replacement, machine mode support, a reset request interface, and error correction code (ECC).
Nios V/g (High-performance processor core variant)	Optimized for performance-critical applications, the Nios V provides multiplication/division capabilities, cache management, tightly coupled memory, and single-precision floating-point extension. It features state-machine replacement, 5 pipeline stages, machine mode support, optional debug mode, a reset request interface, instruction and data cache, tightly coupled memory, custom instructions, ECC, branch prediction, and lockstep functionality.
Nios V/m (Balanced performance processor core variant)	The optimized processor features a control and status register and a debug module based on the RISC-V Debug Specification 0.13.2. It includes state-machine replacement, configurable 5 pipeline stages, machine mode support, optional debug mode, a reset request interface, and ECC.
Multiprocessor systems	Use multiple Nios V processors in your system to scale performance or to divide software applications into simpler parallel tasks. The hardware and software development tool suites include support for creating custom multicore systems. Nios V processors, combined with the larger density MAX 10 FPGAs are ideal platform for creating high-performance multiprocessor applications.
Custom instructions	Accelerate time-critical software operations by adding custom instructions to the Nios V instruction set where custom hardware can execute the operations faster than any possible software routine. Supported for Nios V/g processors only.
Hardware accelerators	If the process or algorithm that requires performance acceleration is too complex or datapath-dependent for implementation as a custom instruction, it can be implemented as a custom high-performance co-processor unit that can run in parallel to the Nios V processor.
Real-time	The Nios V processor has an option to replace the standard interrupt unit with a low-latency vectored interrupt unit to deliver faster and more deterministic interrupt response. For the ultimate real-time response and determinism, core functions can be implemented in FPGA logic bringing the performance of hardware but without losing the controllability and flexibility of software.
Fast configurable on-chip memory	Create fixed low-latency on-chip memory buffers for performance-critical applications.

Table 1. Options and Enhancements with Nios® V Processors in MAX 10 FPGAs

The Platform Designer system integration tool saves significant time and effort in the FPGA design process by enabling designers to configure intellectual property (IP) and generate interconnect logic to connect IP functions and subsystems. The easy-to-use GUI provides a simple, quick method for configuration and integration of peripherals into FPGA system designs.

The Ashling RiscFree* IDE is a free, comprehensive development package for Nios V processor software design. This package can import the hardware configuration to build a custom board support package for your unique processor configuration and system design, enabling you to start writing software immediately. The Ashling RiscFree IDE contains not just Eclipse-based development tools but also device drivers, a bare-metal Hardware Abstraction Layer (HAL) library, an evaluation version of a real-time operating system (RTOS) and example software. Thanks to its popularity, all the major RTOS vendors support the Nios V processor and active developer community on www.rocketboards.org.

Accelerate Time-to-Market with MAX 10 FPGAs

MAX 10 FPGAs accelerate time-to-market by streamlining development cycles and reducing design complexity. Their single-chip integration eliminates the need for external configuration memory, simplifying prototyping and deployment. The instant-on capability ensures systems are operational within milliseconds, reducing boot time and improving overall efficiency. Pre-built DSP IP cores, reference designs, and seamless integration with tools like Quartus Prime and Nios V processors further reduce development time, enabling designers to focus on innovation rather than infrastructure.

The ability to perform in-field hardware upgrades ensures products can adapt to evolving standards, customer needs, or regulatory requirements without costly redesigns or recalls. This flexibility allows companies to address design errors, add new features, or improve performance post-deployment, significantly reducing the risk of delays and ensuring faster iterations. Additionally, the remote update capability guarantees failsafe updates, minimizing downtime and enhancing system reliability. By combining these features, MAX 10 FPGAs empower designers to bring products to market faster, respond to changing demands more efficiently, and maintain a competitive edge in rapidly evolving industries. This accelerated development process, coupled with the ability to future-proof designs, ensures that MAX 10 FPGAs are a strategic choice for meeting tight deadlines and achieving long-term success.

Accelerate Time-to-Market with Extended Product Life Cycle and Supply Resilience

Nios V processors in MAX 10 FPGAs help developers maximize return on a product by providing life cycle benefits at every stage of a product's life. For time-to-market needs,the hardware programmability of the MAX 10 FPGA allows design errors to be fixed quickly with simple changes to the FPGA design. Being first to market can often mean shipping a less-complete product than desired. MAX 10 FPGA-based systems using a Nios V processor offer the unique advantage of being able to update hardware features to products already deployed in the field, the same way software is updated. This solves several problems:

- Extends product life, allowing the hardware to be feature-filled over time
- Reduces the risk of using hardware that is based on emerging (or changing) standards
- Simplifies hardware bug fixes and eliminates the need for product returns and rework

Altera's commitment to supply resilience and product longevity ensures that MAX 10 FPGAs manufactured will be supported for at least 15 years after initial release, extending to at least until 2040 before End of Life (EOL). This extended product longevity mitigates the risk of obsolescence and minimizes the cost of redesigning, giving customers peace of mind when choosing MAX 10 FPGAs. Customers can rely on these FPGAs for their long-term projects, knowing that they will continue to receive support and supply predictability, agility, and robustness. This strategic commitment to supply chain resilience and product longevity further enhances the value of MAX 10 FPGAs, making them a reliable choice for a wide range of applications.

To accommodate a diverse customer base, embedded processor vendors offer a range of configuration choices within a processor family, but inevitably, many of these processor variants are obsoleted earlier than the rest of the family. Designers who recognize the advantages of soft Nios V processors understand that these processors are not subject to the same market pressures as hard processors. Nios V processor designers have a perpetual license to create and deploy customized Nios V processor-based designs in MAX 10 FPGAs. A perpetual no-cost license is also available through the Self-Service Licensing Center, allowing designers to develop and deploy without extra cost.

This means that even if the underlying FPGA hardware changes, the investment in application software is preserved. One significant advantage of reusing processor architecture is the ability to re-certify products more efficiently. By leveraging a consistent and familiar architecture, companies can reduce the time and cost associated with re-certification processes. This approach not only ensures compliance with industry standards but also maintains the reliability and performance of the product across different hardware iterations. Figure 5 illustrates sales output against a product lifecycle.

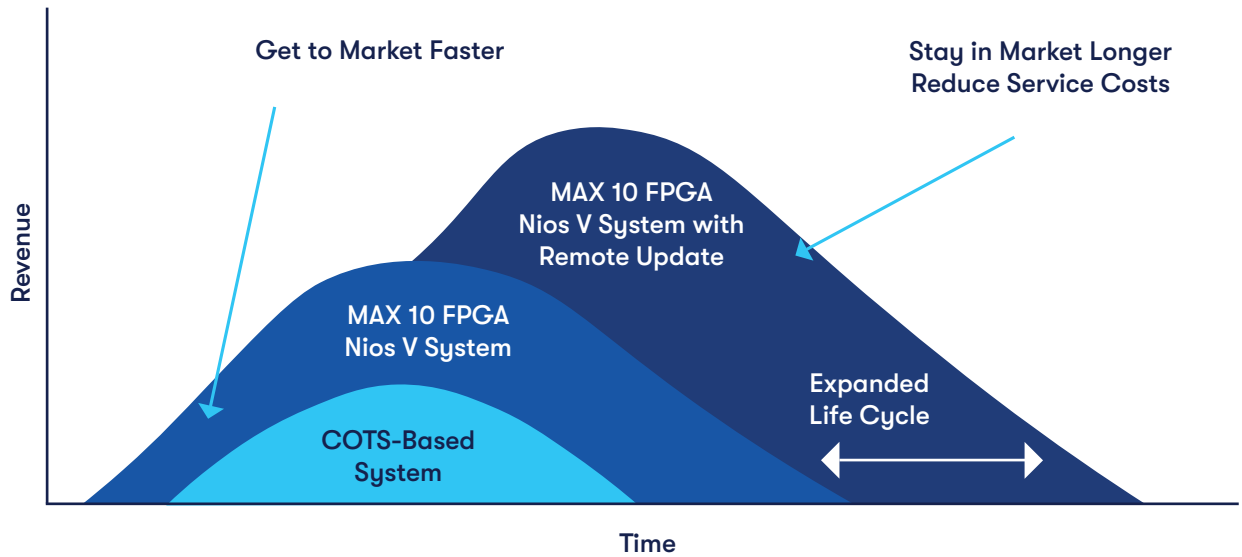

Figure 5. End Product Revenue Extension Using MAX® 10 FPGAs with Nios® V Processors

The feature upgrade and customization capability with Nios V processor systems can eliminate obsolescence risk, extend your end products time-in-market life and maximize ROI of the product. This results in a much lower TCO than traditional COTS processors with their fixed functions and obsolescence risks.

Conclusion

Embedded projects are under increasing pressure to differentiate their products, meet faster time-to-market schedules, and navigate the risks and challenges of processor component obsolescence. Nios V processors used in single-chip MAX 10 FPGAs offers a compelling alternative to traditional microcontrollers, providing unparalleled flexibility, integration, and longevity. Unlike fixed-function COTS processors, MAX 10 FPGAs enable real-time hardware reconfiguration, feature upgrades, and AI-driven optimizations—all within a compact, cost-effective, and power-efficient design.

With an industry-leading toolchain, a perpetual no-cost Nios V processor license, and a guaranteed long product lifecycle, MAX 10 FPGAs deliver a future-proof solution for embedded systems. Designers gain a competitive edge by reducing the total cost of ownership, eliminating obsolescence risks, and maximizing system performance through hardware and software customization. By choosing MAX 10 FPGAs, embedded designers are not just replacingmicrocontrollers, they are unlocking new possibilities for differentiation and long-term success.

Learn More:

For more information about Altera and MAX 10 FPGAs, visit the MAX 10 FPGA web page.

[1] Nios® V Processors

[2] Deploying tinyML* on Altera® FPGAs White Paper

[3] MAX® 10 FPGA Development Kits

[4] MAX® 10 FPGA Partner Boards

[5] SoC and Embedded Developer Design and Simulation Tools

[6] Platform Designer – Altera's System Integration Tool, part of Quartus Prime Software

[7] FPGA Technical Training (classes, eLearning, quick videos, webinars/events)

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