Innovating With a Full Spectrum of 40-nm FPGAs and ASICs with Transceivers

WP-01078-1.4 White Paper

Increasing bandwidth requirements for broadband services are driving silicon vendors to use more and more high-speed serial transceivers. Therefore, next-generation applications feature a wide range of data rates, from a few Mbps to hundreds of Gbps, and integrate multiple protocols and services in a single box. Quickly evolving standards like Ethernet plus the need for increasing data rates make high-speed transceivers a major decision criterion. Standard cell ASICs and ASSPs often do not provide the needed flexibility, and the cost and risk are prohibitive for many customers who must keep up with technology innovation. This paper describes how a full spectrum of 40-nm FPGAs and ASICs with transceivers addresses the challenges in next-generation systems by leveraging the advantages of leading-edge technology and reusing innovations of previous generations.

Introduction

The Internet, in its modern form, is only a little over a decade old, yet it has become the main driver for technology innovation and bandwidth growth. The need for higher bandwidth and data rates is driven largely by the demand to upgrade existing communications systems and the emergence of new applications. Today, web downloads— dominated by video—and point-to-point networks (file sharing) consume 80 percent of the bandwidth. New applications like streaming media (video-on-demand movies and television), voice-over-IP, and Internet gaming are still in the single digits. By that standard, the Internet is still in its infancy and should see strong and undamped growth.

Recent market announcements have covered communication equipment moving to 40- and even 100-Gigabit Ethernet (GbE) ports to achieve higher bandwidth with lower cost, lower power, and a more compact size. In addition, Moore's Law still drives the semiconductor industry to double with the number of transistors in an integrated circuit every two years. The next generation of products uses the 45-nm or 40-nm process to integrate more functions, higher operating performance, logic density, and lower power per function, but the key to meeting the increasing demand for bandwidth is more and faster high-speed serial transceivers.

This paper covers the trends for high-speed serial transceivers and the challenges that system architects and designers face. It reviews specific market requirements and shows that in order to meet these requirements, programmable logic device (PLD) vendors must provide a broad portfolio of devices with transceivers. By covering a full range of logic densities, features, and I/O capabilities, these devices allow customers to develop products that meet their diverse performance, power, and cost targets.

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High-Speed Transceiver Technology Trends

Higher bandwidth and higher data rates are achieved by increasing the data rates of high-speed serial transceivers and increasing the number of transceivers on a device. An interface with 100G bandwidth can be created using:

- 10 10.3-Gbps transceivers (CAUI protocol)
- 20 6.375-Gbps transceivers (Interlaken protocol)
- 40 3.125-Gbps transceivers (XAUI protocol)
- 100 1.25-Gbps transceivers (SGMII protocol, note that this is for illustration purposes only and is not practical)

Considering the need for two ports per device for a full egress and ingress data paths, the number of transceivers can easily exceed the physical limits of even the most modern process technologies if the data rate of the transceivers does not scale accordingly.

Many systems consist of a mixture of DSP blocks, control processor, ASSPs, ASICs, and FPGAs. System architects face the challenge of system partitioning, connecting these devices together, and matching the required performance and bandwidth of the application. In many cases, faster interfaces are not available due to slower ASSP or ASIC innovation. Another challenge is the diversity of protocols provided by these devices, which force architects to make performance trade-offs and reuse legacy interfaces. This is often done by using bridging devices—traditionally FPGAs—to connect legacy and new protocols. Solving these issues ultimately leads to lower system cost.

Data links with transceivers have become key components in systems as they not only support higher data throughput but also are more power efficient and support higher system integration. Serializer/deserializer (SERDES)-transceiver technology is a necessary replacement for older parallel technologies. By using transceiver technology, designers can address key issues that exist in today's high-speed data link designs:

- *Signal integrity*—Serial interfaces provide less delay and less skew versus parallel interfaces. Serial protocol compliance and the ability to drive backplanes require transceivers with excellent signal integrity, low jitter, and low bit-error rate (BER).
- *Board complexity*—The use of serial interfaces leads to board-area reduction, decreased number of board components and board layer count. For example, a PCI Express® (PCIe®) interface reduces the number of pins and board area by 50 percent at twice the bandwidth.
- *Power and heat dissipation*—Serial interfaces provide lower power versus parallel interfaces. For example, the Stratix IV GT FPGA's 10G interface consumes 190 mW at 10.3 Gbps, transceiver PMA power using Altera's 40-nm transceivers. Table 1 provides power details for various data rates on the 40-nm process node.

Table 1. PMA Transceiver Power/Channel Comparison

Data Rate	Arria II GX and Arria II GZ	Stratix IV GX	HardCopy IV GX	Stratix IV GT
3.125 Gbps	100 mW	100 mW	100 mW	100 mW
6.5 Gbps	135 mW	135 mW	135 mW	135 mW
8.5 Gbps	N/A	165 mW	N/A	165 mW
10.3 Gbps	N/A	N/A	N/A	190 mW
11.3 Gbps	N/A	N/A	N/A	200 mW

To summarize, there are three main challenges for system architects:

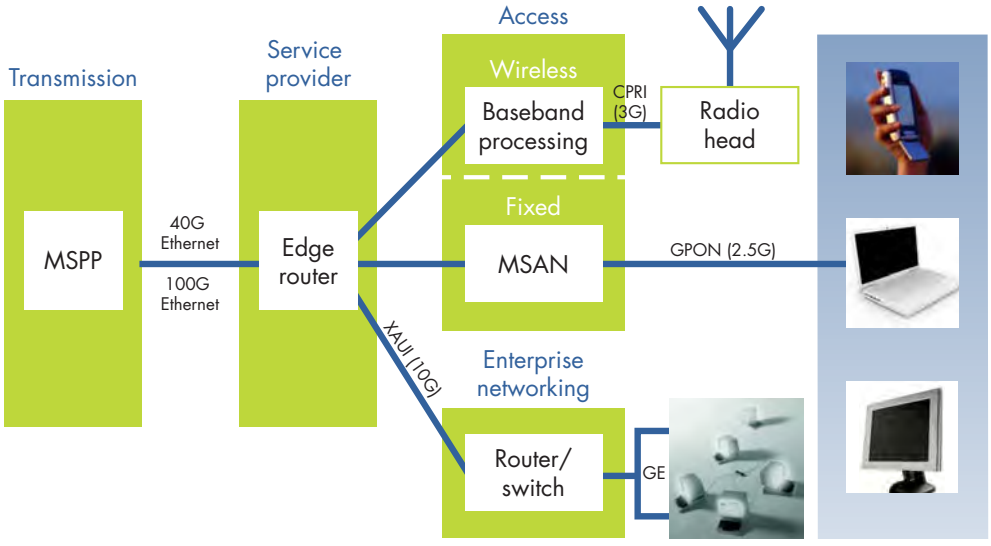
- Increasing bandwidth and data rates require more and faster transceivers
- Diversity and coexistence of evolving standards and legacy high-speed protocols
- Excellent signal integrity required for backplanes and protocol compliance

While transceiver interfaces are the key component that system architects look at first, device selection depends on the functionality, performance, power, and cost targets provided. Ultimately, specific market requirements determine the optimal set of features required for a portfolio of devices with transceivers.

Market Requirements

Figure 1 shows a few examples using Ethernet-based protocols, where transceivers are used in today's communication infrastructure. Serial transceiver technology is used in every part of the network but requires different bandwidths. The closer these get to the customer, the more cost and power-sensitive they must be, while using less bandwidth, transceiver speeds, and numbers. In addition, the ratio of device density to features varies with the processing requirements of the application.

Figure 1. Transceivers in a Communications Infrastructure



Wireline Access, Transmission, and Networking Equipment

Ethernet has evolved into the most widely used physical and link layer protocol today. While 10GbE—first published in 2002 as IEEE Standard 802.3ae—currently is the fastest standard, Ethernet standards for 40GbE and 100GbE are in development by the IEEE. Networks have migrated to packet-based transmission and all-Ethernet-based equipment, with applications ranging from bridging to full data-path processing dominated by packet processing and traffic-management functions. *(1)* Depending on the proximity to the user and location in the network, bandwidths span from 10 Gbps to 20 Gbps, moving to 40 Gbps to 80 Gbps and even further to 100 Gbps. There is no "one size fits all" solution, so devices must be able to support a wide range of densities, features, performance, power, and cost targets.

The key requirements driving technology innovation include the need for integrated 10G transceivers, higher density and high performance, and the support for protocol standards such as Ethernet, GPON, CEI-6/Interlaken, and SONET/SDH.

Wireless Equipment

In the past, wireless standards (air interfaces) have evolved along different technology and geographical paths, but for 3.9G/4G, wider carrier bandwidths (20 MHz) have forced all major new air interfaces to use some form of OFDMA technology. While the orthogonal frequency-division multiple access/multiple-input multiple-output (OFMDA-MIMO) method is expected to create a technological convergence in the upcoming future, current standards migration and deployment is evolutionary.

The main wireless requirements include support for multiple standards in the same system, high signal-processing requirements for next-generation architectures, and the reduction of overall system latency, all of which are driving the need for higher integration. Furthermore, wireless solutions must be highly scalable spanning home basestations called femtocells (as well as picocells, microcells, and macrocells). These market and technical requirements are driving the need for solutions that are so highly integrated that they ultimately are systems on chips (SoCs). In addition, the benefits of these PLDs with transceivers must be comparable or better than alternative solutions:

- Cost and performance in terms of number of users or throughput per unit cost
- Power and footprint in terms of power per Mbps and power per mm^2
- Flexibility and scalability of high-speed transceivers for chip-to-chip, card-to-card, and box-to-box interfaces for different air interfaces and protocols

Again, a universal solution is not available. The key requirements driving technology innovation include higher integration, lower cost, higher performance, signal processing capabilities with integrated DSP functions, and support for application-specific protocols like CPRI/OBSAI and Serial RapidIO®.

Military, Broadcast, Computer and Storage, Test and Medical, and Other Market Segments

Other market segments are extremely diverse in terms of transceiver requirements and optimal density, performance, feature, and power tradeoffs. Standard protocols like PCIe Gen1 and Gen2 and Ethernet are widely used. Some markets have specific requirements with protocols like SDI for broadcast applications, or SATA/SAS, HyperTransport™, and QPI for computer and storage. Because many applications just require transceivers with proprietary protocols, 10G transceivers will be adopted quickly in high-bandwidth bridging applications and will become a main technology driver in many products.

Key Technologies

The technologies used in the portfolio of FPGAs and ASICs with transceivers include process technology, power and performance optimization with Programmable Power Technology, logic fabric, I/Os, and PLLs, external memory interfaces, high-speed serial transceivers, clock data recovery and clock generation, pre-emphasis and equalization, and the use of hard intellectual property (IP) for protocols such as PCIe.

Process Technology and 40-nm Benefits

The 40-nm process offers significant benefits over prior nodes, including the 65-nm node and the more recent 45-nm node. One of the most attractive benefits is higher integration, which allows semiconductor manufacturers to integrate more functionality into smaller dies and offer devices with much higher density.

The 40-nm process also delivers performance benefits. The minimum transistor gate lengths of 40 nm are nearly 38.5 percent shorter than the gate lengths at 65 nm, and 11 percent shorter than the gate lengths at the 45-nm process. The corresponding lower resistance contributes to greater drive strengths at 40 nm, translating to higher performing transistors. The use of strained silicon techniques achieves further performance gains by increasing electron and hole mobility by up to 30 percent, and the resulting transistor performance is up to 40 percent higher.

Although increased density and performance are valuable benefits, one of the most pressing design considerations for today's system developers is power consumption. The 40-nm node provides a benefit here, too, as smaller process geometries reduce the parasitic capacitances that drive up dynamic power consumption. Specifically, Taiwan Semiconductor Manufacturing Company (TSMC)'s 40-nm process technology provides active power downscaling of up to 15 percent over its 45-nm process technology. *(2)*

Unfortunately, reductions in process geometry raise standby power. Altera uses multiple techniques like multi-threshold transistors, multiple transistor channel lengths, and triple-gate oxide to reduce static power, and applies performance versus power tradeoffs in areas of the PLD where performance is not the main criteria, such as within the configuration logic.

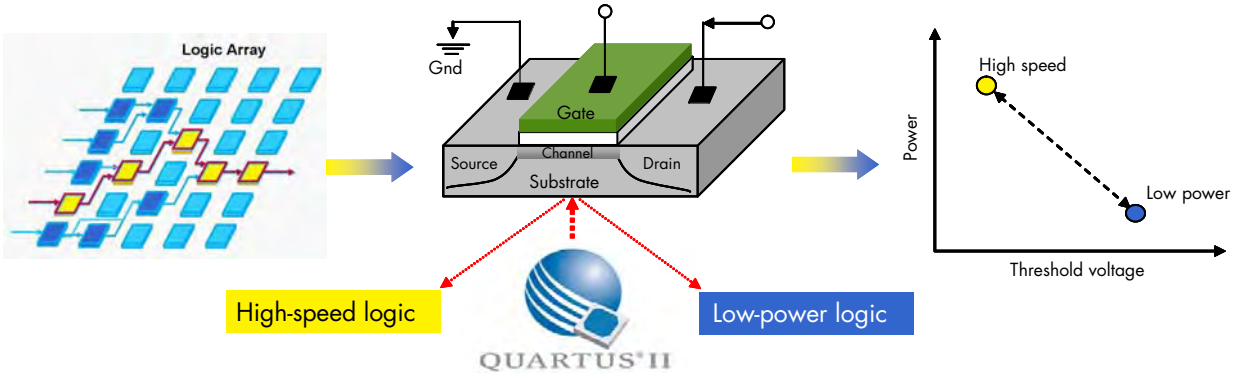
Programmable Power Technology and Performance

Beyond the commonly used circuit design techniques, Altera introduced Programmable Power Technology *(3)* with the 65-nm Stratix® III FPGAs to address static power consumption. Programmable Power Technology reduces static power up to 70 percent and automatically delivers maximum performance at the lowest power for a given design. This innovative technology takes advantage of the fact that, in typical designs, rarely all of the logic resides in the timing-critical path of the applications. Benchmarks show that the ratio between high-performance logic and very little timing slack, and slower logic with enough timing margin is 30:70, on average.

In any design, Altera's Quartus® II development software automatically determines the slack available in each path of the design. This allows it to set the transistors of each logic block, memory, and DSP block automatically to the appropriate mode—high performance or low power—by adjusting the back bias voltage of the transistor:

- In low-power mode, Quartus II software adjusts the back bias voltage, which makes the transistor difficult to turn on. This minimizes subthreshold leakage currents and unwanted static power in non-timing-critical circuit paths (shown in blue in Figure 2).
- In high-performance mode, Quartus II software adjusts the back bias voltage, which makes the transistor easier to turn on in the few timing-critical paths to help meet the design's specified timing constraints and deliver maximum performance (shown in yellow in Figure 2).

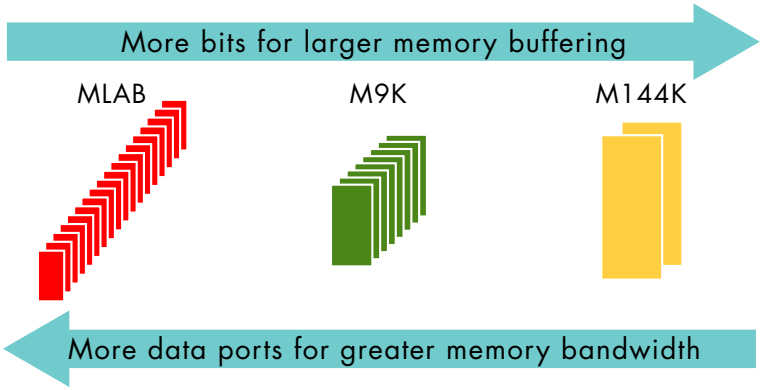
Figure 2. Quartus II Software Minimizes Power and Maximizes Performance



Logic Fabric and General-Purpose I/Os

Altera's 40-nm device fabric uses a common core logic architecture comprising adaptive logic modules (ALMs), TriMatrix on-chip memory blocks and DSP blocks. The ALMs consist of a configurable 8-input fracturable look-up table (LUT), two embedded adders, and two registers, and are routed with the MultiTrack interconnect architecture to support high-speed logic, arithmetic, and register functions with very high device usage. TriMatrix on-chip memory offers maximum efficiency and flexibility by offering three different memory block sizes, shown in Figure 3.

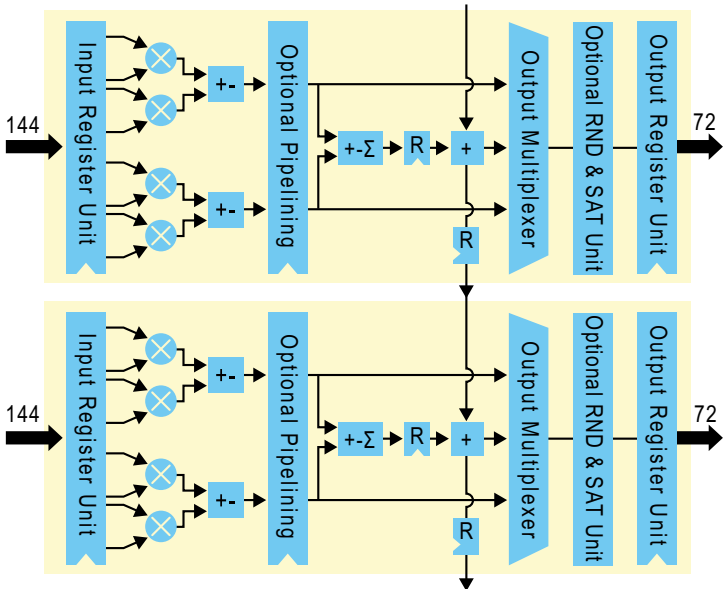
Figure 3. TriMatrix Memory Structure



- 640 bits per block
- Up to 12,600 blocks
- 9K bits per block
- Up to 1,529 blocks
- 144K bits per block
- Up to 64 blocks

The DSP block, shown in Figure 4, is a high-performance silicon architecture with great programmability that delivers optimized processing across many applications. Each DSP block provides eight 18x18 multipliers, as well as registers, adders, subtractors, accumulators, and summation unit—functions that frequently are required in typical DSP algorithms. The DSP block supports variable bit widths and various rounding and saturation modes to meet the exact requirements of an application efficiently.

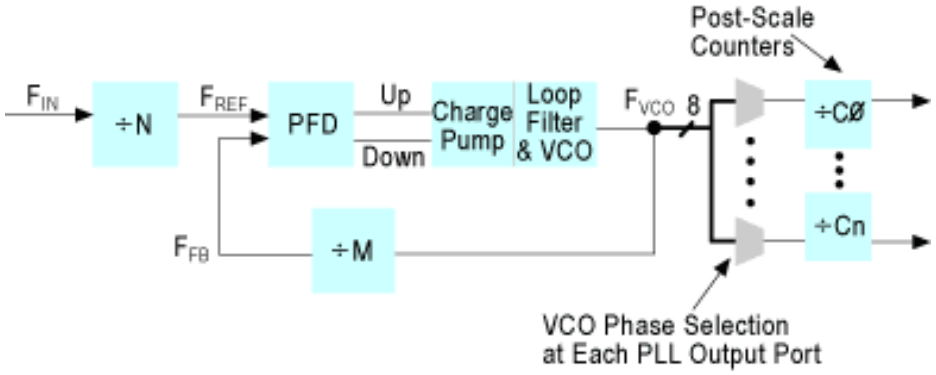
Figure 4. DSP Block Architecture



General-Purpose PLLs

Altera's general-purpose phase-locked loops (PLLs) comprise a closed-loop frequency-control system based on the phase difference between the input clock signal and the feedback clock signal of a controlled oscillator. Figure 5 shows a simplified block diagram of the major components in a PLL.

Figure 5. Block Diagram of a PLL



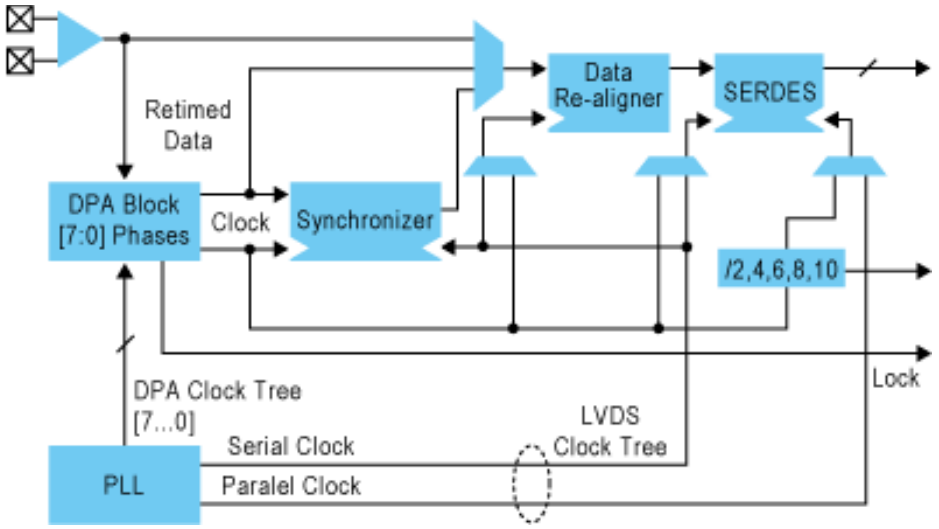
The analog nature of these PLLs provides very low jitter for a robust implementation of clocking schemes. Many configurable clock outputs allow tremendous flexibility for the system clock concept, as well as clock generation for the memory interfaces and I/O interfaces.

High-Speed General-Purpose I/Os and External Memory Interfaces

As shown in Figure 6, the key building blocks of the I/O structure are:

- Single-ended I/O support with programmable slew rate and drive strength, variable delay chains for board-trace compensation, and serial and parallel dynamic on-chip termination (OCT)
- Differential signaling for high-performance LVDS transmission and reception with differential on-chip termination
- Hard dynamic phase alignment (DPA) blocks for multi-lane LVDS-based interfaces to eliminate clock-to-channel and channel-to-channel skew, and clock-forwarding capabilities for soft clock data recovery (CDR)

Figure 6. DPA Block Diagram

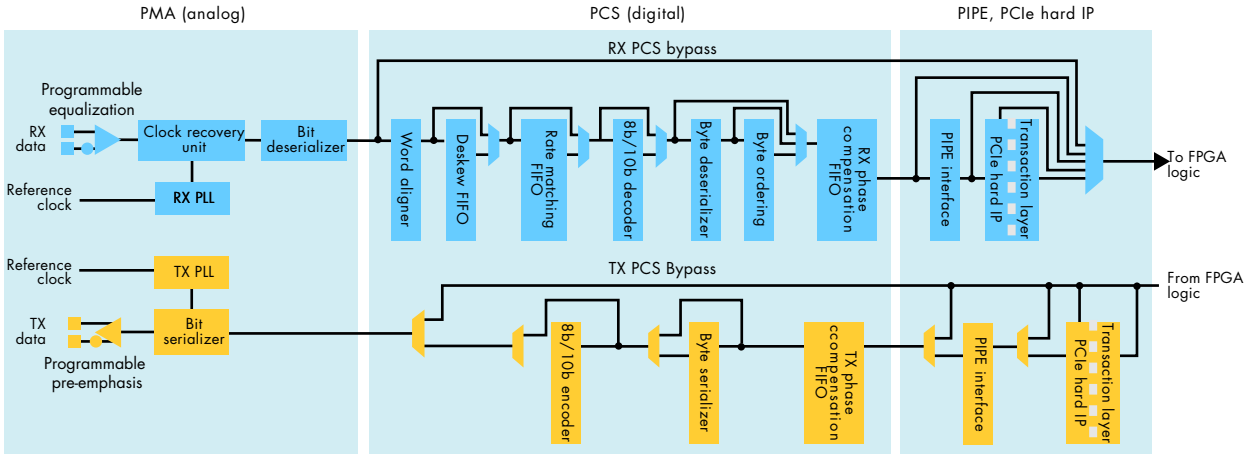


Altera's I/O pins support existing and emerging external memory standards such as DDR, DDR2, DDR3, QDRII, QDRII+, and RLDRAMII. They contain a self-calibrating data path, which constantly and dynamically adjusts itself to provide the highest reliable frequency of operation across process, voltage, and temperature. Other circuitry is included for alignment and synchronization, lane deskew, read/write leveling, and clock-domain crossing functionality.

High-Speed Serial Transceivers

Altera's high-speed transceiver block uses a common architecture (shown in Figure 7) for both the physical medium attachment (PMA) and the physical coding sublayer (PCS). The blocks within the PCS can be bypassed, depending on the designer's requirements.

Figure 7. PMA and PCS Block Diagram



The PMA functionality is used in analog circuitry, and includes:

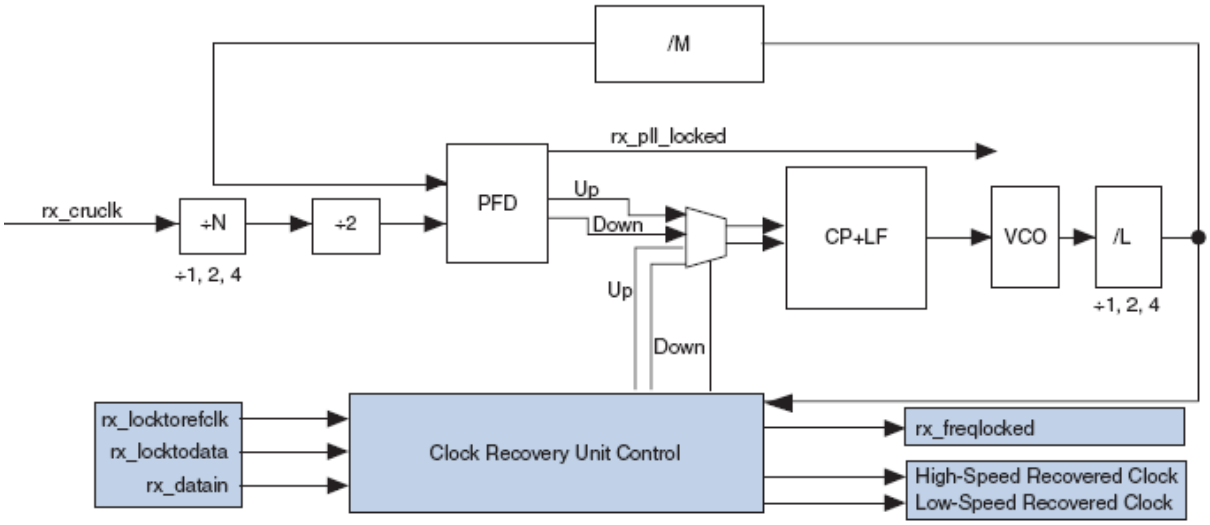
- CDR
- SERDES
- Programmable pre-emphasis and equalization
- I/O buffers with dynamically controllable settings (output differential voltage and differential OCT)

The PCS includes digital functionality to comply with a number of key protocols used in backplane, chip-to-chip, and chip-to-module applications. These digital blocks are optimized for enhanced protocol support, reducing the amount of resources required in the device to create the physical layer of the protocol while maintaining a low-power solution. Combined with specific IP and reference designs, these blocks provide a complete protocol solution, which shortens design cycles and reduces risk. Examples of PCS functions are the 8b/10b encoder/decoder, phase-compensation FIFO buffers, word aligner, and rate matcher to deliver protocol compliance within the transceiver block. In addition, dedicated state machines are included to support the PCIe, GbE, and XAUI protocols.

Clock Data Recovery

As shown in Figure 8, Altera's high-speed CDR circuit uses a hybrid architecture and advances the conventional data-drive architecture by allowing two operating modes. These two modes, lock-to-data and lock-to-reference, can be set automatically or manually. A reference clock is used as input to lock the analog PLL in the CDR unit to the desired frequency. The circuit then switches the input from the reference clock to the data signal to phase-lock the CDR to the data signal, hence recovering the clock embedded in the data. Key advantages of this architecture are improved lock time, lower power consumption, and jitter filtering immunity. As a result, Altera's transceivers provide the lowest jitter and lowest BER necessary for driving backplanes at BER $10E^{-12}$ and beyond, and for protocol compliance.

Figure 8. CDR Architecture



Clock Generation and PLL Technology

Clock generation is an important function in high-speed transceivers. Clock jitter affects both transmitter and receiver performance, and as a result, the BER performance of the high-speed link. A key component of the PLL is the oscillator, which is the major source of jitter. Ideally, high-speed voltage-controlled oscillators (VCOs) provide a wide tuning range, high frequency (GHz), low noise, low power, and are small and highly integrated.

Altera's high-speed transceivers support two types of oscillators, ring oscillators (ROs) and LC tank oscillators (LC tanks). ROs provide high integration, low power, small die area, and excellent jitter over a wide tuning range, and every receive channel has an independent RO operating from 600 Mbps to 10.3 Gbps. However, as frequency increases, phase noise and jitter performance degrade, and LC tanks provide advantages when outstanding phase noise and jitter performance is required at a high frequency. As a drawback, LC tanks contain an inductor and a variable capacitor (varactor), which are larger components.

- Transmit channel ROs
  - Excellent jitter performance for wide frequency range
  - Data range operation from 600 Mbps to 10.3 Gbps

- Transmit channel LC tanks
  - Optimized jitter performance due to technology and narrow operating range
  - LC tank with 4.9–6.375 Gbps optimized for PCIe/CEI-6 compliance
  - LC tank with 9.9–11.3 Gbps optimized for XLAUI/CAUI/CEI-11G compliance

Pre-Emphasis and Equalization

A problem common to all transmission mediums is frequency dependent losses, particularly those related to printed circuit board (PCB) design losses caused by skin effect and dielectric loss. These losses cause greater attenuation of high-frequency components, thus reducing the ability to receive the signal at the far end, reducing drive length, and increasing the BER. Pre-emphasis and equalization are used in Altera's high-speed transceivers to overcome transmission losses and to drive 40" of FR-4 backplane with two connectors.

Pre-emphasis is used in the transmitter of a high-speed transceiver to amplify the high-frequency components of a data signal before it is launched to the channel. Since both prior and future data bits from the generated data signal are known in the transmitter, pre-emphasis techniques are applied to different data bits relative to a main pulse. Altera's pre-emphasis scheme uses a pre-tap followed by a main pulse and two post taps.

Equalization begins in the receiver, acts a high-pass filter to the data signal as it enters the receiver, and then rebuilds the signal to interpret it successfully. There are various equalization schemes available in Altera's high-speed transceivers *(4)*:

- Continuous time linear equalization (CTLE)
- Adaptive dispersion compensation engine (ADCE) *(5)*
- Decision feedback equalization (DFE)

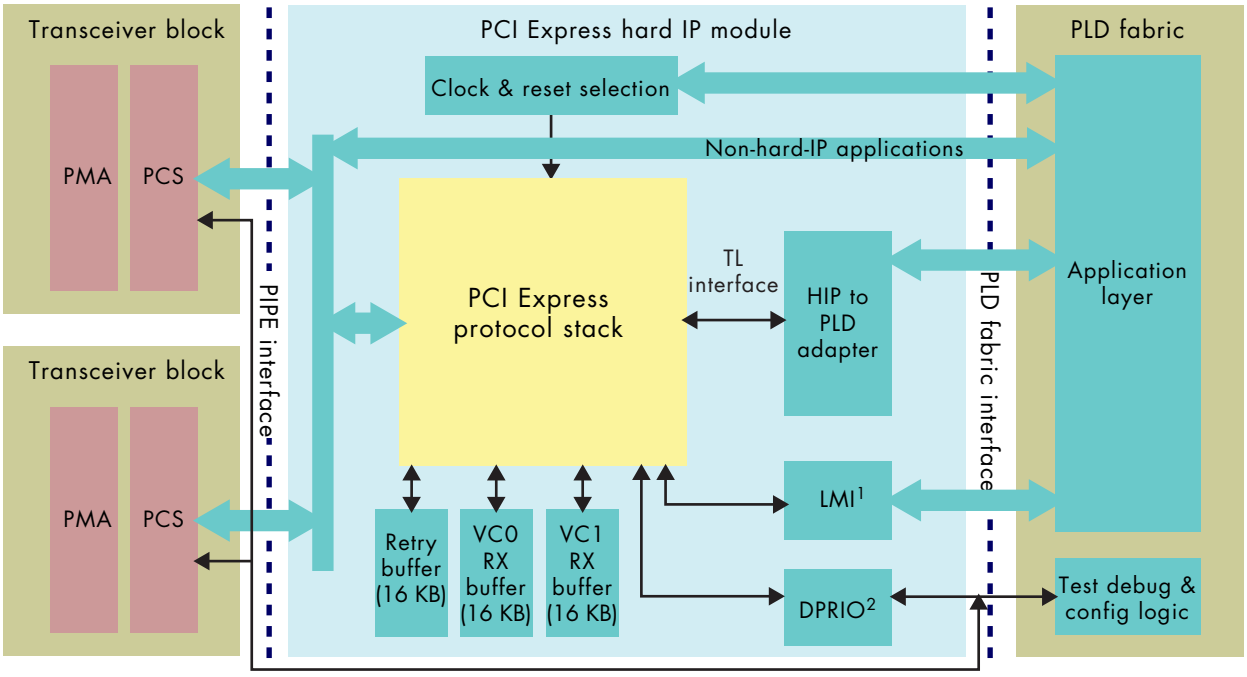
Choosing the optimal settings for equalization from thousands of available settings is challenging due to different data rates and backplanes characteristics. This is facilitated via simulation using transceiver HSPICE models and backplane S-parameter characteristics. But some applications require system card swapping during operation, forcing a quick update of the equalization settings when conditions change. With Plug & Play Signal Integrity, Altera introduced ADCE to support 2.5 Gbps to 6.5 Gbps of up to 40" of FR-4 backplane with hot-swappable transceivers.

Hard IP for PCI Express

The broad adoption of PCIe fostered the evaluation of integrating PCIe functions as pre-verified and standard-compliant hard IP block implementation. Some of the important benefits of PCIe are significant resource savings (up to 40K LEs), lower power, and shorter design cycles with shorter compile times. As shown in Figure 9, the hard IP block embeds all layers of the PCIe protocol stack, including the transceiver modules, physical layer, data link layer, and transaction layer. PCIe hard IP blocks are compliant with the following PCI-SIG specifications:

- PCIe Base Specifications, Rev 1.1 (2.5 Gbps)
- PCIe Base Specifications, Rev 2.0 (2.5 and 5.0 Gbps)

Figure 9. PCIe Hard IP Block



Notes:

(1) LMI: Local management interface

(2) DPRIO: Dynamic partial reconfigurable input/output

Altera's Portfolio of Devices with Transceivers

The development of new device families following Moore's law—double the density every two years—requires a different methodology as the cost to develop parallel and largely unrelated technologies becomes prohibitive. To create a full portfolio of FPGAs and ASICs with transceivers, Altera used the following methodology:

- Reuse of technologies from previous process generations
- Gradual improvements through an evolution of technologies to leverage the advantages of each new process node
- Optimizations of building blocks through variations using a common architecture but with different performance, power, and cost tradeoffs
- Adding revolutionary innovations to address requirements that cannot be addressed by reuse

Portfolio Product Families

Based on TSMC's 40-nm process, each of Altera's FPGAs and ASICs with transceivers is developed with the same proven transceiver architecture that's ideal for high-bandwidth serial interface applications. In each device, the integrated transceiver block is optimized for its targeted applications.

Arria II GX and Arria II GZ FPGAs

Arria® II GX and Arria II GZ FPGAs address cost- and power-sensitive applications while offering a rich feature set in low- to mid-range densities. The maximum transceiver data rate is 6.375 Gbps, which addresses high-speed protocols and bandwidth requirements in key application areas like GPON, IP DSLAM, remote radio heads, broadcast, and bridging in applications with medium performance requirements. The transceivers and I/Os are optimized to support cost-effective implementation by trading off features and performance. While Arria II GX and Arria II GZ FPGAs' fixed power mode does not have the flexibility of Programmable Power Technology, it provides significantly lower static power. Arria II GX and Arria II GZ FPGAs address backplane application with programmable pre-emphasis and equalization, and offer excellent signal integrity. Features such as ADCE and DFE are not included as they are mandatory only for backplane applications with higher data rates to achieve lower cost and lower power.

Stratix IV GX FPGAs

Stratix IV GX FPGAs offer the highest density, highest performance, and lowest power, with transceivers offering up to 8.5 Gbps performance, high bandwidth with up to 48 transceivers, and a rich feature set to support backplane applications and high-speed protocols. Key applications include wireless basestations, 40G/100G applications, high-end routers, and bridging applications with high performance requirements. Superior signal integrity ensures protocol compliance to stringent protocols like PCIe Gen2 and CEI-6. Programmable Power Technology enables high performance in the design's critical timing paths while optimizing power in areas of lower performance.

HardCopy IV GX ASICs

HardCopy® IV GX ASICs address cost- and power-sensitive applications with higher volumes. The performance is comparable to Stratix IV GX FPGAs, which are used as prototyping devices. This unique design methodology, based on a single tool suite with Quartus II development software, enables the lowest risk ASIC with integrated 6.5-Gbps transceivers.

Stratix IV GT FPGAs

While Stratix IV GX FPGAs address 40G/100G applications, the optimized solution needs 10G-capable transceivers. Stratix IV GT FPGAs provide the density, features, and performance advantages of Stratix IV GX FPGAs with integrated 11.3-Gbps transceivers. These enable the optimal system integration of MAC/Framer, packet processing, and traffic management functions with the time-to-market advantage of the programmable fabric. Bridging applications requiring maximum bandwidth also benefit from this device. Stratix IV GT devices can connect directly to optical modules, which, overall, enable the lowest system cost and system power with the least board complexity.

Common IP Portfolio and Development Environment

All of Altera's custom logic devices offer the productivity advantage of a single, comprehensive design software, a common set of IP cores, and a variety of supporting reference designs and design examples.

Portfolio Specifications

This section compares the technical specifications for key criteria of the transceiver portfolio, with Table 2 highlighting the common architectural elements. All element-specific features are supported across all devices.

Table 2. Architectural Elements of Altera Devices

Elements	Arria II GX and Arria II GZ	Stratix IV GX	HardCopy IV GX	Stratix IV GT
40-nm benefits	All	All	All	All
ALMs	18K–163K	29K–212K	N/A	91K–212K
Logic elements (LEs)	45K–350K	73K–531K	2.8M–11.5M *(1)*	228K–531K
Registers	36K–205K	58K–425K	0–531K *(2)*	182K–425K
Tri-Matrix Memory	3.4M–16.4M	6.3M–20.3M	6.3M–20.3M	13.9M–20.3M
M144K blocks	24–36 (Arria II GZ only)	16–64	16–64	22–64
M9K blocks	319–1,248	462–1,280	462–1,280	936–1,280
MLAB memory	0.2M–3.2M	0.8M–6.5M	0–1.625M *(2)*	2.8M–6.4M
DSP blocks	232–1040	384–1288	0–1,288 *(2)*	832–1,288
Analog PLLs	4–8	3–12	2–8	8–12
I/Os	156–726	368–904	368–736	636–754
True LVDS *(3)*	32–144	28–98	28–88	44
Emulated LVDS	TBD	128–256	128–256	192–256
Transceivers	4–24	8–48	8–36	36–48
SEU Mitigation	Yes	Yes	Yes	Yes
Design Security	Yes	Yes	Hard wired	Yes

Notes:

(1) ASIC gates calculated as 12 gates per LE; 5000 gates per 18x18 multiplier.

(2) Built using HCells.

(3) Full duplex pairs that include receive and transmit.

Table 3 compares the portfolio devices regarding power and performance.

Table 3. Altera Device Power and Performance

Power and Performance	Arria II GX and Arria II GZ	Stratix IV GX	HardCopy IV GX	Stratix IV GT
Programmable Power Technology *(1)*	LP only	LP/HP	Not needed	LP/HP
Performance				
Speed Grades	-4, -5, -6	-2/-2x *(2)*, -3, -4	N/A	-1, -2, -3
Clock	500 MHz	600 MHz	600 MHz	600 MHz
DSP	350 MHz	550 MHz	495 MHz	550 MHz
Internal memory	390 MHz	550 MHz	500 MHz	550 MHz
LVDS				
I/O	1 Gbps	1.6 Gbps	1.25 Gbps	1.6 Gbps
DPA	Yes	Yes	Yes	Yes
Memory				
DDR	200 MHz	200 MHz	200 MHz	200 MHz
DDR2	300 MHz	400 MHz	400 MHz	400 MHz
DDR3	300 MHz	533 MHz	533 MHz *(3)*	533 MHz
QDRII	250 MHz	350 MHz	350 MHz	350 MHz
QDRII+	TBD	350 MHz	350 MHz	350 MHz
RLDRAMII	TBD	400 MHz	400 MHz	400 MHz

Notes:

(1) Low power (LP)/high performance (HP)

(2) Support for -2 core and -3 I/O speed-grade. Support for PCIe Gen1 and Gen2 x8.

(3) Pending characterization

Table 4 highlights high-speed transceiver features and performance.

Table 4. Altera's High-Speed Transceiver Features and Performance

Features	Arria II GX and Arria II GZ	Stratix IV GX	HardCopy IV GX	Stratix IV GT *(1)*
3G transceivers	4–16	8–48	8–36	36–48
6G transceivers	N/A	8–48	8–36	36–48
8.5G transceivers	N/A	0–32	N/A	24–32
10G transceivers	N/A	N/A	N/A	12–24
Total transceivers	4–16	8–48	8–36	36–48
Maximum data rate (Gbps)				
Commercial	3.75	8.5	6.5+	11.3
Industrial	3.125	6.5	6.5	11.3 *(2)*
Hard IP for PCIe	1	1–4	2	1 *(1)*
Generation	Gen1	Gen1 and Gen2	Gen1 and Gen2	Gen1 and Gen2
Lane width	x1, x2, x4, x8	x1, x2, x4, x8	x1, x2, x4, x8	x1, x2, x4 *(1)*
Equalization	Yes	Yes	Yes	Yes
Pre-Emphasis	Yes	Yes	Yes	Yes
ADCE	N/A	Yes	Yes	Yes *(1)*
DFE	N/A	Yes	Yes	Yes *(1)*
Backplane	Yes	Yes	Yes	Yes
Maximum data rate	3.75 Gbps	6.5 Gbps	6.5 Gbps	6.5 Gbps

Notes:

(1) Preliminary data, subject to change

(2) 0°C - 100°C

Table 5 shows the available protocols and data rates of each product family.

Table 5. Altera's High-Speed Protocols and Data Rates (Gbps per lane)

Protocol	Arria II GX and Arria II GZ	Stratix IV GX	HardCopy IV GX	Stratix IV GT
3G-SDI	2.97	2.97	2.97	2.97
SDI SD/HD	0.27/1.485	0.27/1.485	0.27/1.485	-
ASI	0.27	0.27	0.27	-
Basic (proprietary)	0.6–3.75	0.6–8.5	0.6–6.5	2.488–11.3 *(1)*
CEI-6G/SR/LR	-	4.976–6.375	4.976–6.375	4.976–6.375
CPRI	0.6144, 1.2288, 2.4576, 3.072	0.6144, 1.2288, 2.4576, 3.072	0.6144, 1.2288, 2.4576, 3.072	3.072
10G Ethernet (XAUI)	3.125	3.125	3.125	3.125
10G Ethernet (XFI, SFI)	-	-	-	10.3125
40G, 100G Ethernet	-	-	-	10.3125
GbE	1.25	1.25	1.25	1.25 (LVDS based)
Fibre Channel	-	1.0625, 2.125, 4.25, 8.5	1.0625, 2.125, 4.25	4.25, 8.5, 10.51875 *(2)*
GPON	1.244 uplink, 2.488 downlink	1.244 uplink, 2.488 downlink	1.244 uplink, 2.488 downlink	2.488 downlink
G.709 OTU-2	-	-	-	10.7
OTN 10GbE with FEC	-	-	-	11.1, 11.3
HiGig+	3.75	3.75	3.75	3.75
HyperTransport 3.0	-	0.4, 2.4, 2.8, 3.2	0.4, 2.4, 2.8, 3.2	2.8, 3.2
Interlaken	-	3.125–6.375	3.125–6.375	3.125–6.375
OBSAI	0.768, 1.536, 3.072	0.768, 1.536, 3.072	0.768, 1.536, 3.072	3.072
PCI Express Gen1, Gen2	2.5, N/A	2.5, 5.0	2.5, 5.0	2.5, 5.0
PCI Express Cable	2.5	2.5	2.5	2.5
RXAUI	-	6.25	6.25	6.25
SAS	1.5, 3.0	1.5, 3.0, 6.0	1.5, 3.0, 6.0	3.0, 6.0
SATA	1.5, 3.0	1.5, 3.0, 6.0	1.5, 3.0, 6.0	3.0, 6.0
SerialLite II	0.6–3.75	0.6–6.375	0.6–6.375	2.488–6.375
Serial RapidIO	1.25, 2.5, 3.125	1.25, 2.5, 3.125	1.25, 2.5, 3.125	2.5, 3.125
SFI-5.1	-	2.488–3.125*(3)*	2.488–3.125 *(3)*	2.488–3.125 *(3)*
SFI-5.2	-	-	-	9.9–11.3
SONET OC-3/OC-12/ OC-48/OC-192	0.155, 0.622, 2.488, N/A	0.155, 0.622, 2.488, N/A	0.155, 0.622, 2.488, N/A	N/A, N/A, 2.488, 9.95 *(4)*
SPAUI	3.125	3.125, 6.25	3.125, 6.25	3.125, 6.25

Notes:

(1) 10G Basic (proprietary)
(2) 10G Fibre Channel
(3) Includes SFI-4.2 and SFI-5.1
(4) 10G SONET/SDH OC-192/STM-64

Conclusion

Increasing bandwidth requirements and data rates demand more and faster transceivers. The diversity of evolving standards and the need for excellent signal integrity for backplane capabilities and protocol compliance drive transceiver innovation on digital devices. To meet the diverse requirements in different markets and applications, digital devices must provide an optimal ratio of density and features while meeting performance, power, and cost targets. Technology innovation and reuse on Altera's portfolio of 40-nm FPGAs and ASICs with transceivers address these requirements and provide the broadest custom-logic portfolio with transceivers.

Each of Altera's 40-nm FPGAs and ASICs with transceivers is created with the same proven transceiver architecture, ideal for high-bandwidth serial interface applications. In each device, the integrated transceiver block is optimized for its targeted applications. Arria II GX and Arria II GZ FPGAs are low-power, cost-effective devices that make building 6.375-Gbps transceiver solutions easy. Stratix IV GX FPGAs are high-performance devices with up to 530K LEs and high levels of transceiver and memory bandwidth. Stratix IV GT FPGAs are the only FPGAs with integrated 11.3-Gbps transceivers, ideal for 40G and 100G applications. HardCopy IV GX ASICs are a package- and pin-compatible ASIC counterpart to Stratix IV GX FPGAs, ready to help lower risk and total cost in ASIC designs with embedded transceivers. Plus, all of Altera's custom logic devices offer the productivity advantage of a single, comprehensive design software, a common set of intellectual property (IP) cores, and a variety of supporting reference designs and design examples.

Further Information

1. Using 10-Gbps Transceivers in 40G/100G Applications: www.altera.com/literature/wp/wp-01080-stratix-iv-gt-40g-100g.pdf
2. *Leveraging the 40-nm Process Node to Deliver the World's Most Advanced Custom Logic Devices*: www.altera.com/literature/wp/wp-01058-stratix-iv-40nm-process-node-custom-logic-devices.pdf
3. *Altera at 40 nm: Jitter-, Signal Integrity-, Power-, and Process-Optimized Transceivers:* www.altera.com/literature/wp/wp-01057-stratix-iv-jitter-signal-integrity-optimized-transceivers.pdf
4. *40-nm Power Management and Advantages:* www.altera.com/literature/wp/wp-01059-stratix-iv-40nm-power-management.pdf
5. "Digitally Assisted Adaptive Equalizer in 90 nm With Wide Range Support From 2.5 Gbps to 6.5 Gbps," DesignCon 2007: www.altera.com/literature/cp/cp-01026.pdf
6. Literature: Stratix IV Devices (E, GX, and GT variants): www.altera.com/literature/lit-stratix-iv.jsp
7. Arria II GX FPGAs: Cost-Optimized, Lowest Power 6G Transceiver FPGAs: www.altera.com/products/devices/arria-fpgas/arria-ii-gx/aiigx-index.jsp

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Document Revision History

Table 6 shows the revision history for this document.

Table 6. Document Revision History

Date	Version	Changes
July 2010	1.4	■ Updated Table 2, Further Information. ■ Minor text edits.
March 2009	1.3	■ Added Table 1. ■ Updated Table 5 (previously Table 4).
February 2009	1.2	Updated Table 4.
February 2009	1.1	Updated Table 4.
February 2009	1.0	Initial release.