Intel® Pentium® Silver and Intel® Celeron® Processor

Specification Update

Formerly known as Jasperlake

Revision 0.5

January 2021

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Contents

1 Preface 5
1.1 Affected Documents 5
1.2 Nomenclature 5
2 Identification Information 6
2.1 Component Identification via Programming Interface 6
2.2 Component Marking Information 6
3 Summary Tables of Changes 8
3.1 Codes Used in Summary Table 8
3.2 Errata Summary Table 8
4 Errata 10

Figure

Figure 2-1. SoC Markings 7

Tables

Table 2-1. Processor Lines Component Identification 6

Revision History

Document Number	Revision Number	Description	Revision Date
634542	0.5	• Initial release	January 2021

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1 Preface

This document is an update to the specifications contained in the documents listed in the Affected Documents. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number/Location
Intel® Pentium® Silver and Intel® Celeron® Processors Datasheet, Volume 1 of 2	633935
Intel® Pentium® Silver and Intel® Celeron® Processors Datasheet, Volume 2 of 2	634545

1.2 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes is incorporated in the next release of the specifications.

Specification Clarifications – This describes the specification in greater detail or further highlight a specifications impact to a complex design situation. These clarifications is incorporated in the next release of the specifications.

Documentation Changes – This includes typos, errors, or omissions from the current published specifications. These changes is incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to he appropriate product specification or user documentation (datasheets, manuals, etc.).

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2 Identification Information

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 2-1. Processor Lines Component Identification

Samples	CPUID	Reserved	Extended Family[1]	Extended Model[2]	Reserved	SoC Type[3]	Family Code[4]	Model Number[5]	Stepping ID[6]
		31:28	27:20	19:16	15:14	13:12	11:8	7:4	3:0
JSL	0x906C0	Reserved	0000000b	1001b	Reserved	00b	0110b	1100b	0000b

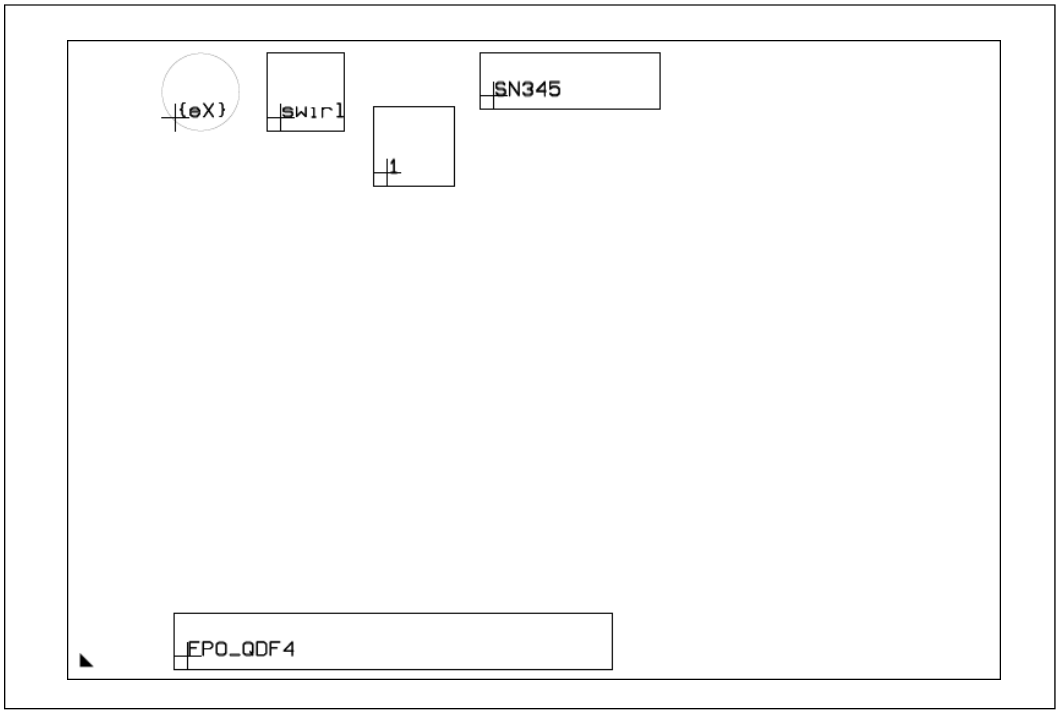
NOTES:

1. The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the SoC belongs to the Intel 386®, Intel 486®, Pentium®, Pentium 4, or Intel® Core™ SoC family.
2. The Extended Model, bits [19:16] in conjunction with the model number, specified in bits [7:4], are used to identify the model of the SoC within the SoC family.
3. The SoC Type, specified in bits [13:12] indicates whether the SoC is an original OEM SoC, an Overdrive SoC, or a dual SoC (capable of being used in a dual SoC system).
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model. Refer to above table for the SoC stepping ID number in the CPUID information.

2.2 Component Marking Information

Intel® Pentium® Silver and Intel® Celeron® Processors SoC is identified by the following component markings:

Figure 2-1. SoC Markings



Pin count:1338 Package Size: 35 mm x 24 mm

Production (SSPEC):
FPO_SSPEC: FPOxxxxxSSPEC

{eX}

SWIR1: Intel logo

Note: "1" is used to extract the unit visual ID (2D ID).

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3 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	Stepping A1	Title
JSL001	No Fix	USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State
JSL002	No Fix	xHCI U1 Exit LFPS Duration
JSL003	No Fix	xHCI Power Management Link Timer
JSL004	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
JSL005	No Fix	SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used
JSL006	No Fix	Intel® Trace Hub Pipe Line Empty
JSL007	No Fix	xHCI CV TD 2.2 Interrupter Handling
JSL008	No Fix	xHCI Link Protocol Field Value
JSL009	No Fix	xHCI Short Packet Event Using Non-Event Data TRB
JSL010	No Fix	eSPI SBLCL Register Bit Not Cleared By PLTRST#
JSL011	No Fix	Leakage On VCC_VNNEXT_1P05 Power Rail With External Bypass VR

Erratum ID	Stepping A1	Title
JSL012	No Fix	xHCI Protocol Speed ID Count Field
JSL013	No Fix	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment
JSL014	No Fix	Time Synchronization with xHCI
JSL015	No Fix	Performance Monitoring Event L2 Prefetches Offcore Response May Overcount
JSL016	No Fix	Performance Monitoring Event Outstanding Modified Write-Back Request May Overcount
JSL017	No Fix	VM-Entry Failure Not Treated Properly if Intel® PT is Enabled
JSL018	Fixed	CLDEMOTE Opcodes May Cause Unpredictable System Behavior
JSL019	No Fix	Intel® PT ToPA Stop May Occur Early When ToPA Region is Comprised of Multiple EPT Pages
JSL020	No Fix	Writing PMC0 Only When All PMCs Are locally Disabled Results in Loss of Reduced Skid PEBS Behavior
JSL021	No Fix	Disabling The APIC While an Interrupt is Being Delivered May Cause a System Hang

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4 Errata

JSL001	USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State
Problem	If a PCH USB 3.2 Type-C port is configured in Device Mode (or in DbC mode) and connected to a external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1. PCH resumes from S3, S4, or S5 state, the port may remain in U2. 2. Port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled. 3. Port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.
Implication	PCH USB Type C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL002	xHCI U1 Exit LFPS Duration
Problem	The xHCI U1 Exit LFPS (t13-t11) duration timing is implemented as 0.6 us to 0.9 us. The USB-IF released a ECN updating this timing value to 0.9 us to 1.2 us.
Implication	USB-IF xHCI CV TD 7.18 may report a failure. Intel has obtained a waiver for TD 7.18 NOTE: No functional issues are expected.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL003	xHCI Power Management Link Timer
Problem	The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.
Implication	USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21. NOTE: No functional issues are expected.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL004	xHCI USB 2.0 ISOCH Device Missed Service Interval
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets. NOTE:This issue has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL005	SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used
Problem	For flash device suspend/resume opcodes, the SPI controller does not use JEDEC SFDPs 13th DWORD bits [15:0], Program Suspend Instruction and Program Resume Instruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend/resume opcodes.
Implication	If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend /resume feature is not functional. In this case, system behavior varies depending on what the suspend/resume instruction is and when it is generated. NOTE: Major flash vendors have been using the same value for bits [31:16] and bits [15:0].
Workaround	None identified. If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.
Status	For the steppings affected, refer to Chapter 3

JSL006	Intel® Trace Hub Pipe Line Empty
Problem	The Intel® Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset 0xD4) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset 0xD8) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).
Implication	There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).
Workaround	None identified. CaptureDone should be cleared or de-asserted after the pipe line is empty.
Status	For the steppings affected, refer to Chapter 3

JSL007	xHCI CV TD 2.2 Interrupter Handling
Problem	The xHCI Host Controller will clear the Interrupt Pending (IP) bit when the Interrupt Enable (IE) bit is set, contrary to the expectation of the xHCI CV TD 2.2 Interrupt Handling test.
Implication	USB-IF xHCI CV TD 2.2 may report a failure. Intel has obtained a waiver for TD 2.2. NOTE: No functional impact is expected.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL008	xHCI Link Protocol Field Value
Problem	The xHCI Host Controller reports the Link Protocol (LP) bits [15:14] as 0x0h in the XECP_SUPP_USB3_5 Super Speed Plus register (xHCI MMIO offset 0x8034). The xHCI spec rev 1.1 (published in Nov. 2017) defines this bit should be set to 0x1h for SuperSpeed USB 10 Gbps port.
Implication	USB-IF xHCI CV TD 1.9 may report a failure. Intel has obtained a waiver for TD 1.9. NOTE: No functional impact is expected.
Workaround	None identified.

Status	For the steppings affected, refer to Chapter 3

JSL009	xHCI Short Packet Event Using Non-Event Data TRB
Problem	The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.
Implication	Transfer may fail due to the packet size error. NOTE: This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.
Workaround	None identified. Intel recommends software to use Data Event TRBs for short packet completion.
Status	For the steppings affected, refer to Chapter 3

JSL010	eSPI SBLCL Register Bit Not Cleared By PLTRST#
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	None identified. NOTE: If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to Chapter 3

JSL011	Leakage On VCC_VNNEXT_1P05 Power Rail With External Bypass VR
Problem	Leakage on VCC_VNNEXT_1P05 power rail may be observed when external bypass VR is operating with VID value of 0.76 V.
Implication	System may shut down due to the external VR over voltage protection (OVP) limits.
Workaround	Platform designs with an external VR must be designed to operate with Over Voltage Protection (OVP) range of: 1.155 V ≤ OVP ≤ 1.365 V for all VID settings (1.05 V and 0.76 V).
Status	For the steppings affected, refer to Chapter 3

JSL012	xHCI Protocol Speed ID Count Field
Problem	The xHCI Host Controller reports an incorrect Protocol Speed ID Count value for the USB 3.2 Supported Protocol Capability register - xHCI MMIO offset 8028 bits [31:28].
Implication	USB-IF xHCI CV TD 1.9 may report a failure. Note: No functional impact is expected.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL013	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment
Problem	If software assigns a 4 GB-aligned address to the Linked List Pointer (LLP_LOn = 0h) for Intel® Serial I/O Controller DMA engine, then the DMA engine interprets this as an empty link list and will not perform DMA transfers.
Implication	An Intel® Serial IO controller (that is UART) may stop operating which may cause the system to hang.
Workaround	Driver software should not assign LLP to a 4 GB-aligned address. NOTE: This issue has been addressed in the Intel Serial IO drivers in the following versions or later: For Microsoft* Windows* 10, I2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1.
Status	For the steppings affected, refer to Chapter 3

JSL014	Time Synchronization with xHCI
Problem	The xHCI does not use the correct time base for time synchronization.
Implication	xHCI Precision Time Measurement is not supported. Note: This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL015	Performance Monitoring Event L2 Prefetches Offcore Response May Overcount
Problem	The performance monitoring event OFFCORE_RESPONSE (Event B7H, UMask 01H and Event B7H, UMask 02H) should count responses matching the request-response configuration specified in MSR_OFFCORE_RSP_0 (1A6H) and MSR_OFFCORE_RSP_1 (1A7H), respectively, for core originated requests. However, due to this erratum, L2 Prefetch requests HW_L2_DATA_RD [bit 4] or HW_L2_RFO [bit 5] may additionally count a subset of L1 Prefetch requests.
Implication	Due to this erratum, software counting L2 prefetches may also count some L1 prefetches.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL016	Performance Monitoring Event Outstanding Modified Write-Back Request May Overcount
Problem	When using the performance monitoring event OFFCORE_RESP.MSR_OFFCORE_RESP0 (Event: B7H, UMask: 01H), and Outstanding Modified Write-Back Offcore Response events are enabled by setting Outstanding [bit 63] as well as COREWB_M [bit 3], COREWB_NONM [bit 12], L1_WB_M [bit 48], or L2_WB_M [bit 49] in MSR_OFFCORE_RSP_0 (MSR 01A6H), the event may over count.
Implication	Software monitoring Outstanding Modified Write-Back requests may observe excessive event counts.
Workaround	None Identified. Software should not rely on the counts for this event.
Status	For the steppings affected, refer to Chapter 3

JSL017	VM-Entry Failure Not Treated Properly if Intel® PT is Enabled
Problem	VM entry should fail if Intel® PT (Processor Trace) is enabled and the "load IA32_RTIT_CTL" VM-entry control is 1.Due to this erratum, the processor will treat this situation as a “VM entry failure during or after loading guest state” instead of treating it as a failure that occurs before loading of guest state. This means that the processor will load state as would be done on a VM exit (a failed VM entry) instead of passing control to the next instruction and setting RFLAGS.ZF.
Implication	Software may see an unexpected type of failure for such VM entries.
Workaround	Software should disable Intel PT before executing VM entry if the "load IA32_RTIT_CTL" VM-entry control is 1.
Status	For the steppings affected, refer to Chapter 3

JSL018	CLDEMOTE Opcodes May Cause Unpredictable System Behavior
Problem	Under complex micro architectural conditions, the opcode bytes 0F 1C /0 in the instruction stream may cause unpredictable system behavior. Note that this can occur regardless of whether these opcode bytes of 0f 1C /0 represent CLDEMOTE (CPUID.7.0.ECX[25] is 1) or represent NOP (CPUID.7.0.ECX[25] is 0).
Implication	When this erratum occurs, it may result in unpredictable system behavior, such as an unexpected Page Fault (#PF), General Protection (#GP), or Undefined Opcode (#UD) exception. Those exceptions may cause an application to unexpectedly close.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to Chapter 3

JSL019	Intel® PT ToPA Stop May Occur Early When ToPA Region is Comprised of Multiple EPT Pages
Problem	If Intel® Processor Trace (PT) is enabled by setting IA32_RTIT_CTL.TraceEn[0] (MSR 0570H) to 1 while executing in a Virtual Machine Extensions (VMX) guest with the "Intel PT uses guest physical addresses" VM-execution control set to 1, and Intel® PT is writing to a ToPA (Table of Physical Addresses) region configured for ToPA stop, such that the ToPA region size is greater than the size of the underlying Extended Page Table (EPT) pages and the IA32_RTIT_OUTPUT_MASK_PTRS.OutputOffset[63:32] (MSR 0561H) value indicates that the next trace byte should be written to the last EPT page in the ToPA region, IA32_RTIT_STATUS.STOPPED[5] (MSR 0571H) will be set immediately rather than when the region is filled.
Implication	ToPA stop may occur before the last page of the associated ToPA region is filled. Intel has only observed this erratum in synthetic test conditions. Intel has not observed this erratum in any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to Chapter 3

JSL020	Writing PMC0 Only When All PMCs Are locally Disabled Results in Loss of Reduced Skid PEBS Behavior
Problem	If IA32_PMC0 (MSR 0C1H) or IA32_A_PMC0 (MSR 04C1H) is written when ENABLE[bit 0] is clear in all IA32_PERFEVTSELx MSRs (MSRs 0187H..018AH), the Performance Monitoring Counter 0 (PMC0) Processor Event-Based Sampling (PEBS) skid for precise events is not guaranteed to be 1 event as required by Reduced Skid PEBS behavior.
Implication	When this erratum occurs, PMC0 will behave like other PMCs, without Reduced Skid PEBS behavior.

Workaround	Writes to PMC0 should occur while at least one PMC is enabled in IA32_PERFEVTSELx.
Status	For the steppings affected, refer to Chapter 3

JSL021	**Disabling The APIC While an Interrupt is Being Delivered May Cause a System Hang**
Problem	Under complex microarchitectural conditions, if software disables the APIC by clearing IA32_APIC_BASE[11] (MSR 1BH) while an interrupt is being delivered, the system may hang.
Implication	Due to this erratum, the system may become unresponsive and hang with an Internal Timer Error with Machine Check Exception (MCACOD=0400h) logged into IA32_MC0_STATUS (MSR 400H).
Workaround	None identified. System software should quiesce the system of pending interrupts before attempting to disable the APIC.
Status	For the steppings affected, refer to Chapter 3

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