

Intel® Pentium® Processor N4200 and Celeron® Processors J3355, J3455 & N3350 for Internet of Things Platforms

Specification Update Addendum - Public

August 2022

Revision 002

Document Number: 615560



You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting: http://www.intel.com/design/literature.htm

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at http://www.intel.com/ or from the OEM or retailer.

Intel, Intel Celeron, Atom, Pentium, and the Intel logo are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others.

Copyright© 2022, Intel Corporation. All rights reserved.

Contents

1.0 Introduction 6

1.1 Terminology 6
1.2 Affected Documents 7
1.3 Reference Documents 8

2.0 Summary Tables of Changes 9

2.1 Codes Used in Summary Table 9

3.0 Identification Information 11

4.0 Component Marking Information 14

5.0 Errata 15

5.1 APL47 System May Experience Inability to Boot or May Cease Operation or Nonfunctioning of LPC, SD card and RTC Circuitry 15
5.2 APLJN-01 Intermittent Display Flicker during Playback of NV12 Pixel Format Video 15
5.3 APLJN-02 Deasserting PCICMD_PCISTS.BME Before Stopping ISP Camera Driver May Lead to a System Hang 16
5.4 APLJN-03 I2C Specification Hold Time May be Violated for PMIC I2C TX_HOLD 16
5.5 APLJN-04 Unexpected #PF, #GP, #UD, or Other Unpredictable System Behavior May Occur 16

6.0 Specification Changes 17

6.1 Datasheet Update 17

6.1.1 SVID Signals Internal Weak Pull-up (1k and 2k) Removal 17
6.1.2 SVID Signals Internal Weak Pull-up (1k and 2k) Removal 18
6.1.3 SVID Signals Internal Weak Pull-up (1k and 2k) Removal 19
6.1.4 Package Information 19

7.0 Specification Clarifications 21

8.0 Documentation Changes 22

Figures

Figure 1. Processor Family Top-Side Markings 14



Tables

Table 1. Terminology 6
Table 2. Affected Documents 7
Table 3. Reference Documents 8
Table 4. Summary Table of Changes 10
Table 5. Component Identification via Programming Interface 11
Table 6. Processor Identification by Register Contents 12
Table 7. Identification Table 13

Revision History

Date	Revision	Description
August 2022	002	• Added new Errata APJN-04: Unexpected #PF, #GP, #UD, or Other Unpredictable System Behavior May Occur
November 2019	001	Initial release

§

1.0 Introduction

This document is an update to the specifications in the documents listed in Table 2. Affected Documents. This document is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools.

Information types defined in Table 1. Terminology consolidated into this document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Terminology

Table 1. Terminology

Term	Description
Processor	Intel® Pentium® processor N4200 and Intel® Celeron® processor J3355, J3455 & N3350 for Internet of Things Platforms
SoC	Intel® Pentium® processor N4200 and Intel® Celeron® processor J3355, J3455 & N3350 for Internet of Things Platforms
Errata	Design defects or errors in engineering samples. Errata may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping assumes that all errata documented for that stepping are present on all devices.
sSpec Number	A five-digit code used to identify products. Products are differentiated by their unique characteristics, for example, core speed, L2 cache size, package type and so on as described in the SoC identification information table. Read all notes associated with each sSpec number.
QDF Number	A four-digit code used to distinguish between engineering samples. These samples are used for qualification and early design validation. The functionality of these parts can range from mechanical only to fully functional. This document has a component identification information table that lists these QDF numbers and the corresponding product details.

Term	Description
Specification Changes	Modifications to the current published specifications. These changes are incorporated in any new release of the specification.
Specification Clarifications	Clarifications of a specification with greater detail or further highlighting a specification's impact to a complex design situation. These clarifications are incorporated in any new release of the specification.
Documentation Changes	Changes to the specification that include typos, errors, or omissions from the current published specifications. These changes are incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available on request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so forth).

1.2 Affected Documents

Table 2. Affected Documents

Document Title	Document No./Location
Intel® Pentium® and Celeron® Processor N and J Series Spec Update	334820
Intel® Pentium® and Celeron® Processor N and J Series: Datasheet Volume 1 of 3	334817
Intel® Pentium® and Celeron® Processor N and J Series: Datasheet Volume 2 of 3	334818
Intel® Pentium® and Celeron® Processor N and J Series: Datasheet Volume 3 of 3	334819

1.3 Reference Documents

Table 3. Reference Documents

Document	Document No./Location
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	252046
Combined Volume Set of Intel® 64 and IA-32 Architecture Software Developer's Manuals	325462
Intel® 64 and IA-32 Intel® Architectures Optimization Reference Manual	248966

§

2.0 Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes, which apply to the listed steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted.

***Note**:* The errata indicated in the following table replace those APLxx errata listed in the Intel® Pentium® and Celeron® Processor N- and J- Series (Formerly Apollo Lake) Specification Update. Any errata that are not replaced must be considered to be applicable to the processors covered by this document. The Specification Changes, Specification Clarifications, or Documentation Changes indicated are in addition to those listed in the Intel® Pentium® and Celeron® Processor N- and J-Series (Formerly Apollo Lake) Specification Update.

2.1 Codes Used in Summary Table

Stepping:

X: Erratum, Specification Change, or Clarification that applies to this stepping.

-: This erratum is fixed in listed stepping or specification change does not apply to list stepping.

Status

Doc: Document change or update that is implemented.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: This erratum has no plans to fix.

Table 4. Summary Table of Changes

Number	Replaced APLxx Erratum Number	Stepping Impacted			Status	Errata Title
		B-0[1]	B-1[1]	F-1		
N/A	APL47	X	X	-	Fixed[2]	System May Experience Inability to Boot or May Cease Operation
APLJN-01	N/A	X	X	-	Fixed[2]	Intermittent Display Flicker During Playback of NV12 Pixel Format Video.
APLJN-02	APL34	X	X	-	Fixed[2]	Deasserting PCICMD_PCISTS.BME Before Stopping ISP Camera Driver May Lead to a System Hang
APLJN-03	APL55	N/A[3]		X	No Fix	I2C Specification Hold Time May be Violated for PMIC I2C TX_HOLD
APLJN-04	N/A	-	-	X	No Fix	Unexpected #PF, #GP, #UD, or Other Unpredictable System Behavior May Occur

NOTES:

1. Only Intel® Pentium® processor N4200 and Intel® Celeron® processors J3355, J3455 & N3350 in Internet of Things platforms are available for this stepping.
2. The fix is only for Intel® Pentium® processor N4200 and Intel® Celeron® processors J3355, J3455 & N3350 for Internet of Things Platforms.
3. This erratum is only applicable to F1-stepping processors. For all other steppings, refer to erratum APL55 in the Intel® Pentium® and Celeron® Processor N- and J- Series Specification Update (Document number: 334820)

§

3.0 Identification Information

The processor stepping is identified in the contents of the following registers:

Table 5. Component Identification via Programming Interface

Reserved	Extended Family[1]	Extended Model[2]	Reserved	Processor Type[3]	Family Code[4]	Model Number[5]	Stepping ID[6]
31:28	27:20	19:16	15:13	12	11:8	7:4	3:0
0000b	0000000b	0101b	000b	0b	0110b	1100b	1000b (A0) 1001b (Bx) 1010b (F1)

NOTES:

1. The Extended Family, bits [27:20] are used in conjunction with the Family Code, specified in bits [11:8], to indicate whether the processor belongs to the Intel 386®, Intel 486®, Pentium®, Pentium Pro, Pentium 4, or Intel Core processor family.
2. The Extended Model, bits [19:16] in conjunction with the model number, specified in bits [7:4], are used to identify the model of the processor within the processor family.
3. The processor Type, specified in bits [13:12] indicates whether the processor is an original OEM processor, an Over Drive processor, or a dual processor (capable of being used in a dual processor system).
4. The Family Code corresponds to bits [11:8] of the EDX register after RESET, bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
5. The Model Number corresponds to bits [7:4] of the EDX register after RESET, bits [7:4] of the EAX register after the CPUID instruction is executed with 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
6. The Stepping ID in bits [3:0] indicates the revision number of that model.

When EAX is initialized to a value of 1, the CPUID instruction returns the Extended Family, Extended Model, Type, Family, Model, and Stepping values in the EAX register.

Note: EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Table 6. Processor Identification by Register Contents

Processor Line	Stepping	Vendor ID[1]	Host Device ID[2]	Graphics Device ID[3]	Revision ID[4]
Intel® Pentium® Processor Series and Intel® Celeron® Processor Series	B-0	8086	5AF0	Intel® Pentium® Processor: 0x5A84 Intel® Celeron® Processor: 0x5A85	0x0A
Processor Line	**Stepping**	**Vendor ID[1]**	**Host Device ID[2]**	**Graphics Device ID[3]**	**Revision ID[4]**
Intel® Pentium® Processor Series and Intel® Celeron® Processor Series	B-1	8086	5AF0	Intel® Pentium® Processor: 0x5A84 Intel® Celeron® Processor: 0x5A85	0x0B
Intel® Pentium® Processor Series and Intel® Celeron® Processor Series	F-1	8086	5AF0	Intel® Pentium® Processor: 0x5A84 Intel® Celeron® Processor: 0x5A85	0x0D

NOTES:

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register at offset 00h–01h in the PCI function 0 configuration space.
2. The Host Device ID corresponds to bits 15:0 of the Device ID Register at Device 0 offset 02h– 03h in the PCI function 0 configuration space.
3. The Processor Graphics Device ID (DID2) corresponds to bits 15:0 of the Device ID Register at Device 2 offset 02h–03h in the PCI function 0 configuration space.
4. The Revision Number corresponds to bits 7:0 of the Revision ID Register at offset 08h in the PCI function 0 configuration space.

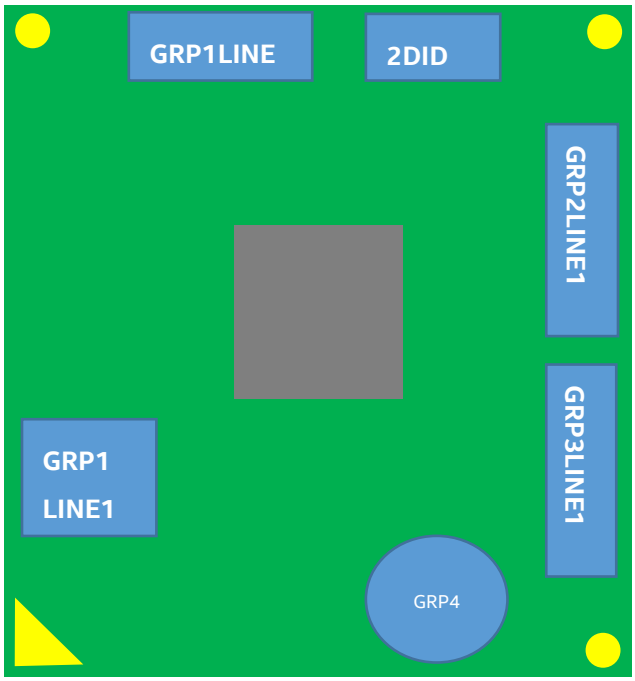
Table 7. Identification Table

S-Spec Number/ QDF	No of Cores	Processor Number	CPUID	Step-ping	Maximum Core Speed	Package	Maximum Integrated Memory Controller Frequency (MT/s)
SR2Y9	4	Pentium® N4200	0x000506C9	B-0	2.5 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)
SR2YB	2	Celeron® N3350	0x000506C9	B-0	2.4 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)
SR2Z9	4	Celeron® J3455	0x000506C9	B-1	2.3 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4
SR2Z8	2	Celeron® J3355	0x000506C9	B-1	2.5 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)
SR2Y9	4	Pentium® N4200	0x000506C9	B-1	2.5 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4
SR2YB	2	Celeron® N3350	0x000506C9	B-1	2.4 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)
S RGVZ/ QTC9	4	Pentium® N4200	0x000506CA	F-1	2.5 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)
S REKH/ QQWL	2	Celeron® N3350	0x000506CA	F-1	2.4 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)
S REKJ/ QQWM	2	Celeron® J3355	0x000506CA	F-1	2.5 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)
S REKK/ QQWN	4	Celeron® J3455	0x000506CA	F-1	2.3 GHz	FCBGA1296, 31x24mm	1866 (DDR3L non-ECC) 1866 (LPDDR3) 2400 (LPDDR4)

4.0 Component Marking Information

Processor shipments are identified by the following component markings and example pictures.

Figure 1. Processor Family Top-Side Markings



SAMPLE MARKING INFORMATION:
GRP1LINE: SN345
GRP1LINE1: swirl
GRP2LINE1: FPO45678
GRP3LINE1: SSPEC
GRP4LINE1: {eX}

§

5.0 Errata

5.1 APL47 System May Experience Inability to Boot or May Cease Operation or Nonfunctioning of LPC, SD card and RTC Circuitry

Problem:	Under certain conditions LPC, SD card and RTC circuitry may stop functioning in the outer years of use.
Implication:	Systems experiencing the LPC circuitry issue may cause operation to cease or inability to boot. Systems experiencing the RTC issue may exhibit an inability to boot or may cease operation. Systems experiencing SD card circuitry issue may cause SD cards to be unrecognized. Intel has only observed this behavior in simulation. Designs that implement the LPC interface at 1.8V signal voltage are not affected by the LPC issue. Systems designed with a coin cell battery are not affected by the RTC issue.
Workaround:	Firmware code changes have been identified and may be implemented as a mitigation for this erratum.
Status:	With these workarounds applied, Intel expects the processors to meet Intel Quality goals.

5.2 APLJN-01 Intermittent Display Flicker during Playback of NV12 Pixel Format Video

Problem:	When playing NV12 pixel format video, display buffer underruns may occur.
Implication:	When playing NV12 pixel format video, intermittent display flicker may be seen.
Workaround:	None.
Status:	For the steppings affected, Summary Tables of Changes

5.3 APLJN-02 Deasserting PCICMD_PCISTS.BME Before Stopping ISP Camera Driver May Lead to a System Hang

Problem:	If PCICMD_PCISTS.BME (Bus configured by BIOS: Device: 3; Function: 0; Offset: 4h; Bit 2) is deasserted without first stopping the ISP camera driver, the system may hang.
Implication:	If the PCICMD_PCISTS.BME register bit in the ISP is deasserted, while the ISP is processing a data stream, the system may hang.
Workaround:	Software should not deassert BME without first stopping the ISP camera driver.
Status:	For the steppings affected, Summary Tables of Changes.

5.4 APLJN-03 I2C Specification Hold Time May be Violated for PMIC I2C TX_HOLD

Problem:	PMIC I2C TX_HOLD time may not meet the I2C Fast Mode Plus (Fm+) specification minimum hold time of 260ns.
Implication:	The I2C Fast Mode Plus (Fm+) TX_HOLD time specification may not be met.
Workaround:	It is possible for a BIOS update to contain a workaround for this erratum.
Status:	For the steppings affected, Summary Tables of Changes.

NOTES:

1. This erratum is only applicable to F1-stepping processors. For all other steppings, refer to erratum APL55 in the Intel® Pentium® and Celeron® Processor N- and J- Series Specification Update (Document number: 334820)

5.5 APLJN-04 Unexpected #PF, #GP, #UD, or Other Unpredictable System Behavior May Occur

Problem:	Under complex micro architectural conditions, the processor may execute incorrect instruction bytes, leading to #PF, #GP, #UD, or other unpredictable system behavior.
Implication:	Due to this erratum, the system may exhibit unpredictable behavior, including unexpected Undefined Opcode (#UD), Page Fault (#PF), or General Protection (#GP) exceptions.
Workaround:	It may be possible for BIOS to contain a workaround for this erratum.
Status:	For the steppings affected, Summary Tables of Changes.

§

6.0 Specification Changes

6.1 Datasheet Update

Table and sections below will be updated as described below. These changes are relevant only for the Intel® Pentium® processor N4200 and Intel® Celeron® processors J3355, J3455 & N3350..

6.1.1 SVID Signals Internal Weak Pull-up (1k and 2k) Removal

Table 5-55 in Datasheet Volume 1 (Document number: 334817) will be updated as described below:

Table 5-31. SVID Signal Group DC Specification (SVID_DATA, SVID_CLK, SVID_ALERT_N)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1	1.1	V	1.05V Nominal
VIH	Input High Voltage	0.6825		V	@1.05V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.3675	V	@1.05V nominal (0.35*Vcc)
VOL	Output Low Voltage		0.45	V	@3mA Load
IPAD	Pad Leakage Current	-5	5	µA	
ZDN	Driver Pull-down Impedance	15	26	Ohm	20 Ohm Nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 1.25 ns]		2.2	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 1.25 ns]		-0.31	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 2.5 ns]		2.14	V	1,2

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 2.5ns]		-0.25	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 5 ns]		2.09	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 5ns]		-0.2	V	1,2

NOTES:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US
2. Tj = 1050C

6.1.2 SVID Signals Internal Weak Pull-up (1k and 2k) Removal

Section 22.1.296 in Datasheet Volume 3 (Document number: 334819) will be updated as below:

22.1.296 Pad Configuration DW1 (PAD_CFG_DW1_SVID0_ ALERT_B) — Offset 75Ch

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings supported by the buffer. The settings for [13:10] correspond to: 0 000: none 0 100: 20k wpd 1 000: none 1 100: 20k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination All others reserved. If a reserved value is programmed, pad may malfunction. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in sw/fw in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily.

6.1.3 SVID Signals Internal Weak Pull-up (1k and 2k) Removal

Section 22.1.298 in Datasheet Volume 3 (Document number: 334819) will be updated as below:

22.1.298 Pad Configuration DW1 (PAD_CFG_DW1_SVID0_DATA) — Offset 764h

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings supported by the buffer. The settings for [13:10] correspond to: 0 000: none 0 100: 20k wpd 1 000: none 1 100: 20k wpu 1 111: (optional) Native controller selected by Pad Mode controls the Termination All others reserved. If a reserved value is programmed, pad may malfunction. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in sw/fw in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, wpu/wpd settings should be programmed first to ensure the input does not float momentarily.

6.1.4 Package Information

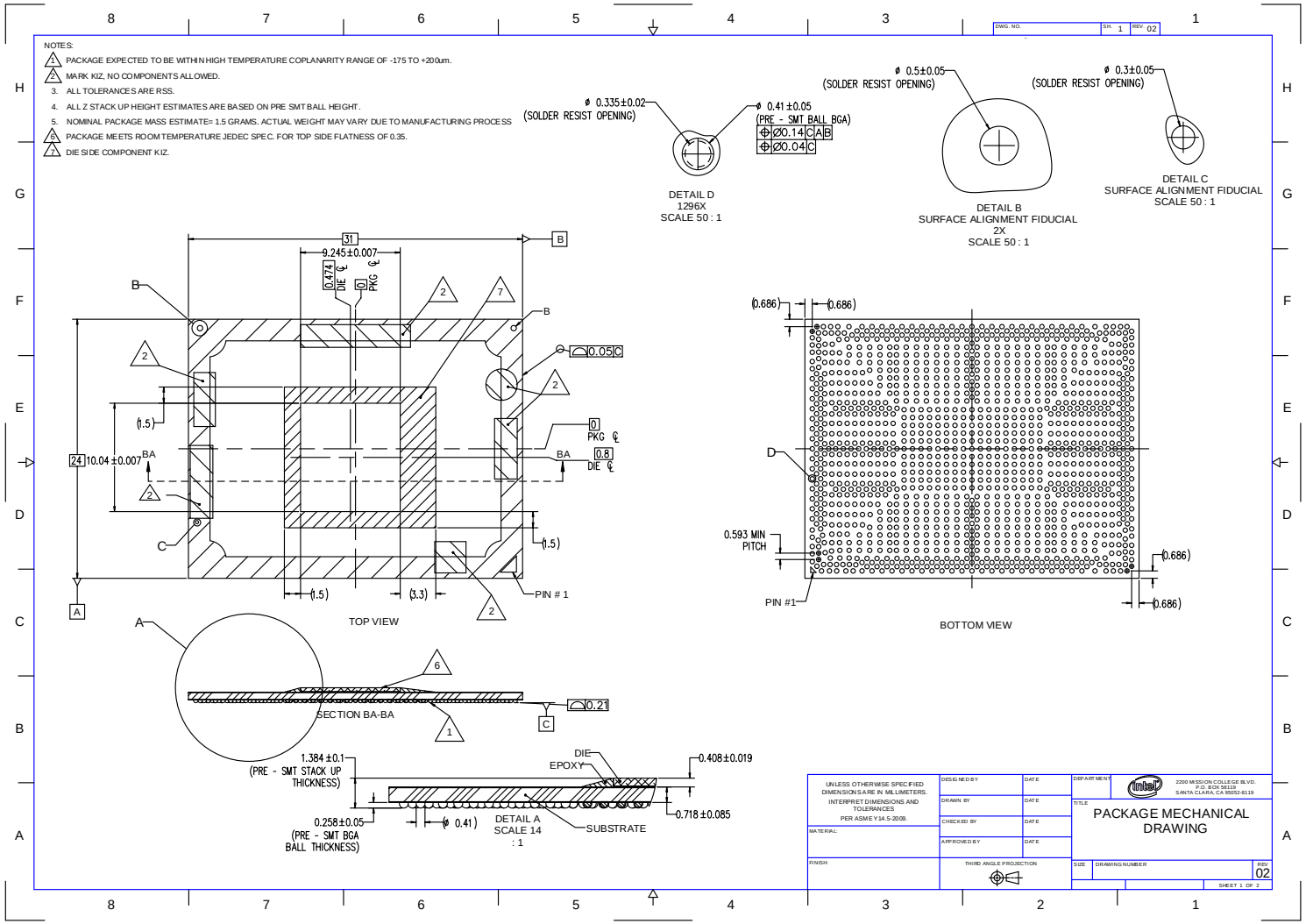
6.1.4.1 Package Attributes

For the Intel® Pentium® processor N4200 and Intel® Celeron® processors J3355, J3455 & N3350, Table 7-1 in Datasheet Volume 1 (Document number: 334817) is updated as described below:

Category	SoC
Z-height	1.384 mm ± 0.1

6.1.4.2 Package Diagrams

For the Intel® Pentium® processor N4200 and Intel® Celeron® processors J3355, J3455 & N3350, Figure 7-1 in EDS Volume 1 (Document number: 334817) is updated as described below:


NOTES:
1. PACKAGE EXPECTED TO BE WITHIN HIGH TEMPERATURE COPLANARITY RANGE OF -175 TO +200um.
2. MARK KIZ, NO COMPONENTS ALLOWED.
3. ALL TOLERANCES ARE RSS.
4. ALL Z STACK UP HEIGHT ESTIMATES ARE BASED ON PRE SMT BALL HEIGHT.
5. NOMINAL PACKAGE MASS ESTIMATE= 1.5 GRAMS. ACTUAL WEIGHT MAY VARY DUE TO MANUFACTURING PROCESS
6. PACKAGE MEETS ROOM TEMPERATURE JEDEC SPEC. FOR TOP SIDE FLATNESS OF 0.35.
7. DIE SIDE COMPONENT KIZ.
DETAIL D
1296X
SCALE 50 : 1
DETAIL B
SURFACE ALIGNMENT FIDUCIAL
2X
SCALE 50 : 1
DETAIL C
SURFACE ALIGNMENT FIDUCIAL
SCALE 50 : 1
TOP VIEW
BOTTOM VIEW
SECTION BA-BA
DETAIL A
SCALE 14
: 1
SUBSTRATE
DIE
EPOXY
PIN # 1
PIN #1
PACKAGE MECHANICAL
DRAWING

7.0 Specification Clarifications

There are no specification clarifications in this revision of the Specification Update.

§

8.0 Documentation Changes

There are no documentation changes in this revision of the Specification Update.

§