Intel® Pentium® Silver and Intel® Celeron® Processors

Datasheet Volume 1 of 2

Revision 005

July 2021

Document Number: 336560

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Revision History

Document Number	Revision Number	Description	Revision Date
336560	001	Initial Release	February 2018
336560	002	• Updated GPIO table with default PU and ISH GPIOs • Added QDP DRAM Package Support in Table 3-2 • Updated Table 3-25 • Updated Table 5-2	April 2019
336560	003	• Updated Table 5-2	September 2019
336560	004	• Updated Table 3-2 • Updated Table 3-4 • Replaced Hammock Harbor with 'Time-Synchronization Support'.	April 2020
336560	005	• Added Section 3.2.1.5 System Memory Timing Support	July 2021

1 Introduction

Intel® Pentium® Silver and Intel® Celeron® Processors is the Intel® Architecture (IA) SoC that integrates the next generation Intel processor Atom® Core, Graphics, Memory Controller, and I/O interfaces into a single System-on-Chip (SoC) solution.

Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Throughout this document Intel® Pentium® Silver and Intel® Celeron® Processors is referred as **SoC**.

Throughout this document Intel® Pentium® Silver and Intel® Celeron® Processors families refer to:

- Intel® Pentium® Silver N5000
- Intel® Pentium® Silver J5005
- Intel® Celeron® N4000 and N4100
- Intel® Celeron® J4105 and J4005

1.1 SoC Features

Table 1-1. SoC Features (Sheet 1 of 3)

Interface	Category	SoC
CPU	Number of Cores	2[1]/4
	Burst Speed	Dependent on number of active cores and CPU SKU
	LFM/HFM	800MHz/1.1-2GHz
Package	Type	24x25 mm 8L Type-3
	I/O count	616
	Pin count	1090
	Minimum Ball pitch	0.546 mm
	Z-height	1.344 mm +/-0.092
Graphics	Gen	Gen9LP
	Frequency	Up to 800 MHz
	Execution Units	12/18

Table 1-1. SoC Features (Sheet 2 of 3)

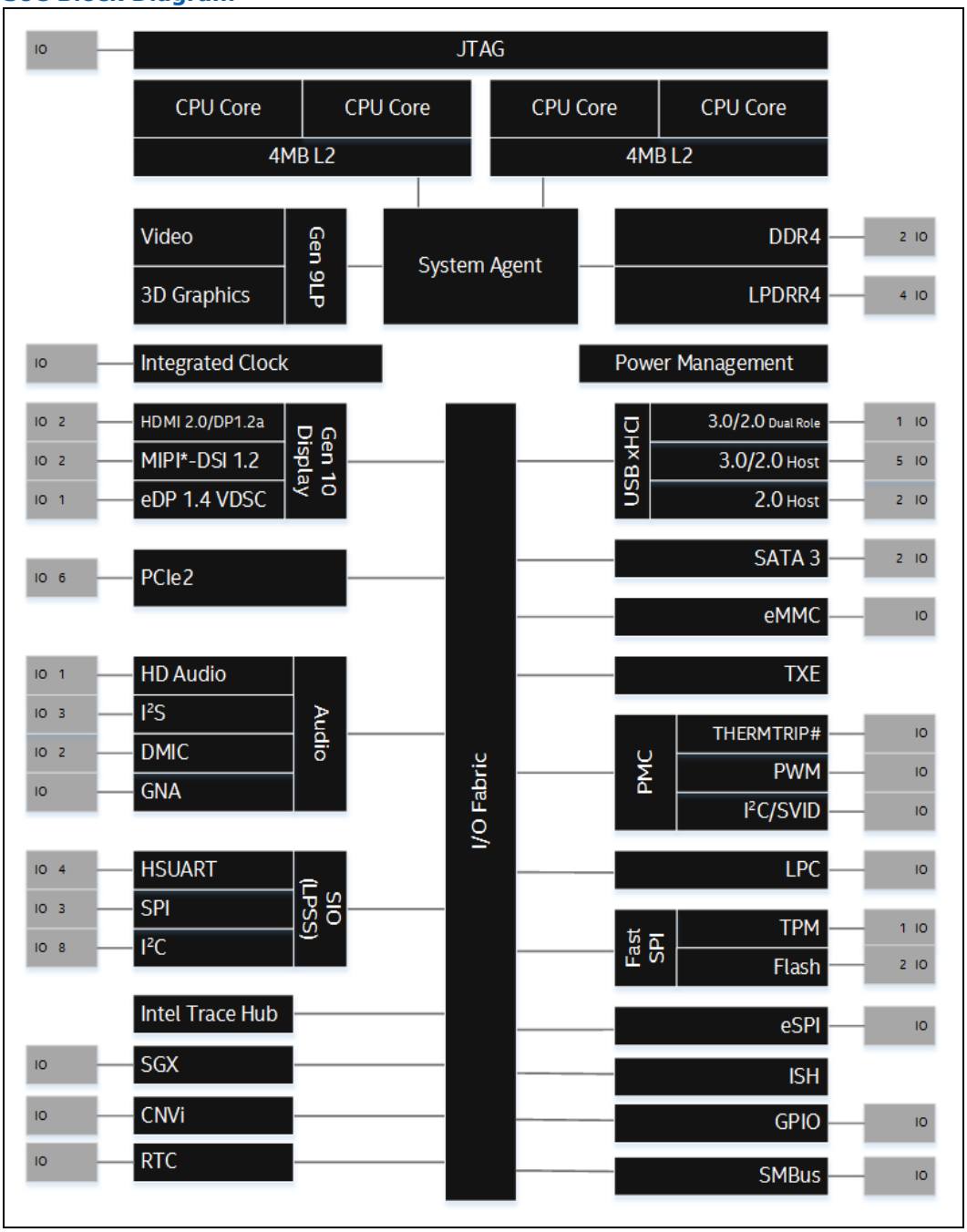
Interface	Category	SoC
Display	Gen	Gen10
	MIPI*-DSI ports	2x4 supported (DSI1.2 1G)
	Max MIPI*-DSI Resolution	1920x1080 @ 60 Hz (1 x 4) (No Compression) 2560x1600 @ 60 Hz (2 x 4) (No compression)
	Maximum DSI Data rate	1.0 Gb/s
	DDI ports (external)	2x (DP1.2a and HDMI 2.0a)
	Maximum DDI (external) Resolution	DP1.2a: Upto 4096×2160 @ 60 Hz 24bpp HDMI2.0a: Upto 4096x2160 @ 60 Hz 24bpp
	eDP* ports	1 (x4 eDP 1.4)
	Maximum eDP* Resolution	Up to 4096×2160 @ 60 Hz 24bpp
	Maximum DDI Data Rate	5.4 Gb/s (DP/eDP) 5.94 Gb/s (HDMI)
Memory	Interface	2 x 64b DDR4(non-ECC) 4 x 32b LPDDR4
	Supported transfer data rates (MT/s)	DDR4 and LPDDR4: up to 2400
Audio	Number of Ports	3x I2S 4x DMIC 1x HD Audio (HDA/mHDA Codec)
	Hardware acceleration	GNA (hardware speech acceleration)
	Maximum I2S Speed	Master Clock: 19.2 MHz, Bit Clock: 12.288 MHz
USB	USB 3.0 SuperSpeed Port	6 (2 dedicated port[1x Dual Role], 3x multiplexed with PCIe* 2.0, 1x multiplexed with SATA 3.0)
	Maximum USB 3.0 Speed	5Gb/s
	USB 2.0 Ports	8 (1x USB dual role, 7x Host)
	Maximum USB 2.0 Speed	480Mb/s
PCIe* Gen2	Ports	Up to 4 Device Clocks 6 Lanes (3x dedicated lanes and 3x multiplexed with USB 3.0) x1, x2, x4
	Maximum Speed	5.0GT/s
SATA Gen3	Ports	2
	Maximum Speed	Gen 3 (6.0Gb/s)
Storage	eMMC*	5.1/5.0 (HS400 DDR Mode) 4.5 (HS200 SDR Mode)
	Maximum eMMC* speed	HS400 @ 400MB/s HS200 @ 200MB/s

Table 1-1. SoC Features (Sheet 3 of 3)

Interface	Category	SoC
SIO	I2C Ports	8 ***Note:*** Third Party NFC is supported on this interface
	Maximum I2C Maximum Speed	3.4 Mb/s [1.8V mode] 1 Mb/s [3.3V Mode]
	HSUART	4[2]
	Maximum HSUART speed	115.200kb/s (standard 16550) 3.6864Mb/s (high-speed 16750)
	SPI	Controller: 2 Device supported: 1
	Maximum SPI Speed	25Mb/s
ISH	Gen	4.0
	I2C	3(Sensors)
	UART	3(Sensors)
	SPI	2(Sensors)
	GPIO	25Mb/s
iLB	Fast SPI	Controller: 1 Devices supported: 4 (2 for Flash, 1 for TPM, 1 for Touch) (FST_SPI supports up to 3 loads) eSPI=50MHz
	Maximum Fast SPI Frequency	FST SPI = 50 MHz
PMC	I2C (PMIC)	1
	Maximum I2C speed	3.4Mb/s
LPC	Ports	1 Port, Devices Supported: 2 (EC + dTPM)
	Maximum Speed	25 MHz
SMBus	Ports	1
	Maximum Speed	100 KHz
Security	Intel® Trusted Execution Engine (Intel® TXE) 3.0	AACS (alternate seed scramble reset for eDP display authentication support), HDCP 2.2 decryption, secure boot from eMMC*/SPI.
	SGX	Software Guard Extensions or secure enclaves SGX 2.0
Connectivity	Wi-Fi	Integrated CNVi, 1x1/2x2 802.11-abgn/acR2/80MHz/160MHz/ MU/MIMO or discrete solution using PCIe
	BT*	Integrated CNVi BT 5.0 or discrete solution using USB

Notes:
1. For a Dual Core SKU, core0 and core1 are enabled.
2. When CNVi is enabled, 2 ports of HSUART are unavailable.

Figure 1-1. SoC Block Diagram



1.2 Terminology

Term	Description
AACS	Advanced Access Content System
ACPI	Advanced Configuration and Power Interface

Term	Description
AHCI	Advanced Host Controller Interface
CCI	Camera Control Interface
CCM	Closely Coupled Memory
CFIO	Configurable In/Out
CMOS	Complementary MOS
Cold Reset	Full reset is when PWROK is de-asserted and all system rails except VCCRTC are powered down
CRU	Clock Reset Unit
CSE	Converged Security Engine ***Note:*** This is the same as TXE3.0 - Trusted Execution Technology.
CSI	Camera Serial Interface
DE	Display Engine
DMIC	Digital Microphone
DnX	Download and Execute
DP*	DisplayPort*
DTS	Digital Thermal Sensor
DVS	Descriptive Video Services
eDP*	embedded DisplayPort*
EIOB	Electronic In/Out Board
EMI	Electromagnetic Interference
eMMC*	embedded Multi Media Card
GMM	Gaussian Mixture Model
HDCP	High-Bandwidth Digital Content Protection
HDMI*	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video and multi-channel digital audio on a single cable. HDMI transmits all Advanced Television Systems Committee (ATSC) HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details are available at http://www.hdmi.org/)
HPET	High Precision Event Timer
HSMV	High Speed Medium Voltage
IGD	Internal Graphics Unit
Intel® TXE	Intel® Trusted Execution Engine 3.0 ***Note:*** This is also called CSE - Converged Security Engine.
IPC	Inter-Processor Communication
ISH	Integrated Sensor Hub
ISP	Image Signal Processor
LCD	Liquid Crystal Display
LPC	Low Pin Count
LPDDR	Low Power Dual Data Rate memory technology
LPE	Low Power Engine
LSMV	Low Speed Medium Voltage
MIPI*-CSI	MIPI*-Camera Interface Specification
MIPI*-DSI	MIPI*-Display Interface Specification

Term	Description
MPEG	Motion Picture Experts Group
MPO	Multi Plane Overlay
MSHV	Medium Speed High Voltage
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands
MSR	Model Specific Register, as the name implies, is model-specific and may change from processor model number (n) to processor model number (n+1). An MSR is accessed by setting ECX to the register number and executing either the RDMSR or WRMSR instruction. The RDMSR instruction will place the 64-bits of the MSR in the EDX: EAX register pair. The WRMSR writes the contents of the EDX: EAX register pair into the MSR
PCIe*	PCI Express*
PMC	Power Management Controller
PMU	Power Management Unit
PSP	Programmable Serial Protocol
Rank	A unit of DRAM corresponding to the set of SDRAM devices that are accessed in parallel for a given transaction. For a 64-bit wide data bus using 8-bit (x8) wide SDRAM devices, a rank would be eight devices. Multiple ranks can be added to increase capacity without widening the data bus, at the cost of additional electrical loading
RTC	Real Time Clock
SATA	Serial ATA
SCI	System Control Interrupt—SCI is used in the ACPI protocol.
SDRAM	Synchronous Dynamic Random Access Memory
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.
SIO (LPSS)	Serial I/O (also called LPSS—Low Power Sub System)
SMBus	System Management Bus
SMC	System Management Controller or External Controller refers to a separate system management controller that handles reset sequences, sleep state transitions, and other system management tasks
SMI	System Management Interrupt is used to indicate various system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity)
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Protocol
TMDS	Transition-Minimized Differential Signaling. TMDS is a serial signaling interface used in HDMI to send visual data to display. TMDS is based on low-voltage differential signaling with 8/10b encoding for DC balancing
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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2 Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and the small size of the package, some interfaces share their pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.

2.1 PCI Device ID

Table 2-1. PCI Configuration Matrix (Sheet 1 of 2)

Device ID	Device Description	Device	Function	Comments
0x31F0	Host Bridge	0	0	
0x318C	DPTF	0	1	
0x3190	GNA	0	3	
0x3184	Graphics and Display controller	2	0	
0x31DC	CNVi	12	0	
0x3192	Primary to SideBand Bridge	13	0	
0x3194	PMC (Power Management Controller)	13	1	
0x3196	Fast SPI	13	2	
0x31EC	Shared SRAM	13	3	
0x3198	High Definition Audio	14	0	
0x31A2	Integrated Sensor Hub (ISH)	17	0	
0x31E3	SATA	18	0	
0x31D8	PCIe* x4	19	0	
0x31D9	PCIe* x4	19	1	
0x31DA	PCIe* x4	19	2	
0x31DB	PCIe* x4	19	3	
0x31D6	PCIe* x2	20	0	
0x31D7	PCIe* x2	20	1	
0x31A8	USB-Host (xHCI)	21	0	
0x31AA	USB-Device (xDCI)	21	1	
0x31AC	I^2C 0	22	0	SIO
0x31AE	I^2C 1	22	1	SIO
0x31B0	I^2C 2	22	2	SIO
0x31B2	I^2C 3	22	3	SIO
0x31B4	I^2C 4	23	0	SIO
0x31B6	I^2C 5	23	1	SIO
0x31B8	I^2C 6	23	2	SIO
0x31BA	I^2C 7	23	3	SIO

Table 2-1. PCI Configuration Matrix (Sheet 2 of 2)

Device ID	Device Description	Device	Function	Comments
0x31BC	UART 0	24	0	SIO
0x31C0	UART 2	24	2	SIO
0x31C2	SPI 0	25	0	SIO
0x31CC	eMMC	28	0	
0x31E8	LPC	31	0	
0x3197	eSPI	31	0	
0x31D4	SMBUS	31	1	

2.2 Power Bus Definitions

Table 2-2. Power Bus Definitions

Power Type	Voltage Range (V)	Tolerance	Power Well Description	Power System States		
				On in S0iX	On in S3	On in S4/S5
VCC_VCG	0.45–1.45	+/- 35mV	Variable voltage supply to CPU and Graphics Core	No	No	No
VNN	0.45–1.45	+/- 50mV	Variable voltage supply to other (non core) logic	No	No	No
VCCRAM_1P05	1.05	+/- 5%	Fixed voltage rail for Internal Logic	No	No	No
VCC_1P05_INT	1.05	+/- 5%	Fixed voltage rail for Internal Logic	No	No	No
VDD2_1P2_CPU	1.2	+/- 5%	Fixed voltage rail for SoC L2	Yes	Yes	Yes
VDD2_1P2_AUD_ISH	1.2	+/- 5%	Fixed voltage rail for Audio and ISH I/O Logic	Yes	Yes	Yes
VDD2_1P2_MPHY	1.2	+/- 5%	Fixed voltage rail for MPHY Logic	Yes	Yes	Yes
VDD2_1P2_USB2	1.2	+/- 5%	Fixed voltage rail for USB2 I/O	Yes	Yes	Yes
VDD2_1P2_DSI_CSI	1.2	+/- 5%	Fixed voltage rail for MIPI* I/Os	Yes	Yes	Yes
VDD2_1P2_PLL	1.2	+/- 5%	Fixed voltage rail for PLLs	Yes	Yes	Yes
VCC_1P8V_A	1.8	+/- 5%	Fixed voltage rail for all GPIOs	Yes	Yes	Yes
VCC_3P3V_A	3.3	+/- 5%	Fixed voltage rail for GPIO, I/O logic, and USB2 PHY	Yes	Yes	Yes
VDDQ	1.2	+/- 5%	Fixed voltage rail for DDR4 IO	Yes	Yes	No
	1.1	+/- 5%	Fixed voltage rail for LPDDR4 IO	Yes	Yes	No
VCCRTC_3P3V	3.3	+/- 5%	Fixed Voltage rail for RTC (Real Time Clock)	Yes	Yes	Yes

2.3 Memory Interface Signals

2.3.1 DDR4 Interface Signals

Table 2-3. DDR4 System Memory Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
MEM_CH0/CH1_DQ[63:0]	I/O	VDDQ	**Data Buses:** Data signals interface to the SDRAM data buses.
MEM_CH0/CH1_DQSP[7:0] MEM_CH0/CH1_DQSN[7:0]	I/O	VDDQ	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.
MEM_CH0/CH1_CLKP[1:0] MEM_CH0/CH1_CLKN[1:0]	I/O	VDDQ	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of MEM_CH0/CH1_CLKP and the negative edge of their complement MEM_CH0/CH1_CLKN are used to sample the command and control signals on the SDRAM.
MEM_CH0/CH1_CKE[1:0]	I	VDDQ	**Clock Enable:** (1 per Rank). These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).
MEM_CH0/CH1_CS[1:0]_N	I	VDDQ	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
MEM_CH0/CH1_ODT[1:0]	I	VDDQ	**On Die Termination:** (1 per rank). Active SDRAM Termination Control.
MEM_CH0/CH1_MA[16:0]	I	VDDQ	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. • A10 is sampled during Read/Write commands to determine whether Auto pre-charge should be performed to the accessed bank after the Read/Write operation. HIGH: Auto pre-charge LOW: No Auto pre-charge • A10 is sampled during a Pre-charge command to determine whether the Pre-charge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be pre-charged, the bank is selected by bank addresses. • A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH: No burst chop
MEM_CH0_BA[1:0] MEM_CH1_BA[1:0]	I	VDDQ	**Bank Select:** These signals define which banks are selected within each SDRAM rank.
MEM_CH0_BG[1:0] MEM_CH1_BG[1:0]	I	VDDQ	**Bank Group:** These signals define which bank group is selected within each SDRAM rank.
MEM_CH0_ACT_N MEM_CH1_ACT_N	I	VDDQ	**Activation Command Input:** When asserted, the following command signals change function to be address signals MA[16:14]: MA16, MA15 and WE_N/MA14.
MEM_CH0_VREFCA MEM_CH1_VREFCA	I	VDDQ	Memory Reference Voltage for Command and Address.
MEM_CH0_VREFDQ MEM_CH1_VREFDQ	I	VDDQ	**Memory Reference Voltage for DQ**
MEM_CH0_RESET_N MEM_CH1_RESET_N	I	VDDQ	**Channel Reset Signal**

Table 2-3. DDR4 System Memory Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
MEM_CH0_WE_N MEM_CH1_WE_N	I	VDDQ	**Wake Enable signals** ***Note:*** When ACT_N is asserted, this signal changes function to be address signal MA14.
MEM_CH0_RCOMP MEM_CH1_RCOMP	N/A	VDDQ	**Channel Compensation**

2.4 LPDDR4 Interface Signals

Table 2-4. LPDDR4 System Memory Signals

Signal Name	Dir.	I/O Voltage	Description
MEM_CH0/CH1_DQA[31:0] MEM_CH0/CH1_DQB[31:0]	I/O	VDDQ	**Data Buses:** Data signals interface to the SDRAM data buses.
MEM_CH0/CH1_DQSA[3:0]_P/N MEM_CH0/CH1_DQSB[3:0]_P/N	I/O	VDDQ	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.
MEM_CH0_CLKA/B_P/N MEM_CH1_CLKA/B_P/N	I/O	VDDQ	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of MEM_CH0/CH1_CLKP and the negative edge of their complement MEM_CH0/CH1_CLKN are used to sample the command and control signals on the SDRAM.
MEM_CH0/CH1_CKE[1:0]A MEM_CH0/CH1_CKE[1:0]B	I	VDDQ	**Clock Enable:** (1 per rank) These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR.
MEM_CH0/CH1_CS[1:0]A MEM_CH0/CH1_CS[1:0]B	I	VDDQ	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
MEM_CH0/CH1_CAA[5:0]	I/O	VDDQ	**Command Address:** These signals are used to provide the multiplexed command and address to the SDRAM.
MEM_CH0/CH1_CAB[5:0]	I/O	VDDQ	**Command Address:** These signals are used to provide the multiplexed command and address to the SDRAM.
MEM_CH0_RCOMP MEM_CH1_RCOMP	N/A	VDDQ	**Channel Compensation**
MEM_CH0/CH1_RESET_N	I	VDDQ	**Channel Reset:** This signal is used to reset the individual channels.

2.5 Display—Digital Display Interface (DDI) Signals

Table 2-5. Digital Display Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
DDI0_TXP[3:0]	O	V1P05	Port 0: Transmit Signals for DP/HDMI
DDI0_TXN[3:0]	O	V1P05	Port 0: Transmit Complement Signals for DP/HDMI

Table 2-5. Digital Display Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
DDI0_AUXP	I/O	V1P05	Port 0: Display Port Auxiliary Channel for DP
DDI0_AUXN	I/O	V1P05	Port 0: Display Port Auxiliary Channel Complement for DP
DDI0_DDC_SCL[1]	I/O	V1P8/V3P3	Port 0: I^2C Clock for HDMI
DDI0_DDC_SDA[1]	I/O	V1P8/V3P3	Port 0: I^2C Data for HDMI
DDI1_TXP[3:0]	O	V1P05	Port 1: Transmit Signals for DP/HDMI
DDI1_TXN[3:0]	O	V1P05	Port 1: Transmit Complement Signals for DP/HDMI
DDI1_AUXP	I/O	V1P05	Port 1: Display Port Auxiliary Channel for DP
DDI1_AUXN	I/O	V1P05	Port 1: Display Port Auxiliary Channel Complement for DP
DDI1_DDC_SCL[1]	I/O	V1P8/V3P3	Port 1: I^2C Clock for HDMI*
DDI1_DDC_SDA[1]	I/O	V1P8/V3P3	Port 1: I^2C Data for HDMI*
EDP_TXP[3:0]	O	V1P05	Transmit Signals for eDP*
EDP_TXN[3:0]	O	V1P05	Transmit Complement Signals for eDP*
EDP_AUXP	I/O	V1P05	Display Port Auxiliary Channel for eDP*
EDP_AUXN	I/O	V1P05	Display Port Auxiliary Channel Complement for eDP*
EDP_RCOMP_P/N	I/O	V1P05	This signal is used for pre-driver slew rate compensation
PNL[0,1]_BKLTCTL[1]	O	V1P8/V3P3	Panel Backlight Brightness Control (for eDP*/MDSI)
PNL[0,1]_BKLTEN[1]	O	V1P8/V3P3	Panel Backlight Enable (for eDP*/MDSI)
PNL[0,1]_VDDEN1[1]	O	V1P8/V3P3	Panel Power Enable (for eDP*/MDSI)
DDI[2:0]_HPD[1]	I	V1P8/V3P3	Digital Display Interface Hot-Plug Detect. ***Notes:*** 1. These are multiplexed signals and need to be enabled through GPIO programming. 2. DDI2 is a dedicated eDP* port. 3. A logic inversion circuit with a mandatory pull up resistor is required on the platform.
Note: 1. I/O Voltage is controlled by Soft Straps.			

2.6 MIPI*-DSI Interface Signals

Table 2-6. MIPI*-DSI Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
MDSI_A_CLKN	O	V1P244	MIPI* Clock output for pipe A
MDSI_A_CLKP	O	V1P24	MIPI* Clock complement output for pipe A
MDSI_A_DN[3:0]	I/O	V1P24	MIPI* Data Lane 3:0 for Pipe A
MDSI_A_DP[3:0]	I/O	V1P24	MIPI* Data Lane 3:0 complement for Pipe A
MDSI_C_CLKN	O	V1P24	MIPI* Clock output for pipe C
MDSI_C_CLKP	O	V1P24	MIPI* Clock complement output for pipe C
MDSI_C_DN[3:0]	I/O	V1P24	MIPI* Data Lane 3:0 for Pipe C
MDSI_C_DP[3:0]	I/O	V1P24	MIPI* Data Lane 3:0 complement for Pipe C
MDSI_RCOMP	I/O	V1P24	This signal is used for pre-driver slew rate compensation. An external precision resistor of 150 Ω ±1% should be connected between MDSI_RCOMP and GND

Table 2-6. MIPI*-DSI Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
MDSI_A_TE	I	V1P8	MIPI*-DSI tearing effect signal (Port A)
MDSI_C_TE	I	V1P8	MIPI*-DSI tearing effect signal (Port C)
MIPI_I^{2}C_SDA	I/O	V1P8	I^{2}C Serial Data for MIPI* Port
MIPI_I^{2}C_SCL	I/O	V1P8	I^{2}C Serial Clock for MIPI* Port

2.7 SVID Signals

Table 2-7. SVID Interface Signals

Signal Name	Dir.	I/O Voltage	Description
SVID_CLK	O, OD	V1P05/V1P8[1]	SVID Clock signal
SVID_DATA	I/O, OD	V1P05/V1P8[1]	SVID Data signal
SVID_ALERT_N	I	V1P05/V1P8[1]	SVID Alert signal
Note: 1. When used as GPIO signal.			

2.8 eMMC* Signals

Table 2-8. eMMC* Interface Signals

Signal Name	Dir.	I/O Voltage	Description
EMMC_CLK	O	V1P8	eMMC* Clock
EMMC_D[7:0]	I/O	V1P8	**eMMC Port Data bits 0 to 7:** Bi-directional port used to transfer data to and from eMMC* device.
EMMC_CMD	I/O	V1P8	**eMMC Port Command:** This signal is used for card initialization and transfer of commands.
EMMC_RST_N	O	V1P8	**eMMC Reset:** This signal is used to Reset the eMMC* Card.
EMMC_PWR_N[1]	O	V1P8/V3P3	**eMMC Power Enable**: This signal is used to power cycle the eMMC* Card.
EMMC_RCLK	I	V1P8	**eMMC Return Clock:** Return Clock/Data Strobe signal.
EMMC_RCOMP	I	V1P8	**eMMC RCOMP:** This signal is used for pre-driver slew rate compensation.
Note: 1. I/O Voltage is controlled by Hardware Strap(GPIO_168).			

2.9 System Management (SM) Bus

Table 2-9. SMBus Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
SMB_ALERT_N[1]	I/O	V1P8/V3P3	**SMBus Alert:** This signal is used to wake the system or generate SMI#. External pull-up resistor is required.
SMB_CLK[1]	I/O	V1P8/V3P3	**SMBus Clock:** External pull-up resistor is required.
SMB_DATA[1]	I/O	V1P8/P3V3	**SMBus Data:** External pull-up resistor is required.

Table 2-9. SMBus Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
Note: 1. The voltage selection is controlled by soft straps per pad. The hard strap selects the RCOMP registers for either 1.8V or 3.3V operation and should be tied to match the soft strap settings.			

2.10 USB Interface Signals

2.10.1 USB 2.0 Interface Signals

Table 2-10. USB 2.0 Interface Signals

Signal Name	Dir.	I/O Voltage	Description
USB2_DN[7:0]	I/O	V3P3	**USB2 Data:** High speed serialized data I/O.
USB2_DP[7:0]	I/O	V3P3	
USB2_RCOMP	I	V3P3	**Resistor Compensation:** This signal is used for pre-driver slew rate compensation.
USB2_DUALROLE	I/O	V1P8	**USB Dual Role:** The Signal is to identify if a Host or Device is connected to its port.
USB2_VBUS_SNS	I	V1P8	USB VBus Sense line
USB_OC[1:0]_N	I	V1P8	Used by the controller to disable I/O in case of overcurrent ***Note:*** USB_OC[1:0]_N can be individually configured for the USB ports.

2.10.2 USB 3.0 Interface Signals

Table 2-11. USB 3.0 Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
USB3_P[1:0]_TXP/N	O	V1P24	**Differential Transmitter serial data outputs (Port0 and Port1):** SuperSpeed Serialized data outputs.
USB3_P[1:0]_RXP/N	I	V1P24	**Differential Receiver serial data inputs (Port0 and Port1):** SuperSpeed serialized data inputs.
PCIE_P5_USB3_P2_TXP/N	O	V1P24	**Differential Transmitter serial data outputs (Port2):** Multiplexed PCIe*2/Super-Speed Serialized data outputs.
PCIE_P5_USB3_P2_RXP/N	I	V1P24	**Differential Receiver serial data inputs (Port2):** Multiplexed PCIE*2/SuperSpeed serialized data inputs.
PCIE_P4_USB3_P3_TXP/N	O	V1P24	**Differential Transmitter serial data outputs (Port3):** Multiplexed PCIE*2/Super-Speed Serialized data outputs.
PCIE_P4_USB3_P3_RXP/N	I	V1P24	**Differential Receiver serial data inputs (Port3):** Multiplexed PCIE*2/SuperSpeed serialized data inputs.
PCIE_P3_USB3_P4_TXP/N	O	V1P24	**Differential Transmitter serial data outputs (Port4):** Multiplexed PCIE*2/Super-Speed Serialized data outputs.

Table 2-11. USB 3.0 Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
PCIE_P3_USB3_P4_RXP/N	I	V1P24	**Differential Receiver serial data inputs (Port4):** Multiplexed PCIE*2/SuperSpeed serialized data inputs.
SATA_P1_USB3_P5_TXP/N	O	V1P24	**Differential Transmitter serial data outputs (Port5):** Multiplexed SATA3/Super-Speed Serialized data outputs.
SATA_P1_USB3_P5_RXP/N	I	V1P24	**Differential Receiver serial data inputs (Port5):** Multiplexed SATA3/SuperSpeed serialized data inputs.
PCIE2_USB3_SATA3_RCOMP_N	O	V1P24	**Resistor Compensation:** This signal is used for pre-driver slew rate compensation. This signal is common to PCI2, USB3, and SATA3 compensation.
PCIE2_USB3_SATA3_RCOMP_P	O	V1P24	

2.11 PCIe Interface Signals

Table 2-12. PCIe Gen2 Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
PCIE_P[2:0]_TXP/N	O	V1P24	**Differential Transmitter serial data outputs:** PCIE*2 data outputs. Tied to PCIe* x4 controller.
PCIE_P[2:0]_RXP/N	I	V1P24	**Differential Transmitter serial data outputs:** PCIE*2 data input. Tied to PCIe* x4 controller.
PCIE_P3_USB3_P4_TXP/N	O	V1P24	**Differential Transmitter serial data outputs:** multiplexed PCIE*2/SuperSpeed Serialized data outputs. Tied to PCIe* x4 controller.
PCIE_P3_USB3_P4_RXP/N	I	V1P24	**Differential Receiver serial data inputs:** multiplexed PCIE*2/SuperSpeed serialized data inputs. Tied to PCIe* x4 controller.
PCIE_P4_USB3_P3_TXP/N	O	V1P24	**Differential Transmitter serial data outputs:** multiplexed PCIE*2/SuperSpeed Serialized data outputs. Tied to PCIe* x2 controller.
PCIE_P4_USB3_P3_RXP/N	I	V1P24	**Differential Receiver serial data inputs:** multiplexed PCIE*2/SuperSpeed serialized data inputs. Tied to PCIe* x2 controller.
PCIE_P5_USB3_P2_TXP/N	O	V1P24	**Differential Transmitter serial data outputs:** multiplexed PCIE*2/SuperSpeed Serialized data outputs. Tied to PCIe* x2 Controller.
PCIE_P5_USB3_P2_RXP/N	I	V1P24	**Differential Receiver serial data inputs:** multiplexed PCIE*2/SuperSpeed serialized data inputs. Tied to PCIe* x2 Controller.
PCIE_CLKOUT[3:0]P/N	I/O	V1P05	PCIe* Output Clocks
PCIE_WAKE[3:0]_N[1]	I	V1P8/V3P3	PCIe* Wake Signals

Table 2-12. PCIe Gen2 Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
PCIE_CLKREQ[3:0]_N[1]	I/O	V1P8/V3P3	**PCIE Clock Request**: Used for devices that need to request one of the four output clocks. Each clock request maps to the matching clock output (for example, PCI_CLKREQ[0] maps to PCIE_CLKP/N[0]). These signals are multiplexed and may be used by other functions.
PCIE2_USB3_SATA3_RCOMP_N	O	V1P24	**Resistor Compensation:** This signal is used for pre-driver slew rate compensation. This signal is common for PCI*2, USB3 and SATA3 compensation.
PCIE2_USB3_SATA3_RCOMP_P	O	V1P24	
PCIE_REF_CLK_RCOMP	O	V1P05	**Resistor Compensation:** PCI reference clock compensation resistor signal.
Note: 1. I/O Voltage is controlled by Soft Straps.			

2.12 SATA Interface Signals

Table 2-13. SATA3 Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
SATA_P0_TXP/N	O	V1P24	**Serial ATA Differential Transmit Pair 0:** These outbound SATA Port 0 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s.
SATA_P0_RXP/N	I	V1P24	**Serial ATA Differential Receive Pair 0:** These inbound SATA Port 0 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s.
SATA_GP0[1]	I/O	V1P8/V3P3	**Serial ATA Port [0] General Purpose Inputs:** When configured as SATA_GP0, this is an input pin that issued as an interlock switch status indicator for SATA Port 0. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. ***Note:*** This is a GPIO pin.
SATA_GP1[1]	I/O	V1P8/V3P3	**Serial ATA Port [1] General Purpose Inputs:** When configured as SATA_GP1, this is an input pin that issued as an interlock switch status indicator for SATA Port 1. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. ***Note:*** This is a GPIO pin.
SATA_DEVSLP0[1]	I/O	V1P8/V3P3	**Serial ATA Port [0] Device Sleep:** This is an open-drain pin on the SoC side. SoC will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that is internal to the SATA device, per DEVSLP specification). SoC will drive pin low to signal an exit from DEVSLP state. ***Note:*** This is a GPIO pin and can be mapped to SATA Port 0.

Table 2-13. SATA3 Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
SATA_DEVLSP1[1]	I/O	V1P8/V3P3	**Serial ATA Port [1] Device Sleep:** This is an open-drain pin on the SoC side. SoC will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that is internal to the SATA device, per DEVSLP specification). SoC will drive pin low to signal an exit from DEVSLP state. Design Constraint: As per platform guidelines, no external pull-up or pull-down termination required when used as DEVSLP. ***Note:*** This is a GPIO pin. This pin can be mapped to SATA Port 1.
SATA_LED_N[1]	I/O	V1P8/V3P3	**Serial ATA LED:** This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. ***Note:*** This is a GPIO pin.
SATA_P1_USB3_P5_TXP/N	O	V1P24	**Serial ATA Differential Transmit Pair 1:** These outbound SATA Port 1 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s. The signals are multiplexed with USB3, Port 5 signals.
SATA_P1_USB3_P5_RXP/N	I	V1P24	**Serial ATA Differential Receive Pair 1:** These inbound SATA Port 1 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s. The signals are multiplexed with USB3 Port 5 signals.
PCIE2_USB3_SATA3_RCOMP_N	O	V1P24	**Compensation Resistor:** This signal is used for pre-driver slew rate compensation. ***Note:*** This signal is common for PCIe*2, USB3 and SATA3 compensation.
PCIE2_USB3_SATA3_RCOMP_P	O	V1P24	
Note: 1. I/O Voltage is controlled by Soft Straps.			

2.13 SPI NOR Interface

2.13.1 Fast Serial Peripheral Interface (SPI) Signals

Table 2-14. Fast Serial Peripheral Interface (SPI) Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
FST_SPI_MOSI_IO0	I/O	V1P8	**Fast SPI Data Pad:** Data Input/output pin for the SoC.
FST_SPI_MISO_IO1	I/O	V1P8	
FST_SPI_IO2	I/O	V1P8	
FST_SPI_IO3	I/O	V1P8	
FST_SPI_CLK	I/O	V1P8	**Fast SPI Clock:** When the bus is idle, the owner will drive the clock signal low.
FST_SPI_CS0_N	I/O	V1P8	**Fast SPI Chip Select 0:** Used as the SPI bus request signal for the first SPI Flash devices.
FST_SPI_CS1_N	I/O	V1P8	**Fast SPI Chip Select 1:** Used as the SPI bus request signal for the second SPI Flash devices.

Table 2-14. Fast Serial Peripheral Interface (SPI) Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
FST_SPI_CS2_N	I/O	V1P8	**Fast SPI Chip Select 2:** Used as the SPI bus request signal for the TPM device. ***Note:*** This is a GPIO pin
Note: These signals will be tri-stated when the SoC is in Sx state (will need RSMRST_N to be asserted).			

2.14 PMC SPI Interface Signals

Table 2-15. PMC Serial Peripheral Interface (SPI) Signals

Signal Name	Dir.	I/O Voltage	Description
PMC_SPI_FS0	O	V1P8	**SPI Debug ports**
PMC_SPI_FS1	O	V1P8	
PMC_SPI_FS2	O	V1P8	
PMC_SPI_CLK	O	V1P8	
PMC_SPI_RXD	I	V1P8	
PMC_SPI_TXD	O	V1P8	

2.15 SIO SPI (Serial Peripheral Interface) Signals

Table 2-16. SIO Serial Peripheral Interface (SPI) Signals

Signal Name	Dir.	I/O Voltage	Description
SIO_SPI_0_TXD	I/O	V1P8	**SIO SPI 0 Data Pad:** Data Input/Output pin for the SoC.
SIO_SPI_0_RXD	I/O	V1P8	
SIO_SPI_0_FS0	I/O	V1P8	**SIO SPI 0 Frame Select:** Used as the SPI bus request signal.
SIO_SPI_0_FS1	I/O	V1P8	**SIO SPI 0 Frame Select:** Used as the SPI bus request signal.
SIO_SPI_0_CLK	I/O	V1P8	**SIO SPI 0 Clock:** SPI Clock signal.
SIO_SPI_[1/2]_TXD	I/O	V1P8	**SIO SPI Data Pad:** Data Input/Output pin for the SoC. ***Note:*** This is a GPIO pin.
SIO_SPI_[1/2]_RXD	I/O	V1P8	
SIO_SPI_[1/2]_FS0	I/O	V1P8	**SIO SPI Frame Select:** Used as the SPI bus request signal. ***Note:*** This is a GPIO pin.
SIO_SPI_[1/2]_FS1	I/O	V1P8	**SIO SPI Frame Select:** Used as the SPI bus request signal. ***Note:*** This is a GPIO pin.
SIO_SPI_[1/2]_CLK	I/O	V1P8	**SIO SPI Clock:** SPI Clock signal. ***Note:*** This is a GPIO pin.

2.16 JTAG Interface Signals

Table 2-17. JTAG Interface Signals

Signal Name	Dir.	I/O Voltage	Description
JTAG_TCK	I/O	V1P8	**JTAG Test Clock:** Provides the clock input for the SoC Test Bus (also known as, Test Access Port).
JTAG_TDI	I/O	V1P8	**JTAG Test Data Input:** Transfers serial test data into the processor.
JTAG_TDO	I/O, OD	V1P8	**JTAG Test Data Output:** Transfers serial test data out of the processor.
JTAG_TMS	I/O	V1P8	**JTAG Test Mode Select:** A JTAG specification support signal used by debug tools.
JTAG_TRST_N	I/O	V1P8	**JTAG Test Reset:** Asynchronously resets the Test Access Port (TAP) logic.
JTAG_PRDY_N	I/O, OD	V1P8	**Probe Mode Ready:** SoC response to PREQ_B assertion. Indicates SoC is in probe mode.
JTAG_PREQ_N	I/O	V1P8	**Probe Mode Request:** Requests the SoC to enter probe mode. SoC will response with PRDY_B assertion once it has entered.
JTAGX	I/O	V1P8	Tap master control

2.17 Audio Interface Signals

Table 2-18. Audio Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O voltage	Description
AVS_I2S[0/1]_MCLK	I/O	V1P8	MCLK for Master Mode operation or GPIO.
AVS_I2S[0/1]_BCLK	I/O	V1P8	Analog microphone I2S Bit Clock – bi-directional. In master mode the BCLK is supplied by the SoC. In slave mode, BCLK serves as an input.
AVS_I2S[0/1]_WS_SYNC	I/O	V1P8	Word Select or SYNC input – marks the beginning of serial sample.
AVS_I2S[0/1]_SDI	I/O	V1P8	Analog microphone I2S Data in – serial data input.
AVS_I2S[0/1]_SDO	I/O	V1P8	Audio Codec I2S Data out – serial data out.
AVS_I2S2_BCLK	I/O	V1P8	Analog microphone I2S Bit Clock – bi-directional. In master mode the BCLK is supplied by the SoC, in slave mode serves as an input. ***Note:*** This is a GPIO pin.
AVS_I2S2_WS_SYNC	I/O	V1P8	Word Select or SYNC input – marks the beginning of serial sample. ***Note:*** This is a GPIO pin.
AVS_I2S2_SDI	I/O	V1P8	Analog microphone I2S Data in – serial data input. ***Note:*** This is a GPIO pin.
AVS_I2S2_SDO	I/O	V1P8	Audio Codec I2S Data out – serial data out. ***Note:*** This is a GPIO pin.

Table 2-18. Audio Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O voltage	Description
AVS_DMIC_CLK_A1	I/O	V1P8	**DMIC Clock:** Digital Microphone Clock for channel A (Voice trigger microphone).
AVS_DMIC_CLK_B1	I/O	V1P8	**DMIC Clock:** Digital Microphone Clock for channel B (Secondary microphone).
AVS_DMIC_DATA_1	I/O	V1P8	**DMIC Data:** First microphone pair data input.
AVS_DMIC_CLK_AB2	I/O	V1P8	**DMIC Clock:** Second microphone pair Clock (Common for the second pair).
AVS_DMIC_DATA_2	I/O	V1P8	**DMIC Data:** Second microphone pair Data (Common for the second pair).
AVS_HDA_BCLK	I/O	V1P8	**HD Audio Bit Clock:** Up to 24-MHz serial data clock generated by the Intel® High Definition Audio (Intel® HD Audio) controller.
AVS_HDA_WS_SYNC	I/O	V1P8	**HD Audio Word Select or SYNC:** 48 KHz fixed rate frames sync to the codec. Also used to encode the stream number.
AVS_HDA_SDI	I/O	V1P8	**HD Audio Serial Data In:** Serial TDM data input from the codec. The serial input is single-pumped for a bit rate of up to 24 Mb/s. The signal contains integrated pull-down resistors, which are enabled while the primary well is powered.
AVS_HDA_SDO	I/O	V1P8	**HD Audio Serial Data Out:** Serial TDM data output to the codecs. The serial output is double-pumped for a bit rate of up to 48 Mb/s.
AVS_HDA_RST_N	I/O	V1P8	**HD Audio Reset:** Master H/W Reset to internal/external codec.

2.18 High Speed UART Interface Signals

Table 2-19. UART Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
SIO_UART0_RXD	I/O	V1P8	UART1 data send
SIO_UART0_TXD	I/O	V1P8	UART1 data output
SIO_UART0_RTS_N	I/O	V1P8	UART1 Ready to Send
SIO_UART0_CTS_N	I/O	V1P8	UART1 Clear to Send
SIO_UART2_RXD	I/O	V1P8	UART2 data input
SIO_UART2_TXD	I/O	V1P8	UART2 data output
SIO_UART2_RTS_N	I/O	V1P8	UART2 Ready to Send
SIO_UART2_CTS_N	I/O	V1P8	UART2 Clear to Send
SIO_UART[3/1]_RXD	I/O	V1P8	UART data input ***Note:*** This is a GPIO pin.
SIO_UART[3/1]_TXD	I/O	V1P8	UART data output ***Note:*** This is a GPIO pin.
SIO_UART[3/1]_RTS_N	I/O	V1P8	UART Ready to Send ***Note:*** This is a GPIO pin.

Table 2-19. UART Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
SIO_UART[3/1]_CTS_N	I/O	V1P8	UART Clear to Send ***Note:*** This is a GPIO pin.

2.19 I²C Interface Signals

Table 2-20. I²C Interface Signals

Signal Name	Dir.	I/O Voltage	Description
SIO_I²C[4:0]_SDA	I/O	V1P8	I²C Serial Data
SIO_I²C[4:0]_SCL	I/O	V1P8	I²C Serial Clock
SIO_I²C[7:5]_SDA[1]	I/O	V1P8/V3P3	I²C Serial Data
SIO_I²C[7:5]_SCL[1]	I/O	V1P8/V3P3	I²C Serial Clock
MIPI_I²C_SDA	I/O	V1P8	I²C Serial Data for MIPI* Port
MIPI_I²C_SCL	I/O	V1P8	I²C Serial Clock for MIPI* Port
PMIC_I²C_SDA	I/O	V1P8	I²C Serial Data for PMIC
PMIC_I²C_SCL	I/O	V1P8	I²C Serial Clock for PMIC

Note:
1. I/O Voltage is controlled by Soft Straps.

2.20 Power Management Signals

Table 2-21. PM Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
PMU_BATLOW_N[1]	I/O	V1P8/V3P3	**Battery Low:** This signal indicates that there is insufficient power to boot the system. Assertion will prevent wake from S3–S5 state. This signal can also be enabled to cause an SMI# when asserted.
PMU_PLTRST_N[1]	I/O	V1P8/V3P3	**Platform Reset:** This signal is used to reset devices on the platform (such as SIO, LAN, processor, and so forth.). This signal is asserted during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O port CF9h). The SoC drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O port CF9h).
PMU_PWRBTN_N[1]	I/O	V1P8/V3P3	**Power Button:** Power button input signal. Used to wake the SoC from power button press. The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3- S4 states. This signal has an internal 16 ms de-bounce on the input.
PMU_RSTBTN_N[1]	I/O	V1P8/V3P3	**Reset Button:** Reset button input signal.
PMU_SLP_S0_N[1]	I/O	V1P8/V3P3	**S0 Sleep Control**: Controls power delivery subsystem. Asserted low in S0ix and G3 state.
PMU_SLP_S3_N[1]	I/O	V1P8/V3P3	**S3 Sleep Control:** Controls power delivery subsystem. Asserted low in S3 and lower.
PMU_SLP_S4_N[1]	I/O	V1P8/V3P3	**S4 Sleep Control**: Controls power delivery subsystem. Asserted low in S4 and lower.
PMU_SUSCLK[1]	I/O	V1P8/V3P3	**Suspend Clock:** Primary RTC clock output.

Table 2-21. PM Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
SUSCLK[1/2][2]	I/O	V1P8/V3P3	**Suspend Clock:** Primary RTC clock output. ***Note:*** This is a GPIO pin.
SUS_STAT_N[1]	I/O	V1P8/V3P3	**Suspend Status:** Asserted to indicate that the system will be entering a Sx state.
SUSPWRDNACK[1]	I/O	V1P8/V3P3	**Sus Power Down Ack:** Indicator from SoC that "always on" rails can be shut down.
SOC_PWROK	I/O	V3P3	**SoC Power OK:** When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for at least 5 ms. This signal can be driven asynchronously. Then this signal is negated, the SoC asserts PLTRST_N.
Note: 1. I/O Voltage is controlled by Hardware Strap(GPIO_168). 2. I/O Voltage is controlled by Soft Straps.			

2.21 Real Time Clock (RTC) Interface Signals

Table 2-22. RTC Interface (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
INTRUDER_N	I	V3P3	**Intruder Detect:** This signal can be set to disable system if box detected open.
RSM_RST_N	I	V3P3	**Resume Well Reset:** Used for resetting the resume well. An external RC circuit is required to guarantee that the resume well power is valid prior to this signal going high.
RTC_TEST_N	I	V3P3	**RTC Battery Test:** An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. If the battery is missing/weak, this signal appears low (asserted) at boot just after the suspend power rail (V3P3) is up since it will not have time to meet Vih (Voltage input high) when V3P3A is high. When asserted, BIOS may clear the RTC CMOS RAM. ***Note:*** Unless CMOS is being cleared (only to be done in the G3 power state) or the battery is low, the signal input must always be high when all other RTC power planes are on.
RTC_RST_N	I	V3P3	**RTC Reset:** An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. When asserted, this signal resets all register bits in the RTC well. ***Notes:*** 1. Unless registers are being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the signal should be de-asserted before the RSM_RST_N signal is de-asserted.
RTC_X1	I	V3P3	**Crystal Input 1:** This signal is connected to a 32.768 KHz crystal (max 50K ESR). If using an external oscillator, the RTCX1 Vih must be within the range of 0.8V to 1.5V (1.5V max).
RTC_X2	O	V3P3	**Crystal Input 2:** This signal is connected to a 32.768 KHz crystal (Max 50K ESR). If using an external oscillator, RTCX2 should be left floating.

Table 2-22. RTC Interface (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
VCC_RTC_EXTPAD	O	V3P3	External Pad for voltage supply.

2.22 CNVi Signals

Table 2-23. CNVi Signals

Signal Name	Dir.	I/O Voltage	Description
CNV_BRI_DT	O	V1P8	Bluetooth* Radio Interface Tx
CNV_BRI_RSP	I	V1P8	Bluetooth* Radio Interface Ex
CNV_RF_RESET_N	O	V1P8	Reset for companion RF (Wi-Fi/Bluetooth*) module
CNV_RGI_DT	O	V1P8	Radio Generic Interface Tx
CNV_RGI_RSP	I	V1P8	Radio Generic Interface Ex
CNV_WGR_CLK_N	I	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WGR_CLK_P	I	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WGR_D[0/1]_N	I	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WGR_D[0/1]_P	I	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WT_CLK_N	O	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WT_CLK_P	O	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WT_D[0/1]_N	O	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WT_D[0/1]_P	O	V1P24	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module.
CNV_WT_RCOMP	O	V1P24	Romp for CNV WT/WGR proprietary interface.
CNV_MFUART[2:0]_RXD	I	V1P8	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module. ***Note:*** This is a GPIO pin.
CNV_MFUART[2:0]_TXD	O	V1P8	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module. ***Note:*** This is a GPIO pin.
CNV_MFUART[0/1]_RTS_N	O	V1P8	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module. ***Note:*** This is a GPIO pin.
CNV_MFUART[0/1]_CTS_N	I	V1P8	Intel proprietary interface between SoC (CNVi) and companion Wi-Fi/Bluetooth* module. ***Note:*** This is a GPIO pin.
XTAL_CLKREQ	O	V1P8	Crystal clock request for companion RF module to send the reference clock to the SoC.

2.23 Integrated Sensor Hub Interface Signals

Table 2-24. Integrated Sensor Hub Interface Signals

Signal Name	Dir.	I/O Voltage	Description
ISH_I^{2}C[2:0]_SDA	I/O, OD	V1P8	I^{2}C Data ***Note:*** This is a GPIO pin.
ISH_I^{2}C[2:0]_SCL	I/O, OD	V1P8	I^{2}C Clock ***Note:*** This is a GPIO pin.
ISH_UART[2:0]_RXD	I/O	V1P8	UART data input ***Note:*** This is a GPIO pin.
ISH_UART[2:0]_TXD	I/O	V1P8	UART data output ***Note:*** This is a GPIO pin.
ISH_UART[2:0]_RTS_N	I/O	V1P8	UART Ready to Send ***Note:*** This is a GPIO pin.
ISH_UART[2:0]_CTS_N	I/O	V1P8	UART Clear to Send ***Note:*** This is a GPIO pin.
ISH_SPI_[0/1]_TXD	I/O	V1P8	**SPI Data Pad:** Data Input/Output pin for the SoC. ***Note:*** This is a GPIO pin.
ISH_SPI_[0/1]_RXD	I/O	V1P8	
ISH_SPI_[0/1]_FS0	I/O	V1P8	**SPI frame Select:** Used as the SPI bus request signal. ***Note:*** This is a GPIO pin.
ISH_SPI_[0/1]_FS1	I/O	V1P8	**SPI Frame Select:** Used as the SPI bus request signal. ***Note:*** This is a GPIO pin.
ISH_SPI_[0/1]_CLK	I/O	V1P8	**SPI Clock:** SPI Clock signal ***Note:*** This is a GPIO pin.

2.24 Low Pin Count (LPC) Bus

Table 2-25. LPC Interface (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Description
LPC_AD[3:0]	I/O, OD	V1P8/V3P3	LPC Multiplexed Command, Address, Data.
LPC_CLKOUT[1:0]	O	V1P8/V3P3	**Clock Out:** 25 MHz output clock.
LPC_CLKRUN_N	IO-OD	V1P8/V3P3	**LPC Clock Run:** Control LPC Clock Signals.
LPC_FRAME_N	O	V1P8/V3P3	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LPC_SERIRQ	I/O	V1P8/V3P3	**LPC SERIRQ:** Serial Interrupt Request.

Table 2-25. LPC Interface (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Description
Note: I/O Voltage is controlled by Hardware Strap(GPIO_83).			

2.25 Miscellaneous Signals

Table 2-26. Miscellaneous Signals

Signal Name	Dir.	I/O Voltage	Description
PROCHOT_N	I/O, OD	V1P8	**Processor Hot**: asserted when the processor die temperature has reached its maximum operating temperature.
THERMTRIP_N	O	V1P8	**Thermal Trip:** THERMTRIP_N will be asserted/driven by the SoC under the following conditions: • In case of a catastrophic thermal event as seen by the SoC. • To indicate that a 'force shutdown' event has occurred. If user presses the power button for the override length (4 seconds), SoC will assert THERMTRIP_N to force a platform G2. • If SOC_PWROK de-asserts unexpectedly during normal platform operation (while PMU_SLP_S3_N or PMU_SLP_S4_N) are de-asserted), then the SoC considers this as an unrecoverable condition and will be asserted THERMTRIP_N to take the system into G2. ***Note:*** In the event of a catastrophic thermal failure (such as failure of cooling system), each thermal sensor can detect that die temperature exceeds thermal specification limits (typically 24-28C above Tjmax) and assert its CAT sensor output. Assertion of CAT must automatically trigger a thermal shut-down of all CPU PLLs, and platform voltage regulators within 500 ms and also trigger the soc thermtrip# I/O pin to be asserted.
GPIO_RCOMP	I/O	V1P8	**Resistor Compensation:** This signal is used for pre-driver slew rate compensation.
VNN_SENSE VCC_SENSE VGI_SENSE VCC0_LDO_SENSE VCC1_LD0_SENSE VCC_VSSSENSE VGI_VSSSENSE	I/O	N/A	VNN Sense signal for voltage feedback to the Voltage Regulator.
VCC_VCG_SENSE_P/N	I/O	N/A	Differential sense line for the VCC VCG rail Voltage Regulator.

2.26 Hardware Straps

Notes:

1. All the straps are sampled at ~95ms after RSM_RST_N de-assertion, where a stable RTC clock is used to count the duration. In cases where the RTC clock is not stable when boot starts, the strap sampling may deviate significantly above ~95ms.
2. The internal termination values listed in this table will be in effect from 3 RTC clock cycles before the strap sampling event until 3 RTC clock cycles after the strap sampling event. The external signal input to each strap must be glitch-free during this time. At 4 RTC clock cycles after the strap sampling event, the termination value will change to the GPIO termination as shown below.
3. If the RTC Clock Timer Bypass strap is enabled, all the straps are sampled a few RTC clock cycles after RSM_RST_N de-assertion.

Table 2-27. Hardware Straps (Sheet 1 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable ***Note:*** If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_43	MDSI_C_TE	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	USB2_OC0_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.

Table 2-27. Hardware Straps (Sheet 2 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_62	SIO_UART0_RTS_N	RSVD	20K PD	This pin must be 0 or not externally driven at time of RSM_RST_N.
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Notes:*** 1. DnX: Download and Execute. 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would download a new firmware image from a recovery host, over USB, and overwrite the image in the storage media.TXE can do it for BIOS part of FW, but strap is needed if TXE FW itself is corrupted.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) ***Note:*** The board should strap this low and do not use otherwise.
GPIO_79	SIO_SPI_0_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_80	SIO_SPI_0_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_81	SIO_SPI_0_FS1	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PU [Pre-ES and ES] 20K PD [ES2[1] and QS]	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	RSVD	20K PU	Ensure that this strap is pulled HIGH
GPIO_85	SIO_SPI_2_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_87	SIO_SPI_2_FS2	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_89	SIO_SPI_2_TXD	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_159	AVS_I2S0_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_163	AVS_I2S1_WS_SYNC	SMBus 1.8V/ 3.3V mode select	20K PU [Pre-ES and ES] 20K PD [ES2[1] and QS]	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)

Table 2-27. Hardware Straps (Sheet 3 of 3)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168[2]	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/ 3.3V mode select	20K PU [Pre-ES and ES] 20K PD [ES2[1] and QS]	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default)
GPIO_177	SMB_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_191	CNV_BRI_DT	eSPI Flash Sharing Mode	20K PD	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS; default) Note: if eSPI mode is disabled (eSPI/LPC hard strap(GPIO_175) is set to select LPC) then the eSPI slave attached flash sharing strap must also be set to 0.
GPIO_192	CNV_BRI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_193	CNV_RGI_DT	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_194	CNV_RGI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_195	CNV_RF_RESET_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_196	XTAL_CLKREQ	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

Notes:
1. ES2 samples will be limited samples for targeted customers.

2. PMU family voltage is controlled by hard strap only, not soft strap. Below is the complete list of GPIOs controlled by GPIO_168 hard strap.

GPIO #	Pin Name
GPIO_98	PMU_PLTRST_N
GPIO_99	PMU_PWRBTN_N
GPIO_100	PMU_SLP_S0_N
GPIO_101	PMU_SLP_S3_N
GPIO_102	PMU_SLP_S4_N
GPIO_103	SUSPWRDNACK
GPIO_104	EMMC_ PWR_N
GPIO_105	GPIO_105
GPIO_106	PMU_BATLOW_N
GPIO_107	PMU_RSTBTN_N
GPIO_108	PMU_SUSCLK
GPIO_109	SUS_STAT_N

2.27 GPIO Multiplexing

Note: SCI Tier 1 Group Details:

No in the spreadsheet corresponds to No SCI;

Yes in the spreadsheet corresponds to the following groups of 32 pads.

Northwest Community = 0 (pads 0:31), 1 (pads 32:63), 2 (pads 64:79)

North Community = 3 (pads 0:31), 4 (pads 32:63), 5 (64:79)

Audio Community = 6 (pads 0:19)SCC Community = 7 (pads 0:31), 8 (pads 32:34)

Table 2-28. GPIO Multiplexing (Sheet 1 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_0	N	20K PD	JTAG_TCK	I/O										
GPIO_1	N	20K PD	JTAG_TRST_N	I/O										
GPIO_10	Y	20K PD					CNV_DEBUG_11	I/O	CNV_DEBUG_02	I/O				
GPIO_100	N	None	PMU_SLP_S0_N	O										
GPIO_101	N	None	PMU_SLP_S3_N	O										
GPIO_102	N	None	PMU_SLP_S4_N	O										
GPIO_103	N	None	SUSPWRDNACK	O										
GPIO_104	N	20K PD	EMMC_PWR_EN_N	O										
GPIO_105	N	20K PD												

Table 2-28. GPIO Multiplexing (Sheet 2 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_106	N	20K PD	PMU_BATLOW_N	I										
GPIO_107	N	20K PD	PMU_RSTBTN_N	I										
GPIO_108	N	None	PMU_SUSCLK	O										
GPIO_109	N	None	SUS_STAT_N	O										
GPIO_11	Y	20K PD					CNV_DEBUG_12	I/O	CNV_DEBUG_03	I/O				
GPIO_110	Y	20K PD	SIO_I2C5_SDA	I/O OD	ISH_I2C0_SDA	I/O OD								
GPIO_111	Y	20K PD	SIO_I2C5_SCL	I/O OD	ISH_I2C0_SCL	I/O OD								
GPIO_112	Y	20K PD	SIO_I2C6_SDA	I/O OD	ISH_I2C1_SDA	I/O OD								
GPIO_113	Y	20K PD	SIO_I2C6_SCL	I/O OD	ISH_I2C1_SCL	I/O OD								
GPIO_114	Y	20K PD	SIO_I2C7_SDA	I/O OD	ISH_I2C2_SDA	I/O OD	SUSCLK1	I/O						
GPIO_115	Y	20K PD	SIO_I2C7_SCL	I/O OD	ISH_I2C2_SCL	I/O OD	SUSCLK2	I/O						
GPIO_116	Y	20K PD	PCIE_WAKE0_N	I/O OD										
GPIO_117	Y	20K PD	PCIE_WAKE1_N	I/O OD										
GPIO_118	Y	20K PD	PCIE_WAKE2_N	I/O OD										
GPIO_119	Y	20K PD	PCIE_WAKE3_N	I/O OD										
GPIO_12	Y	20K PD					CNV_DEBUG_13	I/O	CNV_DEBUG_04	I/O				
GPIO_120	Y	20K PD	PCIE_CLKREQ0_N	I/O										
GPIO_121	Y	20K PD	PCIE_CLKREQ1_N	I/O										
GPIO_122	Y	20K PD	PCIE_CLKREQ2_N	I/O										
GPIO_123	Y	20K PD	PCIE_CLKREQ3_N	I/O										
GPIO_124	Y	20K PD	DDI0_DDC_SDA	I/O OD										
GPIO_125	Y	20K PD	DDI0_DDC_SCL	I/O OD										
GPIO_126	Y	20K PD	DDI1_DDC_SDA	I/O OD	SIO_I2C5_SDA	I/O OD								
GPIO_127	Y	20K PD	DDI1_DDC_SCL	I/O OD	SIO_I2C5_SCL	I/O OD								
GPIO_128	Y	20K PD	PNL0_VDDEN	O										

Table 2-28. GPIO Multiplexing (Sheet 3 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_129	Y	20K PD	PNL0_BKLTEN	O										
GPIO_13	Y	20K PD					CNV_DEBUG_14	I/O	CNV_DEBUG_05	I/O				
GPIO_130	Y	20K PD	PNL0_BKLCTL	O										
GPIO_131	Y	20K PD	DDI0_HPD	I										
GPIO_132	Y	20K PD	DDI1_HPD	I										
GPIO_133	Y	20K PD	DDI2_HPD	I										
GPIO_134	Y	20K PD							ISH_GPIO_10	I/O				
GPIO_135	Y	20K PD							ISH_GPIO_11	I/O				
GPIO_136	Y	20K PD							ISH_GPIO_12	I/O				
GPIO_137	Y	20K PD							ISH_GPIO_13	I/O				
GPIO_138	Y	20K PD			SIO_UART3_RXD	I	ISH_UART0_RXD	I	ISH_GPIO_14	I/O	SATA_GP0	I/O		
GPIO_139	Y	20K PD			SIO_UART3_TXD	O	ISH_UART0_TXD	O	ISH_GPIO_15	I/O	SATA_GP1	I/O		
GPIO_14	Y	20K PD					CNV_DEBUG_15	I/O	CNV_DEBUG_06	I/O				
GPIO_140	Y	20K PD			SIO_UART3_RTS_N	O	ISH_UART0_RTS_N	O			SATA_DEVSLP0	I/O		
GPIO_141	Y	20K PD			SIO_UART3_CTS_N	I	ISH_UART0_CTS_N	I			SATA_DEVSLP1	I/O		
GPIO_142	Y	20K PD			SIO_SPI_1_CLK	I/O	ISH_SPI_0_CLK	I/O			SATA_LEDN	O Only OD		
GPIO_143	Y	20K PD			SIO_SPI_1_FS0	O	ISH_SPI_0_FS0	O	JTAG2_TCK	I				
GPIO_144	Y	20K PD			SIO_SPI_1_FS1	O	ISH_SPI_0_FS1	O	JTAG2_TDI	I	PNL1_VDDEN	O		
GPIO_145	Y	20K PD			SIO_SPI_1_RXD	I	ISH_SPI_0_RXD	I	JTAG2_TMS	I	PNL1_BKLTEN	O		
GPIO_146	Y	20K PD			SIO_SPI_1_TXD	O	ISH_SPI_0_TXD	O	JTAG2_TDO	O Only OD	PNL1_BKLTCTL	O		
GPIO_147	Y	20K PD	LPC_SERIRQ	I/O	ESPI_RESET_N	O								
GPIO_148	Y	None	LPC_CLKOUT0	O	ESPI_CLK	O								
GPIO_149	Y	None	LPC_CLKOUT1	O		I/O								
GPIO_15	Y	20K PD					CNV_DEBUG_16	I/O	CNV_DEBUG_07	I/O				
GPIO_150	Y	20K PD	LPC_AD0	I/O	ESPI_IO_0	I/O								

Table 2-28. GPIO Multiplexing (Sheet 4 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_151	Y	20K PD	LPC_AD1	I/O	ESPI_IO_1	I/O								
GPIO_152	Y	20K PD	LPC_AD2	I/O	ESPI_IO_2	I/O								
GPIO_153	Y	20K PD	LPC_AD3	I/O	ESPI_IO_3	I/O								
GPIO_154	Y	20K PD	LPC_CLKRUN_N	I/O OD										
GPIO_155	Y	20K PD	LPC_FRAME_N	O	ESPI_CS_N	O								
GPIO_156	Y	20K PD	AVS_I2S0_MCLK	O										
GPIO_157	Y	20K PD	AVS_I2S0_BCLK	I/O										
GPIO_158	Y	20K PD	AVS_I2S0_WS_SYNC	I/O										
GPIO_159	Y	20K PD	AVS_I2S0_SDI	I										
GPIO_16	Y	20K PD					CNV_DEBUG_17	I/O	CNV_DEBUG_08	I/O				
GPIO_160	Y	20K PD	AVS_I2S0_SDO	I/O										
GPIO_161	Y	20K PD	AVS_I2S1_MCLK	O										
GPIO_162	Y	20K PD	AVS_I2S1_BCLK	I/O			CNV_BT_I2S_BCLK	I/O						
GPIO_163	Y	20K PD	AVS_I2S1_WS_SYNC	I/O			CNV_BT_I2S_WS_SYNC	I/O						
GPIO_164	Y	20K PD	AVS_I2S1_SDI	I			CNV_BT_I2S_SDI	I						
GPIO_165	Y	20K PD	AVS_I2S1_SDO	I/O			CNV_BT_I2S_SDO	O						
GPIO_166	Y	20K PD	AVS_HDA_BCLK	I/O	AVS_I2S2_BCLK	I/O								
GPIO_167	Y	20K PD	AVS_HDA_WS_SYNC	I/O	AVS_I2S2_WS_SYNC	I/O								
GPIO_168	Y	20K PD	AVS_HDA_SDI	I/O	AVS_I2S2_SDI	I								
GPIO_169	Y	20K PD	AVS_HDA_SDO	O	AVS_I2S2_SDO	I/O								
GPIO_17	Y	20K PU			CNV_MFUART0_RXD	I	CNV_DEBUG_00	I/O						
GPIO_170	Y	20K PD	AVS_HDA_RST_N	I/O	AVS_I2S1_MCLK	O								
GPIO_171	Y	20K PD	AVS_DMIC_CLK_A1	O										
GPIO_172	Y	20K PD	AVS_DMIC_CLK_B1	O										

Table 2-28. GPIO Multiplexing (Sheet 5 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_173	Y	20K PD	AVS_DMIC_DATA_1	I										
GPIO_174	Y	20K PD	AVS_DMIC_CLK_AB2	O										
GPIO_175	Y	20K PD	AVS_DMIC_DATA_2	I										
GPIO_176	Y	20K PD	SMB_ALERT_N	I/O OD										
GPIO_177	Y	20K PD	SMB_CLK	I/O OD	SIO_I2C7_SCL	I/O								
GPIO_178	Y	20K PD	SMB_DATA	I/O OD	SIO_I2C7_SDA	I/O								
GPIO_179	N	20K PD	SDCARD_CLK	I/O										
GPIO_18	Y	20K PU			CNV_MFUART0_TXD	O	CNV_DEBUG_01	I/O						
GPIO_181	N	20K PD	SDCARD_D0	I/O										
GPIO_182	N	20K PD	SDCARD_D1	I/O										
GPIO_183	N	20K PD	SDCARD_D2	I/O										
GPIO_184	N	20K PD	SDCARD_D3	I/O										
GPIO_185	N	20K PD	SDCARD_CMD	I/O										
GPIO_186	Y	20K PU	SDCARD_CD_N	I/O										
GPIO_187	Y	20K PD	SDCARD_LVL_WP	I/O										
GPIO_188	Y	20K PD	SDCARD_PWR_DWN_N	I/O										
GPIO_189	Y	20K PD	OSC_CLK_OUT_0	O										
GPIO_19	Y	20K PU			CNV_MFUART0_RTS_N	O	CNV_DEBUG_02	I/O						
GPIO_190	Y	20K PD	OSC_CLK_OUT_1	O										
GPIO_191	Y	None	CNV_BRI_DT	O			SIO_UART1_RTS_N	O						
GPIO_192	Y	20K PU	CNV_BRI_RSP	I			SIO_UART1_RXD	I						
GPIO_193	Y	None	CNV_RGI_DT	O			SIO_UART1_TXD	O						
GPIO_194	Y	20K PU	CNV_RGI_RSP	I			SIO_UART1_CTS_N	I						
GPIO_195	Y	None	CNV_RF_RESET_N	O			AVS_I2S1_WS_SYNC	I/O						

Table 2-28. GPIO Multiplexing (Sheet 6 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_196	Y	None	XTAL_CLKREQ	O			AVS_I2S1_SDO	I/O						
GPIO_198	N	20K PD	EMMC_CLK	I/O										
GPIO_2	N	20K PU	JTAG_TMS	I/O										
GPIO_20	Y	20K PU			CNV_MFUART0_CTS_N	I	CNV_DEBUG_03	I/O						
GPIO_200	N	20K PU	EMMC_D0	I/O										
GPIO_201	N	20K PU	EMMC_D1	I/O										
GPIO_202	N	20K PU	EMMC_D2	I/O										
GPIO_203	N	20K PU	EMMC_D3	I/O										
GPIO_204	N	20K PU	EMMC_D4	I/O										
GPIO_205	N	20K PU	EMMC_D5	I/O										
GPIO_206	N	20K PU	EMMC_D6	I/O										
GPIO_207	N	20K PU	EMMC_D7	I/O										
GPIO_208	N	20K PU	EMMC_CMD	I/O										
GPIO_209	N	20K PD	EMMC_RCLK	I/O										
GPIO_21	Y	20K PU			CNV_MFUART2_RXD	I	CNV_DEBUG_04	I/O						
GPIO_210	Y	20K PD												
GPIO_211	Y	20K PU	EMMC_RST_N	O										
GPIO_212	Y	20K PU												
GPIO_213	Y	20K PU												
GPIO_214	Y	20K PD												
GPIO_22	Y	20K PU			CNV_MFUART2_TXD	O	CNV_DEBUG_05	I/O						
GPIO_23	Y	20K PU			CNV_GNSS_PA_BLANKING	I	CNV_DEBUG_06	I/O	PMIC_STDBY	O				
GPIO_24	Y	20K PU			CNV_GNSS_FTA	I	CNV_DEBUG_07	I/O	PMIC_PWRGOOD	I				
GPIO_25	Y	20K PU			CNV_GNSS_SYSCK	I	CNV_DEBUG_08	I/O	PMIC_RESET_N	I				
GPIO_26	Y	20K PD	ISH_GPIO_0		SIO_UART1_RXD	I	ISH_UART1_RXD	I	CNV_BT_UART_RXD	I				
GPIO_27	Y	20K PD	ISH_GPIO_1		SIO_UART1_TXD	O	ISH_UART1_TXD	O	CNV_BT_UART_TXD	O				
GPIO_28	Y	20K PD	ISH_GPIO_2		SIO_UART1_RTS_N	O	ISH_UART1_RTS_N	O	CNV_BT_UART_RTS_N	O				
GPIO_29	Y	20K PD	ISH_GPIO_3		SIO_UART1_CTS_N	I	ISH_UART1_CTS_N	I	CNV_BT_UART_CTS_N	I				

Table 2-28. GPIO Multiplexing (Sheet 7 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_3	N	20K PU	JTAG_TDI	I/O										
GPIO_30	Y	20K PD	ISH_GPIO_4		SATA_GP0	I/O								
GPIO_31	Y	20K PD	ISH_GPIO_5		SATA_GP1	I/O								
GPIO_32	Y	20K PD	ISH_GPIO_6		SATA_DEVSLP0	I/O								
GPIO_33	Y	20K PD	ISH_GPIO_7		SATA_DEVSLP1	I/O	SUSCLK1	I/O						
GPIO_34	Y	20K PD	ISH_GPIO_8		SATA_LEDN	O Only OD	SUSCLK2	I/O						
GPIO_35	Y	20K PU	ISH_GPIO_9						SPKR	O			BSSB_CLK	I
GPIO_36	Y	20K PU					CNV_BTEN	I					BSSB_DI	I
GPIO_37	Y	20K PU					CNV_GNEN	I						
GPIO_38	Y	20K PU					CNV_WFEN	I						
GPIO_39	Y	20K PU					CNV_WCEN	I						
GPIO_4	N	20K PU	JTAG_TDO	I/O OD										
GPIO_40	Y	20K PU					CNV_BT_HOST_WAKE_N	O						
GPIO_41	Y	20K PD					CNV_GNSS_HOST_WAKE_N	O						
GPIO_42	Y	20K PD	MDSI_A_TE	I	PWM0	O								
GPIO_43	Y	20K PD	MDSI_C_TE	I	PWM1	O								
GPIO_44	Y	20K PU	USB2_OC0_N	I/O	PWM2	O								
GPIO_45	Y	20K PU	USB2_OC1_N	I/O	PWM3	O								
GPIO_46	Y	20K PD	MIPI_I2C_SDA	I/O OD										
GPIO_47	Y	20K PD	MIPI_I2C_SCL	I/O OD										
GPIO_48	Y	1K PU	PMC_I2C_SDA	I/O OD										
GPIO_49	Y	1K PU	PMC_I2C_SCL	I/O OD										
GPIO_5	N	20K PU	JTAGX	I/O										
GPIO_50	Y	20K PU	SIO_I2C0_SDA	I/O OD										
GPIO_51	Y	20K PU	SIO_I2C0_SCL	I/O OD										
GPIO_52	Y	20K PU	SIO_I2C1_SDA	I/O OD										

Table 2-28. GPIO Multiplexing (Sheet 8 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_53	Y	20K PU	SIO_I2C1_SCL	I/O OD										
GPIO_54	Y	20K PU	SIO_I2C2_SDA	I/O OD										
GPIO_55	Y	20K PU	SIO_I2C2_SCL	I/O OD										
GPIO_56	Y	20K PU	SIO_I2C3_SDA	I/O OD										
GPIO_57	Y	20K PU	SIO_I2C3_SCL	I/O OD										
GPIO_58	Y	20K PU	SIO_I2C4_SDA	I/O OD										
GPIO_59	Y	20K PU	SIO_I2C4_SCL	I/O OD										
GPIO_6	N	20K PU	JTAG_PREQ_N	I/O										
GPIO_60	Y	20K PU	SIO_UART0_RXD	I	ISH_UART0_RXD	I	CNV_GNSS_UART_RXD	I						
GPIO_61	Y	20K PU	SIO_UART0_TXD	O	ISH_UART0_TXD	O	CNV_GNSS_UART_TXD	O						
GPIO_62	Y	20K PU	SIO_UART0_RTS_N	O	ISH_UART0_RTS_N	O	CNV_GNSS_UART_RTS_N	O						
GPIO_63	Y	20K PU	SIO_UART0_CTS_N	I	ISH_UART0_CTS_N	I	CNV_GNSS_UART_CTS_N	I						
GPIO_64	Y	20K PU	SIO_UART2_RXD	I	ISH_UART2_RXD	I	CNV_MFUART1_RXD	I						
GPIO_65	Y	20K PU	SIO_UART2_TXD	O	ISH_UART2_TXD	O	CNV_MFUART1_TXD	O						
GPIO_66	Y	20K PU	SIO_UART2_RTS_N	O	ISH_UART2_RTS_N	O	CNV_MFUART1_RTS_N	O						
GPIO_67	Y	20K PU	SIO_UART2_CTS_N	I	ISH_UART2_CTS_N	I	CNV_MFUART1_CTS_N	I						
GPIO_68	Y	20K PU	PMC_SPI_FS0	O										
GPIO_69	Y	20K PU	PMC_SPI_FS1	O										
GPIO_7	N	20K PU	JTAG_PRDY_N	I/O OD										
GPIO_70	Y	20K PU	PMC_SPI_FS2	O										
GPIO_71	Y	20K PD	PMC_SPI_RXD	I										
GPIO_72	Y	20K PD	PMC_SPI_TXD	O										
GPIO_73	Y	20K PD	PMC_SPI_CLK	O										

Table 2-28. GPIO Multiplexing (Sheet 9 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_74	N	20K PU	THERMTRIP_N	O										
GPIO_75	N	20K PU	PROCHOT_N	I/O										
GPIO_76	N	20K PU	SVID0_ALERT_N	I										
GPIO_77	N	20K PU	SVID0_DATA	I/O										
GPIO_78	N	20K PU	SVID0_CLK	I/O										
GPIO_79	Y	20K PD	SIO_SPI_0_CLK	I/O	ISH_SPI_0_CLK	I/O								
GPIO_8	Y	20K PD					CNV_DEBUG_09	I/O	CNV_DEBUG_00	I/O				
GPIO_80	Y	20K PD	SIO_SPI_0_FS0	O	ISH_SPI_0_FS0	O								
GPIO_81	Y	20K PD	SIO_SPI_0_FS1	O	ISH_SPI_0_FS1	O	FST_SPI_CS2_N	I/O						
GPIO_82	Y	20K PD	SIO_SPI_0_RXD	I	ISH_SPI_0_RXD	I								
GPIO_83	Y	20K PD	SIO_SPI_0_TXD	O	ISH_SPI_0_TXD	O								
GPIO_84	Y	20K PD	SIO_SPI_2_CLK	I/O	ISH_SPI_1_CLK	I/O	TOUCH_SPI_CLK	I/O						
GPIO_85	Y	20K PD	SIO_SPI_2_FS0	O	ISH_SPI_1_FS0	O	TOUCH_SPI_FS0	I/O						
GPIO_86	Y	20K PD	SIO_SPI_2_FS1	O	ISH_SPI_1_FS1	O	TOUCH_SPI_D0	I/O						
GPIO_87	Y	20K PD	SIO_SPI_2_FS2	O			TOUCH_SPI_D1	I/O						
GPIO_88	Y	20K PD	SIO_SPI_2_RXD	I	ISH_SPI_1_RXD	I	TOUCH_SPI_D2	I/O						
GPIO_89	Y	20K PD	SIO_SPI_2_TXD	O	ISH_SPI_1_TXD	O	TOUCH_SPI_D3	I/O						
GPIO_9	Y	20K PD					CNV_DEBUG_10	I/O	CNV_DEBUG_01	I/O				
GPIO_90	N	Native	FST_SPI_CS0_N	I/O										
GPIO_91	N	Native	FST_SPI_CS1_N	I/O										
GPIO_92	N	Native	FST_SPI_MOSI_IO0	I/O										
GPIO_93	N	Native	FST_SPI_MISO_IO1	I/O										
GPIO_94	N	Native	FST_SPI_IO2	I/O										
GPIO_95	N	Native	FST_SPI_IO3	I/O										
GPIO_96	N	Native	FST_SPI_CLK	I/O										

Table 2-28. GPIO Multiplexing (Sheet 10 of 10)

GPIO #	SMI	Default Termination @ PLTRST	Fn 1	Fn 1 Dir	Fn 2	Fn 2 Dir	Fn 3	Fn 3 Dir	Fn 4	Fn 4 Dir	Fn 5	Fn 5 Dir	Fn 6	Fn 6 Dir
GPIO_98	N	None	PMU_PLTRST_N	O										
GPIO_99	N	20K PD	PMU_PWRBTN_N	I										

§ §

3 Functional Description

3.1 Processor Core Overview

Table 3-1. Processor Core Overview

Category	Feature Description
CPU Cores	Quad/Dual IA Processor Core • 1 module of up to 4 core • Supporting Out of Order Execution (OOE) • 14 nm processor Technology
Modules/Caches	• 1 Module • Up to 4 Cores grouped per Module • On-die, 32KB 8-way, L1 instruction cache and 24KB 6-way L1 data cache per core • On-die, 4MiB, 16-way L2 unified cache per module
Architecture	Intel® 64 Bit
Virtualization architecture	Intel full virtualization architecture support • VTx-2 with Extended Page Table • VT-d
Burst Technology	1 core/2 cores/3 cores/4 cores
Thermal Management	Supported by means of Intel® Thermal Monitor (TM1 and TM2)
Power Management	• Support Connected Standby, Modern Standby, and Lucid Sleep • Support system states: S0, S0ix, S3, S4/S5, and RTD3 • Uses Power Aware Interrupt Routing (PAIR)
Boot feature	Support boot from SPI NOR and eMMC (secure and non-secure)
Other features	• Support for a Digital Random Number Generator (DRNG) • Support for Intel Carry-Less Multiplication Instruction (PCLMULQDQ) • Support for SGX

3.2 System Memory Controller

The SoC will support DDR4 and LPDDR4 2G-8G for memory-down platforms. The SoC Memory Controller supports following Memory Technologies two channels for DDR4 and four 32bit channels for LPDDR4.

Table 3-2. System Memory Controller Specifics of Supported Memory Technologies (Sheet 1 of 2)

Technology Attributes	LPDDR4	DDR4
Channels	4 (x32)	2 (x64)
Peak Bandwidth (GB/s)	38.4	38.4
Maximum Data Transfer Rate (MT/s)	2400	2400
Maximum Total System Capacity	8GB	8GB
Raw Card Support	N/A	A(1Rx8) B(2Rx8) C(1Rx16) UDIMM: A(1Rx8) B(2Rx8)

Table 3-2. System Memory Controller Specifics of Supported Memory Technologies (Sheet 2 of 2)

Technology Attributes	LPDDR4	DDR4
Densities (Gb)	8	4,8,16
CMD/Adds pins per channel	6	17
DQ pins per channel	32	64
Voltage Rail (V)	1.1	1.2
DRAM Package Supported	SDP/DDP/QDP	SDP/DDP
Scrambling	Yes	
On Die Termination Control		
Rank Interleaving		
Refresh	No per bank-refresh, only at rank level	
Power Saving Features	Fast Exit Power Down, Self Refresh plus extra features, Power/trunk gating	
Note: ECC is not supported on SoC.		

Table 3-3. DDR4 Configurations

x64 Ch0 (Family 0) Data				x64 Ch1 (Family 1) Data			
x16 BGA	x16BGA	x16BGA	x16BGA	x16BGA	x16BGA	x16BGA	x16BGA
SODIMM (x8 and x16)				SODIMM (x8 and x16)			
UDIMM (x8 and x16)				UDIMM			
x16	x16	x16	x16	SODIMM (x8 and x16)			
x16	x16	x16	x16	UDIMM			
x16	x16	x16	x16	Unpopulated			
SODIMM (x8 and x16)				Unpopulated			
UDIMM (x8 and x16)				Unpopulated			
Unpopulated				SODIMM			
Unpopulated				UDIMM			

Table 3-4. DDR4 Memory Configuration

DRAM Package	Ranks per Package	Density per DRAM Die (Gb)	DQ Width per DRAM	Number of DRAM Die per Package	DRAM Package Capacity (GB)	Number of Packages to Form a x64 Non-ECC Channel
SDP	1	4	16	1	0.5	4
DDP	2	4	16	2	1	4
SDP	1	4	8	1	0.5	8
DDP	2	4	8	2	1	8
SDP	1	8	16	1	1	4
DDP	2	8	16	2	2	4
SDP	1	8	8	1	1	8
DDP	2	8	8	2	2	8
SDP	1	16	16	1	2	4

Table 3-5. LPDDR4 Configurations

CH00	CH01	CH10	CH11	Restrictions
x32 BGA	x32 BGA	x32 BGA	x32 BGA	All Channels Identical
x32 BGA	x32 BGA	Unpopulated		Ch00 identical to Ch01

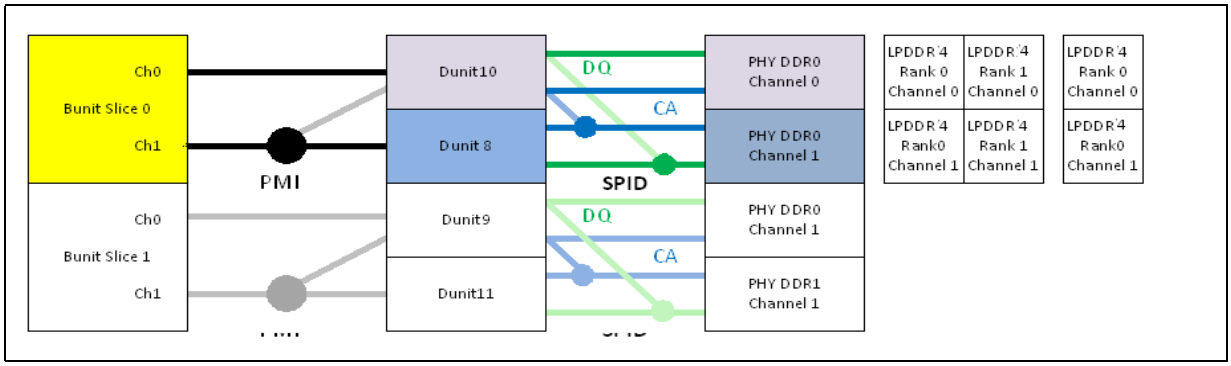
3.2.1 Configurations

This section describes the connectivity of System Agent, D-Unit and PHY Logic This section describes which Bunit Slices, DUnits and PHYs are active when various DRAMs are present. There is one diagram below for each unique set of activations. The diagrams comprehend all supported DRAM configurations, which are depicted on the right of each diagram. Active Agents are colored, inactive are white. Inactive paths are shown with faint colors.

The SoC has 128 DQs and is designed to support memory on a motherboard (memory down). This includes BGA packages on the motherboard or on DIMMs. Ranks on one channel are identical, but may differ across channels.

3.2.1.1 2 Channels of LPDDR4

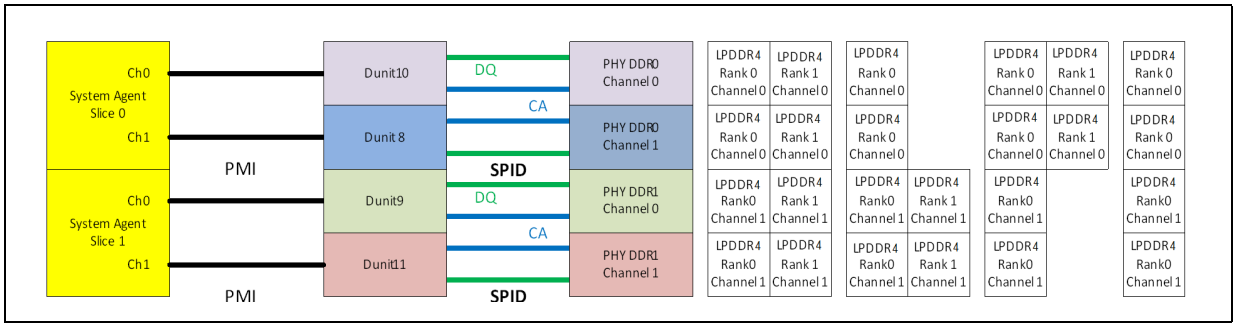
Figure 3-1. 2 Channels of LPDDR4



3.2.1.2 4 Channels of LPDDR4

Four x32 Channels (Ch00, Ch01, Ch10, Ch11) connect to LP Devices. Channels on the same PHY family are identically populated.

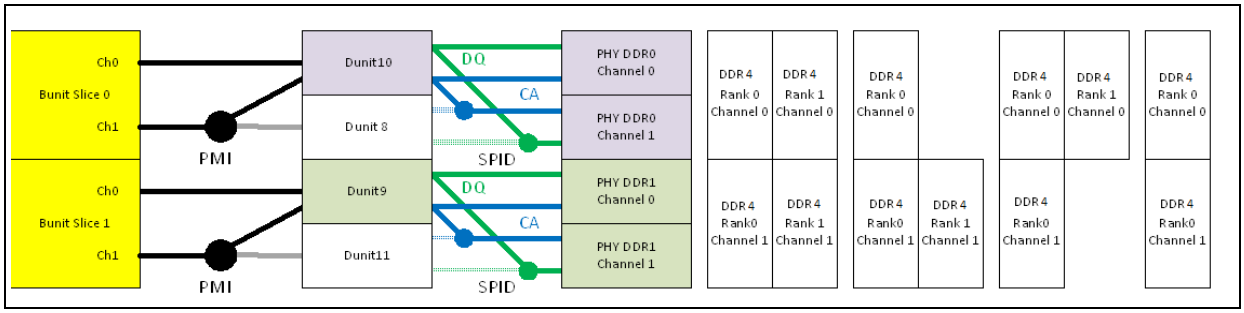
Figure 3-2. 4 Channel LPDDR4 Connectivity



3.2.1.3 DDR4 2 Channel

The SKUs will be supported for two 64-bit PHYs with one D-unit for each PHY. Any combination of ranks may be populated.

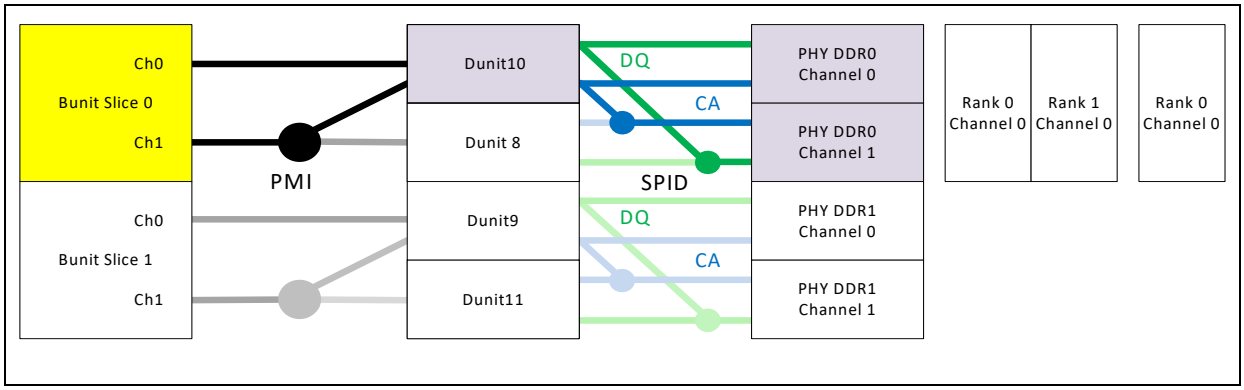
Figure 3-3. 2 Channel



3.2.1.4 DDR4 1 Channel

When only one channel is populated, only slice 0 of the System B-Unit Agents active. There may be 1 or 2 ranks populated.

Figure 3-4. DDR4 1 Channel



3.2.1.5 System Memory Timing Support

The IMC supports the following DDR Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- tRPb = per-bank PRECHARGE time
- tRPab = all-bank PRECHARGE time
- CWL = CAS Write Latency
- Command Signal modes:
  - 2N indicates a new DDR4 command may be issued every 2 clocks
  - 1N indicates a new DDR4/LPDDR4 command may be issued every clock

Table 3-6. DDR4 System Memory Timing Support

RAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (ns)	tRP (ns)	CWL (tCK)	DPC	CMD Mode
DDR4	2400	18	15ns (18 tCK)	15ns (18 tCK)	15,16,17,18	1	2N

Table 3-7. LPDDR4 System Memory Timing Support

RAM Device	Mode	Transfer Rate (MT/s)	tCL (tCK)	tRCD (ns)	tRPpb (ns)	tRPab (ns)	WL (tCK)
LPDDR4	X32	2400	24	18.33ns (22 tCK)	18.33ns (22 tCK)	22	22

3.3 Graphics and Media Engine

Intel 9th generation (Gen 9) LP graphics and media encode/decode engine consists of the following features:

- Three slices of 6 EUs each (3x6); each slice supports 6 threads resulting in a total of 108 available threads.
- Supports 3-D rendering, media compositing, and video encoding.
- Graphics Burst enabled through energy counters.
- Supports DX* (9.3, 10, 11.3, 12), OpenGL* 4.3, OGL ES 3.0, OpenCL* 2.0.
- 4x anti-aliasing.
- Supports Content protection using PAVP 2.0 and HDCP 2.2.

Table 3-8. Hardware Accelerated Video Decode/Encode Codec Support (Sheet 1 of 2)

Codec Format	Decode Level	Encode Level
HEVC (H.265)	MP L5.1 8b/10b, upto 4kx2kp60 MP L5 8b/10b, upto 4Kx2Kp30	MP L4 8b, upto 4kx2kp30 Bit rate: Up to 100 Mbps
H.264	CBP, MP, HP L5.2 up to 1080p240, 4kx2kp60	CBP, MP HP L5.2 up to 1080p240, 4k2kp60
MVC	CBP, MP HP L5.2 4k2kp60	CBP, MP, HP L5.1 4k2kp30
VP8	Up to 4kx2kp60	Upto 4kx2kp30
VP9	Up to 4kx2kp60	Upto 1080p60 Software based only
MPEG2	HD, MP, HL Up to 1080p60	N/A
VC-1	AP L4 Up to 1080p60	N/A
WMV9	MP, HL Up to 1080p30	N/A
JPEG/MJPEG	1067 Mpps (420), 800 Mpps (422), 533 Mpps (444)	1067 Mpps (420), 800 Mpps (422), 533 Mpps (444)
VP9	10b decode @ 4k60	8b @ 1080p60 4W

Table 3-8. Hardware Accelerated Video Decode/Encode Codec Support (Sheet 2 of 2)

Codec Format	Decode Level	Encode Level
HEVC	10b decode @ 4k60	8b @ 1080p60 4W, 10b @ 1080p60 4W

Notes:
1. The above table is for Windows* OS based platform.
2. HEVC 10b Decode is only supported on Windows*10 Graphics Driver.

3.3.1 Graphics Performance

Graphics performance in GFLOPS (Giga-FLoating point OPerations/Second) is calculated by the number of active EUs and graphics engine frequency; each EU can sustain 16 FLOPS:

- Total GFLOPS = Frequency x 18 EUs x 16 FLOPS/EU

The graphics engine frequency, and therefore performance is dependent on Power Limit 1 register (PL1) as shown in the following table:

Table 3-9. GFx Performance Estimate by SoC TDP

SoC TDP	Graphics Frequency (Estimated)	Performance (GFLOPS)
6 W	Up to 750 MHz	216
10 W	Upto 800 MHz	230.4

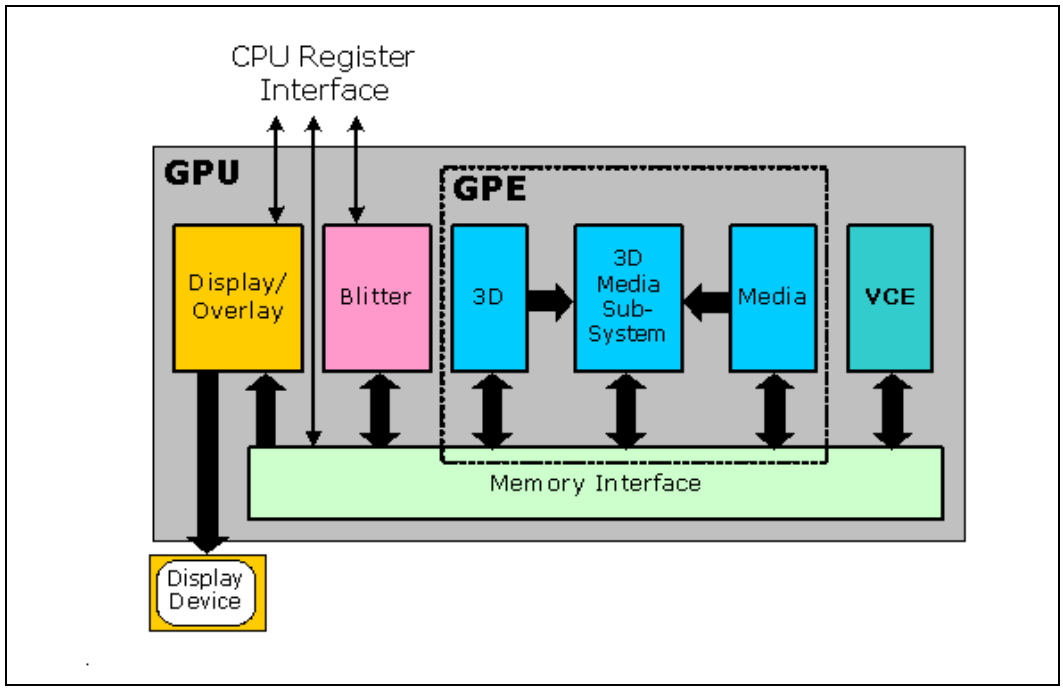
3.3.2 Graphics and Media Engine Overview

The Graphics Processing Unit is controlled by the CPU through a direct interface of memory-mapped IO registers, and indirectly by parsing commands that the CPU has placed in memory. The Display interface and Blitter (block image transferrer) are controlled primarily by direct CPU register addresses, while the 3D and Media pipelines and the parallel Video Codec Engine (VCE) are controlled primarily through instruction lists in memory.

The subsystem contains an array of cores, or execution units, with a number of “shared functions”, which receive and process messages at the request of programs running on the cores. The shared functions perform critical tasks, such as sampling textures and updating the render target (usually the frame buffer). The cores themselves are described by an instruction set architecture, or ISA.

3.3.2.1 Graphics Integration

Figure 3-5. Graphics Unit Diagram



3.3.2.2 3-D Engine

3.3.2.2.1 Features

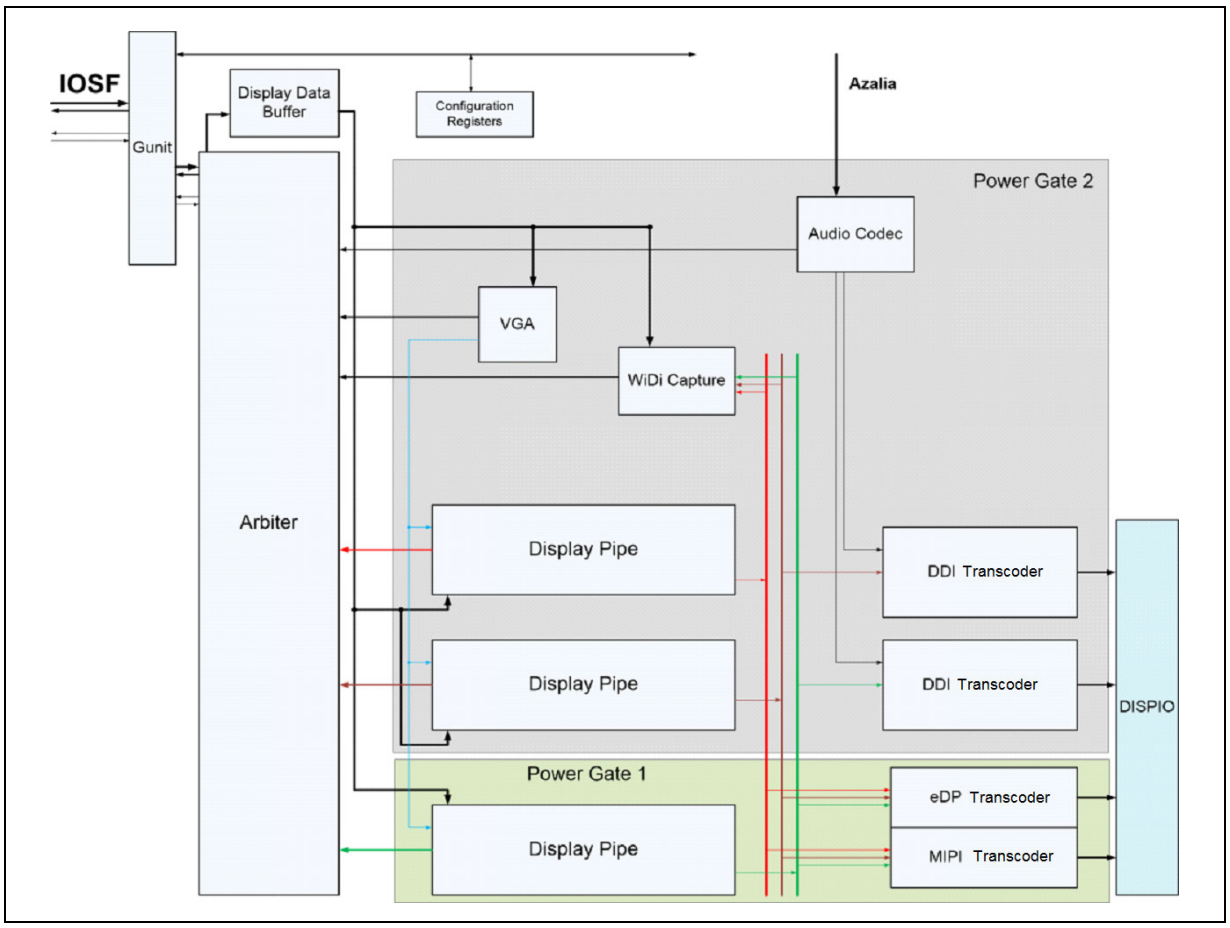
- Deferred Pixel Shading
- On-chip tile floating point depth buffer
- 8-bit Stencil with on chip tile stencil buffer
- 32 parallel depth/stencil tests per clock
- Scissor test (up to 16384 scissor rects supported) Texture parameters
  - 16K x 16K textures
  - Volume textures (2K depth)
  - Stride textures up to 32K size for the stride
  - Full arbitrary non power of two texture support
  - Constrained non power of two stride based textures
  - 1 TB virtual address range
- Address modes
  - All OGL and DirectX texture addressing modes
  - OVG tile fill addressing mode
- Texture lookups
  - Un-normalized/integer 1-D and 2-D texture coordinates (up to 64K x 64K)
  - Multi-sample texture addressing (up to 8 samples per texel)

  - Sample offsets in the range [-31,+32] for 1-D, 2-D and 3-D textures together with multi-sample textures
  - Not-normalized texture lookups (OGL)
  - Integer lookups (DX)
  - Fetch-N-support
  - Gather-4-support
  - Load instruction support
  - Texture writes enabled through the TPU
- Filtering
  - Sample details: sample data and coefficient support
  - Full filtering of all texture filtering, excluding F32/U32/S32/U24/S24
  - Bilinear, bi-cubic, tri-linear and 16:1 anisotropic filtering
  - PCF support
  - Corner filtering support for CEM textures and filtering across faces
- Texture formats
  - All Dx10 and Dx11 texture formats
  - PVRTC I and II including new separate alpha, 1 and 2 channel modes
  - ETC2/EAC
  - Frame buffer compression formats
  - YUV planar support with arbitrary allocation for the planes and up to 16 different configurable coefficients and chroma interpolation
- Gamma support
  - Pre-multiplied alpha
  - Gamma corrected textures on unsigned 8-bits and XR textures
- Mipmapping support
  - Fractional top and bottom LOD clamps (minlod/maxlod)
  - Number of mipmap levels present for a given texture (numlevels) and fractional minimum level (minlevel)
- Output format support
  - Output data conversions, no change and F32 returned to the USC
- Normalization support
  - Normalization support before returning data to USC
- Swizzling support
  - Swizzling bit should be used to replicate the converted result of a single or two channel input from the formatter block to the output buffer.
- Resolution Support
  - Frame buffer maximum size = 8192 x 8192
  - Texture maximum size = 8192 x 8192
- Anti-aliasing
  - 8 x Multi-sampling
  - Programmable sample positions

- Indexed Primitive List support
  - — Bus mastered
  - — Programmable Vertex DMA
- Render to texture
  - — Including twiddled formats
  - — Multiple on-chip Render Targets (MRT)—dependent on availability of on-chip SoC memory used as intermediate data stores not included in HOOD base core Programmable Geometry Shader Support
  - — Direct Geometry Stream Out

3.3.3 Display Engine Overview

Figure 3-6. Display Engine High-level Block Diagram



3.3.3.1 G-Unit

- Device 2 PCI configuration space and interrupt protocol
- Lots of functions for GT, aperture, and Vt-d

3.3.3.2 Arbiter

Arbitrates between the many DMA agents within the display

- HP clients (VC1 pixel reads)
- LP clients (VC0 read/write)

Handles request tagging

3.3.3.3 Display Data Buffer (DBUF)

512 KB

Streaming buffer for the display planes

Y-tile and de-rotation

Reconfigured by software

Allocation of data buffer space is programmable for each display plane.

- Must be contiguous for each plane.
- Must not overlap for enabled planes.
- Must meet large Y-tile space requirements.
- Must meet memory request latency requirements.
- Must use any remaining space to allow higher wake latencies and increase time between high priority reads.

3.3.3.4 VGA

- Legacy display subsystem
- Fetches pixels from memory to form pixel stream

3.3.3.5 Display Pipes

- Fetch and convert the frame buffer data into pixel streams
- Multiple planes per pipe
- Color conversion, scaling, blending

3.3.3.6 Display Ports

- DisplayPort, eDP, HDMI, and MIPI.
- Consume the pixel and audio streams and add the appropriate transport layer for the connected display device.

3.3.3.7 Display IO PHY

- Independent block outside of DE.
- Converts digital port output to drive I/O buffers.
- Parallel to serial conversion for DP and HDMI/DVI.
- Voltage swing and emphasis, compensation.
- Miscellaneous signals through GPIO.

3.3.3.8 Wireless Display

- Operates like a port, but captures the data back to memory.
- Driver or GT media compress the data and send it to wireless NIC.

3.3.4 Audio Codec

- Receives audio commands and data from HD-Audio and supplies a formatted audio stream to the ports.
- Captures data back to memory for wireless display audio.

3.4 Display Controller

The Gen10 Display Engine (DE) provides the ability to connect up to three displays to the SoC using MIPI*-DSI, eDP*, and DP*/HDMI*. When only a single internal display is used (MIPI*-DSI or eDP*), the DE can employ power optimizations to reduce power.

3.4.1 Features of Display Controller

- Supports 3 Display pipes, simultaneous multi-streaming on all three display pipes (1x internal and 2x external displays).
- Implements 2 pixels per clk(2PPC).
- Support 4k display at lower Vnn (target is 0.75V).
- Support 2 MIPI*-DSI 1.2, 1G ports.
- Support 3 DDI ports to enable eDP* 1.4, DP* 1.2a, or HDMI* 2.0a.
  - Supports 1x internal display (eDP* 1.4). DDI2 port is dedicated to eDP*.
  - Supports 2x external display (DP* 1.2a, HDMI 2.0a). DDI0 and DDI1 can be used for external displays.
- Supports Audio on DP* and HDMI*.
- Supports Multi Plane Overlay (MPO).
- Supports Intel® Display Power Saving Technology (Intel® DPST) 6.3, Panel Self Refresh (PSR), and Display Refresh Rate Switching Technology (DRRS).

Table 3-10. Display Features (Sheet 1 of 2)

Feature	MIPI*-DSI	eDP*	DP*	HDMI*
Number of Ports	2 (x4)	1 (x4) (DDI-2)	1 (x4)[1] DDI[1:0]	1 (x4)[1] DDI[1:0]
Maximum Resolution	1x4: 1920 × 1080 @ 60 Hz (without compression) 2x4: 2560x1600 @ 60 Hz (without compression)	4096 × 2160 @ 60 Hz, with SSC	4096 × 2160 @ 60 Hz, with SSC	4096× 2160@ 60 Hz
Data Rate	1.0 GT/s	5.4 GT/s	5.4 GT/s	5.94 GT/s
Standard	DPHY1.1	eDP*1.4	DP*1.2a	HDMI* 2.0a
Power gated during S0ix w/display off	Yes	Yes	Yes	Yes

Table 3-10. Display Features (Sheet 2 of 2)

Feature	MIPI*-DSI	eDP*	DP*	HDMI*
DRRS (Refresh reduction)	Yes (M/N pair)	Yes (Panel command)	N/A	N/A
Self-Refresh with Frame buffer in Panel	Yes (Command Mode)	Yes (PSR)	No	No
Content-Based back light control	DPST6.0 LACE DPST	DPST6/CABC LACE DPST	N/A	N/A
HDCP 2.2	N/A	N/A (ASSR support)	Yes	Yes
PAVP	AES-encrypted buffer, plane control, panic attack			
SEC	All display registers can be accessed by CEC			
HD Audio	N/A	N/A	Yes[2]	Yes
LPE Audio	N/A	N/A	Yes	Yes
Compressed Audio	N/A	N/A	Yes	Yes
VDSC (display stream compression)	Yes	Yes	N/A	N/A

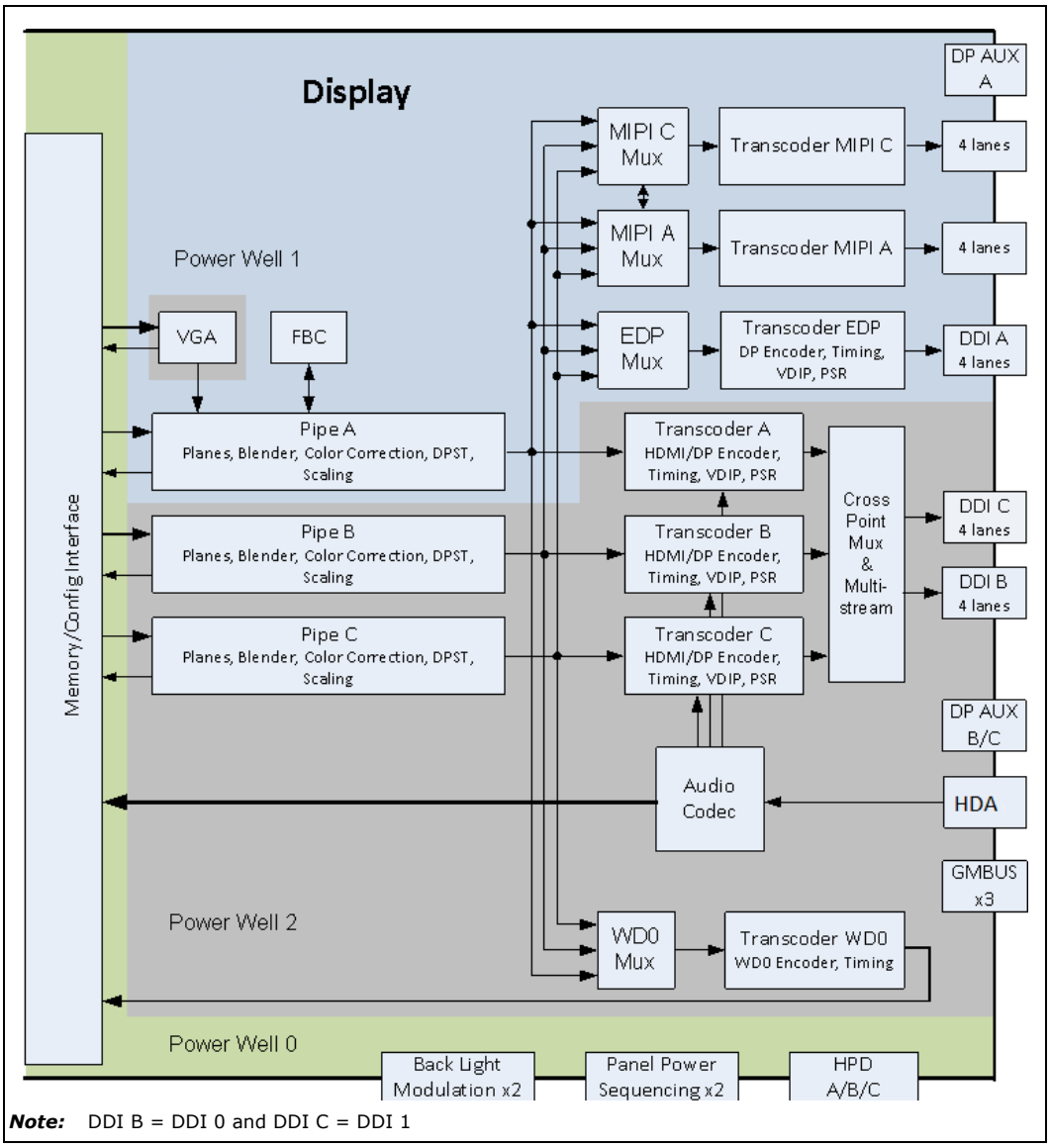
Notes:
1. SoC can support 2 HDMI or 2 DP ports, or one of each.
2. DP audio is limited to two-channel only.

The Generation 10 Display Engine comes with the following features:

- 2PPC to support 4K Display at Vmin
- Rec2020 [color space used for HDR]
- P010/012/016 formats
- HDR static metadata on HDMI
- 7x7 4K high quality scaler
- HDCP2.2
- HDMI2.0
- LACE DPST on pipe A
- 3D Lookup table on pipe A
- CoG 2x2 and 2x1 on eDP
- VDSC on eDP

3.4.2 Display Controller Block Diagram

Figure 3-7. Display Controller Block Diagram



Note: DDI B = DDI 0 and DDI C = DDI 1

Table 3-11. Port Configuration (Sheet 1 of 2)

PORT	MAIN LINK	SIDE BAND	HPD	TYPE
HDMI	4 Lanes 25-300MHz	I^2C	Yes	External

Table 3-11. Port Configuration (Sheet 2 of 2)

PORT	MAIN LINK	SIDE BAND	HPD	TYPE
DisplayPort (DP)	1 - 4 lanes 1.62, 2.7, 5.4GHz	AUX	Yes	External
Embedded DisplayPort (eDP)	1 - 4 lanes 1.62, 2.7, 5.4GHz	AUX	Yes	Internal
MIPI	1-8 lanes	I^2C	No	Internal

3.4.3 Overview of MIPI DSI

The SoC MIPI DSI interface consists of one clock lane and four data lanes. Data lane A0 is the bi-directional data lane for Pipe A. It can receive data from a read command or other messages sent from the display panel.

The output of the display pipe is then formatted to a stream of pixels with necessary timing that is compatible with a specific display port specification like MIPI DSI or and sends out through a physical layer interface.

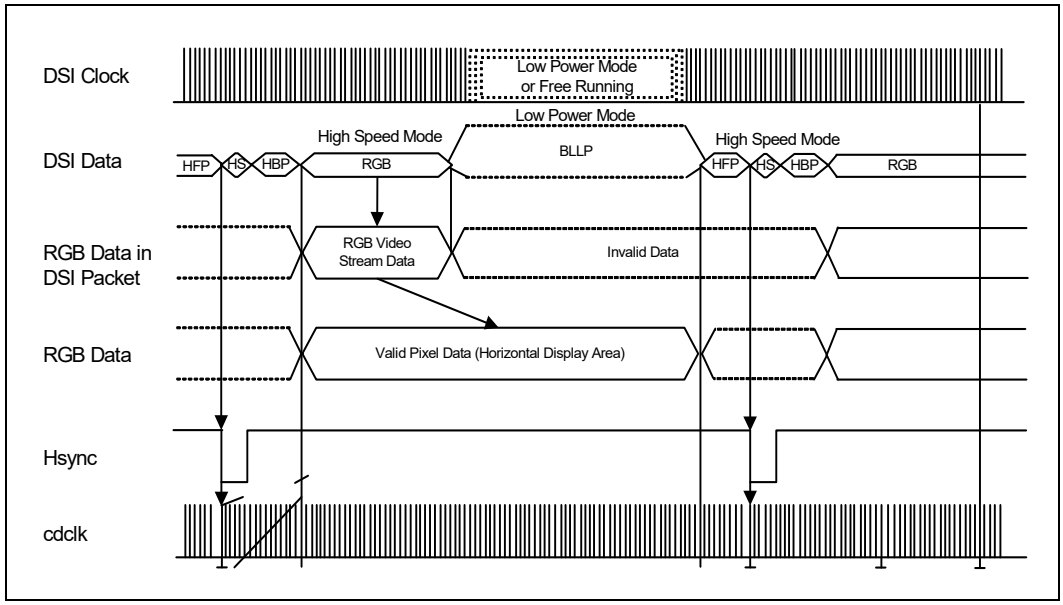
DSI specification identifies two distinct classes of displays:

- Command Mode:
  - Here, displays have a full frame buffer and timing controller on the display panel. Pixels, or commands, are sent to the display panel only when the image is modified in some way. The on-panel controller constantly reads out scan lines of RGB data from its local frame buffer, and refreshes the displayed image. In this architecture, the system can shut down the link between host controller and display to save power. The visible image will be maintained.
  - Type 1 based display architecture with Type A signaling is used by the SoC.
- Video Mode:
  - Here, displays do not have a full frame buffer on the display panel. Instead, they rely on the host processor to store the frame to be displayed, and a constant stream of display refresh traffic from the host processor's display controller to the display panel keeps the image visible and updated on the display. If the link between host processor and display panel is shut down, the image will be lost. Some video-mode displays have a partial frame buffer which enables refresh from the on-panel frame buffer at reduced resolution and/or reduced pixel depth, permitting the host controller link to be shut down to save power.

Video mode is classified as follows, as non-burst mode and burst video mode:

- Burst Video Mode:
  - The below diagram illustrates the operation of burst video stream as DSI packets as received from the DPI interface. In this mode, during the switch over to low power mode, DCS read request commands can be issued to DBI interface. A second channel can be addressed with the limitation of the left out bandwidth of the burst video mode.

Figure 3-8. Burst Video Stream



- Non Burst Video Mode:
  - The below diagram illustrates the operation of non-burst video stream as DSI packets as received from the DPI interface.

Figure 3-9. Non-Burst Video Screen

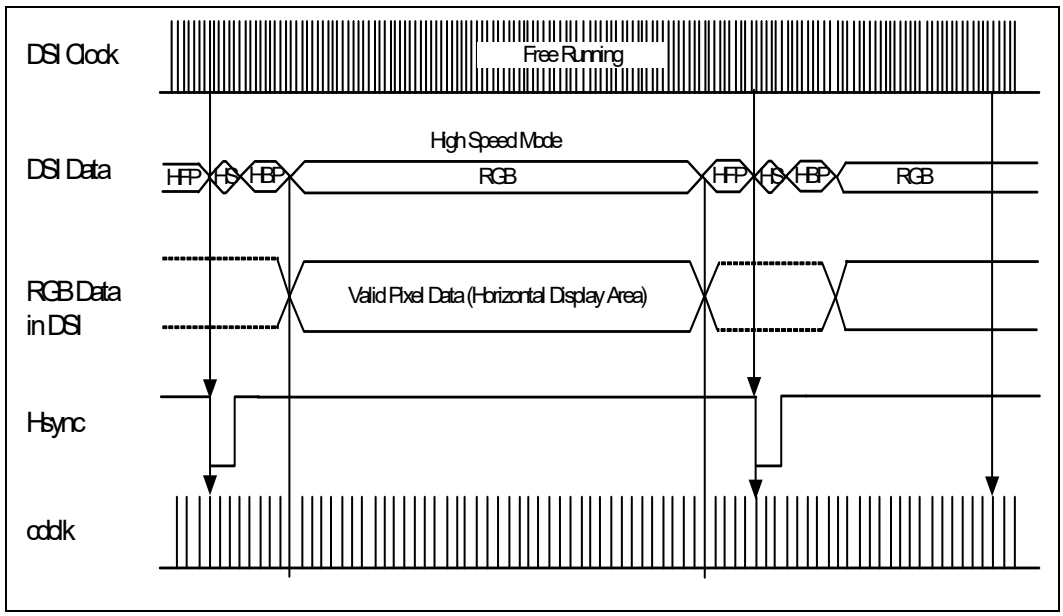


Figure Definitions:

- HFP: DSI Blanking Packet: Horizontal Front Porch
- HS: DSI Sync Event Packet: H Sync Start, H sync end
- HBP: DSI Blanking Packet: Horizontal Back Porch
- BLLP: DSI Packet: Arbitrary sequence of non- restricted DSI packets or Low Power Mode including optional BTA
- RGB: DSI Packet: Arbitrary sequence of pixel stream and Null Packets

3.4.3.1 Video Mode Stream To DSI Packets

DSI timing is conveyed over the DSI serial link as stated below:

Figure 3-10. Timing Parameters in Display Plane

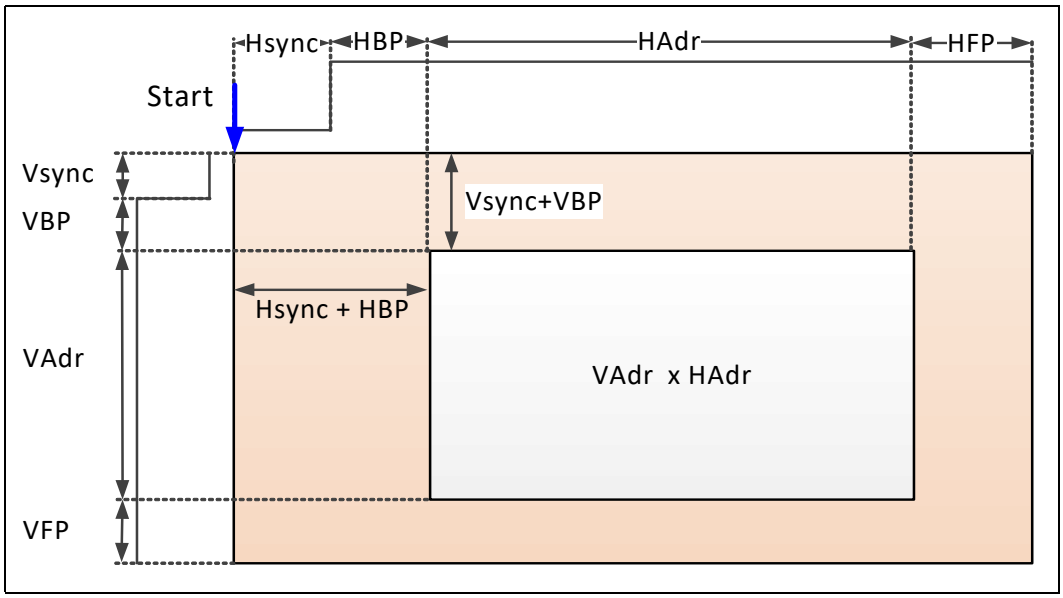


Figure Definitions:

- VFP: Vertical interval when no valid display data is transferred from host to display
- HFP: Horizontal interval when no valid display data is transferred from host to display
- Vsync+VBP: Vertical interval when no valid display date is transferred from host to display
- Hsync+HBP: Horizontal interval when no valid date is transferred from host to display
- VAdrxHAdr: Period when valid display data are transferred from host to display module

Figure 3-11. DSI Packet Flow for Non-burst Communication with Start and End with Video Mode Panels

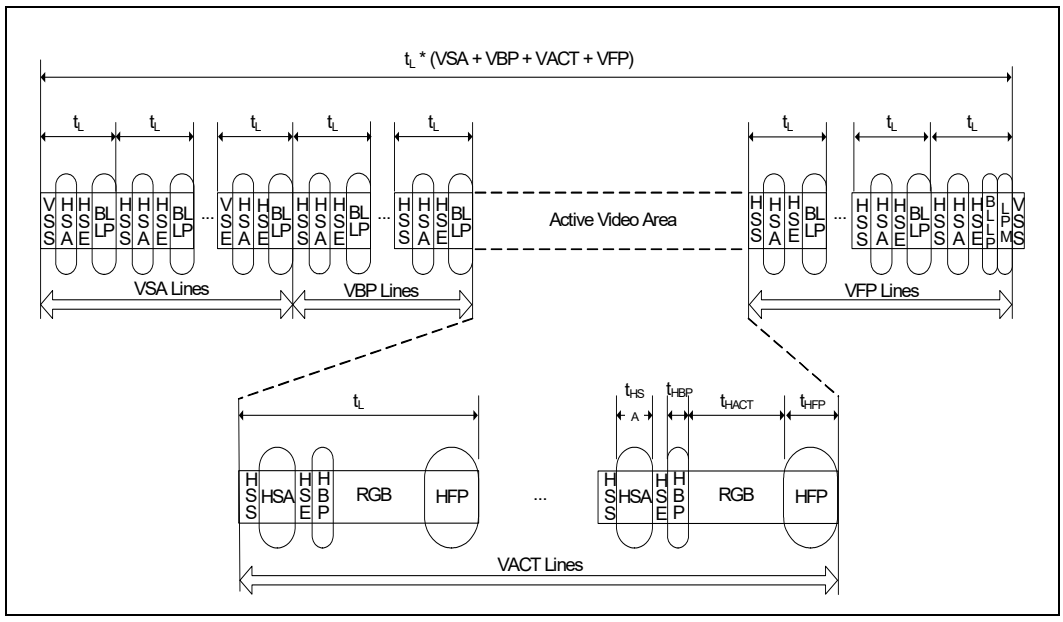


Figure 3-12. DSI Packet Flow for Non-burst Communication with Sync Event with Video Mode Panels

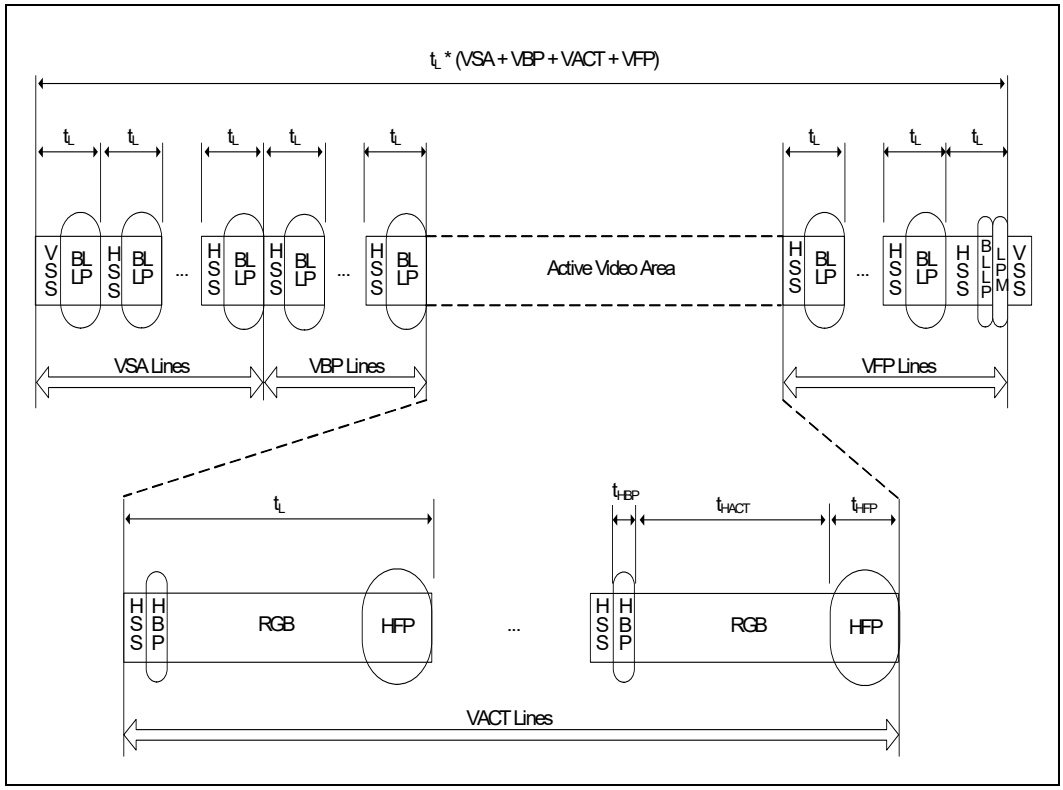
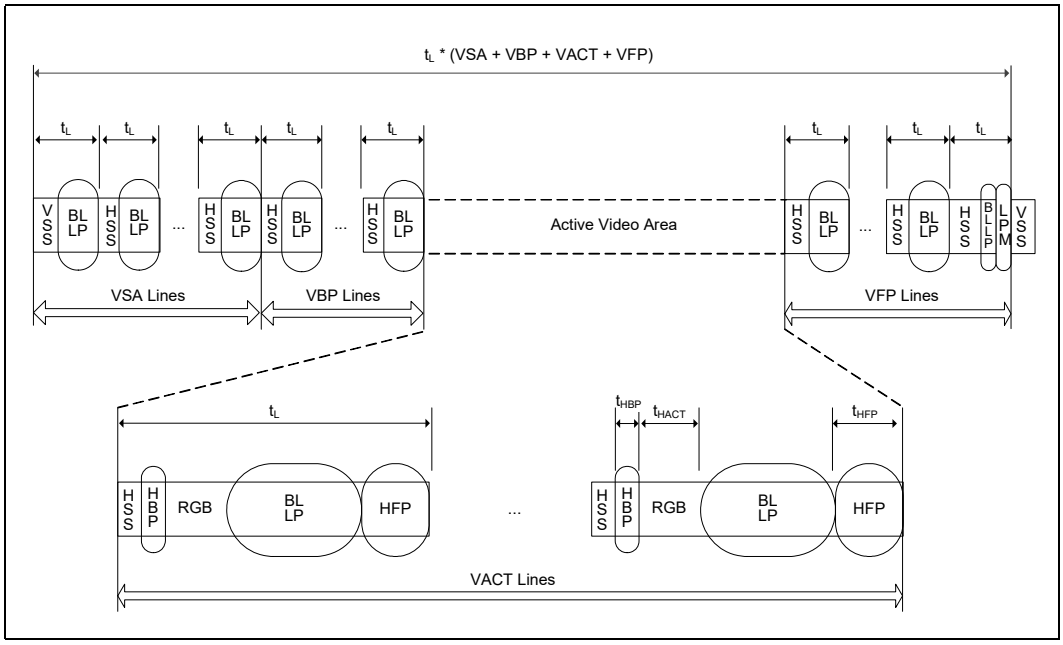


Figure 3-13. DSI Packet Flow for Burst Communication



3.4.3.2 DSI PHY Impedance Compensation (RCOMP)

The SoC contains impedance compensation logic for both the High-Speed Transmitter/ Receiver (100 W differential) and the Low-Power Transmitter (approximately 150 W single ended) to meet rise/fall time and slew-rate specifications.

- The Impedance Compensation process periodically adjusts the driver characteristics to compensate for process, temperate, and voltage variations.

3.4.4 Overview of HDMI Interface

HDMI is a 3.3-V interface that uses TMDS encoding, and requires an active level shifter to get 3.3-V DC coupling. It carries digital video and audio together on the same channel to the external digital display.

3.4.4.1 HDMI Audio Silent Mode Support

HDMI Audio silent mode support is required to meet HDMI specification. In normal audio playback the hardware uses a DMA to fetch audio data from memory buffers. The software driver can enable different buffers, and based on configuration the hardware can be pointed to one buffer at a time. When enabled, a buffer is played until it is completely read by the DMA and sent to HDMI interface.

In silent mode, the software will not enable any of the audio buffers and hardware is required to play zero data.

3.4.4.2 Hot-Plug Sequence

The Hot-Plug sequence can happen when the system is in any state, excluding S3-S5. A HDMI hot-plug event is interpreted only by the HDMI driver. The sequence of hot-plug is as following:

- Driver may force the system to power down a HDMI device when cable is connected, if no media is playing.
- HDMI sink voltage will contact with TMDS terminals when a cable is connected, but SoC TMDS is still in tri-state.
- 5V short protecting is only active when the HDMI device is in active state.

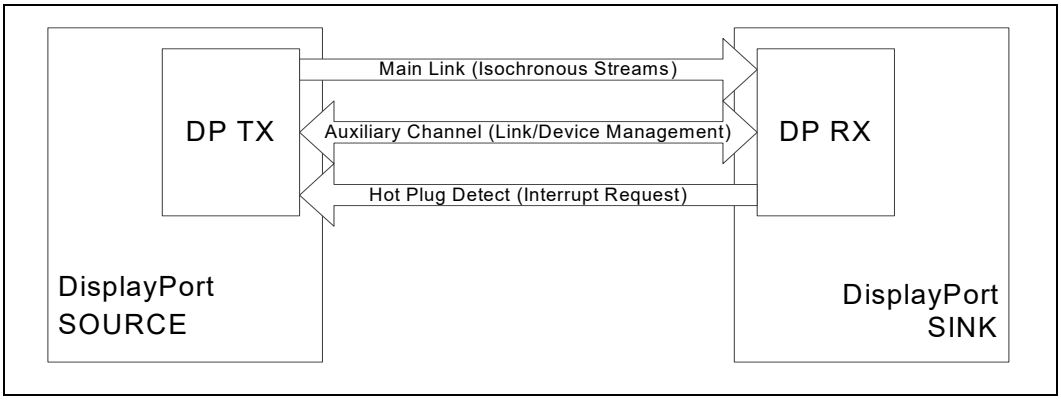
3.4.5 Overview of Display Port

Display Port is a digital communication interface that utilizes differential signaling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. Display Port is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

A Display Port consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The SoC supports DisplayPort Standard Version 1.2a.

Figure 3-14. DisplayPort* Overview



3.4.6 Overview of Embedded DisplayPort (eDP)

Embedded DisplayPort (eDP) is a embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. Like DisplayPort, Embedded DisplayPort also consists of a Main Link, Auxiliary channel, and a optional Hot Plug Detect signal.

The eDP port can be configured for up-to 4 lanes.

The SoC supports Embedded DisplayPort Standard Version 1.4.

3.4.6.1 DisplayPort Auxiliary Channel

A bidirectional AC coupled AUX channel interface replaces the I^2C for EDID read, link management and device control. I^2C-to-Aux bridges are required to connect legacy display devices.

3.4.6.2 Integrated Audio over HDMI and DisplayPort

SoC can support two audio streams on DP/HDMI ports. Each stream can be programmable to either DDI port. HDMI/DP audio streams can be sent with video streams as follows.

LPE mode: In this mode the uncompressed or compressed audio sample buffers are generated either by OS the audio stack or by audio Lower Power Engine (LPE) and stored in system memory. The display controller fetches audio samples from these buffers, forms an SPDIF frame with VUCP and preamble (if needed), then sends out with video packets.

3.4.6.3 High-Bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor, and TV). The SoC supports HDCP 1.4 (wired)/2.2 (wireless) for content protection over wired displays (HDMI, DisplayPort and Embedded DisplayPort).

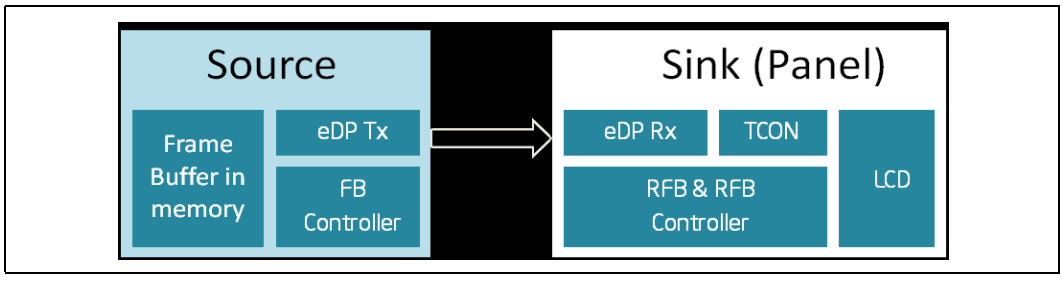
3.4.7 More Features of Display Controller

3.4.7.1 Panel Self Refresh (PSR)

PSR is an eDP feature that allows refresh to stop when the image is unchanging. DE can disable the eDP link and stop reading pixels from memory. The panel stores the unchanging image in it's Remote Frame Buffer (RFB).

DE tracks image changes and automatically enters and exits PSR. PSR2 adds several enhancements, including selective update.

Figure 3-15. Panel Self Refresh Diagram



3.4.7.2 Frame Buffer Compression (FBC)

- FBC compresses pixels as they are displayed
- Compressed data is written into graphics data stolen memory
- Compressed data is fetched the next time a line is displayed

- Power is saved through reduced read bandwidth and increased time between reads
- Changes to the frame buffer are tracked for invalidation

3.4.7.3 Other Power Saving Features

- DPST (Display Power Saving Technology)
  - — Preserves image quality while saving power by reducing backlight brightness
- Dynamic Refresh Rate Switching (DRRS)
  - — Software reduces eDP refresh rate based on activity to reduces memory bandwidth and panel power
- Port compression for eDP
  - — Reduce number of I/O lanes for a given resolution
- Render Compression, NV12
  - — Pixel data is a compressed format to reduce memory bandwidth power
- Rotation DE rotates 90, 180, 270 degrees. Saves power on GT processing steps.

3.5 Audio

Table 3-12. Audio Controller Features

Category	Description
I2S/SSP Interfaces	Three I2S/SSP Interfaces for platform peripherals
DSPs	Two high-performance DSPs configured with: • 32kB 4-way set associative L1 Instruction Cache • 64kB 4-way set associative L1 Data Cache
L2	• L2 Memory controller with the local high-performance interconnect fabric • L2 Cache Controller with cacheing and prefetch capabilities
ROM Size	8 kB ROM
DMA Interfaces	Two, 8-channel universal DMA interfaces for transferring data between memory buffers and peripherals and between memories
DMIC Interfaces	Two, dual-channel **D**igital **MIC**rophone (DMIC) interfaces
HD Audio and LPE Audio	• Supports HD-Audio and LPE Audio for DDI [1:0] (DisplayPort and HDMI)
CODEC	• Supports one external CODEC for attaching audio peripherals
Burst Mode	Local power sequencer for burst-mode data processing in micropower modes (S0ix)

The number of I2S ports has been reduced from 6 to 3 (2 dedicated and 1 multiplexed with HD Audio GPIOs).

SoC will update to GNA hardware speech acceleration engine that adds DNN algorithms (dynamic neural networks).

3.5.1 Audio Subsystem Integration

The Audio Cluster is delivered as a completely configured unit containing the following:

- Two high-performance DSPs configured with 16kB 4-way set associative L1 Instruction Cache and 48kB 3-way set associative L1 Data Cache.
- Two segments of Sonics SSX interconnects bridged through SonicsExpress components.

- L2 Memory controller with the local high-performance interconnect fabric.
- L2 Cache Controller with caching and prefetch capabilities.
- Address translation lookup table for translating the addresses of data structures in the DSP address space into 64-bit addresses in the host address space.
- Host Master interface for outbound transactions to host memory and peers. The interface is capable of generating 64-bit addresses, has 64-bit data width and operates at 200MHz.
- Target Interface with PCIe* Configuration space supporting 64-bit PCI descriptors. The interface has 64-bit data width and operates at 200MHz.
- Two universal DMA interfaces for transferring data between memory buffers and peripherals and between memories.
- Dual-channel Platform HD-A controller.
- Local power sequencer for burst-mode data processing in micropower modes (S0ix).
- HD-A iDISP link controller for sending data samples for HDMI output interface.
- DSP On-chip Debug interface with two JTAG ports.

3.5.2 Audio and Voice Interfaces

- 3 bidirectional I2S Interfaces for platform peripherals
- Two dual-channel PDM directly attached microphone interfaces, each interface supporting two MEMS microphones.
- The AUC has one single-link 24MHz HD-A interface as a configuration option.
- The AUC supports HD Audio link [7 input DMA and 6 out DMA]

3.5.3 HD-Audio to HDMI Interface

The audio stream to on-die HDMI display interface is provided through on-die serial iDisp link. This link is able to carry up to **8 channel audio directed to the HDMI interface.**

The following formats are supported:

- 2-channel L-PCM Audio (IEC 60958, HDMI layout 0) with sampling rate 48KHz (or 44.1KHz) and 16 or 24-bit sample width.
  - OR, with sampling rate 44.1KHz and 16 or 24-bit sample width.
- 8-channel L-PCM Audio (IEC 60958, HDMI layout 1) with sampling rate 48KHz (or 44.1KHz) and 16 or 24-bit sample width.
- Single Multi-channel compressed Audio stream (IEC 61937, HDMI layout 0) with sampling rate 48KHz (or 44.1KHz).

Other formats as specified in **HDMI 2.0a** is supported.

3.5.4 Local Memory

The memory architecture allows for the operation of the Audio Cluster without frequent accesses to DDR in order to save power and keep DDR memory in the system in self-refresh mode when audio processing is primarily done in the audio cluster autonomously.

- L2 RAM – total 640kB split into low power (128kB) and high performance (512kB) sections.
- Two-way L1 dedicated Instruction Caches 16kB (2x16) per DSP core.
- Three-way L1 dedicated Data cache 48kB (3x16) per DSP core.
- 8kB ROM with the boot loader code accessible to the DSPs with minimum power consumption.

The uncorrectable Memory errors generates interrupt request to the DSP that requested the transaction which resulted in error.

3.5.5 Clocks for Audio Cluster

The audio cluster uses the following clocks in different power states:

- Audio I/O Crystal Clock = the 19.2MHz clock produced by the crystal oscillator. This clock drives internal wall clock and audio sample timing in the AUC, and is used as a source of Bit Clock in audio peripherals.
- Audio I/O PLL Clock = the 24.576MHz clock produced by the PLL referenced from crystal oscillator (ratio = 32/25).
- Calibrated Ring Oscillator Clock = the 400MHz ±5% clock produced by low-power ring oscillator. It is internally divided to produce 100MHz clock for the low-power fabric in S0 state.
- HD-Audio PLL audio Clock = the 96MHz ±50ppm clock generated by the SoC PLL. This clock is expected to be available only in S0 state and is used for HD-Audio link interfaces. The AUC uses this clock only in D0.

There are no internal clock generators or PLLs in the AUC; all internal and interface clocks are produced from the clock sources listed above.

3.5.6 Power Management

AUC operations is supported in following states:

Table 3-13. Supported Power States

	S0	S0 IDLE with Display OFF	S0ix/D0i3	S0ix/D3	S0i3	Sx(3-4)/D3
Wake on Voice (WOV)	Yes	Yes	Yes	No	Yes	No
Playback	Yes	Yes	Yes	No	No	No
Note: If WOV capability is enabled.						

3.5.7 Burst Power Processing

The AUC supports burst mode in S0 state, using the local power sequencer and PMC communication.

3.5.8 Operation Modes

The I2S will be used for communicating with the audio peripherals. SSP ports MUST stay active and able to transfer data from memory buffers when the DSP and/or host are in power gated state. They MUST be able to wake the fabric and DMA controllers when the FIFO is filled above the threshold.

SSP ports MUST stay in low power state with the clock disabled when the communication with the audio peripheral is disabled.

The audio peripherals MUST operate in any combination of the following modes selectable individually for each SSP port:

- **Slave mode** – The SoC provides master clock reference, and interface (typically called MCLK) and bit clock (BCLK) to the peripheral. If the desired audio sample rate is Fs, then BCLK and MCLK are in integer relationship with Fs. In this mode, clocks will be synchronous with the SoC source (PLL or crystal) and there is no need to do a variable rate resampling. Note that the master clock reference will be constrained by a low jitter in many peripherals. The typical example of a Slave peripheral is a ADCs or DACs.
- **Slave mode with locally generated Master Clock** – The master clock is provided by means (crystal oscillator or PLL) located on the peripheral device, while BCLK is provided by SoC. In this case, the provided clock is used in the interface section of the peripheral device only, and will not be constrained by the low jitter. The peripheral may have an internal sample rate conversion if needed by design. A typical example is an FM radio or Bluetooth* transceiver.
- **Master Mode** – In this mode the BCLK are generated by the peripheral device from their local references, and fed into SoC. MCLK is provided by the SoC. The sample rate is asynchronous to the local SoC crystal references, and **due to the unknown difference between SoC and peripheral crystal frequency, the sample rate received from such an interface is unknown.** In this mode, the I2S interface must contain a clock estimation circuit, and the signal path must contain a variable rate re sampler which brings the sample rate in synchrony with the local SoC clock generator. A typical example of such device is inputs from S/PDIF or HDMI interfaces, broadcast receivers and cell phone modems.

The AUC has an independent BCLK generators with M/N dividers for each SSP port instantiation for operating them in master mode. The software will be able to update M/N ratio “on-the-fly” at any point in time even if the clock generator is active.

Only one (“global”) source of the audio clock is permitted and also serves as a common audio wall clock; all SSPs will use this clock. Note that global clock applies only to I2S and DMIC interfaces. The HD-Audio interface and iDisp interface always operate on a separate clock from the iCLK PLL.

3.5.9 Audio Cluster Functionality

The Converged Audio Cluster Unit (AUC) performs front-end pre-processing of the audio sample streams coming from microphones, codecs, radios and other sources, filters and applies noise reduction, acoustic echo cancellation and quality enhancement algorithms, and passes these streams to the host CPU or output stage of the audio signal chain.

The audio cluster is used for offloading routine high performance and low power audio operation from the CPU and let it concentrate on critical computational tasks and user interface or sleep when these tasks are not running. This approach creates a new paradigm for power management, when the peripheral devices are fully operational while the host is frequently placed in power conserving sleep state and may be waken by the smart peripherals.

3.5.10 Wake on Voice

The SoC supports Wake on Voice (WOV) from S0ix. As a part of front end processing, the AUC will always listen to the environment, recognize human voice activity, and detect the selected key phrases with optional speaker authentication. When the voice command from authenticated user is encountered, the AUC will wake the host CPU. The AUC will act as a pre-processor in this application.

The AUC also performs back-end post processing of the audio sample streams coming from either front end sources (like pre-processed microphone streams) or from the host subsystem. The streams are mixed and additional per-stream and global per mix effects are applied to them. These effects may be dynamic range compression or expansion, frequency equalization, sample rate conversion, stereo panorama enhancements and other creative effects. The outputs are played through headphones and speakers or passed on to voice band modem for phone calls.

The functions of the signal processing are determined by the DSP firmware; the signal route and the current functionality is set up by control application(s) running on the host CPU.

3.5.11 System Code and Data Security Approach

The audio cluster DSPs MUST be allowed to run authenticated third party firmware. The authentication MUST be performed by the TXE as the service. The AUC calls the TXE services through TXE interprocessor communication interface between TXE and AUC.

The AUC also interacts with the audio driver through Host interprocessor communication interface. Both interfaces are implemented as memory-mapped (primary interface) registers.

3.5.12 Audio DRM Support

The hardware decryption of the audio content will not be provided in cAVS v.1.5.

3.6 Power Management

The SoC supports different power modes providing significant power optimization.

Table 3-14. Power Management Supported Features

Category	Description
ACPI	Support ACPI 5.0
Processor C-States	C0, C1, C1E, C6, C6L, C7, C7L, C8, C9, and C10
Processor Module States	MC0-CC0, MC0-CC6, MC7
Display states	D0, D1, D2, D3, D4, D5, and D9
Graphics States	RC0, RC1, RC6
System Sleep States	S0, S0ix, S3, S4, S5
Power States Management	• Active-state power management — Performance control inputs received from platform firmware and software — Physical constraints observed through sensors in the package — Operating points determined to maximize power performance and energy efficiency • Idle-state power management • Flexible platform states to support phone and tablet usage models • Supports minimal device-to-device operations while most of the package is quiesced • Autonomous power gating
Other Power Features	• Support thermal management • Integrated Sensor Hub (ISH) — Supports “always on” sensing in S0ix modes

Table 3-15. Core C-state OS Definition

Core C-State Name	EAX[7:4]Mwait State Encoding	EAX[3:0]Sub-state encoding	ECX IF=0Break	Latency MSR (IRTL)	L2 Flush	Deepest Module C-state	Deepest S0ix state	Description
C0	1111	xxxx	0	n/a	N	MC0	S0	Skip MWAIT
C1	0000	xxx0	0/1	n/a	N	MC0	S0	Halt execution
C1E	0000	xxx1	0/1	n/a	N	MC0	S0	Halt execution, then drop core voltage and frequency
C6	0010	xxx0	0/1	PKGC6_IRTL (0x60b)	N	MC0	S0	Halt execution, flush core caches, flush core state, stop clock distribution, turn core voltage off
C6L	0010	xxx1	0/1	PKGC7_IRTL (0x60c)	N	MC0	S0	C6 with "long" latency IRTL
C7	0011	xxx0	0/1	PKGC6_IRTL (0x60b)	Y	MC7	S0i3	C7 – Same as C6, shrink LLC according to heuristics

Table 3-15. Core C-state OS Definition

C7L	0011	xxx1	0/1	PKGC7_IRTL (0x60c)	Y	MC7	S0i3	C7 – Same as C6L, shrink LLC in one step
C8	0100	xxxx	0/1	PKGC8_IRTL (0x633)	Y	MC7	S0i3	Same as C7 with C8-specific IRTL
C9	0101	xxxx	0/1	PKGC9_IRTL (0x634)	Y	MC7	S0i3	Same as C7 with C9-specific IRTL
C10	0110	xxxx	0/1	PKGC10_IRTL (0x635)	Y	MC7	S0i3	Same as C7 with C10-specific IRTL

3.6.1 Power Management Overview

This section describes the SoC power management architecture at a high level of abstraction. SoC power management has two parts:

- Primary Compute System (PCS) power management
- I/O Subsystem (IOSS) power management

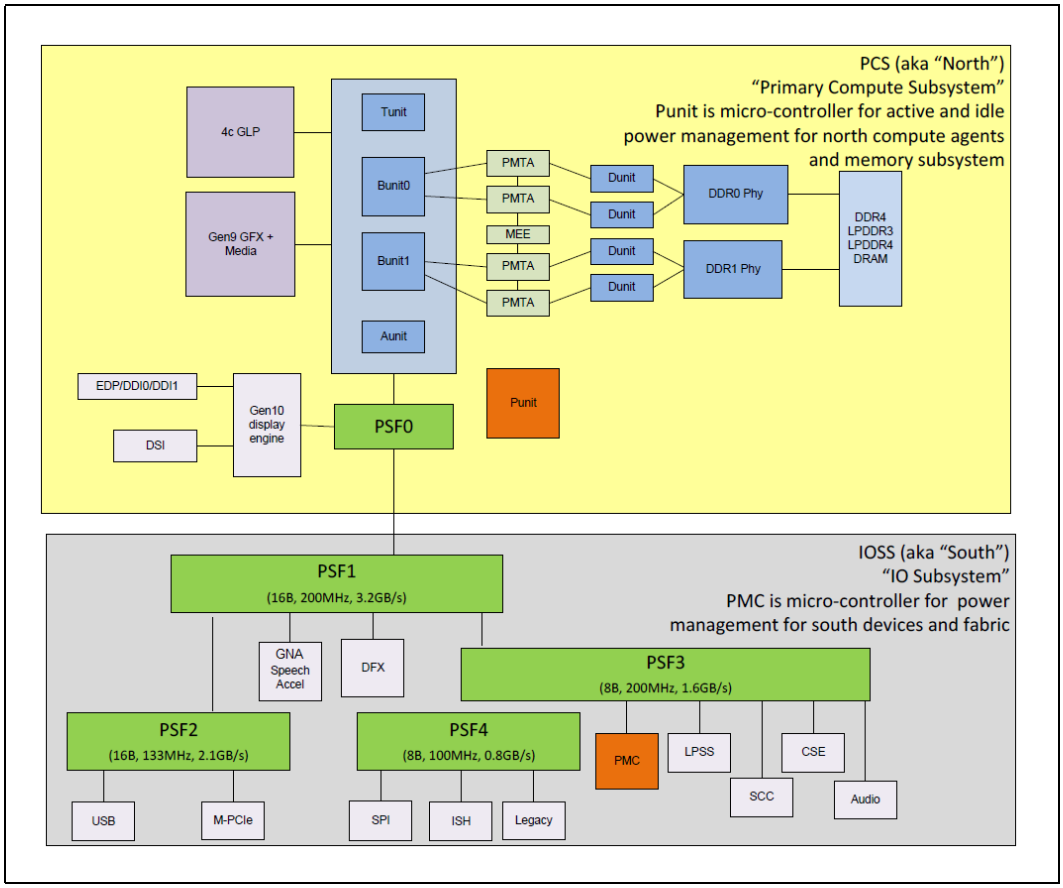
These partitions are illustrated in Figure 3-16.

P-Unit is the power management controller for the PCS (aka "North"). PMC is the power management controller for the IOSS (aka "South").

This chapter describes the SoC power management, including active state power management, power and current management, various level of power states, such as core C-states, module C-states, package C-states and S0ix.

Active state power management, power limiting and thermal management are SoC level power management features that are mainly executed by P-Unit. Low power states, Idle and S0ix are managed by both P-Unit and PMC.

Figure 3-16. PCS and IOSS Power Management Partitioning



3.6.2 P-Unit

3.6.2.1 Hardware Overview

The P-Unit is the power controller for the north complex or Primary Compute Subsystem (PCS) of the SoC. Its primary responsibility is power management of the IA cores, graphics engine (GT), system agent (SA), DDR interface, north IPs connected to (G-Unit, Display), etc. The functionality includes idle power management (C-states, S0ix, etc.), active power management (IA/GT P-states, turbo management, thermal management, etc.), reset, and much more.

P-Unit is the microcontroller that has specifically optimized as a power management controller:

- 8 KB IO register space
- Hardware State Machines
  - — Power and clock sequencer, dispatcher, timer, Voltage/SVID handler, CPU L2 voltage handler, L2 shrink/expand handler, Power-on SM, etc.
- 2 IOSF SideBand Endpoints (PM and SA)
  - — PM IOSF SB for IA, GT power management flow communication (replaces PMLINK).

— SA IOSF SB is used for IA/GT/PMC register interfacing.

— SB endpoints are bridged but segregated topologically.

The rest of the P-Unit is made up of various FSMs, registers, timers, and interfaces to the PM IOSF SB, Main IOSF SB, and PMC.

3.6.2.2 Firmware Overview

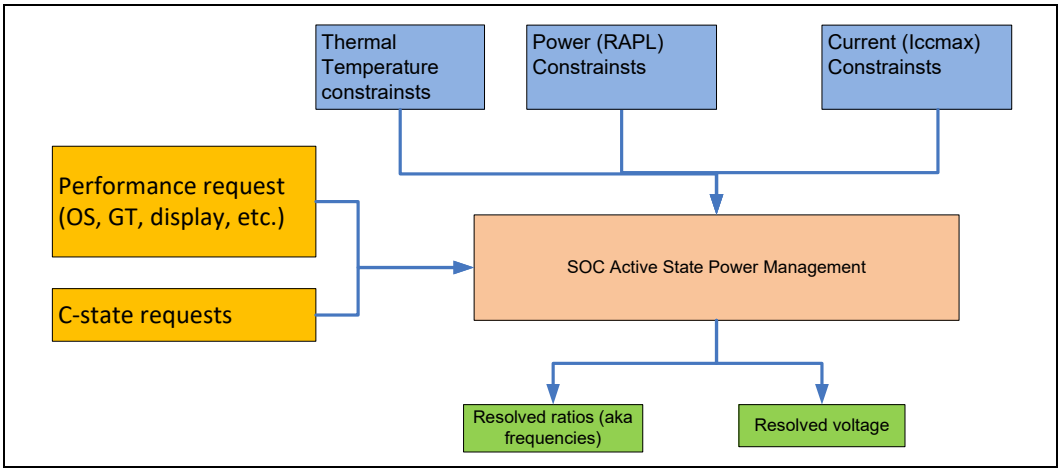
The Pcode firmware is the firmware which runs the P-Unit microcontroller. The control flow is composed of 3 major structural components: reset, slowloop and fastpath.

In run time, Pcode firmware is structured primarily as “slow” background tasks with “fast” critical event handling. “Slow” tasks are partitioned such that execution latency for each task is guaranteed to be less than some fixed limit and in between slow transactions “fast” events are checked for high priority processing. It is important that the slow loop transactions never leave any partially corrupted data structures for fast events to consume.

3.6.3 Active State Power Management

SoC active state power management involves taking all performance requests from OS and drivers, apply power delivery, power and thermal constraints to resolve a final voltage and frequency workpoint for PCS clock and power wells. Workpoints are actively managed for CPU cores, GT, Display, and SA. The primary goal of active state power management is maximizing performance requested by software, given power delivery and thermal constraints of the SoC and platform.

Figure 3-17. Overview of Active State Power Management



The primary actively managed power wells in PCS are as follows:

- VCC_VCG

  —Common power well used to supply cores, graphics. Voltage is set to the maximum of any domain level request. CPU cores have DSLDOs that allow them to run at lower voltage than VCC_VCG as needed.

- L2

—L2 cache used by the CPU module. This cache is supplied by a variable voltage LDO whose input is the Vdd2 / 1.24 V input supply. This voltage is always running at greater than or equal to the CPU core voltage (VCC_VCG or DSLDO).

- Vnn

  —Vnn supplies the entire system agent and nearly every block on the SoC. Vnn may be ramped up or down based on display frequency and voltage requirements.

3.6.4 Core Frequency Targets

3.6.4.1 P-state Requests

In ACPI terminology, a P-state is a visible frequency / voltage operating point. The OS and BIOS has the permissions to make P-state change requests.

3.6.4.2 P-state Table and _PSS Objects

On SoC, CPU core P-state targets correspond to the core clock ratio that is requested. For example, if software wants the part to run at 2.0GHz, it will write 20 into the OS P-state target value (100 MHz * 20 = 2.0 GHz). In order to determine the range of valid ratios, BIOS can read the max efficiency and maximum performance (turbo and non-turbo) encodings out of the IA32_PLATFORM_INFO MSR. This allows for a single BIOS revision to support multiple processors with different P-state/ratio definitions and capabilities.

Table 3-16. P-State Encoding Scheme

P-State	Encoding	Definition
P0	Turbo Operating frequency range	"P0" generally refers to a *range* of clock frequencies in the non-guaranteed region of the core performance. The OS may request the maximum P0 frequency and the SoC will deliver up to that clock frequency depending on environmental constraints such as power or thermal.
P1	Maximum Single Core Operating Point – 1	The first ratio down from the single core max turbo ratio, also known as MNT (Max Non Turbo) point in the past.
P2…PN-1	P1-1 … PN+1	Intermediate operating points.
Pn	Maximum Efficiency Ratio	Maximum efficiency operating point. This is the highest frequency that will run at the lowest voltage. Above Pn, there is both frequency and voltage scaling. Blow Pn, all ratios run at the lowest voltage, and there is only frequency scaling, no voltage scaling.
Pm	Minimum Ratio	Minimum operating point. This is the lowest frequency that will run at the lowest voltage.

3.6.4.3 OS P-State Requests

P-state requests are made by writing the target P-state encoding to IA32_PERF_CTRL MSR (0x199), which is defined per-thread.

3.6.4.4 Turbo Mode

3.6.4.4.1 ACPI P-States and Turbo Mode

In ACPI terminology, each ratio is exposed as a P-state. The maximum ratio of the part is exposed as the P0 ratio. The minimum ratio of the part that the OS is allowed to chose is exposed as the Pn ratio. The following table lists the classes of P-state requests and their meanings. Note that the per-core turbo limits, the guaranteed frequency of the part, and the maximum efficiency ratio of the part are defined by fuses.

3.6.5 Iccmax

3.6.5.1 Iccmax of SoC Rails

Platform voltage regulator (VR) is required to enable Iccmax to support worst case peak and sustained current and power consumptions in order to get the maximal performance that SoC enables. There is no configurable Iccmax control over all rails except VCC_VCG.

3.6.6 Fast Prochot

SoC supports fast prochot feature, when activated, throttle SoC logic within 100usec.

SoC allows SW to configure Prochot through programming firm_configuration MSR. SoC does not support bidirectional prochot, and prochot is configurable to either input only, or output only. Prochot# by default is an input pin.

When Prochot# is asserted (active low), SoC activates core uarch throttler and throttle all domains to Pm or Pn per configuration of FIRM_CONFIG.PROCHOT_RESPONSE [0=Pn (default), 1=Pm].

The PROCHOT# Pin mode is controlled by setting the virtual MSR, POWER_CTRL (i.e. P_CR_FIRM_CONFIG Punit I/O CR). The control bits and descriptions are listed below:

Table 3-17. Prochot Control Configuration Bits

Field Name	POWER_ CTL Bit Range	FIRM_ CONFIG Bit Range	Field Description.
ENABLE_BIDIR_PROCHOT	0	2	Reserved. Not used anymore. Set this field in FIRM_CONFIG register to RO. Default = 0.
PROCHOT_OUTPUT_MODE_DISABLE	21	11	Used to enable input-only PROCHOT. When set to 1, PROCHOT output is disabled and PROCHOT is input-only. Default = 1.
PROCHOT_RESPONSE	25	12	0: Go to Pn on incoming PROCHOT. 1: Go to a state lower than Pn on incoming PROCHOT. Go to Pm on incoming PROCHOT. Default = 0.
PROCHOT_LOCK	23	13	When a 1 is written to this bit, all PROCHOT-related bits listed here (including PROCHOT_LOCK itself) are locked and become read-only.

3.6.7 Ratio Voltage Resolution

When one or more compute agents are active, the power control logic adjusts the operating conditions as needed to reflect request of the SW (i.e. operating system and/or drivers) and the physical temperature and power related constraints. In most cases, objectives are met by adjusting the target frequency of one or more compute agents. The PUNIT is responsible for adjusting compute agent's target clock speed to a discrete operating point. The discrete steps between each of these operating points correspond to compute agent clock ratios. As the target frequency is changed, the operating voltage is also adjusted as required to guarantee correct operation at the new frequencies, and to minimize power consumption at the operating points. Essentially, the operating voltage is adjusted to be just high enough to operate all the circuits at the new target frequencies.

Several factors contribute to the operating point of an active core at any given instant, and the resolved target ratio of all active cores is the minimum of all ratio limits for cores:

- Resolved P-state request
- Max Turbo Limit
- Thermally limited ratio
- RAPL limited ratio
- Prochot limited ratio
- Iccmax limited ratio

Based on a snapshot of these factors, the PUNIT ratio resolution algorithm determines a target ratio and associated voltage (VCC_VCG and LDO voltage) for the core module. When a core is idle (in a lower power C-state than C0), its voting rights can be suspended. The resolved operating point is the highest requested operating point of all active cores.

When resolving the operating point of an individual core, the various contributing factors are weighed independently to come up with three ratio targets: the OS P-state request, the thermally constrained operating target, and the power constrained operating target. The upper and lower bounds of these targets are dictated by fuses in the CPU. These three targets are then weighed and resolved to final ratios for all cores, GT and the package as a whole. The definitions and details of these goals are described in the following sections.

Operating points of GT are impacted by multiple factors as well. At any given instant, and the resolved target ratio is the minimum of all ratio limits related to GT domain:

- GT driver performance request
- Max Turbo Limit
- Thermally limited ratio
- RAPL limited ratio
- Prochot limited ratio
- Iccmax limited ratio

On SoC, compute agents (core, GT) share one operating voltage rail VCC_VCG, and the maximum of all operating voltages required for all compute agents is the final operating voltage of the shared rail, including corrections needed for ITD (inverse temperature dependency).

On SoC, display, SA, MemSS and many other IPs share another operating voltage rail Vnn, and SoC implements algorithms that resolve the operating voltage based on multiple factors such as display DVFS request, temperature and ITD correction, voltage required for MemSS IPs, etc.

Display voltage changes are initiated via the GT driver mailbox, this is captured in the Display DVFS portion of the GT Mailbox section of this document. The mailbox routine is responsible for interpreting the CDCLK frequency request from the driver, selecting the appropriate voltage value, correcting for Inverse Temperature Dependency, and initiating the Vnn voltage change.

Once voltage of VCC_VCG and Vnn are resolved, SoC issues VID to VR to control voltage change.

3.6.8 T-State Support

SW can request T-state through THREAD_T_REQ, and SoC activates duty cycle throttling accordingly.

Note, thermal throttling safety algorithm defines another duty cycle level. SoC algorithm takes the min of the two inputs to configure CPU duty cycle register.

Table 3-18. T-State Supported

T_STATE_REQ	ON-time (OS Requested) %	CPU ON Time	CPU_DTY_CYC (CPU Register)
0000	50	50	100
0001	6.25	50	100
0010	12.5	12.5	111
0011	18.75	12.5	111
0100	25	25	110
0101	31.25	25	110
0110	37.5	37.5	101
0111	43.75	37.5	101
1000	50	50	100
1001	56.25	50	100
1010	62.5	62.5	011
1011	68.75	62.5	011
1100	75	75	010
1101	81.25	75	010
1110	87.5	87.5	001
1111	93.75	87.5	001

3.6.9 Optional Support for Power Delivery Cost Reduction

3.6.9.1 Enable Vnn as a Fixed Voltage Rail

SoC supports Vnn as a fixed voltage rail, with no SVID control neither IMON when VR is a SVID IMVP8 VR. This option is supported only if:

SMIP Register: BASIC_CONFIG, bit-0 "FIXED_VNN_VR"

0 (default) :Vnn VR is VID-controlled, through SVID or I^2C.

1: Vnn VR is a fixed voltage rail.

When the option is supported, Vnn is expected to be fixed at 1.05V to enable performance of all SoC logic, and customers can optionally source Vnn and Vccsram from one platform VR rail of 1.05 V.

3.6.9.2 Enable LPDDR4/DDDR4 Phy to Run on Vnn

SoC with LPDDR4 or DDR4, by default, has DDR phy run on Vccsram, and this is the best power and performance option for SoC with either LPDDR4 or DDR4.

SoC optionally allows LPDDR4 or DDR4 phy to run on Vnn, and Vnn is elevated to support up to 2400MT/s LPDDR4 and DDR4.

This option is supported only if:

0: SoC does not allow DDR Phy powered from Vnn (default)

2) OEM requests this by setting a SMIP input:

SMIP Register: BASIC_CONFIG, bit-1 "DDR_PHY_RAIL_OPTION"

3.6.10 Power Limiting Control

SoC supports MSR and MMIO as interfaces for RAPL (Running Average Power Limit). RAPL MSR interface is consistent with client implementation. The SoC does not support RAPL over PECI interface.

Energy status is always supported independent of enabling of the domain RAPL limits, and SoC supports energy status reporting for all four domains (pkg, DDR, IA and GT).

Note: For any tuning and/or power/performance optimization work, it is recommended to use package energy status and power, not domain (i.e. IA or GT) energy status.

The following table summarizes SoC RAPL support:

Table 3-19. Summary of Supported RAPL Interface

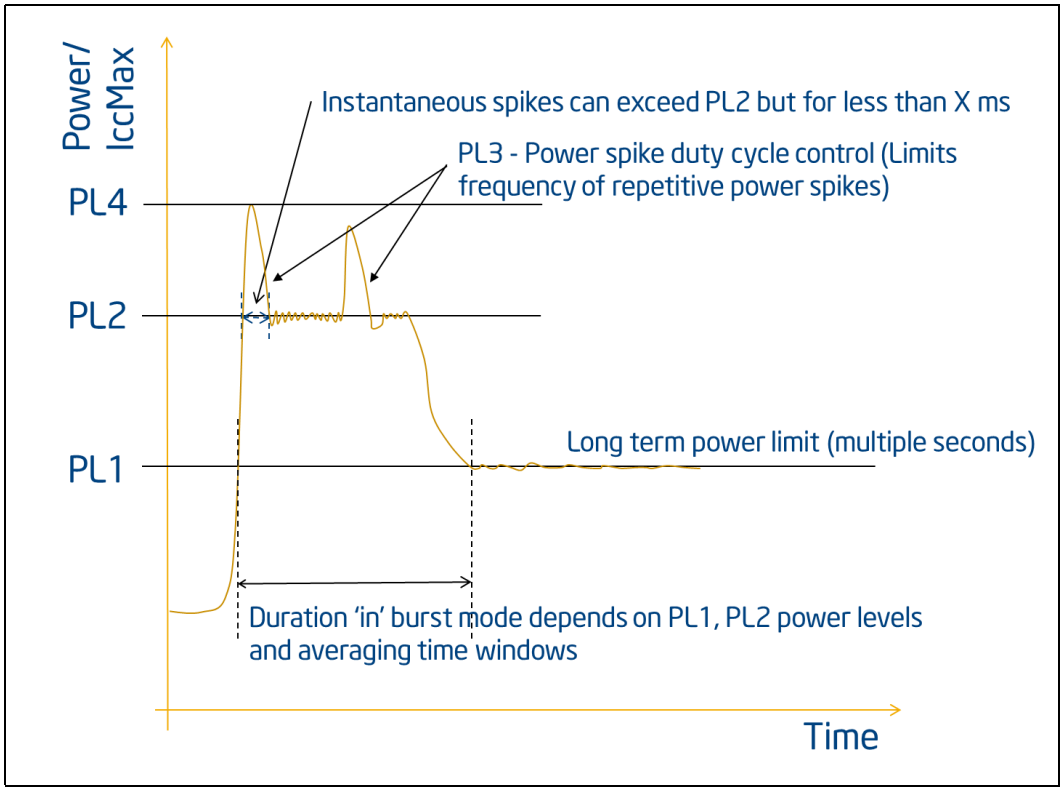
RAPL Interface	Configurable Limits	Energy Status	Perf Status
Package	MSR MMIO	MSR MMIO	No
DDR	No	MSR MMIO	No
IA	NA	MSR MMIO	NA
GT	NA	MSR MMIO	NA

Configurable PL1, PL2 for time Windows* 10 msec and higher are supported. SoC also supports PL3 that engages duty cycle throttling within 10 msec to keep PL3 excursion low and PL4/Pmax that keeps peak instantaneous current within configured limit.

Table 3-20. Summary of Active Power Limiting Interface

Knob	Control Time Scale	Control Domain	Inputs	Use Case
PL1	100ms - 10min	SoC (default) or SoC + Mem (configurable through BIOS mailbox)	Power Limit Time Window (tau)	Control average power over time window, typically for platform thermals
PL2	10ms-100ms	Refer above	Power Limit Time Window (tau)	Control average power over time window, typically for platform or power delivery thermals
PL3	2ms and up	Refer above	Power Limit Time Window (tau) Duty Cycle	Duty cycle control of peak power excursion. Used for managing battery or power supply lifetime degradation
PL4	Instant (a priori)	Refer above	Power Limit	Peak instantaneous power for battery or power supply voltage droop management.

Figure 3-18. Timescale of PLx Controls



3.7 PMC (Power Management Controller)

3.7.1 Overview

- The Power Management Controller subsystem is one of the first subsystem to be functional after reset. It is responsible for the following functionality:
- Conducting system boot flow
- Conducting Warm/Cold/Global resets
- Conducting Sleep state entry (S3/S4/S5—cold off)
- Collecting all wake events and Conducting system wake from sleep states (wake architecture)
- Maintain Timers
- Conducting S0ix entry/exit and wake from S0ix state
- Managing Power Rails
- Handling SMI (System Management Interrupt)
- Handling SCI events (System Control Interrupt)
- PMC uses SVID or I^2C interfaces for communication with PMIC (Power Management IC)

3.7.2 ACPI Timers

Three timers are implemented in the ACPI block.

Table 3-21. ACPI Timers

Timer Name	Function
TCO_TMR	TCO timer is a countdown watchdog timer used by SW to detect SW hangs.
swsmi_tmr	SW to trigger SMI after programmable timeout.
per_smi	SW to trigger SMI interrupt periodically.

All of the timers run off of the PMC functional clock but count off of counter signals.

Table 3-22. ACPI Timer Counter Signals

Timer Name	Change Signal
TCO_TMR	pmc_tick_100ms/6
swsmi_tmr	pmc_tick_1ms
per_smi	pmc_tick_1s

The PMC function clock can be switch from the CRO to the RTC via PMC_CLK_CTL.sel_rtc. The ACPI version of the PMC function clock is enabled via PMC_CLK_CTL.acpi_clk_en.

3.7.2.1 TCO Timer

TCO timer is a countdown timer used by SW to detect SW hangs.

SW should re-load the timer before it reach zero. Reload is accomplished by writing any value to TCO_RLD.tco_val.

If SW fails to re-load the timer before reaching zero, ACPI unit will send SMI interrupt. The SMI must be enabled in order for a S0ix wake to occur on the first expiration.

Timer will than reload 2.4 seconds timeout. If SW fails again to reload the timer, there will be an S0ix wake based on the second_to_sts bit and the ARC will be interrupted and will initiate Type 1 Warm Reset, if PMC_CFG.NO_REBOOT = 0.

TCO timer is loaded with the value stored in ACPI register TCO_TMR.tco_trld_val.

Timer counts down every 0.6 second.

SW or FW can halt the timer using ACPI bit TCO1_CNT.tco_tmr_halt.

Upon 1st expiration, SW should clear TCO_STS.tco_timeout in order to avoid 2nd expiration detection.

If FW ever ignores the interrupt event flag from a second expiration, when the OS is up, the tco_tmr_run should be disabled. This will happen during reset flow. The reason for this is, if TCO_TMR expires a second time, the HW will sets pmc.tco_sts.second_to_sts. On the next boot, BIOS would read this bit and decide to boot in a non-standard manner. It could boot in safe mode by accident.

TCO_TMR is the watchdog timer provided by the ACPI block. It is used by an OS monitor for OS crashes.

The watchdog timer uses a two stage bark and bite configuration. If and OS does not reload the timer and it expires, an interrupt is set and the timer is automatically reloaded. The first expiration interrupt is called a watchdog bark. If the bark interrupt is not handled/cleared and if automatic bark reload expires, the watchdog bite via a forced hardware reset. Forced hardware reset are only possible if the hardware watchdog resets are enabled.

3.7.2.2 Programming

The OS programs the TCO Timer, via the TCO_TMR.tco_trld_val register with an initial value in the initial stages of OS boot. The OS can halt the timer all together via TCO_TMR_HALT.

3.7.2.3 Reloading

An OS-based software agent periodically writes any value to the TCO_RLD register to reload the timer and keep it from generating the SMI (System Management Interrupt), Watchdog Bark. The software agent can read the TCO_RLD register to see if it is near to timing out, and possibly determine if the time-out should be increased. The OS can also modify the values in the TCO_TMR.tco_trld_val register.

3.7.2.4 Watchdog Bark—TCO First Expiration

If the timer reaches 0, an SMI (System Management Interrupt) can be generated. This should only occur if the OS was not able to reload the timer. It is assumed that the OS will not be able to reload the timer if it has locked up.

Note that an S0ix wake will only occur if the tco_tmr SMI is enabled.

Upon generating the SMI, the TCO Timer automatically reloads with the default value of 0x04, approximately 2.4 seconds, and start counting down.

An SMI handler can:

- Read and clear SMI_STS to see that TCO_STS cause the SMI.
- Write any value to the TCO_RLD register to reload the timer to make sure the TCO timer does not reach 0 again.
- The SMI handler should also clear the TCO_STS.TCO_TIMEOUT bit. If the TCO_TIMEOUT bit is left asserted the HW is fully reset to a unfired state.
- Attempt to recover. May need to periodically reload the TCO timer. The exact recovery algorithm will be system-specific.

3.7.2.5 Watchdog Bite—TCO Second Expiration

If the SMI handler was not able to clear the TIMEOUT bit and write to the TCO_RLD register, the timer will reach zero a second time approximately 2.4 seconds later. At that point, the hardware is assumed to be locked up, and the timer will read 0 a second time, which causes the SECOND_TO_STS bit to be set. At that point the logic wake from S0ix via the SECOND_TO_STS bit and will issue a Type 1 Warm Reset, if the reboots are enabled via PM_CFG.no_reboot.

During every boot, BIOS should read the SECOND_TO_STS bit in the TCO_STS register to see if this is normal boot or a reboot due to the timeout. The BIOS may also check the OS_POLICY bits to see if it should try another boot or shutdown.

3.7.2.6 Converting TCO SMI to SCI or NMI

Natively a TCO event can only produce and SMI. What follows are an example flows for how the host could convert the native SMI to an SCI or NMI.

In both examples:

- PMC generates and SMI.
- The host process the SMI in SMM handler.
- The host identifies the source of the SMI as a source it wishes to convert to an alternate type of interrupt.

SMI converted to SCI

- Host disables all sources of SCI except BIOS_RLS.
- If the host wishes to not trigger the normal SCI handler, BIOS should change the SCI vector in pmc.IRQ_SEL_2.SCIS.
- The host writes pmc.sci_en.BIOS_RLS to trigger the SCI event.

SMI converted to NMI

- The host writes the ITSS NMI_NOW bit in private config space. BIOS can write it through P2SB SBREG_BAR.

3.7.2.7 SW SMI Timer

SWSMI timer can be used by SW to trigger SMI after programmable timeout.

SWSMI timer counts via a PMC 1ms timer tick.

The timeout is configured using GCR register GEN_PMCON1.swsmi_ratesel[1:0].

swsmi_ratesel[1:0] decoding is as follows:

- 00 1.5 ms +/- 0.6 ms
- 01 16 ms +/- 4 ms
- 10 32 ms +/- 4 ms
- 11 64 ms +/- 4 ms

Timeout has some variance, as a free running mS strobe is used. Max and min variance are dependent upon which swmi_ratesel is selected, and listed above.

Changes to GEN_PMCON1.swsmi_ratesel can only be made when the timer is disabled.

GEN_PMCON1.swsmi_ratesel resets to 00 when pmc_vnnaon_pok is low.

Upon expiration ACPI bit SMI_STS.swsmi_tmr_sts will be set.

The timer is enabled using ACPI bit SMI_EN.swsmi_tmr_en. It defaults to disabled.

After SMI_STS.swsmi_tmr_sts fires, the timer must be disabled then re-enabled for the timer to count again.

3.7.2.8 Periodic SMI Timer

This timer is used by SW to trigger SMI interrupt periodically.

SMI period is configured by GCR register GEN_PMCON2.per_smi_sel[1:0] as follows:

- 00 64 seconds
- 01 32 seconds
- 10 16 seconds
- 11 8 seconds

When timer expires it will set ACPI bit SMI_STS.periodic_sts.

Writing new value to GEN_PMCON2.per_smi_sel[1:0] clears the timer.

3.7.2.9 PM1 Timer (Disabled/Removed)

The acpi_tmr, sometimes talked of as PM1_TMR, has been disabled and/or removed from the SoC because it was dependent on a 14.318Mhz clock which does not exist in SoC.

The non-existence of this timer is conveyed to the OS by setting the following bits to the specified value in the flags field (offset 112) of the FADT (per the ACPI 5.0 specification).

USE_PLATFORM_CLOCK[15:15] = 0

HW_REDUCED_ACPI[20:20] = 1

No hardware support for PM1 timer (14.318 MHz).

The CPU ucode will handle the PM1 timer and will return a properly scaled value. This is because some OSes require this timer to complete boot. Because the ucode does not have access to the SCI/SMI functionality these interrupts are not supported when the timer overflows. The PMC will never actually see reads to the PM1 timer.

3.7.3 IOSS PM/PMC Block Management

3.7.3.1 PMC Managed IOSS Blocks

Table 3-23. List of PMC Managed IPs (Sheet 1 of 2)

Block	SoC
PSF1	Y
PSF2	Y
PSF3	Y
PSF4	Y
SBR_IOSS	Y
SBR_PCS	Y
P2SB	Y
CUnit	Y
SPI	Y

Table 3-23. List of PMC Managed IPs (Sheet 2 of 2)

Block	SoC
XDCI	Y
XHCI	Y
USB2PHY	Y
USB3MODPHY	Y
PCIE0	Y
PCLKD	Y
MODPHYFIA	Y
Storage-SDC	Y
Storage-EMMC	Y
LPSS-SPI	Y
LPSS-UART	Y
LPSS-I^2C	Y
Audio	Y
TXE	Y
EXI	Y
Intel Trace Hub	Y
Intel Trace Hub VRC	Y
CCI	Y
CCP	Y
ICLK_XTAL	Y
ICLK	Y
GPx_CORE	Y (3)
ITSS	Y
RTC (SIP)	Y
TAM	Y
PCIE1	Y
LPC	Y
SMBUS	Y
PRTC	Y
SATA	Y
MODPHY (SATA cmn lane)	Y
SMBUS	Y

3.7.4 RTC Flows

The PMC only supports the on die RTC. SoC does not utilized PMIC-RTC wells. PMC FW disables RTC restoring from PMIC in boot flow. SoC added the RTC HIP because the functional oscillator and coin-cell backed power are on die.

3.7.5 Handling Host Access to On Die RTC SIP

The PMC is not involved in Host access to the RTC SIP. The Host still access the RTC SIP via port 0x70 and 0x71 but these messages are not forwarded to the PMC.

If PMC FW receives the forwarded IO NP, PMC should do nothing with these IO writes and just send back successful completions. In addition, there is no PMC sync of RTC at boot.

3.7.6 PMC Shadowing of Bits in the RTC Power Well

The PMC shadows a number of bits in the power well provided by the RTC HIP. This space is backed by a coin-cell battery. The type of things shadowed control the boot options for how the SoC should handle a G3 exit. The classic example is PMC.PMCON1.ag3. This BIOS controlled bit tells the SoC if it should go to S5 or S0 after power is restored on a G3 exit.

Table 3-24. PMC RTC Shadowed Bits with Address Map (Sheet 1 of 2)

Reg Group	Register	Bit	Qty
ACPI	GPE0A_EN		
		SMB_WAK_EN[16]	1
		PCIE_WAKE3_EN[8]	1
		PCIE_WAKE2_EN[7]	1
		PCIE_WAKE1_EN[6]	1
		PCIE_WAKE0_EN[3]	1
	PM1_CNT	SLP_TYP[12:10]	3
	PM1_STS_EN	PWRBTNNOR_STS[11]	1
		RTC_EN[26]	1

Table 3-24. PMC RTC Shadowed Bits with Address Map (Sheet 2 of 2)

Reg Group	Register	Bit	Qty
GCR	BIOS_SCRATCHPAD	BIOS_SCRATCHPAD[31:28]	4
	PMC_CFG	PWR_CYC_DUR[9:8]	2
	PMC_CFG2	PB_DB_MODE[10]	1
		PB_DIS[28]	1
	PMCON1	PME_B0_S5_DIS[15]	1
		RPS[2]	1
		AG3E[0]	1
	PMCON3	S4MAW[5:4]	3
		S4ASE[3]	1
Note: Any unlist bit positions are unused and should be ignored.			

3.8 USB Controller

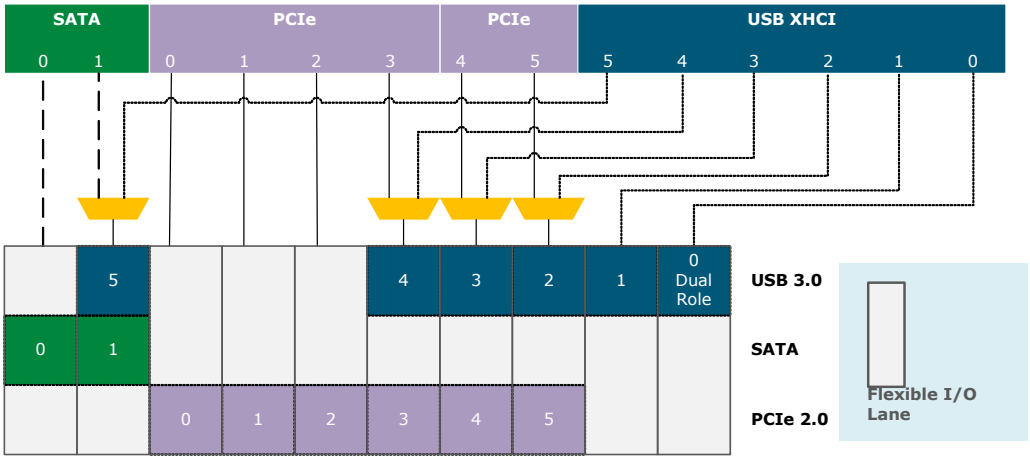
Table 3-25. USB xHCI Controller Features

USB Interface	
Category	**Description**
USB 3.0 SuperSpeed Port	6 (2 dedicated port[1x USB Dual Role], 3x multiplexed with PCIe* 2.0, 1x multiplexed with SATA 3.0)
Peak USB 3.0 Speed	5 Gb/s
USB 2.0 Port	8 (1x Dual Role, 7x Host)
Direct Connect Interface (DCI)	USB Port 0 and Port 1 only
Peak USB 2.0 Speed	480 Mb/s

Table 3-24. Port Assignment for USB

Port/Type	xHCI Port#	PHY	Description
USB Port 0 USB3 (SS) and USB2 (HS/FS) OTG-capable port	SS port 0 HS port 0	USB2 PHY, USB3 MODPHY	Walk-up port with external connector Port 0 is intended to be the OTG (dual role) port, but can also be configured as a host-only port
USB Port 1-5 USB3 (SS) and USB2 (HS/FS/LS) host-only port	SS port 1-5 HS port 1-5	USB2 PHY, USB3 MODPHY	Walk-up host port Used for dock connector on some platforms
USB Port 6-7 USB2 (HS/FS/LS) host-only port	HS port 6-7	USB2 PHY	Walk-up host port
USB Port 8 USB2 (HS/FS/LS) host-only port	HS port 8	iCNV	Internally connected to integration Connectivity IP

Figure 3-19. USB 3.0/PCIe*/SATA Port Mapping



Note: There are 8x USB Ports supported. USB Ports [5:0] can be used as USB2 and USB3 and are mutually exclusive. USB Port 6 and Port 7 can only be used as USB2.

3.8.1 Overview and Block Diagram

The USB sub-system supports 1 DRD (dual-role device), which uses separate host controller (xHCI) and device controller (xDCI) IPs.

3.8.2 Performance Goals

The USB subsystems supports a max bandwidth of 2.128 GB/s.

USB standards define the following data rates per port:

Table 3-25. Performance Goals

USB Speed	Line Rate	Raw Data BW
USB1.1 Full Speed	12 Mb/s	1.5 MB/s uni-directional
USB2.0 High Speed	480 Mb/s	60 MB/s uni-directional
USB3.0 SuperSpeed	5 Gb/s	500 MB/s in each direction (1 GB/s total)

3.8.2.1 xHCI Performance

Each xHCI port is expected to be able to sustain a bandwidth of ≥450MB/s simultaneously in each direction, when running at superspeed (USB3 speed); at high speed (USB2 speed) the bandwidth should be ≥48 MB/s in one direction.

3.8.2.2 xDCI Performance

The xDCI is expected to support ≥450 MB/s simultaneously in each direction, i.e., reads and writes, when running at superspeed. At USB2 speeds, the maximum theoretical bandwidth is 60 MB/s in one direction.

3.8.3 Time-Synchronization Support

SoC supports Time-Synchronization Support through the IOSF-SB Global Time Sync protocol, in order to synchronize interfaces to each other using a precise HW-based mechanism. The objective of this feature is to enable the platform with a time synchronization capability where audio and video can be rendered cooperatively in a way that maintains lip-sync and audio-sync across multiple devices multiple IO controllers and multiple platforms. xHCI implements a type-D agent that supports Time Reporting, but not synchronized start nor clock control. The Time Sync widget is leveraged from the Audio COE.

The USB-specific use cases are to synchronize the USB host controller with Audio/ Graphics subsystems. This allows for audio/video to be rendered with proper audio/lip sync in the following scenarios.

- Audio over USB with Video over GT (graphics core).
- Audio over HD Audio with Video over USB.

3.8.4 Windows Compliance Requirements

64-bit addressing is required in both Host and Device controllers. This requirement is met by the USB subsystem in SoC.

3.8.5 Use Models

3.8.5.1 Connect/Disconnect Detection

To save power, the USB2 PHY 3.3V rail will be kept down until a connection is detected, whenever it is possible (based on receptacle type).

Table 3-26 shows that only as a Standard-A receptacle (typically a PC) there is a need to keep the USB2 PHY on (or it can be turned on/off periodically to save power) to detect a connection/disconnection. In all other cases, the VBUS and ID pin can be used to enable the USB power-up.

When there is a USB connection (as Host or as Device), if in USB3 mode there is a need to activate the termination resistors and sample the LFPS signaling. The Rx.Detect sequence is also required periodically (spec requirement: 12 ms–100 ms).

Table 3-26. USB Connect/Disconnect Scheme—Connector Dependent

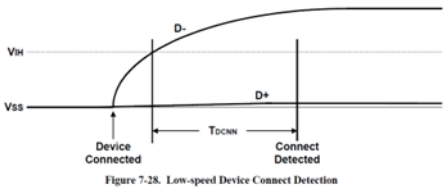
Receptacle	Plug	Way of Detection	comments
Standard-A	Standard-A	D+ and D- sensing (USB2) Rx Detect (USB3)	D+ signal pulled up if FS device attached D- signal pulled up if LS device attached  Figure 7-28. Low-speed Device Connect Detection

Table 3-26. USB Connect/Disconnect Scheme—Connector Dependent

Receptacle	Plug	Way of Detection	comments
Standard-B			Not expected in phone/tablet or PC
Micro-B Mini-B	Micro-B Mini-B	VBUS sensing	
Type-C	Type-C		

The typical platform is expected to use a micro-AB connector on the Dual Role port.

3.8.5.2 Type-C Connector

The USB Type-C receptacle, plug and cable provide a smaller, thinner and more robust alternative to existing USB interconnect (Standard and Micro USB cables and connectors). This new solution targets use in very thin platforms, ranging from ultra-thin notebook PCs down to smart phones where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust. Some key specific enhancements include:

- The USB Type-C receptacle may be used in very thin platforms as its total system height for the mounted receptacle is under 3 mm.
- The USB Type-C plug enhances ease of use by being plug-able in either upside-up or upside-down directions, both directions fully functioning as should be expected by the user.
- The USB Type-C cable enhances ease of use by being plug-able in either direction between host and devices, both directions fully functioning as should be expected by the user.

The Type-C connector supports USB2, USB3.0 and USB3.1, in addition to other non-USB protocols (e.g. display port) and can be used for the Dual Role port connector. There are no markings to identify host vs device ports, and the cable is symmetrical.

3.8.6 Host

3.8.6.1 Host Ports

As a host SoC can connect to any standard USB1.1, USB2, or USB3 device such as mouse, keyboard, disk on key, USB speakers, etc.

3.8.6.2 Debug Device (DbC)

Debug Device (DbC) is a new USB class that enables a USB host controller to be connected as a device to another host controller for debug purpose. It can be used for OS Kernel Debugging or ExI HW Debug interface.

3.8.7 Device

3.8.7.1 Device Port

Port 0 is an dual-role device port. The DRD Port can be used as a Host or as a Device, as selected by the ID pin setting. As a Device it can connect to any Host (Tablet or PC), and can expose various SoC capabilities based on what drivers are available, example:

- Tethering: using the phone as a modem for host for internet connection (portable hotspot)
- Sync-N-Go BOT/UASP/MTP: High-BW (this is supported with standard drivers)
  - MTP: device class; media transfer protocol; used to expose e.g. a camera to a PC using a simplified file system.
- USB accessory mode
- Platform Debug (RTIT)
- ACM (for AT-proxy)
- Camera
- Sensor

3.9 PCI Express

SoC has integrated PCIe* interface with following features:

Note: PCIe* Lanes 3, 4, and 5 are multiplexed with USB3 Ports 4, 3, and 2, respectively. Refer to Figure 3-19 for more information.

Table 3-27. PCIe* Features

PCIe* Interface	
Category	**Description**
PCIe* Interface	PCIe* Gen2 and PCIe* Gen1
PCIe* number of lanes	6 lanes (x3 dedicated and x3 multiplexed with USB 3.0)
PCIe* Maximum Supported Devices	Up to 4 root ports/external device
PCIe* Signal Transfer Rate	PCIe* Gen2: 5GT/s and PCIe* Gen1: 2.5GT/s per root port
PCIe* Clock Frequency	100 MHz (SSC/NSSC Type), Supports 4 reference Clocks (REF CLK)
PCIe* Supported Configuration	Flexible Configuration Supported with any combination of 4 root ports (should not exceed 6 lanes). Example of some common configurations: — (1) x4 + (1) x2 — (4) x1 — (2) x1 + (1) x2 + (1) x2 x1, x2, x4 lane widths (auto negotiated)
Supported Interrupt and Events	• Legacy (INTx) and MSI Interrupts • General Purpose Events • System Error Event
Power Management	• Link State support for L0s, L1, and L2 • L1 Sub-states support • Powered Down in ACPI S3state - L3
PCIe* Compliancy	
Reference	**Revision**
PCI Express* Base Specification	Revision 2.0

3.9.1 PCIE* Port Mapping

Table 3-28. PCIe* Port Mapping

PCIe* Config.	Dev	Function	Root Port/BIOS ASL	Signal Names	Bifurcation
x2	20	0	0/Device(RP01)	PCIE_P4_USB3_P3_Tx/Rx	1 x2, 2 x1
	20	1	1/Device (RP02)	PCIE_P5_USB3_P2_Tx/Rx	
x4	19	0	2/Device (RP03)	PCIE_P0_Tx/Rx	1 x4, 2 x2, 1 x2, 2 x1, 4 x1
	19	1	3/Device (RP04)	PCIE_P1_Tx/Rx	
	19	2	4/Device (RP05)	PCIE_P2_Tx/Rx	
	19	3	5/Device (RP06)	PCIE_P3_USB3_P4_Tx/Rx	
Note: For proper functionality of the PCIE* ports, each CLKREF signal must be associated with the corresponding CLKREQ signal to enable the clocks. Ensure that the BIOS assigns a valid number for the CLKREQ.					

Table 3-29. Supported Configurations for x4 Root Port

Configuration	PCIe* x4			
	Port 0	Port 1	Port 2	Port 3
1 x4	x4			
2 x2	x2		x2	
1 x2, 2 x1	x2		x1	x1
4 x1	x1	x1	x1	x1
2 x1, 1 x2	x1	x1	x2	

Table 3-30. Supported Configuration for x2 Root Port

Configuration	Port 0	Port 1
1x 2	x2	
2 x1	x1	x1

3.9.2 PCIe* GPIO Requirements

The PCIe Controller requires additional GPIOs for signaling to and from the device. The following GPIOs are required:

- PCIE_CLKREQ#
- PCIE_WAKE#

Note: PCIE_CLKREQ# and PCIE_WAKE# are default functions (within the GPIOs).

Note: These GPIOs exist for each root port/device supported.

3.9.3 PCIE_CLKREQ#

Since L1 Substates are supported, the CLKREQ# GPIO is required to be bi-directional. One GPIO per port is required. The pad operates in native/functional mode which provides the signal control to the SoC for controlling the CLKREQ functionality.

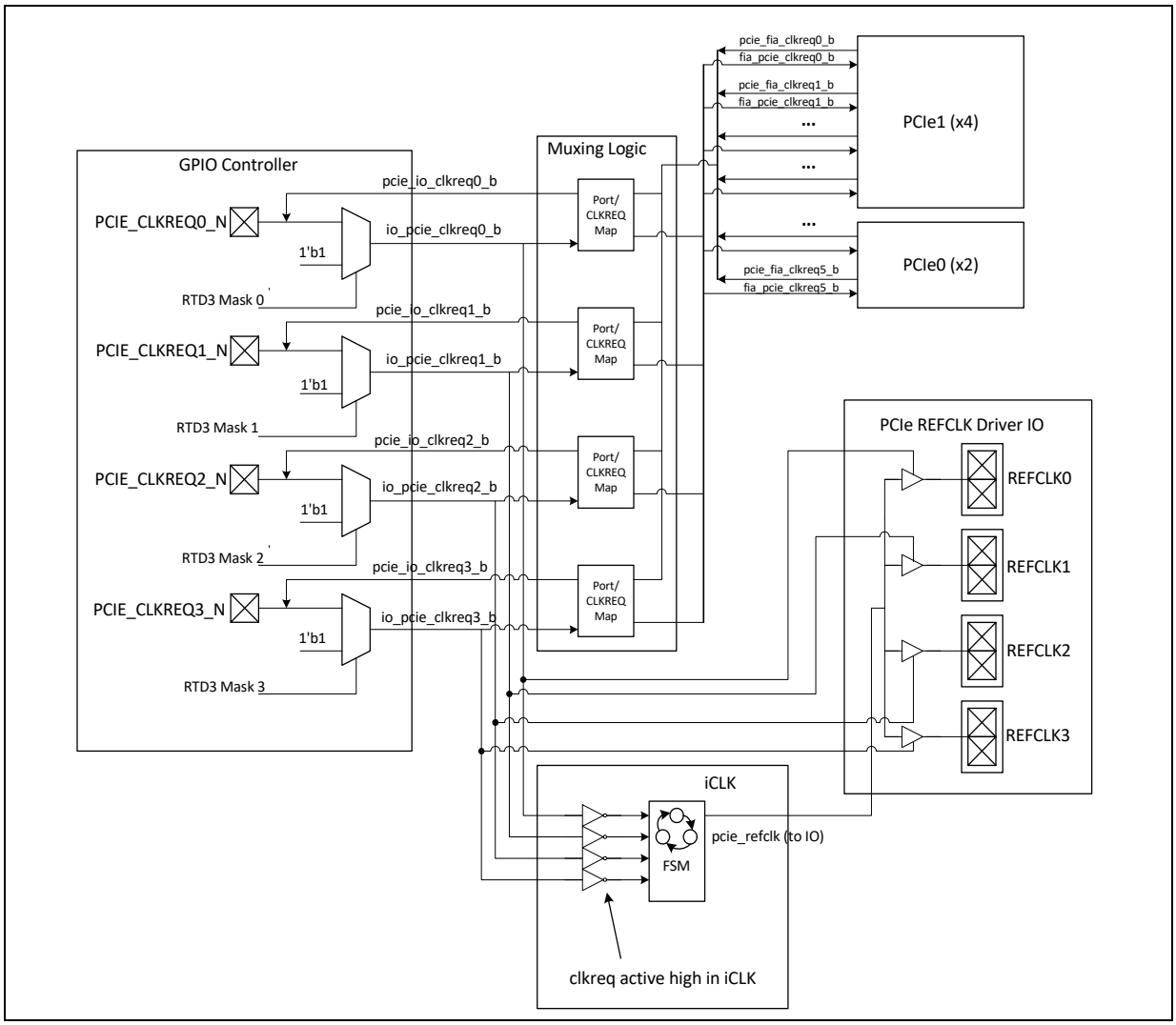
CLKREQ# is used for devices to request the 100 MHz reference clock provided by the SoC. For L1.Substate support is also used to wake from L1.OFF.

3.9.3.1 CLKREQ# Connectivity

SoC supports up to 6 lanes. However, only 4 devices/ports are supported. Therefore, only 4 CLKREQ# GPIOs are required. The SoC provides the CLKREQ# GPIO multiplexing to accommodate the 6 lanes.

Configuration registers are provided to map the CLKREQ# GPIOs to the ports. multiplexing logic is provided between the GPIO Controller and PCIe Controller.

Figure 3-20. CLKREQ Connectivity



3.9.4 PCIE_WAKE#

This is an input to SoC. 1 (One) GPIO per port is required. SoC supports 4 (four) WAKE#. The pin operates in native/functional mode and provides an input to the SoC to monitor the WAKE# activity.

WAKE# is used for devices to wake from Sx, S0ix, or Runtime D3 (RTD3).

3.9.5 PCIe REFCLK IO

SoC provides the 100 MHz Reference Clock to the external devices. A differential analog clock buffer exists for each REFCLK provided to the platform.

3.9.5.1 PCIe* GPIO IO Standby

The following table defines the way that the PCIe related GPIOs should be configured during Sx, S0ix for IO Standby to maintain functionality throughout Sx, S0ix.

3.9.6 Interrupt Generation

The root port generates interrupts on behalf of power management, link bandwidth management, Link Equalization Request and link error events, when enabled. These interrupts can either be pin-based, or can be MSI (Message Signaled Interrupt), when enabled.

When an interrupt is generated via the legacy pin, the pin is internally routed to the SoC interrupt controllers. The pin that is driven is based upon the setting of the STRPFUSECFG.PXIP configuration registers.

Table 3-31 summarizes interrupt behavior for MSI and wire-modes. In the table "bits" refers to the PME interrupt bits.

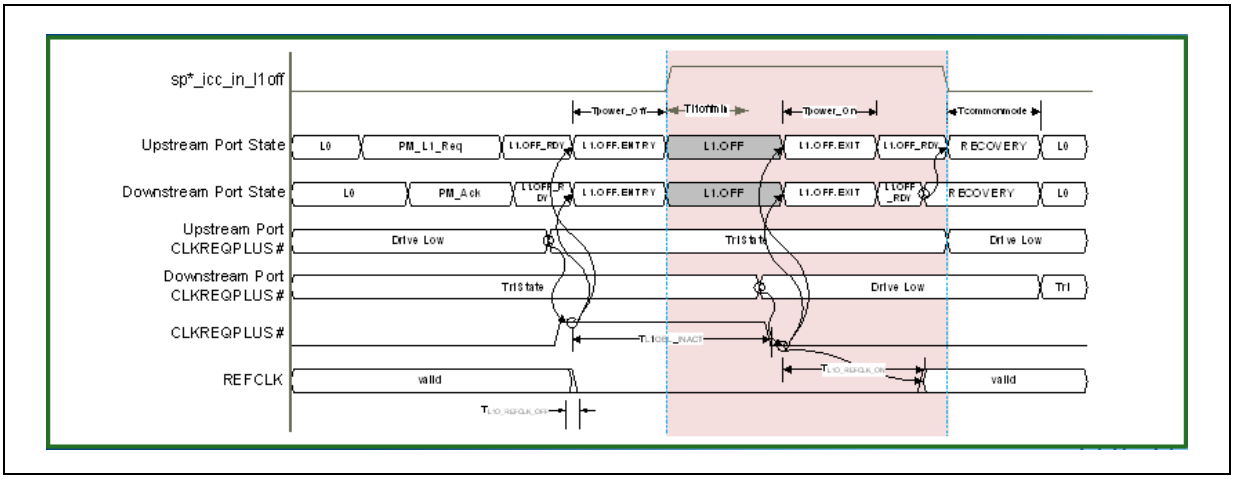
Table 3-31. MSI Versus PCI IRQ Actions

Interrupt Register	Wire-Mode Action	MSI Action
All bits 0	Wire inactive	No action
One or more bits set to 1	Wire active	Send message
One or more bits set to 1, new bit gets set to 1	Wire active	Send message
One or more bits set to 1, software clears some (but not all) bits	Wire active	Send message
One or more bits set to 1, software clears all bits	Wire inactive	No action
Software clears one or more bits, and one or more bits are set on the same clock	Wire active	Send message

3.9.7 TREFCLK_ON Timer Support

During L1.OFF, PCIe defines a TREFCLK_ON timer which defines the minimum amount of time from CLKREQ# assertion to REFCLK valid. BIOS is to detect the PCIe device L1.OFF support capability and its Tpowerup_max, and enable the mechanism if supported. As part of the enabling, BIOS is to program the ICC Trefclk_min parameters such that Trefclk_min >= Tpowerup_max.

Figure 3-21. Trefclk_On Timing Waveform



3.9.8 Power Management

3.9.8.1 Power Gating

The controller power gating will only happen when both ports are part of the same x2 controller and all 4 ports of the x4 Controller are in a state which allows power gating and power gating is enabled. Per-port controller, power gating is not supported. When any of the ports exit power gating, the whole x2 or x4 controller will be brought out of power gating.

Note: To support S0ix all PCIE RP must be in RTD3 (cold) where the link is in L23_RDY (L23 Ready) or Functional Disable.

3.9.8.2 S3/S4/S5 Support

Software initiates the transition to S3/S4/S5 by performing an I/O write to the Power Management Control register in the SoC. After the I/O write completion has been returned to the processor, the Power Management Controller will signal each root port to send a PME_Turn_Off message on the downstream link. The device attached to the link will eventually respond with a PME_TO_Ack followed by sending a PM_Enter_L23 DLLP (Data Link Layer Packet) request to enter L23. The Express ports and Power Management Controller take no action upon receiving a PME_TO_Ack. When all the Express port links are in state L23, the Power Management Controller will proceed with the entry into S3/S3/S5.

Prior to entering S3, software is required to put each device into $D3_{HOT}$. When a device is put into $D3_{HOT}$, it will initiate entry into a L1 link state by sending a PM_Enter_L1 DLLP. Under normal operating conditions when the root ports sends the PME_Turn_Off message, the link will be in state L1. However, when the root port is instructed to send the PME_Turn_Off message, it will send it whether or not the link was in L1. Endpoints attached to the SoC can make no assumptions about the state of the link prior to receiving a PME_Turn_Off message.

3.9.8.3 Resuming from Suspended State

The root port contains enough circuitry in the suspend well to detect a wake event through the WAKE# signal and to wake the system. When WAKE# is detected asserted, an internal signal is sent to the power management controller of the SoC to cause the system to wake up. This internal message is not logged in any register, nor is an interrupt/GPE generated due to it.

3.9.8.4 Device Initiated PM_PME Message

When the system has returned to a working state from a previous low power state, a device requesting service will send a PM_PME message continuously, until acknowledged by the root port. The root port will take different actions depending upon whether this is the first PM_PME that has been received, or whether a previous message has been received but not yet serviced by the operating system.

If this is the first message received (RSTS.PS), the root port will set RSTS.PS, and log the PME Requester ID into RSTS.RID. If an interrupt is enabled using RCTL.PIE, an interrupt will be generated. This interrupt can be either a pin or an MSI if MSI is enabled using MC.MSIE.

If this is a subsequent message received (RSTS.PS is already set), the root port will set RSTS.PP. No other action will be taken.

When the first PME event is cleared by software clearing RSTS.PS, the root port will set RSTS.PS, clear RSTS.PP, and move the requester ID into RSTS.RID. If RCTL.PIE is set, an interrupt will be generated. If RCTL.PIE is not set, a message will be sent to the power management controller so that a GPE can be set. If messages have been logged (RSTS.PS is set), and RCTL.PIE is later written from a 0b to a 1b, an interrupt will be generated. This last condition handles the case where the message was received prior to the operating system re-enabling interrupts after resuming from a low power state.

3.9.9 Latency Tolerance and Reporting (LTR)

The root port supports the extended Latency Tolerance Reporting (LTR) capability. LTR provides a means for device endpoints to dynamically report their service latency requirements for memory access to the root port. Endpoint devices should transmit a new LTR message to the root port each time its latency tolerance changes (and initially during boot). The SoC uses the information to make better power management decisions. The processor uses the worst case tolerance value communicated by the SoC to optimize C-state transitions. This results in better platform power management without impacting endpoint functionality.

Note: Endpoint devices that support LTR must implement the reporting and enable mechanism detailed in the PCI-SIG “Latency Tolerance Reporting Engineering Change Notice” (www.pcisig.com).

3.9.10 L1 Substate Support

PCIe Root Port supports L1 Sub-states. In order to meet the low power requirements SoC supports the new L1 Sub-States - L1.OFF and L1.SNOOZ.

Note: In the PCI Express specification, L1.OFF is called L1.2 and L1.SNOOZ is called L1.1.

These L1 sub-states allow more aggressive power saving mechanisms. It also enables lower idle power, ASPM, improves exit latency compared to traditional L1.

Refer to PCIE-SIG ECN (Engineering Change Notice) for more details.

Note: To support L1.OFF (L1.2) and L1.SNOOZ (L1.1), CLKREQ# is re-defined as a bi-directional signal. Either Root Port or device can initiate exit from L1.OFF by asserting the out-of-band CLKREQ# signal to power up the PHYs on both sides of the link in parallel.

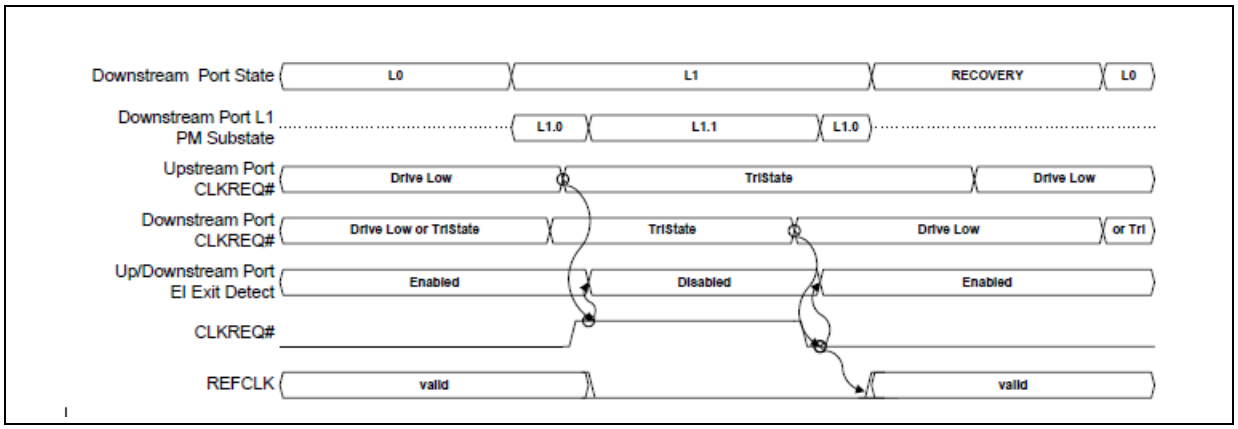
3.9.11 L1 Substate LTR Thresholds

Each root port contains LTR Threshold registers for each L1 substate. The root port will quickly use up the LTR sent from the device, and compare the value against these threshold registers to make the determination to allow L1 entry or not (device always requests L1, root port responds).

3.9.11.1 L1.SNOOZ Threshold

Refer to PCIe_SIG ECN for more details.

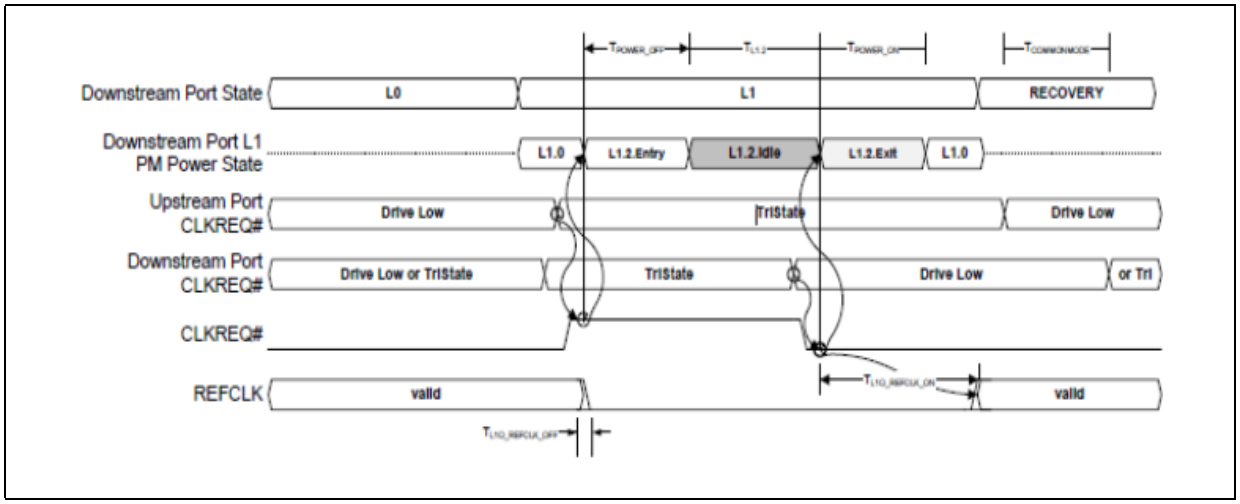
Figure 3-22. L1.SNOOZ (L1.1) Exit Waveform



3.9.11.2 L1.OFF Threshold

Refer to PCIe-SIG ECN for more details.

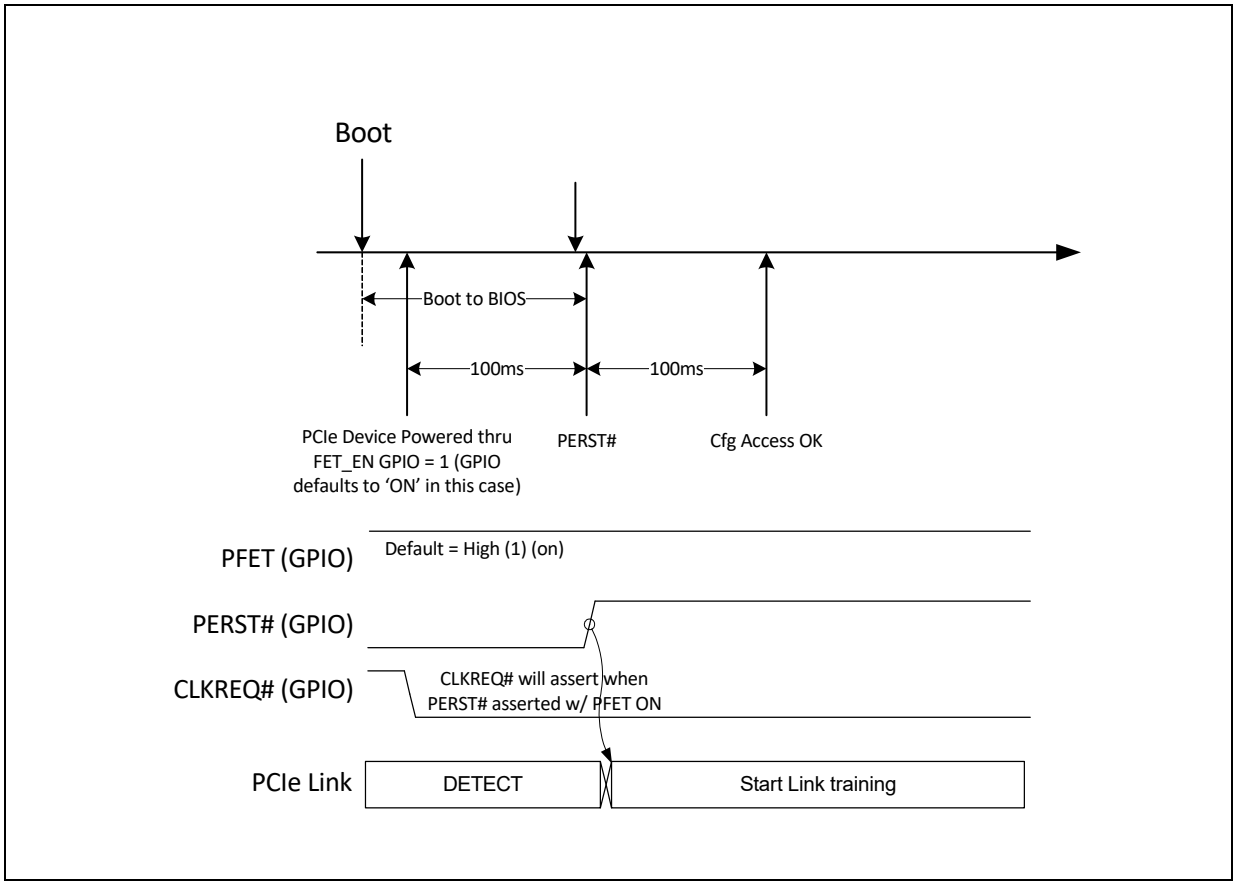
Figure 3-23. L1.OFF (L1.2) Exit Waveform



3.9.11.3 Platform Power Sequence (Cold Boot)

The timing diagram below illustrates the platform level sequencing of the PCIe Controller, PCIe GPIOs (to bring the device up).

Figure 3-24. Cold Boot Platform Level Sequence



3.9.11.4 PCIe RTD3 Entry/Exit

The device D3 state represents the non-functional device power management state where the entry and exit from this state is fully managed by software. Main power can be removed from the device in this state. Conventionally, the device is put into a D3 state as part of the flow to transition the system from an S0 to Sx system sleep state.

Runtime D3 (RTD3) constitutes the hardware and software enhancements to put the Root Port and device into a $D3_{cold}$ state, even when the system is in S0, when the device is no longer needed by the software. The tolerable exit latency from RTD3 is long, given software participation in putting the Root Port and device in this power management state.

A device in RTD3 is prohibited from generating any activity other than a wake event, through the PCIE_WAKE_N pin. The device must wait until software has fully restored the device to an operational D0 state before initiating any transactions.

Access to the device's host interface is prohibited while in RTD3. The OS and/or device driver must queue all new IO accesses while the device is in RTD3 and transition the device back to an operational state before accessing its host interface. IO queuing must be done in a manner that does not stall software, given the potentially long device recovery latency.

SoC supports PCIe Run Time D3 (RTD3).

3.9.12 Function Disable

In general, the PCIe Function Disable flows are the same for the x2 and x4 controllers.

The following is the BIOS Flow for Function Disabling:

Cold Boot/Cold Reset:

- Reads BIOS Function disable registers in PMC (Refer Note)
  - 2 bits for PCIe0 ports 0/1
  - 4 bits for PCIe1 ports 0/1/2/3
- BIOS will then enable the Power Management in PCIe RP through IOSF SB to enable maximum power savings. Chassis defined clkreq/clkack pairs will be deasserted

Note: For the BIOS Function Disable flow, the PMC will bring up PCIe normally and when BIOS executes it will write the PCIe function disable bits in the PMC. BIOS will then force a reset and on subsequent boot, PMC will see the function disable bits and will treat them in the same manner as the port disable fuses.

3.9.12.1 PCIe Controller Function 0 Requirements

Because the PCIe Controller is a multi-function device, function 0 must always be present for enumeration. If enumeration does not see function 0 for a device, it will assume device does not exist and move on with enumeration.

The RPFN - Root Port Function Number allows the BIOS to assign different function numbers to a physical Root Port. This allows the BIOS to disable any Root Port and still have Function 0 enabled. So should port 0 be function disabled, BIOS can remap function 0 to port 1.

Note: In SoC, this applies to both the x2 and x4 controllers.

3.9.12.2 Dynamic Link Throttling

Root Port supports dynamic link throttling as a mechanism to help lower the overall component power, ensuring that the component never operates beyond the thermal limit of the package. Dynamic link throttling is also used as a mechanism for ensuring that the ICC_{max} current rating of the voltage regulator is never exceeded. The target response time for this particular usage model is < 100 us.

If dynamic link throttling is enabled, the link will be induced by the Root Port to enter TxL0s and RxL0s based on the throttle severity indication received. To induce the link into TxL0s, new TLP requests and opportunistic flow control update will be blocked. Eventually, in the absence of TLP and DLLP requests, the transmitter side of the link will enter TxL0s.

The periodic flow control update, as required by the PCI Express Base Specification is not blocked. However, the flow control credit values advertised to the component on the other side of the link will not be incremented, even if the periodic flow control update packet is sent. Once the other component runs out of credits, it will eventually enter TxL0s, resulting in the local receiver entering RxL0s.

Each of the Root Ports receives four throttle severity indications; T0, T1, T2 and T3. The throttling response for each of the four throttle severity levels can be independently configured in the Root Port TNPT.TSLxM register fields. This allows the duty cycle of the Throttling Window to be varied based on the severity levels, when dynamic link throttling is enabled.

A Throttling Window is defined as a period of time where the duty cycle of throttling can be specified. A Throttling Window is sub-divided into a Throttling Zone and a Non-Throttling Zone. The period of the Throttling Zone is configurable through the TNPT.TT field. Depending on the throttle severity levels, the throttling duration specified by the TNPT.TT field will be multiplied by the multipliers configurable through TNPT.TSLxM.

The period of the Throttling Window is configurable through the TNPT.TP field. The Throttling Window is always referenced from the time a new Throttle State change indication is received by the Root Port or from the time the throttling is enabled by the configuration register. The Throttling Window and Throttling Zone timers continue to behave the same as in L0 or L0s even if the link transitions to other LTSSM states, except for L1, L23_Rdy and link down. For L1 case, the timer is allowed to be stopped and hardware is allowed to re-start the Throttling Window and the corresponding Throttling Zone timers on exit from L1.

3.9.12.3 Separate Reference Clock with Independent SSC (SRIS)

The current PCI-SIG "PCI Express* External Cabling Specification" (www.pcisig.com) defines the reference clock as part of the signals delivered through the cable. Inclusion of the reference clock in the cable requires an expensive shielding solution to meet EMI requirements.

The need for an inexpensive PCIe* cabling solution for PCIe* SSDs requires a cabling form factor that supports non-common clock mode with spread spectrum enabled, such that the reference clock does not need to be part of the signals delivered through the cable. This clock mode requires the components on both sides of a link to tolerate a much higher ppm tolerance of ~5600 ppm compared to the PCIe Base Specification defined as 600 ppm.

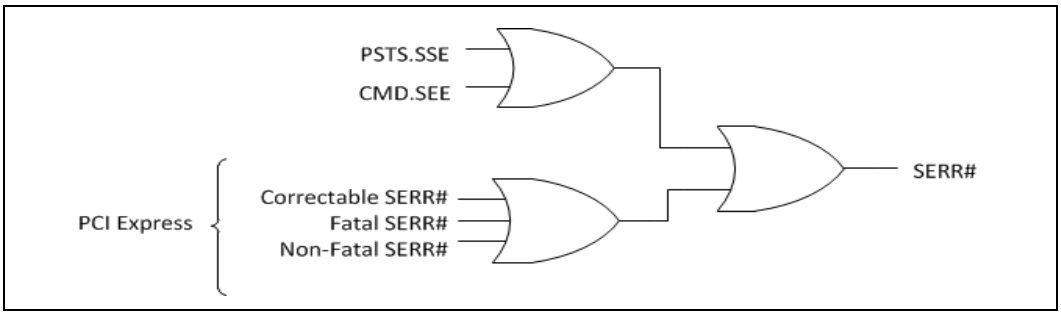
SoftStraps are needed as a method to configure the port statically to operate in this mode. This mode is only enabled if the SSD connector is present on the motherboard, where the SSD connector does not include the reference clock. No change is being made to PCIe* add-in card form factors and solutions.

ASPM L0s is not supported in this form factor. The L1 exit latency advertised to software would be increased to 10 us. The root port does not support Lower SKP Ordered Set generation and reception feature defined in SRIS ECN.

3.9.12.4 SERR# Generation

SERR# may be generated using two paths—through PCI mechanisms involving bits in the PCI header, or through PCI Express* mechanisms involving bits in the PCI Express capability structure.

Figure 3-25. Generation of SERR# to Platform



3.9.12.5 PCI Express* Lane Polarity Inversion

The PCI Express* Base Specification requires polarity inversion to be supported independently by all receivers across a Link - each differential pair within each Lane of a PCIe* Link handles its own polarity inversion. Polarity inversion is applied, as needed, during the initial training sequence of a Lane. In other words, a Lane will still function correctly even if a positive (Tx+) signal from a transmitter is connected to the negative (Rx-) signal of the receiver. Polarity inversion eliminates the need to untangle a trace route to reverse a signal polarity difference within a differential pair and no special configuration settings are necessary in the SoC to enable it. It is important to note that polarity inversion does not imply direction inversion or direction reversal; that is, the Tx differential pair from one device must still connect to the Rx differential pair on the receiving device, per the PCIe* Base Specification. Polarity Inversion is not the same as "PCI Express* Controller Lane Reversal".

3.9.12.6 PCI Express* Controller Lane Reversal

Each PCIe* Controller support end-to-end lane reversal across the four lanes mapped to a controller for the 1 motherboard PCIe* configurations listed below. Lane Reversal means that the most significant lane of a PCIe* Controller is swapped with the least significant lane of the PCIe* Controller while the inner lanes get swapped to preserve the data exchange sequence (order).

Note: Lane Reversal Supported Motherboard PCIe* Configurations = 1x4 and 2x1+1x2 PCI Express* Controller Lane Reversal is not the same as PCI Express* Lane Polarity Inversion.

3.10 Serial ATA (SATA)

The SoC has an integrated Serial ATA (SATA) host controller with independent DMA operation on up to 2 SATA ports.

Note: SATA Port 0 is dedicated for SATA, while SATA Port 1 is multiplexed with USB3, Port 5 can be configured to be used for either interface. Refer Figure 3-19 for more information.

Table 3-32. SATA Interface

SATA Interface	
Category	**Description**
SATA Interface	SATA Gen3, Gen2, and Gen1
SATA number of ports	2 SATA Ports
SATA Signaling Transfer Rate	SATA Gen3: 6 Gbps - Gen2: 3 Gbps - Gen1: 1.5 Gbps
SATA Data Speed	SATA Gen3: 600 MB/second - Gen2: 300 MB/second - Gen1: 150 MB/second
SATA Clock Frequency	100 MHz (SSC/NSSC Type)
SATA Compliancy	
Reference	**Revision**
SATA Specification Compliancy	Revision 3.1 (Also supports optional sections of the SATA Revision 2.6/2.0 Specification.)
AHCI Specification Compliancy	Revision 1.3.1
SATA II: Extensions to SATA 1.0	Revision 1.0 (AHCI support is required for some elements)

Table 3-33. SATA Supported Features

Supported Features	
Feature	**Description**
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers
Auto Activate for DMA	Collapses a DMA Setup then DMA Activate sequence into a DMA Setup only
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot-plug
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention
Host and Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states
Staggered Spin-Up	Enables the host to spin up hard drives sequentially to prevent power load problems on boot
DEVSLP	Device Sleep (DEVSLP) is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state
AHCI DMA PRD format	Allows software to communicate between system memory and SATA devices
AHCI Mode Support	The application layer operate in AHCI Host Bus Adaptor (HBA) mode
Dynamic clock gating and dynamic trunk gating	Enables automatic gating off of peripherals that are not being used until CPU or a DMA engine needs to use.

Table 3-34. SATA Non-Supported Features

Non-Supported Features
Port Multiplier
FIS Based Switching
Command Based Switching
IDE Mode
Cold Presence Detect
Function Level Reset (FLR)
Command Completion Coalescing
Enclosure Management

3.10.1 Functional Description

The SoC SATA host controller (D18:F0) supports AHCI.

SoC SATA controller does not support legacy IDE mode or combination mode. Each interface is supported by an independent DMA controller.

The SoC SATA controller interacts with an attached mass storage device through a register interface that is compatible with an SATA AHCI host adapter. The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

3.10.2 SATA 6 Gb/s Support

The SoC SATA controller is SATA 6 Gb/s capable and supports 6 Gb/s transfers with all capable SATA devices. The SoC SATA controller also supports SATA 3 Gb/s and 1.5 Gb/s transfer capabilities.

3.10.3 SATA Feature Support

The SoC SATA controller is capable of supporting all AHCI 1.3 and AHCI 1.3.1, refer to the Intel web site on Advanced Host Controller Interface Specification for current specification status: http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html.

The SoC SATA controller does not support:

- Port Multiplier
- FIS Based Switching
- Command Based Switching
- IDE mode or combination mode
- Cold Presence Detect
- Function Level Reset (FLR)

3.10.4 Power Management Operation

Power management of the SoC SATA controller and ports will cover operations of the host controller and the SATA link.

3.10.4.1 Power State Mappings

The D0 PCI Power Management (PM) state for device is supported by the SoC SATA controller.

- **D0** – Controller is on and available for IO.
- **D3** – Controller is inactive, not available for IO.

The SATA specification defines three link states:

- **Active** – PHY logic and PLL are both on and in active state.
- **Partial** – PHY logic is powered up, and in a reduced power state. The link PM exit latency to active state maximum is 10 ns.
- **Slumber** – PHY logic is powered up, and in a reduced power state. The link PM exit latency to active state maximum is 10 ms.
- **Devslp** – PHY logic is powered down. The link PM exit latency from this state to active state maximum is 20 ms.

3.11 Storage

SCS is the Storage and Communication Subsystem. It includes the following:

- eMMC* 5.1 used for NVM storage (SSD)
- HS400 DDR mode: 400 MB/s
- eMMC* 5.1 adds command queuing, to enable better pipelining and therefore performance
- SoC supports boot from eMMC*; an additional SPI flash is not needed

The following interfaces are part of the Storage subsystem:

Table 3-35. Storage Interface Usage

Interface	Type	Use
eMMC*	Storage	Internal storage device

Table 3-36. eMMC* Features

Category	Feature Supported
eMMC* Specification	embedded Multi-Media Card* Product Standard v5.1, JESD84-B50
eMMC* Signaling	• eMMC* v5.1: HS400 DDR Mode • eMMC* v4.5: HS200 SDR Mode
Transfer Modes	Support transfer the data in 1-bit, 4-bit and 8-bit modes
Mode of Operation	Support both ADMA2/DMA and Non-DMA Modes
Boot Modes	Support both eMMC* Secure and Non-Secure Boot
Cyclic Redundancy Check	Support CRC7 for command and CRC16 for data integrity
Others	Support Interrupt Coalescing and Command Queuing

Table 3-37. eMMC* Working Modes

eMMC* Mode	Data Rate	Maximum Clock Frequency	Maximum Data Throughput
Compatibility	Single	26 MHz	26 MB/s
High Speed SDR	Single	52 MHz	52 MB/s
High Speed DDR	Dual	52 MHz	104 MB/s
HS200	Single	200 MHz	200 MB/s
HS400	Dual	200 MHz	400 MB/s

3.11.1 Storage Overview

The Storage and Communication Subsystem (SCS) is a collection of various peripherals used to interface storage elements and external communication devices.

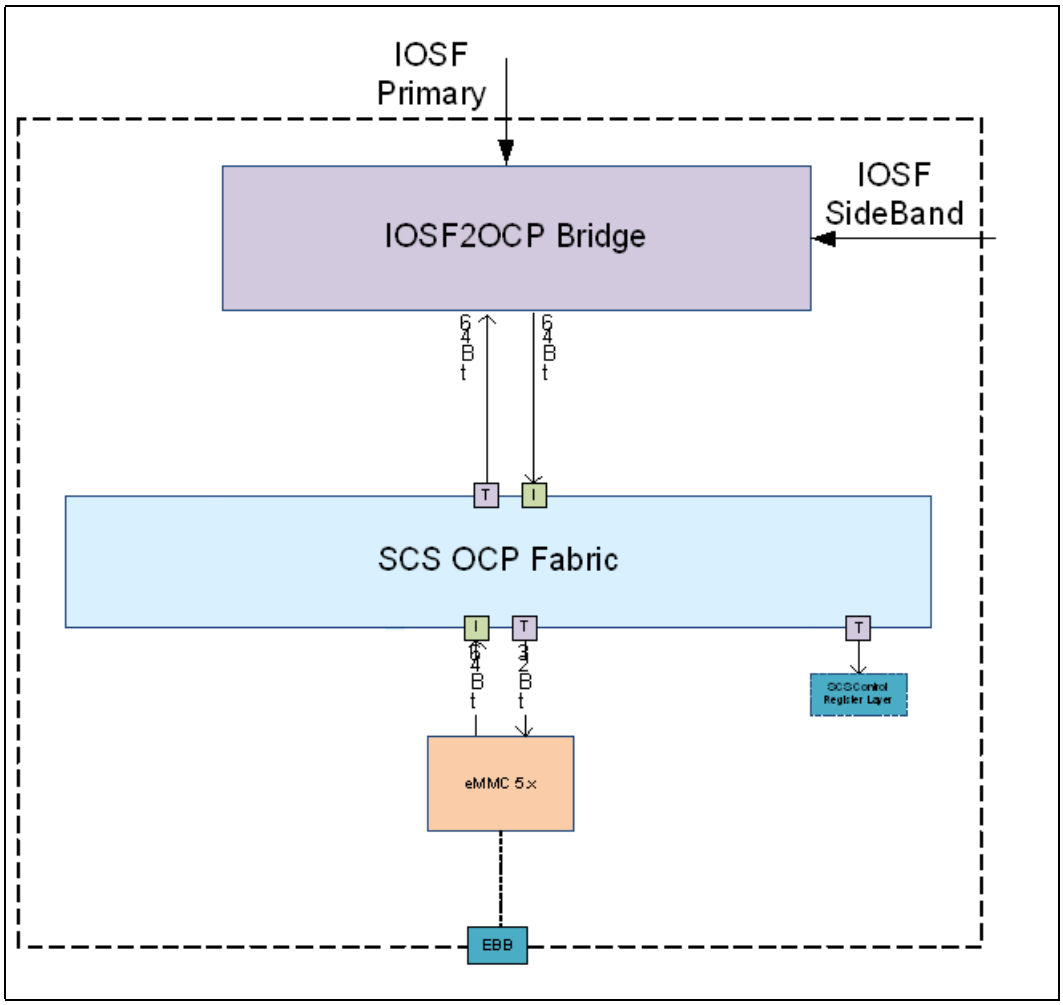
The following interfaces are part of the SoC Storage Subsystem:

Table 3-39. Storage Interface Usage

Interface	Type	Use
eMMC	Storage	Internal storage device

The SCS subsystem is located on the OCP domain under the IOSF2OCP bridge which converts the IOSF traffic to and from the internal OCP protocol which the various IPs support.

Figure 3-26. Storage Subsystem Block Diagram



The SCS (Storage and Communications Cluster) consists of the following major blocks:

I. IOSF2OCP Bridge.
II. OCP Fabric.
III. Controllers
   — eMMC*: 5.1 Controller

3.11.1.1 IOSF2OCP Bridge

The IOSF2OCP Bridge serves as the gateway of the SCS into the IOSF domain. It has two main functions:

1. Convert from IOSF to OCP Bus protocol and vice versa. The bridge converts data transaction from IOSF to the IPs native bus interface of OCP.
   It has 2 IOSF endpoints.
   — Primary IOSF endpoint that connects to the SoC PSF
   — Sideband IOSF endpoint that connects to the sideband topology.

2. Provide full PCI compatibility for the OCP native IPs.
   The bridge contains all the IPs PCI configuration space parameters as the IPs are natively OCPs and do not support PCI configuration parameters.

3.11.1.2 OCP Fabric

The OCP fabric provides the interconnect inside the SCS subsystem. The OCP fabric enables the host to access any of the IPs and the IPs to place data inside the DDR as masters.

3.11.2 Controllers

3.11.2.1 eMMC* Controller

The Controller handles eMMC* Protocol at transmission, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness.

The eMMC* main use case is to connect on an on board external storage device.

3.12 Serial I/O (SIO) (LPSS)

SIO (LPSS) is a collection of slow I/Os used to interface various external devices in the platform.

Table 3-40. Serial I/O Supported Interfaces

Interface	Number of Ports	Maximum Speed
[SIO] I^2C	8	3.4 Mb/s
[SIO] HSUART	4	115,200 kb/s (standard 16550) 3.6864 Mb/s (high-speed 16750)
[SIO] SPI	3	25 Mb/s

Table 3-41. SIO—I^2C Features (Sheet 1 of 2)

Category	Feature Supported
SIO - I^2C Interface	Two-wire, I^2C serial interface comprising a Serial Data line (SDA) and a Serial Clock (SCL)
Loading Range	Limited to 400 pF maximum
Addressing	7b or 10b addressing ***Note:*** Ignores CBUS addresses (an older ancestor of I^2C that used to share the I^2C bus).
Operation Modes	• Master I^2C operation only • Interrupt or polled-mode operation • Handles Bit and Byte waiting at all bus speeds ***Note:*** I^2C Multi Masters,I^2C Slave Mode and I^2C Generic Call are not supported.

Table 3-41. SIO—I²C Features (Sheet 2 of 2)

Category	Feature Supported
Maximum bit rate	High-speed mode supporting a maximum bit rate of 3.4Mb/s ***Note:*** Simultaneous configuration of FM or FM+ is not supported in Fast-mode Plus.
Data Transfer	• 64B transmit (TX) and receive (RX) Host Controller FIFOs • 64B iDMA FIFO per channel with up to 32B Burst capability ***Notes:*** 1. IDMA handshaking interface is compatible with the DW_OCP_IDMAc handshaking interface. 2. DMA mode is not supported when Slice is assigned to Intel® Trusted Execution Engine (Intel® TXE).
Driver/SW Support	• Component parameters for configurable software driver support • SW Controlled serial data line (SDA) and a serial clock (SCL) • Programmable SDA hold time (tHD; DAT)

Table 3-42. SIO—HSUART Features

Category	Feature Supported
SIO—HSUART Interface	Four-Wire HSUART signal Interface using RTS/CTS Control only.
Addressing	Programmable character properties, such as number of data bits per character (5b to 8b), optional parity bit (even or odd parity) and number of stop bits (1b, 1.5b, or 2b).
Operation Modes	• Functionality based on the 16550 and 16750 industry standards • Transmitter Holding Register Empty (THRE) interrupt mode • Prioritized interrupt identification ***Note:*** HSUART Slave Mode is not supported.
Maximum bit rate	• Up to 3.6864 MT/s Auto Flow Control mode as specified in the 16750 standard • Programmable serial data baud rate • Programmable baud supported [baud rate = (serial clock frequency)/(16× divisor)]
Data Transfer	• 64 B transmit (TX) and receive (RX) Host Controller FIFOs • 64 B iDMA FIFO per channel with up to 32B Burst capability • DMA signaling with two programmable modes • Programmable FIFO enable/disable • Line break generation and detection ***Notes:*** 1. DMA mode is not supported when Slice is assigned to TXE. 2. UART 16550 8b Legacy mode is not required when Slice is assigned to TXE. 3. There is no external read enable signal for RAM wake-up when using external RAMs.
Driver/SW Support	• Software-controlled CTS overwrite (for 2-wire interface there is no flow control operation) • Loopback mode enables greater testing of Modem Control and Auto Flow Control features ***Note:*** Modem and status lines are independently controlled. Serial Infrared (SIR) per the Infrared Data Association (IrDA) 1.0 is not supported.

Table 3-43. SIO—SPI Features (Sheet 1 of 2)

Category	Feature Supported
SIO–SPI Interface	Receive Without Transmit (RWOT) half duplex mode.
Addressing	Supports data sizes from 4-bit to 32-bit in length and FIFO depths of 64 entries.

Table 3-43. SIO—SPI Features (Sheet 2 of 2)

Operation Modes	• Master SPI operation only • Operates as Motorola* SPI ***Notes:*** 1. SPI Slave Mode is not supported. 2. Network modes from one to eight time slots are not supported with independent transmit and receive (TX and RX).
Maximum bit rate	Support Programmable baud rate
Data Transfer	• 256 B Transmit (TX) and Receive (RX) Host Controller FIFOs • 128 B iDMA FIFO per channel with up to 64 B Burst capability ***Notes:*** 1. Single DMA transactions are supported. 2. DMA mode is not supported when Slice is assigned to TXE.
Driver/SW Support	• Software control for chip-select override • Programmable Polarity for clock and chip select signals

3.12.1 LPSS - I^{2}C Interface Overview

The SoC implements 8 independent I^{2}C Interface. Both 7-bit and 10-bit addressing modes are supported. These controllers operate in master mode only.

3.12.1.1 I^{2}C - Protocol

The I^{2}C bus is a two-wire serial interface, consisting of a serial data line (SDA) and a serial clock (SCL). These wires carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a "transmitter" or "receiver," depending on the function of the device. Devices can also be considered as masters or slaves when performing data transfers. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The I^{2}C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain or open-collector to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance 10 specification of 400 pF. Data is transmitted in byte packages.

3.12.1.2 I^{2}C Modes of Operation

The I^{2}C module can operate in the following modes:

- Standard mode (with a bit rate up to 100 Kb/s)
- Fast mode (with a bit rate up to 400 Kb/s)
- Fast-Mode Plus (with a bit rate up to 1 Mb/s)
- High-Speed mode (with a bit rate up to 3.4 Mb/s)[1]

Note: 1. Not supported by I^{2}C5-I^{2}C7 in 3.3 V configuration.

Note: Higher speeds require tuning of the analog buffers.

The I^{2}C can communicate with devices only using these modes as long as they are attached to the bus. Additionally, high speed mode, fast mode plus and fast mode devices are downward compatible.

- High-speed mode devices can communicate with fast mode and standard mode devices in a mixed speed bus system.
- Fast mode device can communicate with standard mode devices in a 0-100 Kb/s I^2C bus system.

However, according to the I^2C specification, standard mode devices are not upward compatible and should not be incorporated in a fast-mode I^2C bus system since they cannot follow the higher transfer rate and unpredictable states would occur.

3.12.1.3 Functional Description

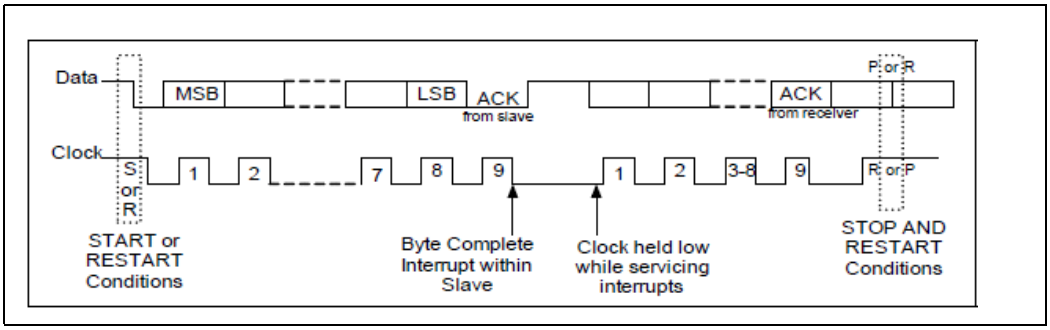
- The I^2C master is responsible for generating the clock and controlling the transfer of data.
- The slave is responsible for either transmitting or receiving data to/from the master.
- The acknowledgment of data is sent by the device that is receiving data, which can be either a master or a slave.
- Each slave has a unique address that is determined by the system designer.

When a master wants to communicate with a slave, the master transmits a START/ RESTART condition that is then followed by the slave's address and a control bit (R/W), to determine if the master wants to transmit data or receive data from the slave.

The slave then sends an acknowledge (ACK) pulse after the address.

- If the master (master-transmitter) is writing to the slave (slave-receiver). The receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition.
- If the master is reading from a slave (master-receiver). The slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse.
- This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition. This behavior is illustrated in below figure.

Figure 3-27. Data Transfer on the I^2C Bus



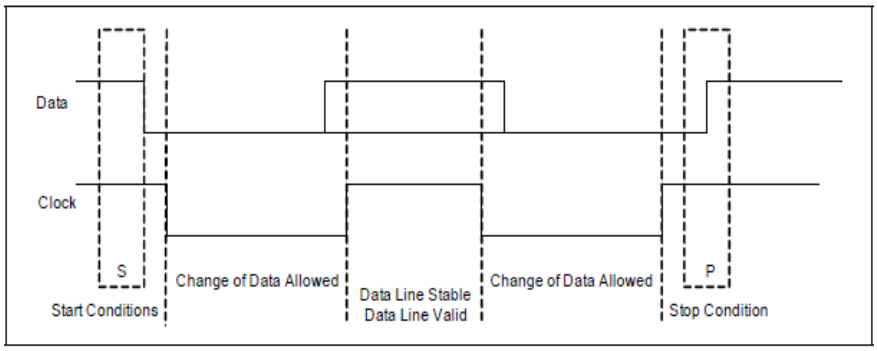
3.12.1.4 START and STOP Conditions

When the bus is idle, both the clock and data signals are pulled high through external pull-up resistors on the bus.

When the master wants to start a transmission on the bus, the master issues a START condition.

- This is defined to be a high-to-low transition of the data signal while the clock is high.
- When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the data line while the clock is high. Below figure shows the timing of the START and STOP conditions.
- When data is being transmitted on the bus, the data line must be stable when the clock is high.

Figure 3-28. START and STOP Conditions



The signal transitions for the START/STOP conditions, as depicted above, reflect those observed at the output of the master driving the I^2C bus. Care should be taken when observing the data/clock signals at the input of the slave(s), because unequal line delays may result in an incorrect data/clock timing relationship.

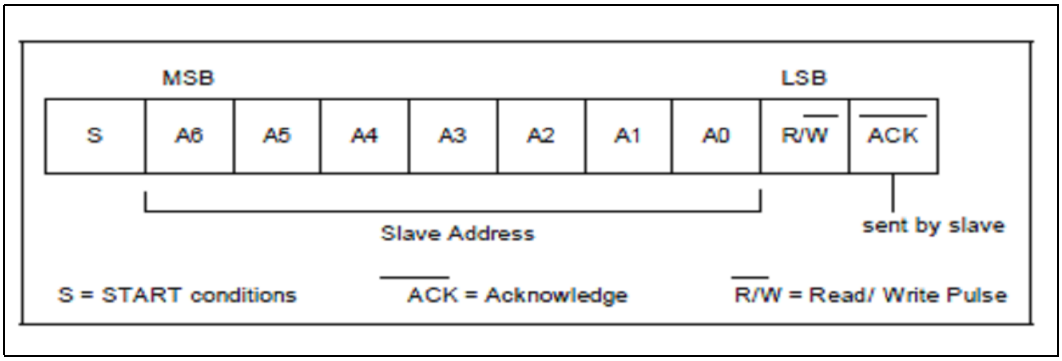
3.12.1.5 Addressing Slave Protocol

There are two address formats – 7-bit address format and 10-bit address format. Do take notes, the SoC did not support mixed address and mixed address format – that is, a 7-bit address transaction followed by a 10-bit address transaction or vice versa.

Seven-bit Address Format

- During the seven-bit address format, the first seven bits (bits 7:1) of the first byte set the slave address and the LSB bit (bit 0) is the R/W bit as shown in below figure.
- When bit 0 (R/W) is set to 0, the master writes to the slave. When bit 0 (R/W) is set to 1, the master reads from the slave.

Figure 3-29. Seven-Bit Address Format



Ten-bit Address Format

- During 10-bit addressing, 2 bytes are transferred to set the 10-bit address. The transfer of the first byte contains the following bit definition.

The first five bits (bits 7:3) notify the slaves that this is a 10-bit transfer. The next two bits (bits 2:1) set the slaves address bits 9:8, and the LSB bit (bit 0) is the RW bit.

The second byte transferred sets bits 7:0 of the slave address.

Figure 3-30 shows the 10-bit address format.

Figure 3-30. Ten-Bit Address Format

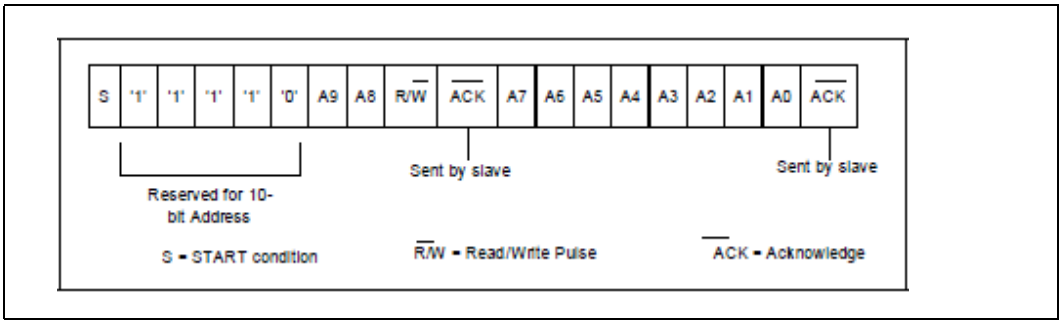


Table 3-44. I^2C Definition of Bits in First Byte

Slave Address	RW Bit	Description
0000 000	0	General Call Address - The I^2C controller places the data in the receive buffer and issues a General Call interrupt.
0000 000	1	START byte - For more details, refer to I^2C bus specification.
0000 001	X	CBUS address - I^2C controller ignores these accesses.
0000 010	X	Reserved
0000 011	X	Reserved
0000 1XX	X	High-speed master code
1111 1XX	X	Reserved
1111 0XX	X	Ten (10) - bit slave addressing

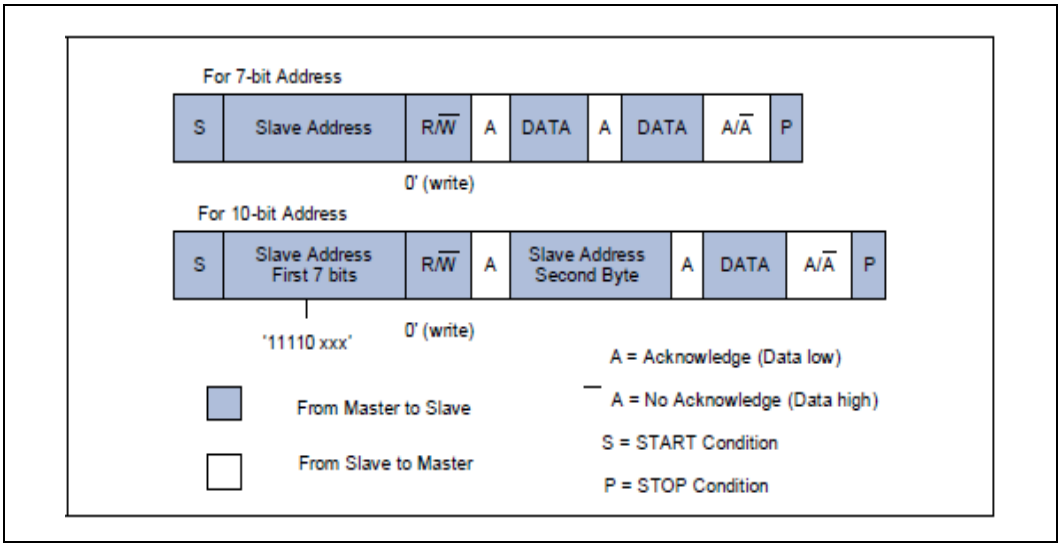
3.12.1.6 Transmit and Receive Protocol

The master can initiate data transmission and reception to/from the bus, acting as either a master-transmitter or master-receiver. A slave responds to requests from the master by either transmitting data or receiving data to/from the bus, acting as either a slave-transmitter or slave-receiver, respectively.

Master-Transmitter and Slave-Receiver All data is transmitted in byte format, with no limit on the number of bytes transferred per data transfer. After the master sends the address and RW bit or the master transmits a byte of data to the slave, the slave-receiver must respond with the acknowledge signal (ACK). When a slave-receiver does not respond with an ACK pulse, the master aborts the transfer by issuing a STOP condition. The slave must leave the data line high so that the master can abort the transfer.

If the master-transmitter is transmitting data as shown in below figure, then the slave-receiver responds to the master-transmitter with an acknowledge pulse after every byte of data is received.

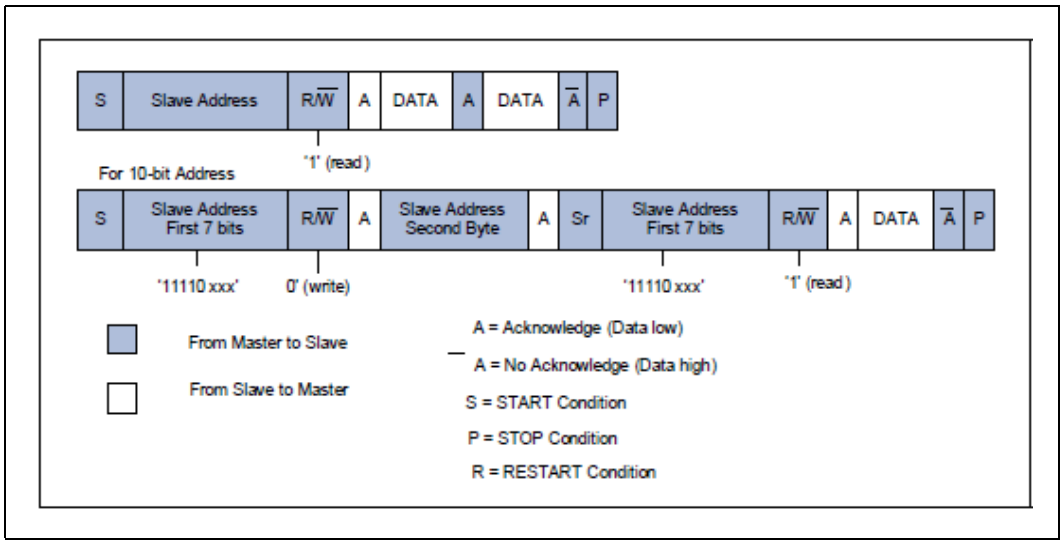
Figure 3-31. Master Transmitter Protocol



Master-Receiver and Slave-Transmitter If the master is receiving data as shown in below figure, the master responds to the Slave-Transmitter with an acknowledge pulse after a byte of data has been received, except for the last byte. This is the way the Master-Receiver notifies the Slave- Transmitter that this is the last byte. The Slave-Transmitter relinquishes the data line after detecting the No Acknowledge (NACK) so that the master can issue a STOP condition.

When a master does not want to relinquish the bus with a STOP condition, the master can issue a RESTART condition. This is identical to a START condition except it occurs after the ACK pulse. The master can then communicate with the same slave.

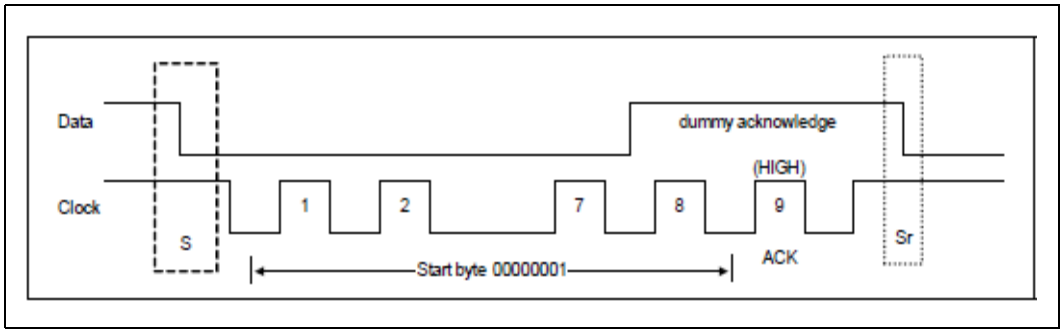
Figure 3-32. Master Receiver Protocol



3.12.1.7 START BYTE Transfer Protocol

The START BYTE Transfer protocol is set up for systems that do not have an on-board dedicated I^2C hardware module. When the I2C controller is a master, it supports the generation of START BYTE transfers at the beginning of every transfer in case a slave device requires it. This protocol consists of 7 '0's being transmitted followed by a 1, as illustrated in below figure. This allows the processor that is polling the bus to under-sample the address phase until 0s are detected. Once the microcontroller detects a 0, it switches from the under sampling rate to the correct rate of the master.

Figure 3-33. START Byte Transfer



The START BYTE procedure is as follows:

1. Master generates a START condition.
2. Master transmits the START byte (0000 0001).
3. Master transmits the ACK clock pulse. (Present only to conform with the byte handling format used on the bus.)
4. No slave sets the ACK signal to 0.
5. Master generates a RESTART (R) condition.

A hardware receiver does not respond to the START BYTE because it is a reserved address and resets after the RESTART condition is generated.

3.12.1.8 Use Case

Master Mode Operation

To use the I^2C controller as a master, perform the following steps:

1. Disable the I^2C controller by writing 0 (zero) to IC_ENABLE.ENABLE.
2. Write to the IC_CON register to set the maximum speed mode supported for slave operation IC_CON.SPEED and to specify whether the I^2C controller starts its transfers in 7/10 bit addressing mode when the device is a slave (IC_CON.IC_10BITADDR_SLAVE).
3. Write to the IC_TAR register the address of the I^2C device to be addressed. It also indicates whether a General Call or a START BYTE command is going to be performed by I^2C. The desired speed of the I^2C controller master-initiated transfers, either 7-bit or 10-bit addressing, is controlled by the IC_TAR.IC_10BITADDR_MASTER bit field.
4. Write to the IC_HS_MADDR register the desired master code for the I^2C controller. The master code is programmer-defined.
5. Enable the I^2C controller by writing a 1 in IC_ENABLE.
6. Now write the transfer direction and data to be sent to the IC_DATA_CMD register. If the IC_DATA_CMD register is written before the I^2C controller is enabled, the data and commands are lost as the buffers are kept cleared when the I^2C controller is not enabled.

The I^2C controller is not enabled (IC_ENABLE.ENABLE=0)The I^2C controller supports updating of the IC_TAR.IC_TAR and IC_TAR.IC_10BITADDR_MASTER. The IC_TAR register can be written to provided the following conditions are met:

- The I^2C controller is not enabled (IC_ENABLE.ENABLE=0)

The I^2C controller supports switching back and forth between reading and writing based on what is written in IC_CMD register. To transmit data, write the data to be written to the lower byte of the I^2C Rx/Tx Data Buffer and Command Register (IC_DATA_CMD). The IC_DATA_CMD.CMD should be written to 0 for I^2C write operations. Subsequently, a read command may be issued by writing “don't cares” to IC_DATA_CMD.DAT register bits, and a 1 should be written to the IC_DATA_CMD.CMD bit.

Disabling the I^2C Controller

The register IC_ENABLE allows software to unambiguously determine when the hardware has completely shutdown in response to the IC_ENABLE.ENABLE register being cleared from 1 to 0.

Procedure

1. Define a timer interval ($t_{i^2c\_poll}$) equal to 10 times the signaling period for the highest I^2C transfer speed used in the system and supported by the I^2C controller. For example, if the highest I^2C transfer mode is 400 Kb/s, then this $t_{i^2c\_poll}$ is 25 µs.
2. Define a maximum time-out parameter, MAX_T_POLL_COUNT, such that if any repeated polling operation exceeds this maximum value, an error is reported.

3. Execute a blocking thread/process/function that prevents any further I^2C master transactions to be started by software, but allows any pending transfers to be completed.
4. The variable POLL_COUNT is initialized to zero (0).
5. Clear IC_ENABLE.ENABLE to zero (0).
6. Read the IC_ENABLE_STATUS.IC_EN bit. Increment POLL_COUNT by one. If POLL_COUNT >= MAX_T_POLL_COUNT, exit with the relevant error code.
7. If IC_ENABLE_STATUS.IC_EN is 1, then sleep for ti^2c_poll and proceed to the previous step. Otherwise, exit with a relevant success code.

3.12.2 LPSS - UART Interface Overview

The LPSS implements 2 independent Universal Asynchronous Receiver/Transmitter (UART) Interfaces;UART0 and UART2 respectively. These four interfaces are controlled by a separate instance of an UART Controller. UART0, incorporates a UART Host Controller, Convergence Layer and integrated IDMA.

3.12.2.1 UART DMA Controller

The UART controller 1 (UART0) have an integrated DMA controller. Each channel contains a 64-byte FIFO. Max burst size supported is 32 bytes. UART controller 2 (UART2) only implements the host controllers and does not incorporate a DMA. Therefore, UART2 is restricted to operate in PIO mode only.

The DMA can operate in the following modes:

- Memory to peripheral transfers. This mode requires that the peripheral control the flow of the data to itself.
- Peripheral to memory transfer. This mode requires that the peripheral control the flow of the data from itself.

The DMA supports the following modes for programming:

- Direct programming. Direct register writes to DMA registers to configure and initiate the transfer.
- Descriptor based linked list. The descriptors will be stored in memory (e.g. DDR or SRAM). The DMA will be informed with the location information of the descriptor. DMA initiates reads and programs its own register. The descriptors can form a linked list for multiple blocks to be programmed.
- Scatter Gather mode.

3.12.2.2 UART Interrupts

UART interface has an interrupt line which is used to notify the driver that service is required.

When an interrupt occurs, the device driver needs to read both the host controller and DMA interrupt status registers to identify the interrupt source. Clearing the interrupt is done with the corresponding interrupt register in the host controller or DMA.

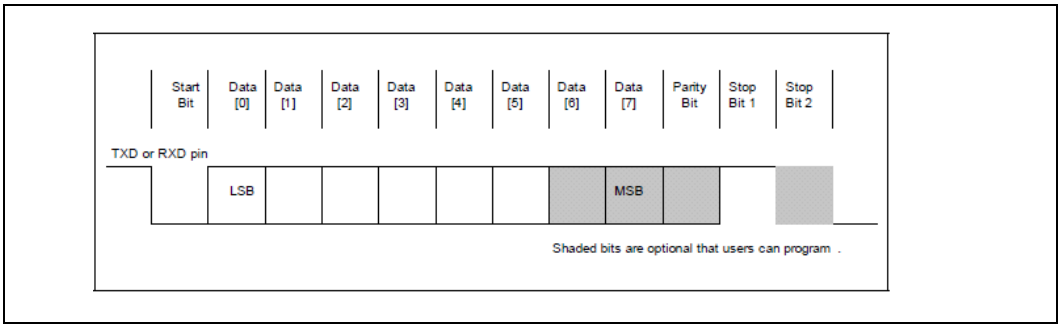
All interrupts are active high and their behavior is level interrupt.

3.12.2.3 UART Function

The UART transmits and receives data in bit frames as shown in Figure 3-34.

- Each data frame is between 7 and 12 bits long, depending on the size of data programmed and if parity and stop bits are enabled.
- The frame begins with a start bit that is represented by a high-to-ow transition.
- Next, 5 to 8 bits of data are transmitted, beginning with the least significant bit. An optional parity bit follows, which is set if even parity is enabled and an odd number of ones exist within the data byte; or, if odd parity is enabled and the data byte contains an even number of ones.
- The data frame ends with one, one-and-one-half, or two stop bits (as programmed by users), which is represented by one or two successive bit periods of a logic one.

Figure 3-34. UART Data Transfer Flow



3.12.2.4 Baud Rate Generator

The baud rates for the UARTs are generated with from the serial clock frequency (Sclock) by programming the DLH and DLL registers as a divisor. The hexadecimal value of the **divisor** is (IER_DLH[7:0]<<8) | RBR_THR_DLL[7:0].

Fbase is the system clock frequency in Hz (100,000,000 in decimal when the system clock frequency is 100 MHz.).

The output baud rate is as follows:

baud rate = (Sclk) / (16 * divisor)

- Sclk = (Fbase*M)/N
- Fbase = 100MHz
- M = reg_CLOCKS.M_VAL
- N = reg_CLOCKS.N_VAL
- Divisor (Most Significant Bits) = DLH[7:0] (Offset 04h)
- Divisor (Least Significant Bits) = DLL(7:0] (Offset 00h)

Table 3-45. Baud Rates Achievable with Different DLAB Settings

DLH,DLL Divisor	DLH,DLL Divisor Hexadecimal	Baud Rate
Sclock = 1.84320 MHz		
1	0001	115200
2	0002	57600
3	0003	38400
6	0006	19200
12	000C	9600
24	0018	4800
48	0030	2400
192	00C0	600
384	0180	300
Sclock = 58.9824 MHz		
4	0004	921600
8	0008	460800
16	0010	230400
24	0018	153600
Sclock = 32.768 MHz		
8	0008	256000
16	0010	128000

Notes:
1. DLH and DLL are only accessible when LCR.DLAB (Offset 48h, Bit 7) = 1b.
2. 307.2k baud is easily achievable from the possible configurations of M, N and Divisor.

3.12.3 LPSS SIO SPI Overview

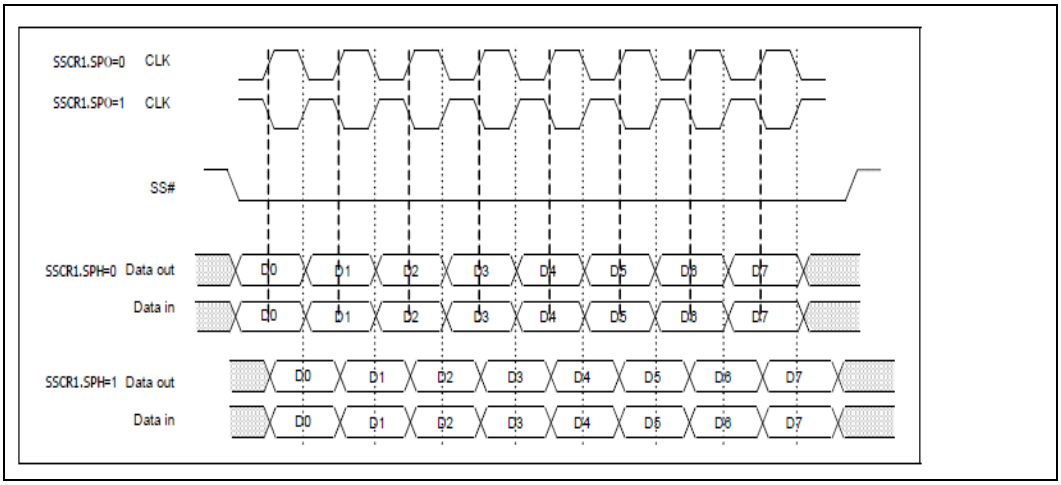
The LPSS SIO SPI is a full-duplex synchronous serial interface. It can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and many other devices which use serial protocols for transferring data. It supports the Motorola‘s* Serial Peripheral Interface (SPI) protocol.

3.12.3.1 Clock Phase and Polarity

SPI clock phase and clock polarity overview.

- The SSCR1.SPO polarity setting bit determines whether the serial transfer occurs on the rising edge of the clock or the falling edge of the clock.
  - — When SSCR1.SPO = 0, the inactive or idle state of SIO_SPI_CLK is low.
  - — When SSCR1.SPO = 1, the inactive or idle state of SIO_SPI_CLK is high.
- The SSCR1.SPH phase setting bit selects the relationship of the serial clock with the slave select signal.
  - — When SSCR1.SPH = 0, SIO_SPI_CLK is inactive until one cycle after the start of a frame and active until 1/2 cycle after the end of a frame.
  - — When SSCR1.SPH = 1, SIO_SPI_CLK is inactive until 1/2 cycle after the start of a frame and active until one cycle after the end of a frame.

Figure 3-35. 8-bit Data Transfer with Different Phase and Polarity Settings



3.12.3.2 Mode Numbers

The combinations of polarity and phases are referred to as modes which are commonly numbered according to the following convention, with SSCR1.SPO as the high order bit and SSCR1.SPH as the low order bit.

Table 3-46. SPI Modes

Mode	SSCR1.SPO	SSCR1.SPH
0	0	0
1	0	1
2	1	0
3	1	1

3.12.3.3 Frame Direction

The SSCR1.SFRMDIR bit is a read-write bit that determines whether the SSP is the master or slave with respect to driving the SSPSFRM. When SSCR1.SFRMDIR=0, the SSP generates the SSPSFRM internally, acts as the master and drives it. When SSCR1.SFRMDIR=1, the SSP acts as the slave and receives the SSPSFRM signal from an external device. When the SSP is to be configured as a slave to the frame, the external device driving frame must wait until the SSSR.CSS bit is cleared after enabling the SSP before asserting frame (i.e., not external clock cycles are needed, the external device just needs to wait a certain amount of time before asserting frame). When the GPIO alternate function is selected for the SSP, this bit has precedence over the GPIO direction bit (i.e. if SFRMDIR=1, the GPIO is an input, and if SFRMDIR=0, then the pin is an output). Therefore, the SCLKDIR and SFRMDIR bits should be written to before

the GPIO direction bits (to prevent any possible contention of the SSPSCLK or SSPSFRM pins). Also, when the SCLKDIR bit is set, the SSCR0.NCS and SSCR0.ECS bits must be cleared.

3.13 Fast SPI/eSPI

This SoC implements a fast SPI as the interface for boot loader flash storage. This interface implements 3 chip select signals, allowing up to 2 flashed devices and one TPM device to be connected and can run up to 50 MHz for optimal boot time.

The same controller implements a secondary SPI bus as interface for a touch controller. This interface can run up to 50 MHz and supports SSC (spread-spectrum clocking).

The same controller also implements an Enhanced Serial Peripheral Interface (eSPI) to support connection of an Embedded Controller (EC) or a Super I/O (SIO) to the platform, as an alternative to the LPC interface.

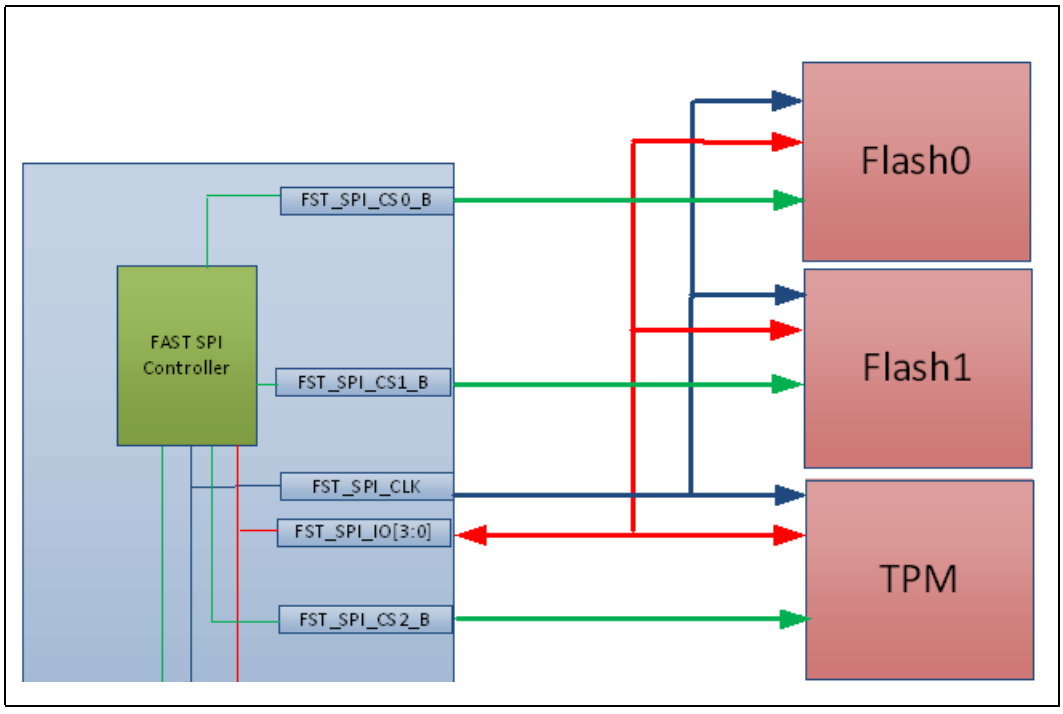
Note: The LPC and eSPI interfaces are mutually exclusive since they are multiplexed on the same package balls. The active interface is determined by the GPIO_175 hard strap.

3.13.1 FAST SPI Overview

The controller supports a maximum of two FST SPI devices, using two chip select signals.

1. Two Flash devices
2. TPM

Figure 3-36. Platform SPI-NOR Connectivity



The above diagram shows one possible configuration for the SPI controller. The takeaway is that there are dedicated pins for the data/address bus is shared between up to three devices.

3.13.1.1 Descriptor Mode

Descriptor Mode is required to enable many features of the SoC:

- Trusted Execution Engine
- Secure Boot
- PCI Express* root port configuration
- Supports for two SPI components using two separate chip select pins
- Hardware enforced security restricting master accesses to different regions
- Soft Strap region providing the ability to use Flash NVM to remove the need for pull-up/pull-down resistors for strapping SoC features
- Support for the SPI Fast Read instruction and frequencies greater than 20 MHz
- Support for Single Input, Dual Output Fast reads
- Use of standardized Flash instruction set

SPI Flash Regions

Only masters can access the 3 regions: The SoC CPU core running BIOS code and the Trusted Execution Engine. The only required region is Region 0, the Flash Descriptor. Region 0 must be located in the first sector of Device 0.

Flash Regions Sizes

SPI Flash space requirements differ by platform and configuration. Table 3-47 indicates the space needed in the Flash for each region.

Table 3-47. Region Size Versus Erase Granularity of Flash Components

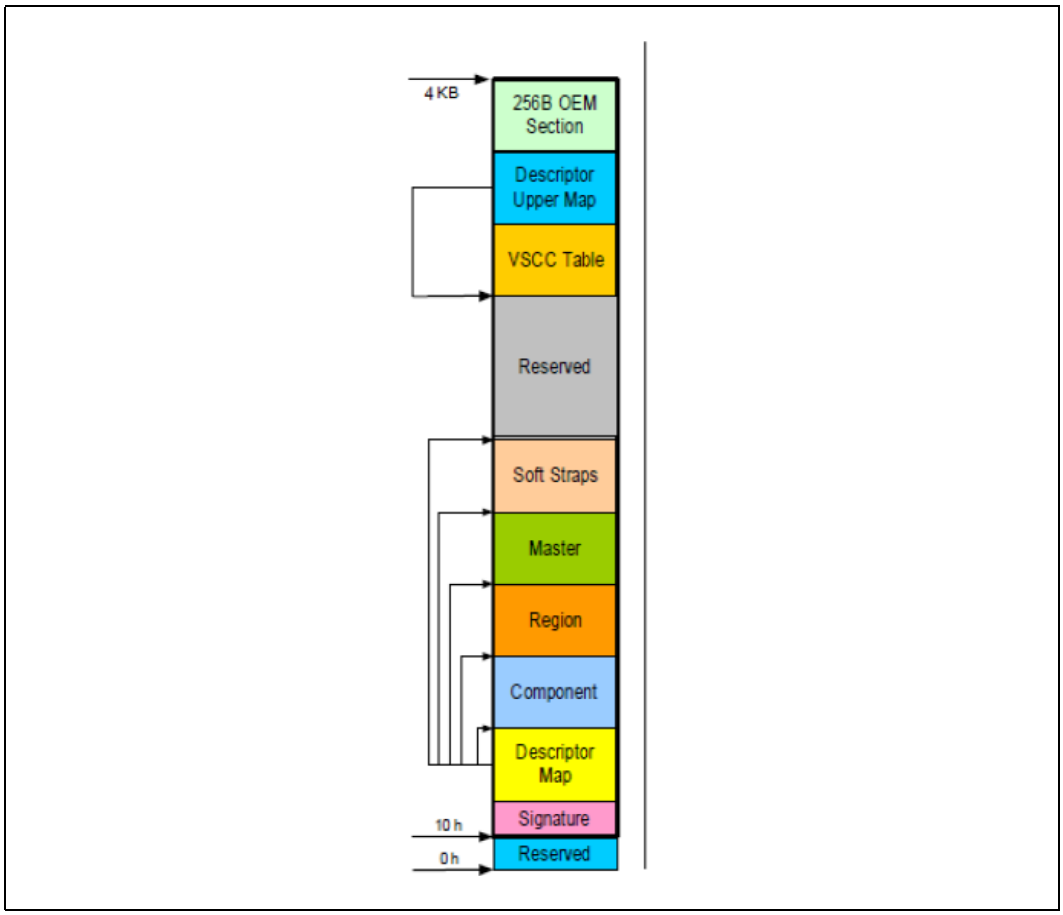
Region	Size with 4 KB Blocks	Size with 8 KB Blocks	Size with 64 KB Blocks
Descriptor	4 KB	8 KB	64 KB
BIOS	Varies by Platform	Varies by Platform	Varies by Platform
Trusted Execution Engine	Varies by Platform	Varies by Platform	Varies by Platform

3.13.1.2 Flash Descriptor

The maximum size of the Flash Descriptor is 4 KB. If the block/sector size of the SPI Flash device is greater than 4 KB, the Flash descriptor will only use the first 4 KB of the first block. The Flash descriptor requires its own block at the bottom of memory (00h). The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read only when the system containing the SoC leaves the manufacturing floor.

The Flash Descriptor is made up of eleven sections as indicated in below figure.

Figure 3-37. Flash Descriptor Sections



- The **Reserved** section at offset 0h is related to functionality not supported by the SoC.
- The **Signature** section selects Descriptor Mode as well as verifies if the Flash is programmed and functioning. The data at the bottom of the Flash (offset 10h) must be 0FF0A55Ah in order to be in Descriptor mode.
- The **Descriptor Map** section defines the logical structure of the Flash in addition to the number of components used.
- The **Component** section has information about the SPI Flash in the system including:
  - Density of each component.
  - Illegal instructions (such as chip erase).
  - Frequencies for read, fast read and write/erase instructions.
- The **Region** section points to the four other regions as well as the size of each region.
- The **Master** region contains the security settings for the Flash, granting read/write permissions for each region and identifying each master by a requester ID.
- The **Soft Straps** section contains parameter bits that can be used to configure SoC features and/or behaviors.

- The **Reserved** section between the top of the **Soft Straps** section and the bottom of the **VSCC Table** is reserved for future SoC usages.
- The **VSCC Table** section holds the JEDEC ID and the VSCC (Vendor Specific Component Capabilities) information of the entire SPI Flash supported by the NVM image.
- The **Descriptor Upper Map** section determines the length and base address of the **VSCC Table** section.
- The **OEM Section** is 256 Bytes reserved at the top of the Flash Descriptor for use by an OEM.

DnX Support

The expectation is that when the platform fails to boot the user will force a re-boot into DnX mode. If the descriptor is invalid but the DnX mode indication is false, then the desired behavior is for the flash controller to allow the CSME to come up and run using the old non-descriptor mode restrictions, however no flash controller behavior is guaranteed.

Descriptor Security Override Strap

A strap is implemented on to allow descriptor security to be overridden when the strap is sampled low.

If the strap is set (0b), it will have the following effect:

- The Master Region Read Access and Master Region Write Access permissions that were loaded from the Flash Descriptor Master Section will be overridden giving every master read and write permissions to the entire Flash component including areas outside the defined regions.

3.13.1.3 Flash Access

There are two types of Flash accesses: Direct Access and Program Register Access.

Direct Access

- Direct writes are not allowed for any master.
- The SoC CPU core is only allowed to do a direct read of the BIOS region.
- The Trusted Execution Engine is only allowed to do a direct read of the Trusted Execution Engine region.

Program Register Access

- Reads, Writes and Erases are all supported.
- Program Register Access may use Hardware or Software Sequencing.
- Program Register Accesses are not allowed to cross a 4 KB boundary and can not issue a command that might extend across two components.
- Software programs the FLA corresponding to the region desired.
  - —Software must read the devices Primary Region Base/Limit address to create a FLA.

Each master accesses the Flash through a set of memory mapped registers that are dedicated to each device.

There are two separate control and status registers that software can use when using register access to the Flash. The Hardware Sequencing control/status registers rely on hardware to issue appropriate Flash instructions and atomic sequences. The Software Sequencer puts control into the hands of the software for what instructions to issue and when.

The goal is to support all Flash components through hardware sequencing. Software sequencing is intended only for a back-up strategy.

3.13.1.4 Security

- Calculated Flash Linear Address (FLA) must fall between primary region base/limit.
- Direct Read Cache contents are reset to 0's on a read from a different master.
- Only primary region masters can access the registers.
- Masters are only allowed to read or write those regions they have read/write permission.
- Using the Flash region access permissions, one master can give another master read/write permissions to their area.
- Using the five Protected Range registers, each master can add separate read/write protection above that granted in the Flash Descriptor for their own accesses.
  - — Example: BIOS may want to protect different regions of BIOS from being erased.
  - — Ranges can extend across region boundaries.

3.13.1.5 Soft Flash Protection

There are two types of Flash protection that are not defined in the Flash descriptor supported by the SPI controller:

1. Flash Range Read and Write Protection
2. Global Write Protection

Flash Range Read and Write Protection

The SPI controller provides a method for blocking reads and writes to specific ranges in the Flash when the Protected Ranges are enabled. This is achieved by checking the read or write cycle type and the address of the requested command against the base and limit fields of a Read or Write Protected range. Protected range registers are only applied to Programmed Register accesses and have no effect on Direct Reads.

Note: Once BIOS has locked down the Protected BIOS Range registers, this mechanism remains in place until the next system reset.

3.13.2 eSPI Overview

eSPI is a replacement for the legacy LPC bus which is the traditional connection point for the platform’s embedded controller (EC). eSPI and LPC are mutually-exclusive platform configurations – when eSPI is enabled, LPC is disabled and vice versa.

3.13.2.1 SPI and eSPI Platform Configurations

There are two broad categories of platform configuration from the SPI/eSPI IP perspective:

LPC is enabled, and eSPI is enabled. As mentioned previously these are mutually-exclusive conditions.

3.13.2.2 LPC Enabled

LPC-Based with Optional Flash Sharing. In this mode, the EC is connected to the platform via LPC. EC may have its own flash, or share flash with the platform via pin connection.

Figure 3-38. EC Flash Sharing

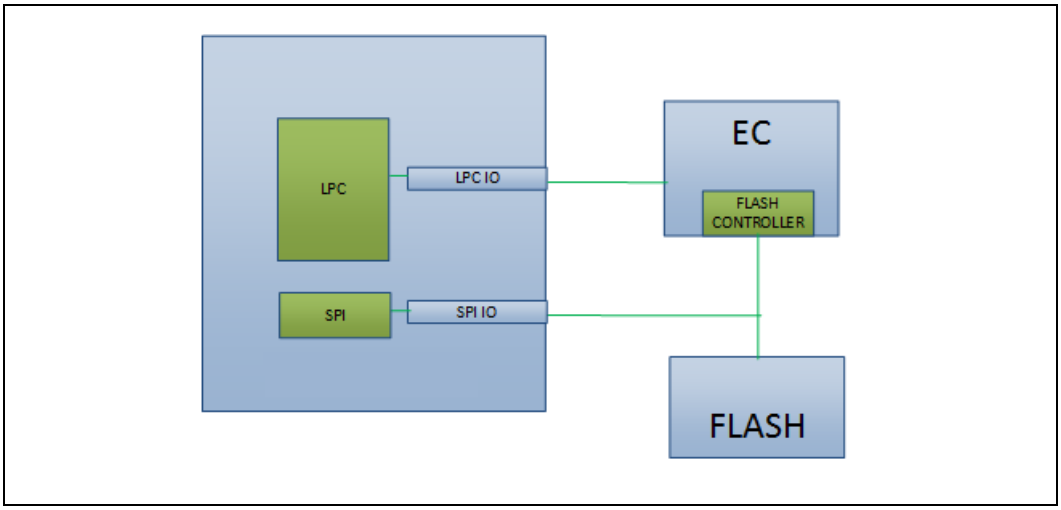
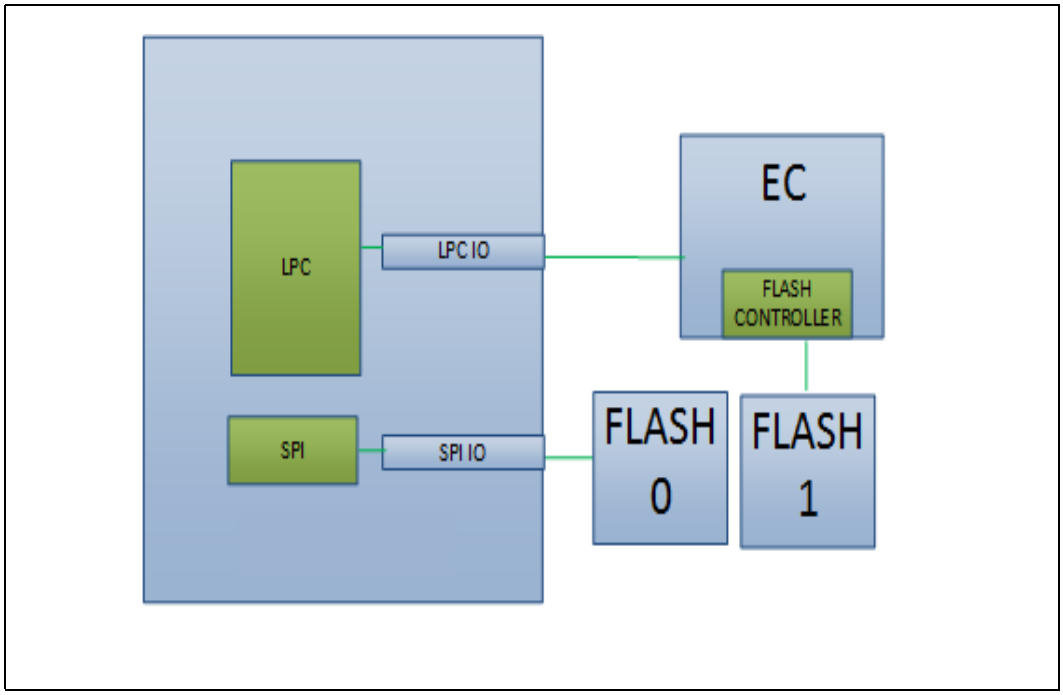


Figure 3-39. EC Dedicated Flash

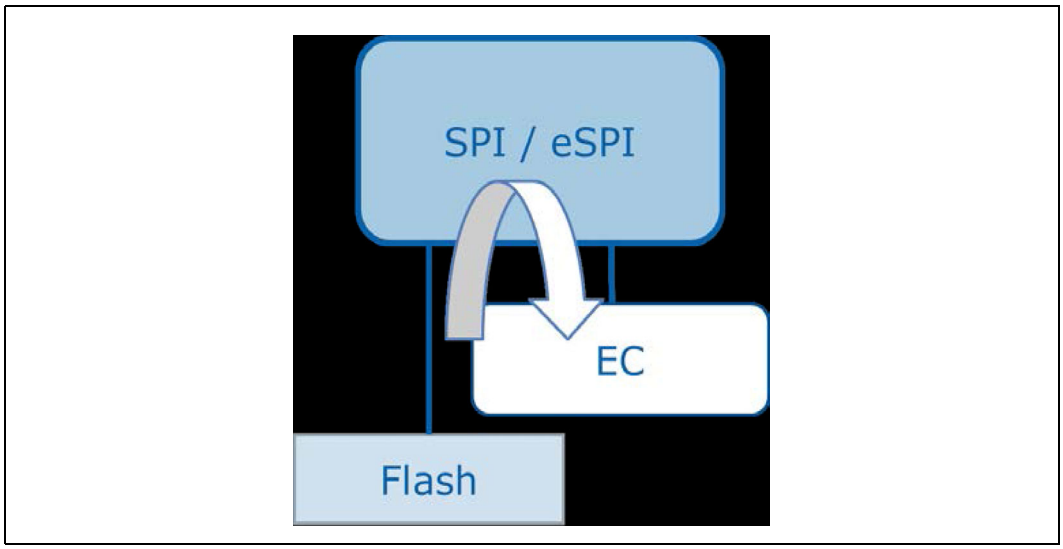


3.13.2.3 eSPI Enabled

Master-Attach Flash Mode

In Master-Attached flash mode, EC accesses platform flash via eSPI via the Flash Sharing channel. Because SPI/eSPI is an Always-On in SoC, flash remains accessible to EC in Sx.

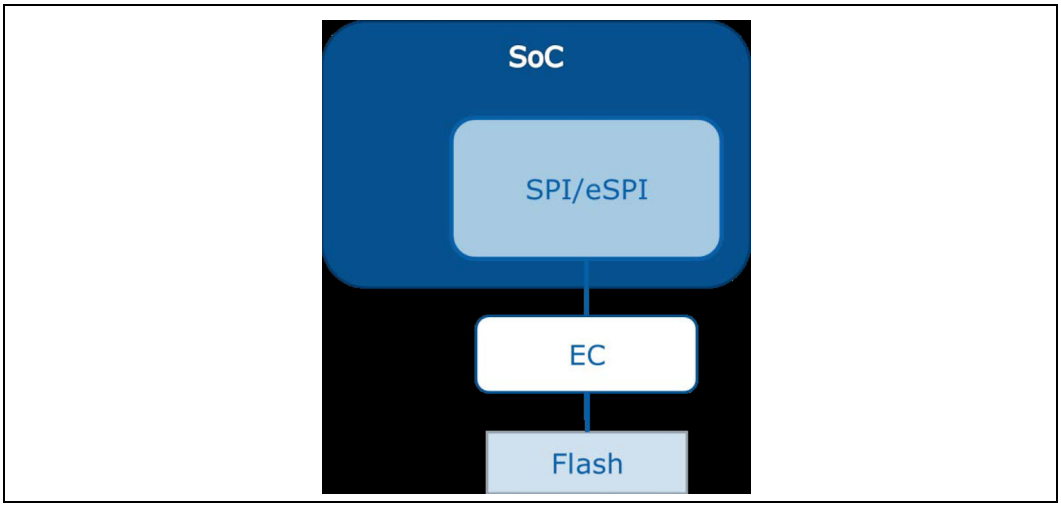
Figure 3-40. Master-Attach Flash Mode



Slave-Attach Flash Mode

In Slave-Attach Flash mode, the boot flash is owned and controlled by the EC, external to the SPI, as in the figure below. In this mode, SPI flash accesses are routed to the EC and return to the requester. Note the SPI will handle this routing internally, so that accessing agents need not be aware to whom their request routes

Figure 3-41. Slave-Attach Flash Mode



eSPI is multiplexed on top of the existing LPC pins in the following manner.

Table 3-48. eSPI/LPC Multiplexing

GPIO #	Existing Function1 (LPC mode)	New Function2 (eSPI mode)
LPC_AD0	LPC_AD0	ESPI_IO_0
LPC_AD1	LPC_AD1	ESPI_IO_1
LPC_AD2	LPC_AD2	ESPI_IO_2
LPC_AD3	LPC_AD3	ESPI_IO_3
LPC_FRAMEB	LPC_FRAMEB	ESPI_CSB
LPC_ILB_SERIRQ	LPC_ILB_SERIRQ	ESPI_RESETB
LPC_CLKRUNB	LPC_CLKRUNB	GP-In
LPC_CLKOUT0	LPC_CLKOUT0	ESPI_CLK
LPC_CLKOUT1	LPC_CLKOUT1	ESPI_CLK_FB

The feedback (loop-back) clock above has a slightly different implementation than other existing feedback clocks. In the case of Fast-SPI, the feedback clock buffer is a physically separate buffer that sits next to the actual clock buffer and has no additional functionality than timing calibration inside the CFIO PHY. eSPI did not add a separate physical buffer, but simply utilized the existing clock buffer as the feedback clock in Function 2, eSPI mode.

Two new pin straps were also added for eSPI:

1. The first (eSPI or LPC) simply allows the platform to select between LPC vs. eSPI. This strap is needed because the interface type must be chosen before BIOS is running. (BIOS can normally select the function on each GPIO).
2. The second pin strap (eSPI Flash Sharing Mode) is used to determine if Master-Attached or Slave-Attached Flash Sharing is utilized on the platform.

3.14 Intel Legacy Block

3.14.1 Interrupt and Timer Sub System

- 8259 Controllers
  - Registers mapped to fixed I/O locations
  - Uses Messages to CPU to indicate interrupt
  - 15 total interrupts
- I/O APIC
  - Registers mapped to fixed I/O locations
  - Uses Messages to CPU to indicate interrupt
- 8254 timers
  - Registers mapped to fixed I/O locations
  - Has 3 internal timers
  - Timer 0 - used for OS timer tick
  - Timer 1 - Unused
  - Timer 2- used for “beep” speaker
- HPET - High Performance Event Timers
  - Includes one periodic timer, seven one-shots (total eight comparators)
  - Improved resolution, reduced overhead
  - Results in fewer interrupts to CPU
- LPC (Low Pin Count) Bus
  - All LPC devices need to support CLOCKRUN protocol.

3.15 GPIO

3.15.1 GPIO Feature Overview

SoC contains general purpose input and output (GPIO) pads. The high level features of GPIO are:

- Total of 215 GPIO capable pins.
- 1.8V, 3.3V signaling available on GPIO signals.

Note: Check the GPIO Multiplexing Table 2-28 for more details.

- Each GPIO pad can be configured as an input or output signal.
- Most pads are multiplexed between GPIO mode and native mode function(s).
- Configurable GPIO pad ownership by TXE to TXE itself, ISH or host.

- SCI/GPE and IOxAPIC interrupt capable on all GPIOs.
- GPI GPE Status and GPE Enable registers in GPIO Community.
- Direct IOxAPIC interrupts available on select GPIO.
- 32 pins from two communities can be selected as direct interrupt wake events.
- Eight pins from two communities can be selected as TXE wake events.
- SMI capable on selected GPIOs (NMI not implemented on SoC).
- GPIO registers accessible through IOSF-SB.

3.15.2 Functional Description

3.15.2.1 GPIO Communities

GPIOs are divided into communities:

- Northwest: Display, USB, I^2C, UART, and Thermal GPIO
- North: power management GPIO, I^2C, Display, LPC/eSPI, SPI
- Audio: Audio GPIO
- SCC: SMBus, Clock, CNV, eMMC

All of the communities are powered by the AON domain, and are available in all power states. Many of the signals are driven by VNN domains, so isolation is done locally and IOStandby may be employed.

3.15.2.2 GPIO Buffer Types

There are six types of GPIO buffers with differing characteristics. Summary is listed here:

1. High-speed, medium voltage (HSMV)
   - Output frequencies up to 200 MHz
   - 50/67/100/200 Ω Output impedance
   - Optional internal 20 KΩ pull-up/pull-down
2. Low-speed, medium voltage (LSMV)
   - Reduced version of HSMV with output frequencies up to 25 MHz
   - 200 Ω impedance
   - Optional internal 20 KΩ pull-up/pull-down
   - Generally used for static signaling
3. Medium-speed, medium voltage (MSMV)
   - Open-drain only medium speed CFIO
   - Output frequencies up to 50 MHz
   - Optional current source for high-speed open drain operation
   - 35/200 Ω impedance
   - Optional internal 1K/2K/20 KΩ pull-up, and 20 KΩ pull-down
4. High-speed, high voltage (HSHV)
   - ‘High voltage’ refers to supporting 3.3 V operation.

- This buffer also supports selectable 3.3 V/1.8 V operation, and the voltage can be selected per-pad
- Output frequencies up to 50MHz at 3.3 V
- 40-60 Ω drive impedance
- Optional internal 20 KΩ pull-up/pull-down

5. Medium-speed, high voltage (integrated MSHV)
   - This buffer also supports 3.3 V operation in addition to 1.8 V
   - Additional ESD protection is not included in this buffer
   - This buffer is used on LPC, SMBUS, and the PMU family of signals
   - Output frequencies up to 50MHz at both 3.3 V and 1.8 V
   - Optional current source for high-speed open drain operation (only at 1.8 V)
   - 40-60 Ω drive impedance
   - Optional internal 1K/2K/20 KΩ pull-up, and 20KΩ pull-down
6. Medium Speed, Medium Voltage (MSMV) CFIO
   - This buffer allows 1.05V-open-drain operation
   - This buffer is solely used on the SVID interface. Use of this buffer for SVID allows SoC to communicate with both types of platform power delivery scenarios

3.15.3 Summary of Registers

GCR.GPIO_GPE_CFG - Maps the ACPI GPE0[b-d] registers to GPIO communities. Each of gpe0_dw[1-3] is a lookup which maps a read/write to gpe0[b-d]_[en,sts] to a particular GPIO community and offset. Note that ACPI GPE0a (i.e. GPE0[31:0]) is reserved for SoC internal events and cannot be mapped to a GPIO community. This explains why gpe0_dw0 is reserved.

ACPI.GPE0[b-d]_[en,sts] - Reads/writes to this register will result in the transaction being forwarded to the corresponding GPIO community based on the GPIO_GPE_CFG register configuration.

Table 3-49. Register Mapping from GPIO_GPE_CFG to SCI Tier 1 Group (Sheet 1 of 2)

GPIO_GPE_CFG gpe0_dw[3:1] value mapping	SCI Tier1 Group	GPIO Community Status Register	CR Address Offset	GPIO Community Enable Register	CR Address Offset	Note
15	RSVD	GPI_GPE_STS_scc_0	0x0130	GPI_GPE_EN_scc_0	0x0150	If programmed will map to SCI Tier1 Group 0
14	RSVD	GPI_GPE_STS_scc_0	0x0130	GPI_GPE_EN_scc_0	0x0150	If programmed will map to SCI Tier1 Group 0
13	RSVD	GPI_GPE_STS_scc_0	0x0130	GPI_GPE_EN_scc_0	0x0150	If programmed will map to SCI Tier1 Group 0
12	RSVD	GPI_GPE_STS_scc_0	0x0130	GPI_GPE_EN_scc_0	0x0150	If programmed will map to SCI Tier1 Group 0
11	RSVD	RSVD7[1]	0x0138	RSVD7[1]	0x0158	GPIO destination is RSVD
10	RSVD	RSVD7[0]	0x0134	RSVD7[0]	0x0154	GPIO destination is RSVD

Table 3-49. Register Mapping from GPIO_GPE_CFG to SCI Tier 1 Group (Sheet 2 of 2)

9	7	GPI_GPE_STS_audio_0	0x0130	GPI_GPE_EN_audio_0	0x0150	
8	6	GPI_GPE_STS_NORTH_2	0x0138	GPI_GPE_EN_NORTH_2	0x0158	
7	5	GPI_GPE_STS_NORTH_1	0x0134	GPI_GPE_EN_NORTH_1	0x0154	
6	4	GPI_GPE_STS_NORTH_0	0x0130	GPI_GPE_EN_NORTH_0	0x0150	Default/Reset value for gcr.gpio_gpe_cfg.gpe0_dw1
5	3	GPI_GPE_STS_NORTHWEST_3	0x013C	GPI_GPE_EN_NORTHWEST_3	0x015C	
4	2	GPI_GPE_STS_NORTHWEST_2	0x0138	GPI_GPE_EN_NORTHWEST_2	0x0158	
3	1	GPI_GPE_STS_NORTHWEST_1	0x0134	GPI_GPE_EN_NORTHWEST_1	0x0154	Default/Reset value for gcr.gpio_gpe_cfg.gpe0_dw1
2	0	GPI_GPE_STS_NORTHWEST_0	0x0130	GPI_GPE_EN_NORTHWEST_0	0x0150	
1	9	GPI_GPE_STS_scc_1	0x0134	GPI_GPE_EN_scc_1	0x0154	
0	8	GPI_GPE_STS_scc_0	0x0130	GPI_GPE_EN_scc_0	0x0150	Default/Reset value for gcr.gpio_gpe_cfg.gpe0_dw1

3.15.4 GPIO Architecture

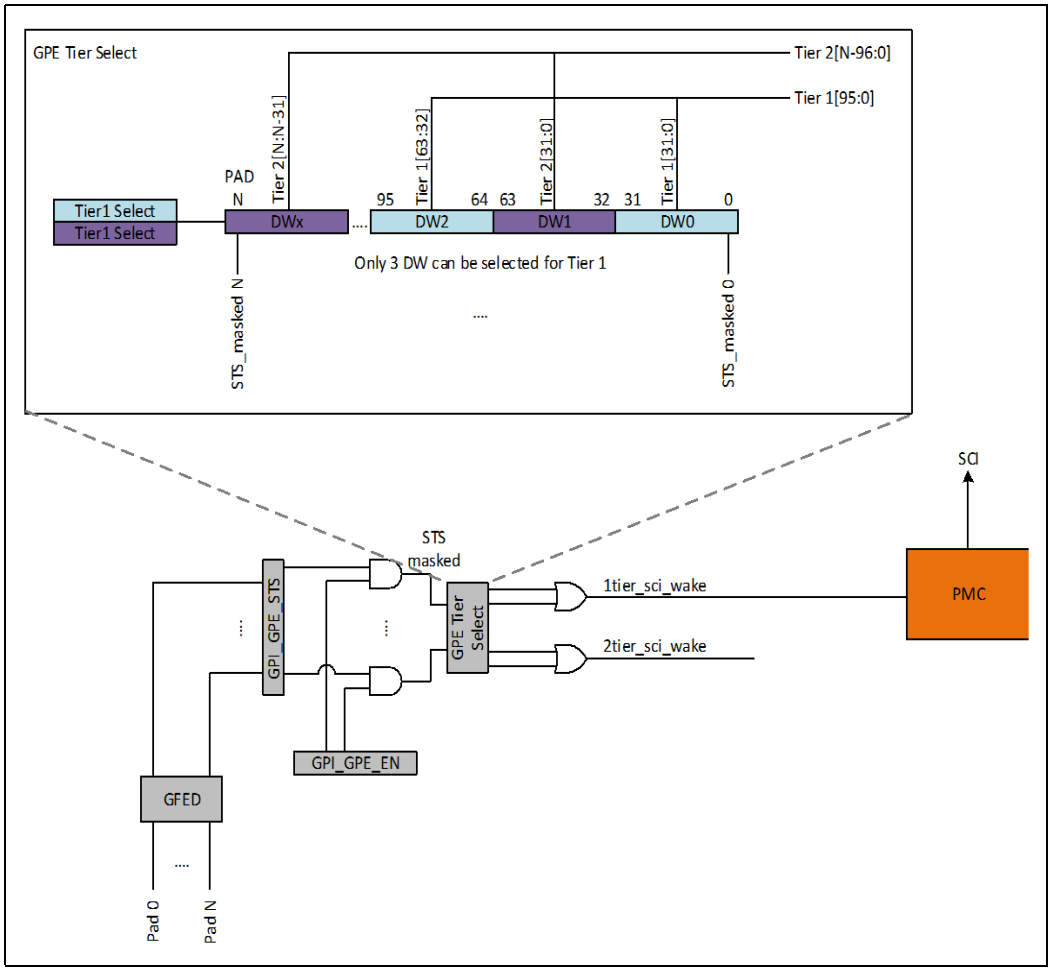
The GPIO controller implements the "2-tier" SCI mechanism. The ACPI register for SCI events must be in the PMC address space, and is only 128 bits long. Of those 128 bits, only 96 are allowed for GPIO.

This means that out of all the GPIO, only 72 can be selected and some are not available because they fall into the "reserved" section and have no status bits. The capabilities table clarifies which pins may be used to generate an SCI and report their status. The SCI capable pins are broken into ten groups of 24 and are numbered in the table. Only three of these groups can be mapped to the ACPI register, and they are selected in the GPE0_DW* fields of the MISCCFG community register.

Note: All communities must have the same settings for the GPE0_DW* fields. Groups are unique across all communities, and in order to prevent false SCI wire triggering the settings should be the same across communities.

The concept of a "tier2" wake event where the groups not mapped to the 96 bit ACPI register can still cause a wake event. SoC does not support the second tier, so only those pads mapped to the ACPI can generate wake events. The below figure shows the mapping to the first tier (wake event) and the unused second tier.

Figure 3-42. SCI/GPE Group Mapping to GPE0_DW* Register



For each pad capable of making an SCI/GPE event, there is a field named GPIOIRoutSCI in the per-pad DW0 register that is used to enable the SCI event generation. All SCI enabled pad trigger outputs are ORed together and sent out as a single wire to the PMC. Internally the PMC ORs the five community wires together into a single wake event.

When the PMC sees an SCI/GPE wake event, it will wake the system and send an SCI to the host. The host will then send a sideband read to the ACPI register that will be proxied to the appropriate GPIO GPI_SPE_STS based on the GPE0_DW* mapping, which the PMC is also aware of.

3.15.5 GPIO Capabilities

All GPIOs can be configured as either input or output. All pins that default to GPIO mode input have their output drivers tri-stated including during power-on and reset. If a certain pin state is desired to be maintained on the GPIO mode input pins, external pull up or down is needed. All pins that default as GPIO outputs of 0 level shall not glitch high during power-on and reset.

3.15.5.1 Offset 010h - Miscellaneous Configuration (MISCCFG)

This register is meant to house miscellaneous configuration fields like dynamic clock gating enable, test mode etc. and is implemented per Community.

Bits	Access Type	Default	Description	Reset
31:20	RW	0	Reserved	Powergood Only
19:16	RW	0100	GPIO Group to GPE_DW0 assignment encoding (**GPE0_DW2**[2:0]): This register assigns a specific GPIO Group to the ACPI GPE0 [95:64] (aka ACPI_GPE0d) 0h = reserved[11:0]&group0[19:0] 1h = reserved[7:0]&group1[23:0] 2h = reserved[7:0]&group2[23:0] 3h = reserved[31:0] 4h = reserved[27:0]&group4[3:0] 5h = reserved[7:0]&group5[23:0] 6h = reserved[23:0]&group6[7:0] 7h = reserved[7:0]&group7[23:0] 8h = reserved[20:0]&group8[10:0] 9h = reserved[21:0]&group9[9:0]	Powergood Only
15:12	RW	0011	GPIO Group to GPE_DW0 assignment encoding (**GPE0_DW1**[2:0]): This register assigns a specific GPIO Group to the ACPI GPE0[63:32] (aka ACPI_GPE0c) 0h = reserved[11:0]&group0[19:0] 1h = reserved[7:0]&group1[23:0] 2h = reserved[7:0]&group2[23:0] 3h = reserved[31:0] 4h = reserved[27:0]&group4[3:0] 5h = reserved[7:0]&group5[23:0] 6h = reserved[23:0]&group6[7:0] 7h = reserved[7:0]&group7[23:0] 8h = reserved[20:0]&group8[10:0] 9h = reserved[21:0]&group9[9:0]	Powergood Only
11:8	RW	0010	GPIO Group to GPE_DW0 assignment encoding (**GPE0_DW0**[2:0]): This register assigns a specific GPIO Group to the ACPI GPE0[31:0] (aka ACPI_GPE0b) 0h = reserved[11:0]&group0[19:0] 1h = reserved[7:0]&group1[23:0] 2h = reserved[7:0]&group2[23:0] 3h = reserved[31:0] 4h = reserved[27:0]&group4[3:0] 5h = reserved[7:0]&group5[23:0] 6h = reserved[23:0]&group6[7:0] 7h = reserved[7:0]&group7[23:0] 8h = reserved[20:0]&group8[10:0] 9h = reserved[21:0]&group9[9:0]	Powergood Only
7:4	RW	0	Reserved	Powergood Only
3	RW	0	**GPIO Driver IRQ_ROUTE[1:0]:** Specifies the APIC IRQ globally for all GPP_A and GPP_B pads (GPI_IS with corresponding GPI_IE enable). 0 = IRQ14 1 = IRQ15	Powergood Only

Bits	Access Type	Default	Description	Reset
2	RW	0	GSX Static Local Clock Gating (GSXSLCGEn) Specify whether the GSX controller should be statically clock gated for power saving if it is not enabled (even though the capability is available). 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating	Powergood Only
1	RW	0	GPIO Dynamic Partition Clock Gating Enable (GPDPCGEn) Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating	Powergood Only
0	RW	0	GPIO Dynamic Local Clock Gating Enable (GPDLCGEn) Specify whether the GPIO Community should perform local clock gating 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating	Powergood Only

3.15.5.2 GPIO Interrupt and Wake Capabilities

All GPIOs can be configured as either input or output. All pins that default to GPIO mode input have their output drivers tri-stated including during power-on and reset. If a certain pin state is desired to be maintained on the GPIO mode input pins, external pull up or down is needed. All pins that default as GPIO outputs of 0 level shall not glitch high during power-on and reset.

The following tables show GPIO capabilities. The table summarizes the pins by function showing the maximum capabilities and pins available; the actual pins available in any application may be reduced by pin multiplexing.

3.15.6 Power State Considerations

GPIO are capable of making several different types of interrupts to the system. These include shared IRQ, direct IRQ, SMI, SCI, etc. but many of them generate messages to the APIC, and due to the low power states employed by SoC power management it is necessary to handle these interrupts differently during S0ix.

3.15.6.1 IO-Standby

SoC introduces a new feature called GPIO “IO-Standby”, which enables customers to set the “default” logic of each GPIO pin in a power-friendly state when the SoC enters S0ix or Sx power states. There are two per-pin registers that control its behavior, shown in the lists below. The first controls the Tx and Rx behavior; the second controls the on-die termination.

GPIO IO-Standby Tx/Rx Settings:

0 = Tx enabled driving last value driven, Rx enabled

1 = Tx enabled driving 0, Rx disabled and Rx driving 0 back to its controller internally

2 = Tx enabled driving 0, Rx disabled and Rx driving 1 back to its controller internally

3 = Tx enabled driving 1, Rx disabled and Rx driving 0 back to its controller internally

4 = Tx enabled driving 1, Rx disabled and Rx driving 1 back to its controller internally

5 = Tx enabled driving 0, Rx enabled

6 = Tx enabled driving 1, Rx enabled

7 = Hi-Z, Rx driving 0 back to its controller internally

8 = Hi-Z, Rx driving 1 back to its controller internally

9 = Tx disabled, Rx enabled

15 = IO-Standby is ignored for this pin (same as functional mode)

GPIO IO-Standby Termination Settings:

0 = Same as functional mode (no change)

1 = Disable Pull-up and Pull-down (no on-die termination)

2 = Enable Pull-down

3 = Enable Pull-up

Note: Refer to Volume 2 for more details on the setting.

Note: By default in hardware, each GPIO is programmed as '0' for Tx/Rx behavior and '0' for termination behavior. Intel's reference BIOS changes these settings to recommended starting points assuming a platform usage similar to the Intel Reference design boards. With "IO-Standby" each customer has the option to modify the setting of the every GPIO to best match their specific platform implementation.

For example, if a customer chooses to use an I^2C port as two GPIOs, the customer can also modify the IO-Standby register settings to match the new GPIO usage for that platform implementation.

3.15.7 Wire Based Wake Events

GPIO Supports Wire Based Wake events. The individual types of wake event supported are described below.

3.15.7.1 SCI/GPE Wake

SoC GPIO supports SCI (System Control Interrupt)/GPE Event.

The SCI capable pins are broken into ten groups of 24 and are numbered in the table. Only three of these groups can be mapped to the ACPI register, and they are selected in the GPE0_DW* fields of the MISCCFG community register. All communities must have the same settings for the GPE0_DW* fields. Groups are unique across all communities, and in order to prevent false SCI wire triggering the settings should be the same across communities.

The GPIO can be configured to enable as SCI/GPE through the DW0 register by setting the GPIOIRoutSCI field. All SCI enabled pad trigger outputs are ORed together and sent out as a single wire.

Note: Only the pads which are mapped to the ACPI can generate wake events.

3.15.7.2 Shared IRQ

Shared IRQ is a mechanism where any pin can be used to create an interrupt to the IOxAPIC.

In S0, an ASSERT_IRQ message with either source 0x14 or 0x15 (selectable in the GPIO_DRIVER_IRQ_ROUTE of the MISCCFG register). There are status and enable registers named GPI_INT_STS and GPI_INT_EN associated with this IRQ.

When in S0ix, the status outputs of all pads in a community are ORed together and sent as a wake event.

3.15.7.3 Direct IRQ

The direct IRQ, or reduced hardware, IRQ mode allows a GPIO to send an interrupt to the IOxAPIC using a fixed IRQ number which is enabled by the GPIOIRoutIOxAPIC field in each pad's DW0 register. There are no status/enable registers associated with this interrupt mechanism.

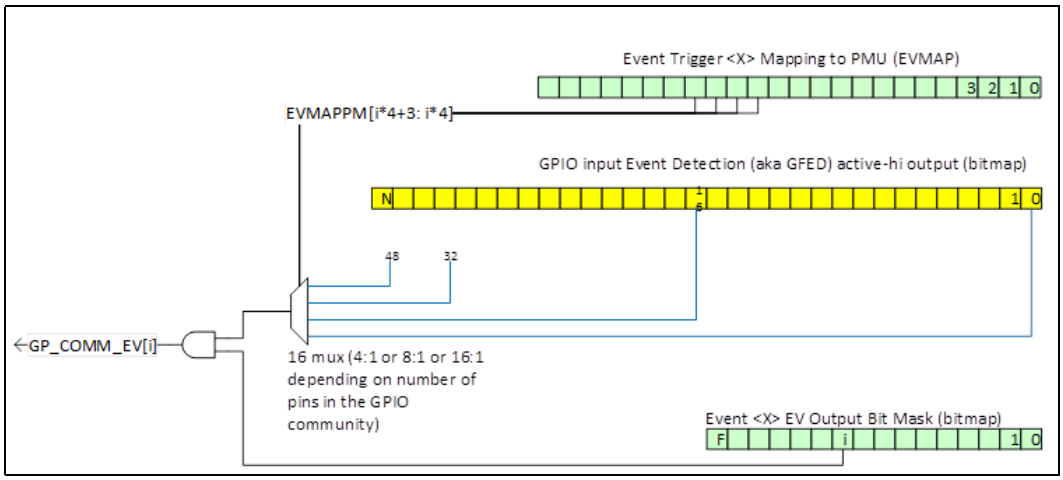
Only two communities have the capability to generate these wake wires: Northwest and North. There are 16 wake wires per community (total of 32 wires) that may be mapped to the direct IRQ capable GPIOs in that community.

Note: S3 wake by GPIO Direct IRQ method is NOT supported.

3.15.7.3.1 Event Multiplex Mapping

Since there are more direct IRQ capable GPIO than wake wires from the community, the SoC provides event multiplexing capability which allows the pads to be mapped down to just 16 wake wires per capable community. The event multiplex is show in Figure 3-43.

Figure 3-43. Event Multiplex



In this example, wire0 can select output 0, 16, 32, etc. The multiplex size depends on the community size:

16 < X ≤ 32 = 2:1 multiplex

32 < X ≤ 64 = 4:1 multiplex

64 < X ≤ 128 = 8:1 multiplex

128 < X ≤ 256 = 16:1 multiplex

Most communities are 4:1 or 8:1

Note: Only single pad out of the table can be routed to multiplex Out.

Table 3-50. Northwest Community Event Select Mapping (TXE and Direct IRQ)

Northwest Community (TXE and Direct IRQ Wake Wires)													
Pads							80						
Multiplex Out	Multiplex Select												
7		6		5		4	3		2		1	0	
0	112	96	80	LPSS_UART2_RXD	64	PMC_I2C_SDA	48	GPIO_32	32	GPIO_16	16	TCK	
1	113	97	81	LPSS_UART2_TXD	65	PMC_I2C_SCL	49	GPIO_33	33	GPIO_17	17	TRST_B	
2	114	98	82	LPSS_UART2_RTS_B	66	LPSS_I2C0_SDA	50	GPIO_34	34	GPIO_18	18	TMS	
3	115	99	83	LPSS_UART2_CTS_B	67	LPSS_I2C0_SCL	51	GPIO_35	35	GPIO_19	19	TDI	
4	116	100	84	PMC_SPI_FS0	68	LPSS_I2C1_SDA	52	GPIO_36	36	GPIO_20	20	TDO	
5	117	101	85	PMC_SPI_FS1	69	LPSS_I2C1_SCL	53	GPIO_37	37	GPIO_21	21	JTAGX	
6	118	102	86	PMC_SPI_FS2	70	LPSS_I2C2_SDA	54	GPIO_38	38	GPIO_22	22	CX_PREQ_B	
7	119	103	87	PMC_SPI_RXD	71	LPSS_I2C2_SCL	55	GPIO_39	39	GPIO_23	23	CX_PRDY_B	
8	120	104	88	PMC_SPI_TXD	72	LPSS_I2C3_SDA	56	GPIO_40	40	GPIO_24	24	GPIO_8	
9	121	105	89	PMC_SPI_CLK	73	LPSS_I2C3_SCL	57	GPIO_41	41	GPIO_25	25	GPIO_9	
10	122	106	90	THERMTRIP_B	74	LPSS_I2C4_SDA	58	GP_INTD_DSI_TE1	42	GPIO_26	26	GPIO_10	
11	123	107	91	PROCHOT_B	75	LPSS_I2C4_SCL	59	GP_INTD_DSI_TE2	43	GPIO_27	27	GPIO_11	
12	124	108	92	EMMC_RST_B	76	LPSS_UART0_RXD	60	USB_OC0_B	44	GPIO_28	28	GPIO_12	
13	125	109	93	GPIO_212	77	LPSS_UART0_TXD	61	USB_OC1_B	45	GPIO_29	29	GPIO_13	
14	126	110	94	GPIO_213	78	LPSS_UART0_RTS_B	62	DSI_I2C_SDA	46	GPIO_30	30	GPIO_14	
15	127	111	95	GPIO_214	79	LPSS_UART0_CTS_B	63	DSI_I2C_SCL	47	GPIO_31	31	GPIO_15	

Table 3-51. Northwest Community Mapping (TXE and Direct IRQ)

North Community (CSE and Direct IRQ Wake Wires)													
Pads							80						
Multiplex Out							Multiplex Select						
7			6		5		4	3			2	1	0
0	112	96	80	GPIO_140	64	HV_DDI0_DDC_SDA	48	PMU_SUSCLK	32	FST_SPI_MOSI_IO0	16	SVID0_ALERT_B	0
1	113	97	81	GPIO_141	65	HV_DDI0_DDC_SCL	49	SUS_STAT_B	33	FST_SPI_MISO_IO1	17	SVID0_DATA	1
2	114	98	82	GPIO_142	66	HV_DDI1_DDC_SDA	50	LPSS_I2C5_SDA	34	FST_SPI_IO2	18	SVID0_CLK	2
3	115	99	83	GPIO_143	67	HV_DDI1_DDC_SCL	51	LPSS_I2C5_SCL	35	FST_SPI_IO3	19	LPSS_SPI_0_CLK	3
4	116	100	84	GPIO_144	68	PANEL0_VDDEN	52	LPSS_I2C6_SDA	36	FST_SPI_CLK	20	LPSS_SPI_0_FS0	4
5	117	101	85	GPIO_145	69	PANEL0_BKLTEN	53	LPSS_I2C6_SCL	37	FST_SPI_CLK_FB	21	LPSS_SPI_0_FS1	5
6	118	102	86	GPIO_146	70	PANEL0_BKLTCTL	54	LPSS_I2C7_SDA	38	PMU_PLTRST_B	22	LPSS_SPI_0_RXD	6
7	119	103	87	LPC_ILB_SERIRQ	71	HV_DDI0_HPD	55	LPSS_I2C7_SCL	39	PMU_PWRBTN_B	23	LPSS_SPI_0_TXD	7
8	120	104	88	LPC_CLKOUT0	72	HV_DDI1_HPD	56	PCIE_WAKE0_B	40	PMU_SLP_S0_B	24	LPSS_SPI_2_CLK	8
9	121	105	89	LPC_CLKOUT1	73	HV_EDP_HPD	57	PCIE_WAKE1_B	41	PMU_SLP_S3_B	25	LPSS_SPI_2_FS0	9
10	122	106	90	LPC_AD0	74	GPIO_134	58	PCIE_WAKE2_B	42	PMU_SLP_S4_B	26	LPSS_SPI_2_FS1	10
11	123	107	91	LPC_AD1	75	GPIO_135	59	PCIE_WAKE3_B	43	SUSPWRDNACK	27	LPSS_SPI_2_FS2	11
12	124	108	92	LPC_AD2	76	GPIO_136	60	PCIE_CLKREQ0_B	44	EMMC_DNX_PWR_EN_B	28	LPSS_SPI_2_RXD	12
13	125	109	93	LPC_AD3	77	GPIO_137	61	PCIE_CLKREQ1_B	45	GPIO_105	29	LPSS_SPI_2_TXD	13
14	126	110	94	LPC_CLKRUNB	78	GPIO_138	62	PCIE_CLKREQ2_B	46	PMU_BATLOW_B	30	FST_SPI_CS0_B	14
15	127	111	95	LPC_FRAMEB	79	GPIO_139	63	PCIE_CLKREQ3_B	47	PMU_RESETBUTTON_B	31	FST_SPI_CS1_B	15

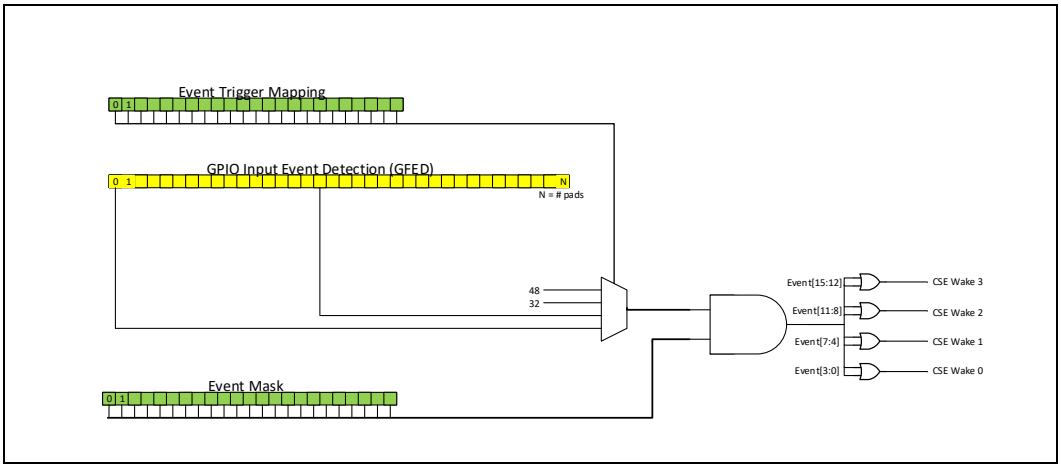
Note: Each of the 16 wake wires within the NW and N communities has a mask register and a mapping register. Refer the EVOUTEN_* and EVMAP_* registers in the register section for a description of the selection. An important note is that the EVMAP register allows any pin in a community to potentially be selected as a wake wire, but it is up to the programmer to make sure it makes to a pin that is direct IRQ capable, and enabled.

3.15.7.4 TXE Wake Events

The TXE requires up to eight level sensitive GPIO as event wires. Usually, these are selected and sent directly to the TXE for dispatch, but in the case of S0ix the TXE will not be active and will require PMC intervention in order to wake. In order to perform this, the same eight wires are sent to the PMC so that it can wake the system. Upon wake, the TXE will sense the wires and dispatch the event.

Two communities are capable of making four TXE wake wires each: North and Southwest. The same event multiplex hardware used for the direct IRQ was employed so that the TXE wires could be flexible, but the sixteen event wires must be reduced to four per community. The decision was to OR groups of four together at the slight loss of flexibility. Figure 3-44 shows how the sixteen event outputs are reduced to four outputs sent to both the TXE and PMC from each of the two capable communities.

Figure 3-44. TXE Event Multiplex



Selection for the TXE event multiplex out is shown in Northwest Community table for the North and in for the Southwest.

3.15.8 Triggering

GPIO pads have “sticky” bits on the input. As long as the signal goes active for at least two clocks (or four if partition clock gating is enabled), SoC will keep the sticky status bit active. The IOSF-SB Generic Interrupt message generation and IOSF-SB GPIO Virtual Wire message generation are subjected to the same triggering as above.

If the system is in an S0 state, the GPI are sampled at 25MHz, so the signal only needs to be active for about 80ns to be latched. In S0ix states, the GPI are sampled at 32.768 kHz, and thus must be active for at least 61 microseconds to be latched.

3.15.9 Host Interrupts

This section is only applicable for the following:

- Pads under host ownership (PAD_OWN), and
- in GPIO Mode (PADCFG.PMode)

During host ownership, TXE–do not own such pads and are not notified of any GPIO input event.

3.15.9.1 SCI/GPE

Registers:

- GPI_GPE_STS and GPI_GPE_EN bits.
  - — located in each Community under GPIO register map.
- Qualifier for SCI/GPE generation is located in each GPIO pad's PADCFG.GPIRoutSCI register.

Mechanism:

- Each Community shall deliver its sci_wake wire to PMC.

3.15.9.2 SMI

Registers:

- GPI_SMI_STS and GPI_SMI_EN are located in each Community
- Qualifier for SMI generation is located in each GPIO's PADCFG.GPIRoutSMI register.
- Mechanism:
- Each Community shall deliver SMI to PMC. PMC aggregates the SMI events from different GPIO Community.

3.15.9.3 GPIO-to-IOxAPIC

Registers:

- No status register in GPIO.
- Qualifier for IOxAPIC entry interrupt generation is located in each GPIO's PADCFG.GPIRoutIOxAPIC register.

3.15.9.4 GPIO Driver Mode

Registers:

- GPI_INT_STS and GPI_INT_EN are located in each Community

3.15.9.5 Clear Status Bits after Mode or Direction Switching

SW/IA FW is recommended to clear the SMI/NMI/GPE0/GPI STS bit when switching PMode register field from Native mode to GPIO Mode or switching GPIOTxDis field from output to input. Hardware may set the STS bits when the switching happens depending on the state of input signal coming from I/O.

3.15.10 Miscellaneous

3.15.10.1 Output Operation in GPIO Mode

In GPIO Mode, a GPIO may be configured to operate as push-push output or open-drain output. Push-pull output involves the following register setting:

- PMode='00'; GPIOTxDis='0'

- Software writes '0' or '1' to GPIOTxState in order to achieve corresponding pad state

Open-drain output involves the following register setting:

- PMode='00'; GPIOTxState='0'
- Software writes:
- '0' to GPIOTxDis in order to achieve '0' pin state
- '1' to GPIOTxDis in order to achieve high-Z pin state (or external pull-up)

Note: The pin direction should be input when the pin strap is sampled (at the rising edge of the sampling signal). Sometime after the pin strap sampling the pin direction is changed to the default direction, which can be output or input as specified in the pin list.

3.15.10.2 Dual-Voltage Default Configuration

All dual-voltage buffers are designed to use the 3.3V rail by default. Once RSMRST_N is deasserted, indicating that platform rails are stable, the buffer switches to use the rail indicated by the VCCIOSEL input, which is driven by the SIP controller. For hard-strap controlled dual-voltage GPIO families, the hard-strap value from the platform (0=3.3 V, 1=1.8 V) propagates straight through to the buffer VCCIOSEL input as soon as power is applied and is latched in the SIP when pmc_int_pok is asserted, which happens after RSMRST_N is deasserted. For soft-strap controlled dual-voltage GPIO families, there is a default value driven by the SIP controller that take effect after RSMRST_N is deasserted. Then when the soft straps are pulled, the SIP will drive the desired setting on the VCCIOSEL input to the HIP. So, for soft-strap controlled GPIOs, there is a period of time during boot where the GPIO will be in the default voltage mode.

To avoid EOS (electrical over-stress – reliability concern) of the SoC when there are 3.3 V devices on platform, the requirement is to default all dual-voltage GPIOs to 3.3 V mode after RSMRST_N switches 0->1. Conversely, to avoid EOS of any 1.8 V platform devices connected to a dual-voltage GPIO family that is controlled by soft-straps, the GPIOs should be configured to have internal 20 KΩ pull-down terminations with the Tx buffers disabled, by default. This is to prevent the GPIO from driving a 3.3 V signal to a 1.8 V device, and potentially damaging the device.

3.15.11 RTC (Real Time Clock)

The SoC contains a real-time clock with 242 bytes of battery-backed RAM. The real-time clock performs two key functions—keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a 3.3V battery.

The RTC supports two lockable memory ranges. By setting bits in the configuration space—two, 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

3.15.12 Features

- SoC has an integrated Real-Time Clock (RTC), a Motorola* MC146818B-compatible RTC with 242 bytes of battery-backed RAM.

- The RTC operates on a 32.768 KHz crystal and a 3.3V battery.
- The RTC performs two key functions—keeping track of the time of day and storing system data, even when the system is powered down.
- The RTC supports two lockable memory ranges. By setting bits in the configuration space two, 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC supports a date alarm that allows for scheduling a wake up event up to 30 days in advance. The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device with two banks of static RAM with 128 bytes each, although the first bank has 114 bytes for general purpose usage. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122ms to 500ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. Daylight savings compensation is optional. The hour is represented in twelve or twenty-four hour format and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola* MS146818B.The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions.

The time and calendar data should match the data mode (BCD or binary) and hour mode (12 or 24 hour) as selected in register B. The programmer MUST make sure that data stored in these registers within the reasonable values ranges and represents a possible date and time. The exception to these ranges is to store a value of C0 - FF in the Alarm bytes to indicate a “don’t care” situation. All Alarm conditions must match to trigger an Alarm Flag, which could trigger an Alarm Interrupt if enabled. The SET bit in register B should be 1 while programming these locations to avoid clashes with update cycles. Access to time and date information is done through the RAM locations. If a RAM read from the ten time and date bytes is attempted during an update cycle, the value read will not necessarily represent the true contents of those locations. Any RAM writes under the same conditions will be ignored.

Note: The hardware must be capable of receiving writes to the RTC registers at any time (including during the update cycles) even though the usage model recommends forcing the SET bit to ‘1’. Existing software is known to do this. The host-initiated write must take precedence over the hardware update in the event of a collision.

Note: The leap year determination for adding a 29th day to February does not take into account the end-of-the-century exceptions. The logic simply assumes that all years divisible by 4 are leap years. According to the Royal Observatory Greenwich, years that are divisible by 100 are typically not leap years. In every fourth century (years divisible by 400, like 2000), the 100-year-exception is over-ridden and a leap-year occurs. Note that the year 2100 will be the first time in which the current RTC implementation would incorrectly calculate the leap-year.

3.15.13 Update Cycles

An update cycle occurs once a second, if the SET bit of register B is not asserted and the divide chain is properly configured. During this procedure, the stored time and date will be incremented, overflow will be checked, a matching alarm condition will be checked, and the time and date will be rewritten to the RAM locations. The update cycle

will start at least 488ms after the UIP bit of register A is asserted, and the entire cycle will not take more than 1984ms to complete. The time and date RAM locations (0-9) will be disconnected from the external bus during this time.

To avoid update and data corruption conditions, external RAM access to these locations can safely occur upon the detection of either of two conditions. When an updated-ended interrupt is detected, almost 999ms is available to read and write the valid time and date data. If the UIP bit of Register A is detected to be low, there is at least 488ms before the update cycle begins.

Warning: The overflow conditions for leap years and daylight savings adjustments are based on more than one date or time item. To ensure proper operation when adjusting the time, the new time and data values should be set at least two seconds before one of these conditions (leap year, daylight savings time adjustments) occurs.

3.15.14 Interrupts

The real-time clock interrupt is internally routed within the SoC to both the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the ICH prior to connection to the interrupt controller, nor is it shared with any other interrupt. IRQ8# from the SERIRQ stream is ignored. However, the High Performance Event Timers (HPET) can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

3.15.15 Lockable RAM Ranges

The RTC's battery-backed RAM supports two 8-byte ranges that can be locked via the PCI config space. If the locking bit is set, the corresponding range in the RAM will not be readable or writeable. A write cycle to those locations has no effect. A read cycle to those locations will not return the location's actual value (undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to relock the RAM range.

3.15.16 Century Rollover

The hardware detects the case when the year rolls over from 99 to 00 (e.g., a rollover from December 31, 1999, 11:59:59 p.m. to 12:00:00 a.m. on January 1st, 2000). Upon detecting the rollover, the SoC sets the NEWCENTURY_STS bit. If the system is in an S0 state, this will cause an SMI#. The SMI# handler can update registers in the RTC RAM that are associated with the century value.

3.16 Integrated Sensor Hub

The Integrated Sensor Hub (ISH) serves as the connection point for many of the sensors on a platform. The ISH enables lower power sensor handling without waking the CPU. ISH is designed with the goal of "Always On, Always Sensing" and it provides the following functions to support this goal:

3.16.1 ISH Overview

The Integrated Sensor Hub (ISH) serves as the connection point for many of the sensors on the platform. It is designed with the goal of "Always On, Always Sensing" and it provides the following functions to support this goal.

ISH Supported Functions:

- — Acquisition and sampling of sensor data
- — Low-power sensor fusion
- — Local execution and support for location algorithms
- — Providing sensor data to separate processor for localization or stabilization
- — The ability to combine data from individual sensors to create a more complex virtual sensor that can be directly used by the firmware/OS
- — TXE for security sensitive data and code transfers
- — Power management of ISH and all attached sensors and communications devices
- — Low power operation through clock and power gating of the ISH blocks together with the ability to manage the power state of the external sensors
- — The ability to operate independently when the host platform is in a low power state (S0ix only)

The ISH is an offload engine that takes over the role of sensor control and data processing from the main processor. The goal is to provide persistent access to sensors while enabling the system to remain in a low power state until a change in the environment indicates that the system needs to be woken up. The ISH receives information from sensors and runs algorithms on this data to sense such changes in the environment. It also manages the power states of the individual sensors.

The ISH delivers higher-level packets of information to the Host CPU and to the TXE. Sensor data is delivered using the Human Input Device (HID) packet format which abstracts details of the individual sensors and relieves the host CPU and TXE from having to know any details on sensor implementation and operation. The ISH also handles sample rate mismatches between multiple subscribers.

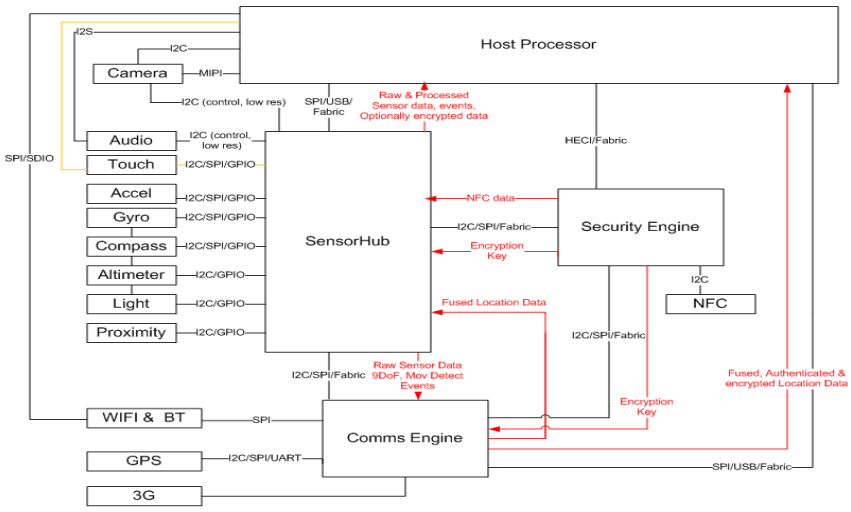
3.16.2 ISH Key Components

- A combined cache for instructions and data
  - — ROM space intended for the boot loader
  - — SRAM space for code and data
- Interfaces to sensor peripherals (I^2C and GPIO)
- An interface to main memory
- Out of Band signals for clock and wake-up control
- Part of the PCI tree on the host

3.16.3 Sensor Hub System

Diagram below shows the Integrated Services Hub (ISH) in the context of the full-chip SoC architecture

Figure 3-45. Conceptual Block Diagram of Sensor Hub Ecosystem



Note: In above figure, the various sensors and peripherals are notional for illustration purposes.

3.16.4 Feature Summary

Table 3-52. ISH Feature Summary

Feature	Characteristics
Micro Controller Speed	S0, S0iX: 100 MHz;
SRAM	640 kB with bank independent power gating
IPC	Inter Process Communications (IPC) to the Host, TXE, PMC, Audio, and Imagine Shared DDR based data transfer (Both at S0 and S0ix) Need to wake system S0 from S0ix for P2P
Memory hierarchy	ROM Memory: 32 kB (intended for the bootloader and core system code) L1 Cache (instruction or data): 32 kB RAM space: up to 640 kB Data/Code cache (with ECC) System DRAM used as paging device IMR accessible DDR
Timer	• Monotonic RTC counter • Watchdog timer • Wake Up timer • One Shot or Periodic timer (PTT) for HPET • APIC Timer (periodic or one-shot)
Other Interfaces	• Interfaces to Sensor peripherals (I^2C, SPI, UART, GPIO) • An interface to main memory • Out of Band signals for clock and wakeup control

3.16.5 Hardware Consideration

3.16.5.1 ISH Interfaces

The ISH is the primary connection point for all sensors on the platform. Through the external peripheral interface ISH connects to the sensor components, or other communication devices on the board. Some of the sensors also dedicated interrupt/ wake signals which are input via the GPIOs.

Table below shows typical sensors that might be connected to SoC via the ISH.

Table 3-53. Interface Descriptions

Interface	Feature	Suggested Configuration Sensors/Devices Connecting to the Port
I^2C_0	100 kHz and 400 kHz, Multi master support 1.7 Mb/s I^2C	Accelerometer, Gyro, magnetometer, proximity, ambient light, barometric pressure
I^2C_1	100 kHz and 400 kHz, Multi master support 1.7 Mb/s I^2C	NFC
I^2C_2	100 kHz and 400 kHz, Multi master support 1.7 Mb/s I^2C	Communications sideband
SPI_0	25 MHz	Biometric/Touchscreen
SPI_1	25 MHz	Communications
UART_0	High Speed	GNSS/GPS
UART_1	High Speed	Wi-Fi/BT*/BTLe sideband
UART_2	High Speed	—
GPIO [15-0]	16, Edge and Level triggered interrupts,	Possible uses: • Accelerometer; INT • Magnetometer; INT • Gyroscope; 2 INT • ALS and PS; 2 INT • Barometer, Altimeter; 1 INT • Ambient temperature, Humidity; 1 INT • Biometric; 1 INT

3.16.6 Power Management

3.16.6.1 Power Rails

ISH has one power rail, VDD2 SRAM rail (1.24 V) for the 640 kB paging SRAM.

3.16.6.2 Supported Power States

ISH is functional in S0, S0i1 and S0i2 states of the SoC. In S0i3 will be capable of responding to wakes from sensors via GPIOs, UART, Timers, PMC or from a host access.

ISH Usages can be split into following broad categories.

- Data Acquisition, Sampling and Fusion
- Sensor Interfacing and Power Management
- Position Localization

- Communications Hub

Following table identifies the device power states supported by ISH and the capabilities that remain active in that device power state.

Table 3-54. Supported Device Power States

ISH State	SoC State	Description
D0	S0/S0ix	All logic active Some banks of SRAM could be in internal retention or power gated state
D0i1	S0/S0ix	ISH clock gated SRAM could be in internal retention or partially power gated state
D0i2	S0/S0x	ISH SRAM in Retention
D0i3	S0/S0x/S0i3	ISH SRAM Power gated mIA L1 cache and ROM are power gated

D0i3 Power is the lowest power state for ISH. ISH is not running an application/code in this state, but is capable of detecting wake from sensors attached and also from any of the subscribers (Host, TXE, and LPE). ISH can be completely power gates in this with states saved to DRAM, shared SRAM or PMC to achieve the lowest power.

3.16.7 Programming Considerations

3.16.7.1 Address Mapping

ISH claims memory regions via BAR0 and BAR1. BAR0 claims 8 kB range mapped to internal IPC and other host visible registers; BAR1 claims 4 kB range and is mapped to config space enabled in ACPI mode. This means that the Host CPU only has access to the IPC registers exposed via BAR0.

The Memory Map from Host CPU Perspective is limited to select registers. These registers include:

- The PCI config registers.
- An MMIO space decoded by BAR0 (set via the PCI Config space). This space includes the IPC registers, doorbells, and various status registers.

An MMIO space decoded by BAR1 (set via the PCI Config sp---ace). This space includes an alias to the PCI config space. BAR1 is only used if the PCI config space is “hidden” (aka ACPI mode).

- Software must NOT attempt to access registers in the ILB range that are not specifically associated with the IOAPIC or the HPET. Accesses to disabled sub-blocks could cause the MinuteIA to lock up.

3.17 SMBus

3.17.1 Overview

SoC provides a System Management Bus (SMBus) 2.0 host controller. The SoC is capable of communicating with I^2C compatible devices.

The SMB Host Controller is used to send commands to other SMB slave devices. Software sets up the host controller with an address, command, and for writes, data and optionally PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it will generate an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMB interface: Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/ Word, Process call, Block Read, Block Write and Block write-block read process call.

The SMB Host Controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMB Host Controller will perform the requested transaction and interrupt the processor (or generate an SMI#) when its finished. Once a START command has been issued, the values of the "active registers" (Host Control, Host Command, Transmit Slave Address, Data0, Data1) should not be changed or read until the interrupt status bit (INTR) has been set (indicating the completion of the command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMB Host Controller will update all registers while completing the new command.

3.17.2 Command Protocol

In all of the following commands, the Host Status Register (offset 00h) is used to determine the progress of the command. While the command is in operation, the HOST_BUSY bit is set. If the command completes successfully, the INTR bit is set in the Host Status Register. If the device does not respond with an acknowledge, and the transaction times out, the DEV_ERR bit is set. If s/w sets the KILL bit in the Host Control Register while the command is running, the transaction will stop and the FAILED bit will be set after SoC forces a time-out. In addition, if KILL bit is set during the CRC cycle, both the CRCE and DEV_ERR bits will also be set. When KILL bit is set, SoC will abort current transaction by asserting SMBCLK low for greater than the time-out period, assert a STOP condition and then releases SMBCLK and SMBDATA. However, setting the KILL bit does not cause SoC to force a time-out if it is not performing a transaction.

3.17.2.1 Quick Commands

When programmed for a Quick Command, the Transmit Slave Address Register is sent.

Table 3-55 shows the order. The PEC byte is never appended to the Quick Protocol. Software should force the PEC_EN bit to '0' when performing the Quick Command for possible future enhancements. Also, Quick Command with I^2C_EN set produces undefined results. Software must force the I^2C_EN bit to 0 when running this command.

3.17.2.2 Send Byte/Receive Byte

Table 3-55. Quick Command Protocol

Bit	Description
1	Start Condition
2-8	Slave Address - 7 bits
9	Read / Write Direction
10	Acknowledge from slave
11	Stop

For the Send Byte command, the Transmit Slave Address and Device Command Registers are sent.

The Receive Byte is similar to a Send Byte, the only difference being the direction of data transfer. When programmed for the receive byte command, the Transmit Slave Address Register is sent. The data received is stored in the DATA0 register.

The order sent/received without PEC is shown in Table 3-56, “Send/Receive Byte Protocol without PEC” on page 156. Send Byte/Receive Byte command with I^2C_EN set produces undefined results. Software must force the I^2C_EN bit to 0 when running this command.

3.17.2.3 Write Byte/Word

Table 3-56. Send/Receive Byte Protocol without PEC

Send Byte Protocol		Receive Byte Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Read
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Data byte from slave
19	Acknowledge from slave	19	NOT Acknowledge
20	Stop	20	Stop

Table 3-57. Send/Receive Byte Protocol with PEC

Send Byte Protocol		Receive Byte Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Read
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Data byte from slave
19	Acknowledge from slave	19	Acknowledge
20-27	PEC	20-27	PEC from slave
28	Acknowledge from slave	28	Not Acknowledge
29	Stop	29	Stop

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a write byte/word command, the Transmit Slave Address, Device Command, and Data0 Registers are sent. In addition, the Data1 Register is sent on a write word command.

The order of bits without PEC is shown in Table 3-58. Write Byte/Word command with I^2C_EN set produces undefined results. Software must force the I^2C_EN bit to 0 when running this command.

3.17.2.4 Read Byte/Word

Table 3-58. Write Byte/Word Protocol without PEC

Write Byte Protocol		Write Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Command code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20-27	Data Byte - 8 bits	20-27	Data Byte Low - 8 bits
28	Acknowledge from Slave	28	Acknowledge from Slave
29	Stop	29-36	Data Byte High - 8 bits
		37	Acknowledge from slave
		38	Stop

Table 3-59. Write Byte/Word Protocol with PEC

Write Byte Protocol		Write Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Command code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20-27	Data Byte - 8 bits	20-27	Data Byte Low - 8 bits
28	Acknowledge from Slave	28	Acknowledge from Slave
29-36	PEC	29-36	Data Byte High - 8 bits
37	Acknowledge from Slave	37	Acknowledge from slave
38	Stop	38-45	PEC
		46	Acknowledge from slave
		47	Stop

Reading data is slightly more complicated than writing data. First SoC must write a command to the slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The slave then returns 1 or 2 bytes of data.

When programmed for the read byte/word command, the Transmit Slave Address and Device Command Registers are sent. Data is received into the DATA0 on the read byte, and the DAT0 and DATA1 registers on the read word.

3.17.2.5 Process Call

Table 3-60. Read Byte/Word Protocol without PEC

Read Byte Protocol		Read Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Command code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20	Repeated Start	20	Repeated Start
21-27	Slave Address - 7 bits	21-27	Slave Address - 7 bits
28	Read	28	Read
29	Acknowledge from slave	29	Acknowledge from slave
30-37	Data from slave - 8 bits	30-37	Data Byte Low from slave - 8 bits
38	NOT acknowledge	38	Acknowledge
39	Stop	39-46	Data Byte High from slave - 8 bits
		47	NOT acknowledge
		48	Stop

Table 3-61. Read Byte/Word Protocol with PEC (Sheet 1 of 2)

Read Byte Protocol		Read Word Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Command code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20	Repeated Start	20	Repeated Start
21-27	Slave Address - 7 bits	21-27	Slave Address - 7 bits
28	Read	28	Read
29	Acknowledge from slave	29	Acknowledge from slave
30-37	Data from slave - 8 bits	30-37	Data Byte Low from slave - 8 bits
38	Acknowledge	38	Acknowledge
39-46	PEC from slave	39-46	Data Byte High from slave - 8 bits
47	NOT acknowledge	47	Acknowledge
48	Stop	48-55	PEC from slave
		56	NOT acknowledge

Table 3-61. Read Byte/Word Protocol with PEC (Sheet 2 of 2)

Read Byte Protocol		Read Word Protocol	
		57	Stop

The process call is so named because a command sends data and waits for the slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition. When programmed for the process call command, the SoC transmits the Transmit Address, Device Command, and DATA0 and DATA1 registers. Data received from the device is stored in the DATA0 and DATA1 registers. The value written into bit 0 of the Transmit Slave Address Register (SMBus Offset 04h) needs to programmed to 0.

Note: If the I^2C_EN bit is set, then the Command field will not be sent.

The Process Call command with I^2C_EN set and either the PEC_EN or AAC bit set produces undefined results. Software must either force the I^2C_EN bit or both PEC_EN and AAC bits to 0 when running this command.

Table 3-62. Process Call Protocol Without PEC

Bit	Description
1	Start
2-8	Slave Address - 7 bits
9	Write
10	Acknowledge from Slave
11-18	Command code - 8 bits (Skip if I^2C_EN is set)
19	Acknowledge from slave (Skip if I^2C_EN is set)
20-27	Data byte Low - 8 bits
28	Acknowledge from Slave
29-36	Data Byte High - 8 bits
37	Acknowledge from slave
38	Repeated Start
39-45	Slave Address - 7 bits
46	Read
47	Acknowledge from slave
48-55	Data Byte Low from slave - 8 bits
56	Acknowledge
57-64	Data Byte High from slave - 8 bits
65	NOT acknowledge
66	Stop

3.17.2.6 Block Read/Write

Table 3-63. Process Call Protocol with PEC

Bit	Description
1	Start
2-8	Slave Address - 7 bits
9	Write
10	Acknowledge from Slave
11-18	Command code - 8 bits
19	Acknowledge from slave
20-27	Data byte Low - 8 bits
28	Acknowledge from Slave
29-36	Data Byte High - 8 bits
37	Acknowledge from slave
38	Repeated Start
39-45	Slave Address - 7 bits
46	Read
47	Acknowledge from slave
48-55	Data Byte Low from slave - 8 bits
56	Acknowledge
57-64	Data Byte High from slave - 8 bits
65	Acknowledge
66-73	PEC from slave
74	NOT acknowledge
75	Stop

SoC contains a 32-byte buffer for read and write data which can be enabled by setting bit '1' of the Auxiliary Control register at offset 0Dh in I/O space, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the Intel ICH3, an interrupt was generated after every byte. On SoC, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

This change to the Intel ICH3 requires the SoC is required to check the byte count field. Currently, the byte count field is transmitted but ignored by the hardware as software will end the transfer after all bytes it cares about have been sent or received

The Block Write command with I^2C_EN set and either the PEC_EN or AAC bit set produces undefined results. Software must either force the I^2C_EN bit or both PEC_EN and AAC bits to 0 when running this command.

3.17.2.7 SMBus Mode

The block write begins with a slave address and a write condition. After the command code SoC issues a byte count describing how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

When programmed for a block write command, the Transmit Slave Address, Device Command, and Data0 (count) registers are sent. Data is then sent from the Block Data Byte register; the total data sent being the value stored in the Data0 Register. On block read commands, the first byte received is stored in the Data0 register, and the remaining bytes are stored in the Block Data Byte register.

3.17.2.8 I^2C Mode

The format of the command changes slightly for block commands if the I^2C_EN bit is set. SoC will still send the number of bytes (on writes) or receive the number of bytes (on reads) indicated in the DATA0 register. However, it will not send the contents of the DATA0 register as part of the message.

BLOCK WRITE IF I^2C_EN BIT IS SET

The format of the command changes slightly for a Block Write if the I^2C_EN bit is set. SoC will still send the number of bytes indicated in the DATA0 register. However, it will not send the contents of the DATA0 register as part of the message.

The Block Write command with I^2C_EN set and the PEC_EN bit set produces undefined results. Software must force the PEC_EN bit to 0 when running this command.

Table 3-64. Block Read/Write Protocol without PE (Sheet 1 of 2)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Command code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20-27	Byte Count - 8 bits (skip this step if I2C_EN bit set)	20	Repeated Start
28	Acknowledge from Slave (skip this step if I2C_EN bit set)	21-27	Slave Address - 7 bits
29-36	Data Byte 1 - 8 bits	28	Read
37	Acknowledge from Slave	29	Acknowledge from slave
38-45	Data Byte 2 - 8 bits	30-37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge

Table 3-64. Block Read/Write Protocol without PE (Sheet 2 of 2)

Block Write Protocol		Block Read Protocol	
	Data Bytes / Slave Acknowledges...	39-46	Data Byte 1 from slave - 8 bits
	Data Byte N - 8 bits	47	Acknowledge
	Acknowledge from Slave	48-55	Data Byte 2 from slave - 8 bits
	Stop	56	Acknowledge
			Data Bytes from slave/ Acknowledge
			Data Byte N from slave - 8 bits
			NOT Acknowledge
			Stop

3.17.2.9 I²C Read

Table 3-65. Block Read/Write Protocol with PEC

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2-8	Slave Address - 7 bits	2-8	Slave Address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11-18	Command code - 8 bits	11-18	Command code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20-27	Byte Count - 8 bits	20	Repeated Start
28	Acknowledge from Slave	21-27	Slave Address - 7 bits
29-36	Data Byte 1 - 8 bits	28	Read
37	Acknowledge from Slave	29	Acknowledge from slave
38-45	Data Byte 2 - 8 bits	30-37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
...	Data Bytes / Slave Acknowledges...	39-46	Data Byte 1 from slave - 8 bits
...	Data Byte N - 8 bits	47	Acknowledge
...	Acknowledge from Slave	48-55	Data Byte 2 from slave - 8 bits
...	PEC – 8 bits	56	Acknowledge
...	Acknowledge from Slave	...	Data Bytes from slave/ Acknowledge
...	Stop	...	Data Byte N from slave - 8 bits
		...	Acknowledge
		...	PEC from slave – 8 bits
		...	NOT Acknowledge
		...	Stop

The I²C Read command with either PEC_EN or AAC bit set produces undefined results. Software must force both PEC_EN and AAC bits to 0 when running this command.

This command allows SoC to perform block reads to certain I²C devices, such as serial E2PROMs. The SMBus Block Read supports the 7-bit addressing mode only. However this does not allow access to devices that need to use the I²C "Combined Format" that has data bytes after the address. Typically these data bytes correspond to an offset (address) within the serial memory chips.

To support these devices, SoC implements an I²C Read command with the following format:

SoC will continue reading data from the peripheral until the NACK is received.

Table 3-66. I^2C Multi-Byte Read

Bit	Description
1	Start
2-8	Slave Address - 7 bits
9	Write
10	Acknowledge from slave
11-18	Send DATA1 register
19	Acknowledge from slave
20	Repeated Start
21-27	Slave Address - 7 bits
28	Read
29	Acknowledge from slave
30-37	Data Byte 1 from slave - 8 bits
38	Acknowledge
39-46	Data Byte 2 from slave - 8 bits
47	Acknowledge
	Data Bytes from slave/ Acknowledge
	Data Byte N from slave - 8 bits
	NOT Acknowledge
	Stop

Note: This new command is supported independent of the setting of the I^2C_EN bit.

Note: The value written into bit 0 of the Transmit Slave Address Register (SMBus Offset 04h) must be 0.

3.17.2.10 Block Write—Block Read Process Call

The block write-block read process call is a two-part message. The call begins with a slave address and a write condition. After the command code the host issues a write byte count (M) that describes how many more bytes will be written in the first part of the message. If a master has 6 bytes to send, the byte count field will have the value 6 (0000 0110b), followed by the 6 bytes of data. The write byte count (M) cannot be zero.

The second part of the message is a block of read data beginning with a repeated start condition followed by the slave address and a Read bit. The next byte is the read byte count (N), which may differ from the write byte count (M). The read byte count (N) cannot be zero.

The combined data payload must not exceed 32 bytes. The byte length restrictions of this process call are summarized as follows:

- M ≥ 1 byte
- N ≥ 1 byte
- M + N ≤ 32 bytes

The read byte count does not include the PEC byte. The PEC is computed on the total message beginning with the first slave address and using the normal PEC computational rules. It is highly recommended that a PEC byte be used with the Block Write-Block Read Process Call. Software must do a read to the command register (offset 2h) to reset the 32byte buffer pointer prior to reading the block data register.

Note: There is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

Note: E32B in the Auxiliary Control Register must be set when using this protocol.

3.17.3 I²C Behavior

Table 3-67. Block Write-Block Read Process Call Protocol With/Without PEC (Sheet 1 of 2)

Bit	Description
1	Start
2-8	Slave Address - 7 bits
9	Write
10	Acknowledge from Slave
11-18	Command code - 8 bits
19	Acknowledge from slave
20-27	Data Byte Count (M) - 8 bits
28	Acknowledge from Slave
29-36	Data Byte (1) - 8 bits
37	Acknowledge from slave
38-45	Data Byte (2) - 8 bits
46	Acknowledge from slave
	Data Byte (M) - 8 bits
	Acknowledge from slave
	Repeated Start
	Slave Address - 7 bits
	Read
	Acknowledge from slave
	Data Byte Count (N) from slave – 8 bits
	Acknowledge from master
	Data Byte (1) from slave – 8 bits
	Acknowledge from master
	Data Byte (2) from slave – 8 bits
	Acknowledge from master
	Data Byte Count (N) from slave – 8 bits
	Acknowledge from master (Skip if no PEC)
	PEC from slave (Skip if no PEC)
	NOT acknowledge

Table 3-67. Block Write-Block Read Process Call Protocol With/Without PEC (Sheet 2 of 2)

Bit	Description
	Stop

When the I^2C_EN bit is set SoC SMBus logic will instead be set to communicate with I^2C devices. This forces the following changes:

- The Process Call command will skip the Command code (and its associated acknowledge).
- The Block Write command will skip sending the Byte Count (DATA0).

In addition, SoC supports the I^2C Read command. This is independent of the I^2C_EN bit. When operating in I^2C mode, (I^2C_EN bit set), SoC will never use the 32-byte buffer for any block commands.

3.17.3.1 Heartbeat For Use with D110 or External D101M

SoC does not support sending periodic heartbeat messages through its host CPU visible SMBus.

3.17.4 Slave Interface Behavioral Description

SMBUS does not support SMBUS master on the platform, thus slave write slave read and Host Notify command are not supported.

3.17.5 SMB Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving the SMBDATA line low to signal a start condition. SoC must continuously monitor the SMBDATA line. When SoC is attempting to drive the bus to a '1' by letting go of the SMBDATA line, and it samples SMBDATA low, then some other master is driving the bus and SoC must stop transferring data.

If SoC loses arbitration, the condition is called a collision. SoC sets the BUS_ERR bit in the Host Status Register, and if enabled, generates an interrupt or SMI#. The CPU SoC is responsible for restarting the transaction.

3.17.5.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that SoC as an SMBus master would like. They have the capability of stretching the low time of the clock. When SoC attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time.

SoC must monitor the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

3.17.5.2 Bus Timeout (SoC as SMB Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. SoC will discard the cycle, and set the DEV_ERR bit. The time out minimum is 25 ms. The time-out counter inside SoC will start when the first bit of data is transferred by SoC . The 25 ms will be a count of 800 RTC clocks.

The 25 ms time-out counter should not count under the following conditions:

3.17.5.3 Interrupts/SMI#

SoC SMBus controller uses PIRQB# as its interrupt pin (PIRQB is the value traditionally configured for SMBUS). However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMBUS_SMI_EN bit.

The following tables specify how the various enable bits in the SMBus function control the generation of the interrupt, Host and Slave SMI, and Wake internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario then the Results for all of the activated rows will occur.

Table 3-68. Block Write-Block read Process Call Protocol With/Without PEC

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Config Register, D31:F1:Off140h, Bit 1)	SMBALERT_DIS (Slave Command I/O Register, Offset 51h, Bit 2)	Result
SMBALERT# asserted low (always reported in SMBALERT_STS-Host Status Register, bit 5)	X	X	X	Wake generated
	X	1	0	Slave SMI# generated (SMBUS_SMI_ STS)
	1	0	0	Interrupt generated

Table 3-69. Summary of Enables for SMBus Slave Write and SMBus Host Events

Event	INTREN (Host Control I/ O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Config Register, D31:F4:Off140h, Bit 1)	Result
Slave Write to Wake/ SMI# command	X	X	Wake generated when asleep Slave SMI# generated when awake (SMBUS_SMI_STS)
Any combination of Host Status Register [4:1] asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

Table 3-70. Summary of Enables for the Host Notify Command

HOST_NOTIFY_INTREN (Slave Control I/O Register, Offset 51h, bit 0)	SMB_SMI_EN (Host Config Register, D31:F4:Off140h, Bit 1)	HOST_NOTIFY_WKEN (Slave Control I/O Register, Offset 51h, bit 1)	Result
0	X	0	None
X	X	1	Wake generated
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

3.17.6 CRC Generation and Checking

If the AAC (Automatically Append CRC) bit is set in the Auxiliary Control register, SoC will automatically calculate and drive CRC at the end of the transmitted packet for write cycles, and will check the CRC for read cycles. It will not transmit the contents of the PEC register for CRC. The PEC bit must not be set in the Host Control register if this bit is set, or unspecified behavior will result.

If the read cycle results in a CRC error, the DEV_ERR bit and the CRCE bit in the Auxiliary Status register at offset 0Ch will be set.

3.18 Security Architecture

The Security involves the following sections.

- Trusted Execution Engine 3.0 (TXE3.0)
- Basic SoC security Architecture
  - — Layered SoC Security
  - — Security principles like CIA triad (confidentiality, integrity, and availability)
  - — SoC Trusted Computing Base (TCB)
  - — Adversary Model and Adversary Capabilities
- Access Control Architecture
- SoC IP security
- SoC Assets
- Debug Security
- HDCP2.2
- SGX2.0

3.18.1 SoC Flows

TXE interacts either directly or indirectly with certain IPs. The major direct interactions are captured in the following table:

Table 3-71. TXE Interactions

Flow	SoC Logic Unit
Secure Boot & DnX (Download and Execute)	xDCI (USB2 only), PSF, and eMMC
Firmware Authentication	cAVS, ISH, Imaging, PMC
Content Protection (PAVP, HDCP 2.2, WiDi, Play Ready3 DRM)	Graphics and Display Controller
Fingerprint Reader	LPSS
Provisioning flows	eMMC*, SPI
Secure timer	Protected RTC
NFC Support (reader and secure element)	LPSS

3.18.2 TXE as a Device in Host Space

TXE is exposed to the host as a multi-function PCI device. It supports a project specific number of internal HECI functions, each with a complete PCI header. External PSF recognizes TXE as a device in the host space and routes upstream traffic from TXE to host.

TXE power gating flow is a SW assisted flow where driver allows TXE to power gate most of its logic, but TXE still maintains host visible config space. TXE generates an MSI when it needs to communicate with its driver and its MSI is enabled. TXE supports sending SB PME assert message to PMC when its PME is enabled and FW writes to the PME status bit. TXE may generate SCI and SMI messages if it is configured appropriately.

The following host functionality is supported by TXE:

Agent	Function	Device: Function	Remark
TXE	UMA access	D0:F0	Ghost BDF. UMA access only.
	FTPM	D15:F7	Ghost / ACPI BDF. Used to access only the FTPM buffer in DRAM. Uses HECI1 bus number.
	HECI1	D15:F0	Config and MMIO space.
	HECI2	D15:F1	Config and MMIO space.
	HECI3	D15:F2	Config and MMIO space.

Notes:
1. Ghost / ACPI BDF is used for in order for so that access can be independent of host D3/BME configuration. The ghost / ACPI BDF does not have a config space and may not be disabled by host. In case of D3 or BME=0 fabric does not return completions to TXE and this is required by TXE operation.
2. TXE FW may read from HECI 1 the bus number assigned to that function by host config write in order to write this value to CM devices which do not have host configuration but need access to DRAM.
3. TXE HECI functions support the 16 bit Device ID (DID) as part of the config header. The 16bit DID is composed of 9 MSbits which are set up by the PMC setidvalue SB message, and 7 LBsbits which are fixed per HECI function in a parameter.

3.18.3 Ecosystem Dependencies and External Interfaces

The TXE3.0 IP is not a standalone IP; it has tight interaction with the SoC ecosystem. This chapter reviews the HW impact of these logical interfaces.

3.18.4 PMC

The TXE IP interfaces with the power management controller (PMC) for the following operations:

- PMC updates TXE on SoC level transitions (such as Sx entry/exit, warm/cold reset preparations, TXE/host partition reset). Chassis messages from PMC as part of power-up/reset flows are not supported in TXE.
- TXE requests info on power state transitions.
- TXE requests TXE or global reset.
- Other communication (FW defined).

3.18.5 SPI Controller

TXE accesses flash memory for the following usages:

- Loading and authenticating TXE FW code
- Loading and authenticating PMC patch code and other cores code such as ISH, IE, audio, Imaging
- Secure storage of run-time variables (RPM partition)
- Loading and authenticating IBBl/IBB as part of secure boot
- Loading soft straps (SMIP)

SPI flash is divided to several partitions (TXE, host…). TXE accesses its partition, but may also need to access host partition (for example for DnX).

Table 3-72. Summary of SPI

Item	SPI
Dual access support	• SPI controller supports dual access by Host and TXE. • SPI has a Host partition and TXE partition which can both be accessed during run-time.
Soft straps	• SPI controller reads soft straps directly from SPI flash before TXE comes out of reset. • The SPI controller tries to read soft straps from SPI flash even in production configurations where no SPI flash is present. • GSK_FPULL_SB_RST_PULL_STATUS.HW_CFG_STRAP_PULL_SIZE indicates the number of strap bytes that were pulled by the SPI controller. If the value of this field is 0, then there is no SPI flash present in this configuration and the soft straps should be read from EMMC flash.
DMA access	• The SPI controller does not have a DMA. TXE reads from and writes to SPI by configuring its own DMA in the OCS block.

3.18.6 Field Programmable Fuses (FPF)

TXE FW interacts with the FPF logic to perform the following:

- Burn the fuses in the field/OEM.
- Read the fuses.

3.18.7 Gen Graphics

The TXE IP interfaces with GEN graphics for secure sprite, PAVP using DMI2 RAVDM.

The PAVP interaction is in two phases of the flow: during key provisioning to GEN and during an application execution session.

3.18.8 Display

TXE interfaces with the secure sprite HW in the Display block for Trusted UI.

3.18.9 GPIOs

The TXE IP requires access to GPIO pins (both configuration of GPIOs and interrupt from GPIOs).

3.18.10 cAVS (Audio)

The TXE communicates the cAVS to enable control of a flow where TXE authenticates cAVS code in IMR. TXE FW then indicates to cAVS that it may access the authenticated code in IMR.

3.18.11 LPSS

The LPSS IP contains I^2C and SPI interfaces that can be assigned to and controlled by TXE.

3.18.12 Software Guard Extensions (SGX)

Software Guard Extensions (SGX) is a processor enhancement designed to help protect application integrity and confidentiality of secrets and withstands software and certain hardware attacks. Software Guard Extensions (SGX) creates and operates in protected regions of memory named Enclaves.

Enclave code can be accessed using new special ISA commands that jump into per Enclave predefined addresses. Data within an Enclave can only be accessed from that same Enclave code. The latter security statements hold under all privilege levels including supervisor mode (ring-0), System Management Mode (SMM) and other Enclaves. Software Guard Extensions (SGX) features a memory encryption engine that both encrypt Enclave memory as well as protect it from corruption and replay attacks.

Software Guard Extensions (SGX) benefits over alternative Trusted Execution Environments (TEEs) are:

- Enclaves are written using C/C++ using industry standard build tools.
- High processing power as they run on the processor.
- Large amount of memory are available as well as non-volatile storage (such as disk drives).
- Simple to maintain and debug using standard IDEs (Integrated Development Environment)
- Scalable to a larger number of applications and vendors running concurrently

3.19 CNVi

The SoC supports integrated connectivity (CNVi), which includes Wi-Fi and Bluetooth* (BT)*.

Note: Only the controller is integrated into the SoC; a discrete RF chip is still required on the platform.

CNVi supports:

- Wi-Fi: 1x1 and 2x2 abgn/acR2/MU-MIMO/80 MHz/160 MHz
- BT* 4.2/BT* 5.0

RF Modules:

- JeffersonPeak 2: Wi-Fi 2x2acR2 80MHz/BT* 5.0

Table 3-73. CNVi Landing Zone Across Intel Products

Feature	SoC
Bluetooth* IA UART Host	X
Wi-Fi Wake from Sx/S0ix	X
Co-Existence support (MFUART and GPIOs)	X
Discrete CNV support	X
OBFF Support	X
DTF Support	X
Shared XTAL between SoC and CNV	X

3.20 Thermal Management

There are four main categories of Thermal Management:

- SoC thermal area
- Memory thermal area
- Thermal Interrupt
- Running Average Power Limit algorithm

The SoC thermal area includes SoC thermal sensing, thermal control algorithms, reporting SoC temperature and supporting thermal interrupts.

The Memory thermal area includes memory thermal sensors, control algorithms, reporting memory thermal status, and generating thermal interrupts. The Running Average Power Limit (RAPL) algorithm is a package-level feature for Tskin control which provides energy status reporting, power-limit configuration, and control algorithms.

SoC Thermal Management Features:

- PROCHOT Support
- DPTF—Thermal Interrupt Support
- Thermal Control Algorithm
- Cross Throttling

3.21 Clocking

SoC contains variable frequency, multiple clock domains and multiple power plane clocking schemes with determinism and synchronization requirements in some areas. The architecture also supports various PLL clocking requirements with bypass options to save power.

Table 3-74. Summary of Clock Signals (Sheet 1 of 2)

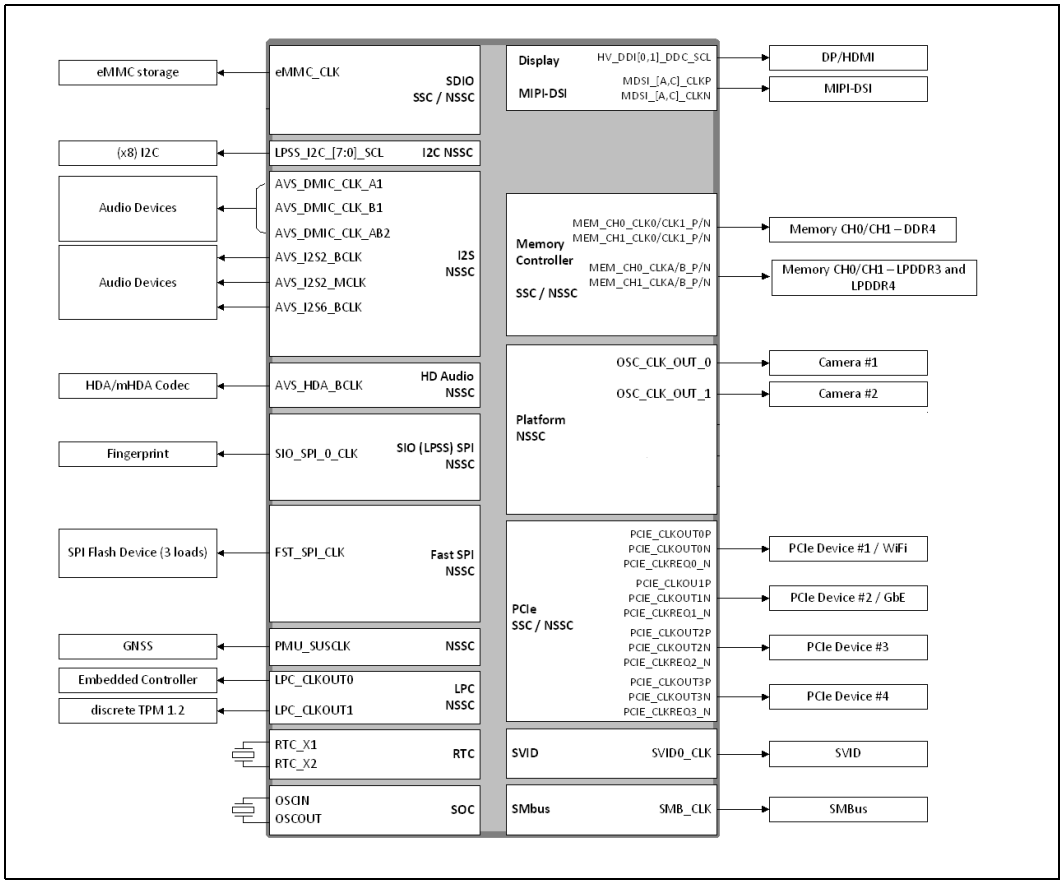
Interface	Clock Signal	Clock Frequency
Memory - DDR4	MEM_CH[0:1]_CLKP/N[0:1]	Upto 1200 MHz
Memory - LPDDR4	MEM_CH[0:1]_CLKP/N[0:1]A/B	Up to 1200 MHz
PCIe*	PCIe_CLKOUT[0:3]P/N	100 MHz

Table 3-74. Summary of Clock Signals (Sheet 2 of 2)

Interface	Clock Signal	Clock Frequency
Storage - eMMC* 4.51 and 5.1	eMMC_CLK	2, 52, 200 MHz
Display - HDMI* DDC	HV_DDI[0,1]_DDC_SCL	100 KHz
Display - MIPI*-DSI	MDSI_[A,C]_CLKP/N	19.2 MHz reference (CLK Frequency 300-1066 MHz)
Audio - HD Audio	AVS_HDA_BCLK (**multiplexed**)	6, 12, 25 MHz
Audio Codec/Analog Microphone- I2S	AVS_I2S1_MCLK AVS_I2S1/2_BCLK (**multiplexed**)	BCLK = 12.288 MHz MCLK = 19.2 MHz
Audio - Digital Microphone	AVS_DMIC_CLK_[A/B]1 AVS_DMIC_CLK_AB2	12 MHz
SIO (LPSS) I^2C	LPSS_I^2C[0:7]_SCL	100 KHz, 400 KHz, 1 MHz, 3.4 MHz
PMIC	PMIC_I^2C_SCL	100 KHz, 400 KHz, 1 MHz, 3.4 MHz
SVID	SVID0_CLK	19.2 MHz
LPC	LPC_CLKOUT[0,1]	25 MHz
SMBus	SMB_CLK	Maximum 100 KHz
SIO (LPSS) SPI	SIO_SPI_0_CLK	25 MHz
FAST SPI - SPI NOR and TPM	FST_SPI_CLK	20, 33, 40, 50 MHz
SPI	SPI_CLK (**multiplexed**)	50 MHz
Platform - OSC_CLK_OUT	OSC_CLK_OUT_[0:1]	6.75, 8, 9.6, 13.6, 14.4, 19.2,24,27.27 MHz
Platform - SUSCLK	PMU_SUSCLK	32.768 KHz
XTAL Source - RTC Clock	RTC_X[1,2]	32.768 KHz
XTAL Source - SoC Clock - as default	OSCOUT OSCIN	19.2 MHz 38.4 MHz[1]

Note:
1. When CNVi is enabled, and the SoC is paired with JfP, XTAL is 38.4MHz and it comes from the JfP module.

Figure 3-46. SoC Clock Mapping



Notes:

1. 19.2 MHz Crystal Clock Oscillator as default.
2. When CNVi is enabled, and the SoC is paired with JfP, XTAL is 38.4 MHz and it comes from the JfP module.
3. Some clocks signals that are not supported but they can be used as GPIO. Refer to GPIO multiplexing table for more information on how to configure these clocks.
4. To save power in deep S0ix, the 19.2 MHz oscillator is shut off and the critical timers and wake-up logic are clocked by means of RTC 32 KHz clock.

§ §

4 Electrical Specifications

4.1 Absolute Maximum and Minimum Specifications

The absolute maximum and minimum specifications are used to specify conditions allowable outside of the functional limits of the SoC, but with possible reduced life expectancy once returned to function limits.

At conditions exceeding absolute specifications, neither functionality nor long term reliability can be expected. Parts may not function at all once returned to functional limits.

Although the processor contains protective circuitry to resist damage from Electrostatic discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

4.2 Thermal Specifications

The following table specifies the thermal limits of SoC operation. Thermal solutions not designed to provide the following level of thermal capability may affect the long-term reliability of the processor and system and more likely result in performance throttling to ensure silicon junction temperatures within Specification.

TjMax defines the maximum operating silicon junction temperature. This is the temperature needed to ensure TDP specifications when running at guaranteed Processor and Graphics frequencies.

Table 4-1. Operating Temperature Range

Parameter	Minimum	Maximum
Operating temperature range of the SoC	0 °C	105 °C

“TDP” defines the thermal dissipated power for a worse case estimated real world thermal scenario. “SDP”, or scenario dissipated power, defines the thermal dissipated power under a lighter workload specific to a user scenario and at a lower thermal junction temperature than TjMax.

4.3 Storage Conditions

This section specifies absolute maximum and minimum storage temperature and humidity limits for given time durations. Failure to adhere to the specified limits could result in physical damage to the component. If this is suspected, Intel recommends a visual inspection to determine possible physical damage to the silicon or surface components.

Table 4-2. Storage Conditions Prior to Board Attach

Symbol	Parameter	Minimum	Maximum
$T_{Absolute\ Storage}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time in Intel Original sealed moisture barrier bag and / or box.	–25 °C	125 °C
$T_{Sustained\ Storage}$	The ambient storage temperature limit (in shipping media) for the sustained period of time as specified below in Intel Original sealed moisture barrier bag and / or box.	-5 °C	40 °C
$RH_{Sustained\ Storage}$	The maximum device storage relative humidity for the sustained period of time as specified below in Intel Original sealed moisture barrier bag and / or box.	60% RH @ 24°C	
$TIME_{Sustained\ Storage}$	Maximum time: associated with customer shelf life in Intel Original sealed moisture barrier bag and / or box.	NA	Moisture Sensitive Devices: 60 months from bag seal date; Non-moisture sensitive devices: 60 months from lot date

Notes:
1. $T_{Absolute\ Storage}$ applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC J-STD-020 documents. The JEDEC, J-STD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
3. Post board attach storage temperature limits are not specified for non-Intel branded boards. Consult board manufacturer for storage specifications.

4.4 Voltage, Current, and Crystal Specifications

Note: The specifications listed below are preliminary and subject to change.

4.4.1 Voltage and Current Specifications

Table 4-3. SoC Power Rail DC Specification and Iccmax (Sheet 1 of 2)

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VCC_VCGI	0 V, 0.45–1.45	**With AVP[1]:** DC Load Line (DCLL) = 6 mΩ Ripple at Iccmax = +/-15 mV TOB[2]_Iccmax = +/-20 mV Overshoot voltage (max) = 100 mV Overshoot duration (max) = 50 µs	Variable voltage supply to CPU and Graphics Core and ISP logic. SVID and I2C VID are voltage control interface supported.	25
VNN_SVID	0 V, 0.45–1.45	+/-5% at VID>1.0 V; +/-50mV at VID<=1.0 V	Variable voltage supply to other (non core) logic	4
VCCRAM_1P05[4]	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	4.5
VCCIOA				
VCC_1P05_INT				

Table 4-3. SoC Power Rail DC Specification and Iccmax (Sheet 2 of 2)

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VDD2_1P2_CPU	1.2	+/-5%	Fixed voltage rail for SoC L2	2
VDD2_1P2_AUD_ISH			Fixed voltage rail for Audio and ISH I/O Logic	
VDD2_1P2_MPHY			Fixed voltage rail for MPHY Logic	
VDD2_1P2_USB2			Fixed voltage rail for USB2 I/O	
VDD2_1P2_DSI_CSI			Fixed voltage rail for MIPI* I/Os	
VDD2_1P2_PLL			Fixed voltage rail for PLLs	
VCC_1P8V_A	1.8	+/-5%	Fixed voltage rail for all GPIOs	0.4
VCC_3P3V_A	3.3	+/-5%	Fixed voltage rail for GPIO, I/O logic, and USB2 PHY	0.15
VDDQ	1.2 (DDR4)	+/-5%	Fixed voltage rail for DDR4 PHY	3
	1.1 (LPDDR4)		Fixed voltage rail for LPDDR4 PHY	
VCCRTC_3P3V	2-3.47		Fixed Voltage rail for RTC (Real Time Clock)	-

Notes:
1. AVP: Active Voltage Positioning (this is the same as DC Load Line).
2. Refer to IMVP8 PWM specifications on Tolerance Budget (TOB) window definition.
3. This requirement is based on JEDEC specifications. Ensure that the voltage regulator is able to meet this requirement for proper system functionality.
4. ISH is not supported on fixed VNN merging to VCC_1P05 rail config.

4.4.2 Power Limiting (PL) values

Table 4-4. PL Values

Symbol	Mobile 6W	Desktop 10W
PL1(W)	6	10
PL1 Tau (S)	28	8
PL2(W)	15	25
PL3 Enable	0	0
PL3(W)	30	30
PL3 Duty Cycle(%)	10	10
PL3 Time Window (ms)	40	40
PL4 Limit (W)	30	30

4.4.3 Crystal Specifications

Table 4-5. Integrated Clock Crystal Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
TPPM	Crystal frequency tolerance and stability	-30	30	ppm	1
PDRIVE	Crystal drive load	100		µW	1, Typical
RESR	ESR	20	80	Ω	1

Table 4-5. Integrated Clock Crystal Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
CLOAD	Crystal load capacitance		12	pF	1
CSHUNT	Crystal shunt capacitance		3	pF	1
Note: These are the specifications needed to select a crystal for the Integrated clock oscillator circuit. Crystal must be at cut, at fundamental frequency, parallel resonance mode.					

Table 4-6. Integrated Clock Oscillation Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
FPLT	Frequency	19.2	38.4	MHz	
TDC	Duty Cycle	40	60	%	1
TPERJIT	Period Jitter		150	ps	
Note: Measured @50% of 1.8V.					

Table 4-7. ILB RTC Crystal Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
FRTC	Frequency		32.768	KHz	Nominal
TPPM	Crystal frequency tolerance	-20	20	ppm	At 25C
PDRIVE	Crystal drive load	0.1	0.5	µW	Nominal
CLOAD	Crystal Load Capacitance		12.5	pF	12 pF Nominal
CSHUNT	Crystal shunt Capacitance		1.3	pF	
C1/C2	Load Capacitance tolerance	-10	10	%	
ESR	Series Resistance		50k	Ω	

4.5 DC Specifications

Platform reference voltages are specified at DC only. VCC measurements should be made with respect to the supply voltages specified in Table 4-3, "SoC Power Rail DC Specification and Iccmax".

Note: $V_{IH/OH}$ Maximum and $V_{IL/OL}$ Minimum values are bounded by VCC and VSS.

4.5.1 Display

4.5.1.1 Display Port Specification

Table 4-8. Display Port* DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VTX-DIFFp-p-Level0	Differential Peak-to-peak Output Voltage Level 0	0.35	0.46	V	
VTX-DIFFp-p-Level1	Differential Peak-to-peak Output Voltage Level 1	0.51	0.68	V	
VTX-DIFFp-p-Level2	Differential Peak-to-peak Output Voltage Level 2	0.69	0.92	V	

Table 4-8. Display Port* DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VTX-DIFFp-p-Level3	Differential Peak-to-peak Output Voltage Level 3	0.85	1.38	V	
VTX-PREEMP-RATIO	No Pre-emphasis	0	0	dB	
VTX-PREEMP-RATIO	3.5 dB Pre-emphasis	2.8	4.2	dB	
VTX-PREEMP-RATIO	6.0 dB Pre-emphasis	4.8	7.2	dB	
VTX-PREEMP-RATIO	9.5 dB Pre-emphasis	7.5	11.4	dB	
VTX-DC-CM	Tx DC Common Mode Voltage	0	2	V	
RLTX-DIFF	Differential Return Loss at 0.675GHz at Tx Package pins	12		dB	1
RLTX-DIFF	Differential Return Loss at 1.35 GHz at Tx Package pins	9	1.6	dB	1
CTX	TX Output Capacitance	0	1.5	pF	2, for HBR 2

Notes:
1. Straight loss line between 0.675 GHz and 1.35 GHz.
2. Represents only the effective lump capacitance seen at the SoC interface that shunts the TX termination.

4.5.1.2 HDMI* Specification

Table 4-9. HDMI* DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
Voff	Single Ended Standby (off), output voltage	-10	10	mV	1
Vswing	Single Ended output swing voltage	400	600	mV	
VOH (<=165 MHz)	Single Ended high level, output voltage	-10	10	mV	1
VOH (>165 MHz)	Single Ended high level, output voltage	-200	10	mV	1
VOL (<=165 MHz)	Single Ended low level, output voltage	-600	-400	mV	1
VOL (>165 MHz)	Single Ended low level, output voltage	-700	-400	mV	1

Note: The Minimum/Maximum values are with reference to VCC_VGI.

4.5.1.3 embedded Display Port* Specification

Table 4-10. embedded Display Port* DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VTX-DIFFp-p-Level0	Differential Peak-to-peak Output Voltage Level 0	0.18	0.22	V	1,2

Table 4-10. embedded Display Port* DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VTX-DIFFp-p-Level1	Differential Peak-to-peak Output Voltage Level 1	0.2	0.275	V	1,2
VTX-DIFFp-p-Level2	Differential Peak-to-peak Output Voltage Level 2	0.27	0.33	V	1,2
VTX-DIFFp-p-Level3	Differential Peak-to-peak Output Voltage Level 3	0.315	0.385	V	1,2
VTX-DIFFp-p-Level4	Differential Peak-to-peak Output Voltage Level 4	0.36	0.44	V	1,2
VTX-DIFFp-p-Level5	Differential Peak-to-peak Output Voltage Level 5	0.405	0.495	V	1,2
VTX-DIFFp-p-MAX	Maximum Allowed Differential Peak-to-peak Output Voltage		1.38	V	3
VTX-DC-CM	Tx DC Common Mode Voltage	0	2	V	1
VTX-PREEMP-RATIO	No Pre-emphasis	0	0	dB	1
VTX-PREEMP-RATIO	3.5 dB Pre-emphasis	2.8	4.2	dB	1
VTX-PREEMP-RATIO	6.0 dB Pre-emphasis	4.8	7.2	dB	1
VTX-PREEMP-RATIO	9.5 dB Pre-emphasis	7.5	11.4	dB	1
RLTX-DIFF	Differential Return Loss at 0.675GHz at Tx Package pins	12		dB	4
RLTX-DIFF	Differential Return Loss at 1.35 GHz at Tx Package pins	9		dB	4
CTX	TX Output Capacitance		1.5	pF	5

Notes:
1. Steps between VTX-DIFFP-P voltages must be monotonic. The actual VTX-DIFFP-P-1 voltage must be equal to or greater than the actual VTX-DIFFP-P-0 voltage; the actual VTX-DIFFP-P-2 voltage must be greater than the actual VTX-DIFFP-P-1 voltage; and so forth.
2. The recommended minimum VTX-DIFFP-P delta between adjacent voltages is in mV.
3. Allows eDP* Source devices to support differential signal voltages compatible with eDP* v1.3 (and lower) devices and designs.
4. Straight loss line between 0.675 GHz and 1.35 GHz.
5. Represents only the effective lump capacitance seen at the SoC interface that shunts the TX termination.

4.5.1.4 Display Port* Aux Channel Specification

Table 4-11. DDI AUX Channel DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VAUX-DIFFp-p	AUX Peak-to-peak Voltage at a transmitting Device	0.29	1.38	V	1
VAUX-TERM_R	AUX CH termination DC resistance		100	W	
VAUX-DC-CM	AUX DC Common Mode Voltage	0	2	V	2
VAUX-TURN-CM	AUX turn around common mode voltage		0.3	V	3
IAUX_SHORT	AUX Short Circuit Current Limit		90	mA	4
CAUX	AC Coupling Capacitor	75	200	nF	5

Table 4-11. DDI AUX Channel DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
Notes: 1. $V_{AUX-DIFFp-p} = 2*\|V_{AUXP} - V_{AUXN}\|$ 2. Common mode voltage is equal to Vbias_Tx (or Vbias_Rx) voltage. 3. Steady-state common mode voltage shift between transmit and receive modes of operation. 4. Total drive current of the transmitter when it is shorted to its ground. 5. All Display Port Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.					

4.5.1.5 Embedded Display Port* AUX Channel Specification

Table 4-12. Embedded Display Port* AUX Channel DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
VAUX-DIFFp-p	AUX Peak-to-peak Voltage at a transmitting Device	0.29	1.38	V	1
VAUX-_TERM_R	AUX CH termination DC resistance		100	W	
VAUX-DC-CM	AUX DC Common Mode Voltage	0	1.2	V	2
VAUX-TURN-CM	AUX turn around common mode voltage		0.3	V	3
IAUX_SHORT	AUX Short Circuit Current Limit		90	mA	4
CAUX	AC Coupling Capacitor	75	200	nF	5
Notes: 1. $V_{AUX-DIFFp-p} = 2*\|V_{AUXP} - V_{AUXN}\|$ 2. Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage. 3. Steady state common mode voltage shift between transmit and receive modes of operation. 4. Total drive current of the transmitter when it is shorted to its ground. 5. All Display Port Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.					

4.5.1.6 DDI Panel GPIO Specification
[PNL0_BKLTCTL, PNL0_BKLTEN, PNL0_VDDEN, PNL1_BKLTCTL, PNL1_BKLTEN, PNL1_VDDEN]

Table 4-13. DDI Panel GPIO Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	3.09	3.47	V	3.3V nominal
VOH	Output HIGH voltage	2.85		V	3mA load
VOL	Output LOW voltage		0.45	V	@ -3mA load
VIH	Input HIGH voltage	2.475		V	
VIL	Input LOW voltage		0.825	V	
CL	Bus Signal Line capacitance		10	pF	
IPAD	Pad Leakage Current	-12	12	µA	
ZUP	Driver Pull-up Impedance	42.5	57.5	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	42.5	57.5	Ω	50 Ω nominal

Table 4-13. DDI Panel GPIO Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
Wpup5K	Weak Pull-up Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal ***Note:*** For DDI_HPD, an external resistor must be used and WPU should be disabled.
Wpdn5K	Weak Pull-down Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpup20K	Weak Pull-up Impedance 20K	15	25	kΩ	20 kΩ nominal ***Note:*** For DDI_HPD, an external resistor must be used and WPU should be disabled.
Wpdn20K	Weak Pull-down Impedance 20K	15	25	kΩ	20 kΩ nominal
Vhys	RX hysteresis		100	mV	
Cin	Pad Capacitance		5	pF	

4.5.1.7 MIPI*-DSI Specification

Table 4-14. MIPI*-DSI DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
ILEAK	Pin Leakage current	-10	10	µA	
VCMTX	HS transmit static common-mode voltage	150	250	mV	
|VCMTX(1,0)|	VCMTX mismatch when output is differential-1 or differential-0		5	mV	
|VOD|	HS transmit differential voltage	140	270	mV	
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0		14	mV	
VOHHS	HS output high voltage		360	mV	
ZOS	Single-ended output impedance	40	62.5	Ω	
ΔZOS	Single-ended output impedance mismatch		10	%	
VOH	Thevenin output high level	1.1	1.3	V	
VOL	Thevenin output low level	-50	50	mV	
ZOLP	Output impedance of LP transmitter	110		Ω	1
VIH	Logic 1 input voltage	880		mV	
VIL	Logic 0 input voltage, not in ULP state		550	mV	
VHYST	Input hysteresis	25		mV	
VIHCD	Logic 1 Contention threshold	450		mV	

Table 4-14. MIPI*-DSI DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VILCD	Logic 0 Contention threshold		200	mV	
Note: Deviates from MIPI*-D-PHY specification, which has minimum ZOLP of 110 Ω.					

4.5.1.8 MIPI*-DSI GPIO Specification [MDSI_A_TE, MDSI_C_TE]

Table 4-15. MIPI*-DSI GPIO Signals DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V_{OH}	Output High Voltage	1.35		V	@1.80V nominal (Vcc-0.45), @1.5mA Load
V_{OL}	Output Low Voltage		0.45	V	@-1.5mA Load
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
V_{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
I_{PAD}	Pad Leakage Current	-5	5	uA	
Z_{UP}	Driver Pull-up Impedance	160	240	Ω	200 Ω nominal
Z_{DN}	Driver Pull-down Impedance	160	240	Ω	200 Ω nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
V_{hys}	RX hysteresis	100		mV	
C_{in}	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 1.25 ns]		2.29	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 1.25 ns]		-0.49	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 5 ns]		2.23	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz <5 ns]		-0.43	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 10 ns]		2.17	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 10 ns]		-0.37	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.2 Memory Specifications

4.5.2.1 DDR4 Specification

Table 4-16. DDR4 DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VDDQ	Nominal Voltage	1.14	1.26	V	@1.2V Nominal
VIL	Input Low Voltage		0.65	V	@RxVref = 0.8 V
VIH	Input High Voltage	0.95		V	@RxVref = 0.8 V
VOL	Output Low Voltage		0.4	V	
VOH	Output High Voltage	0.8		V	@ Ron = 40 Ω/ Iload = 10 mA
IIL	Input Leakage Current	-10	10	µA	
CIO	DQ/DQS/DQS# DDR4-RS IO Pin Capacitance		2	pF	

4.5.2.2 LPDDR4 Specifications

Table 4-17. LPDDR4 DC Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VDDQ	I/O Supply Voltage	1.064	1.176	V	@1.12 V Nominal
VIL	Input Low Voltage		0.175	V	@RxVref=0.3
VIH	Input High Voltage	0.425		V	@RxVref=0.3
VOL	Output Low Voltage		0.4	V	
VOH	Output High Voltage	0.72		V	@ Ron = 40 Ω/ Iload = 10 mA
IIL	Input Leakage Current	-10	10	µA	
CIO	I/O Pin Capacitance		2	pF	

4.5.3 eMMC*

4.5.3.1 eMMC* Specification

Table 4-18. eMMC* Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal

Table 4-18. eMMC* Signal Group DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VOH	Output HIGH voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
VOl	Output LOW voltage		0.45	V	@ -3mA load
VIH	Input HIGH voltage	1.17		V	@1.80 V nominal (0.65*Vcc)
VIL	Input LOW voltage		0.63	V	@1.80 V nominal (0.35*Vcc)
CL	Bus Signal Line capacitance		5	pF	
IPAD	Pad Leakage Current	-5	5	µA	
ZUP	Driver Pull-up Impedance	32	48	Ω	40 Ω nominal
ZDN	Driver Pull-down Impedance	32	48	Ω	40 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	44	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	44	kΩ	20 kΩ nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 200MHz < 0.4ns]		2.13	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200MHz < 0.4ns]		-0.33	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 200MHz < 0.8ns]		2.07	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200MHz < 0.8ns]		-0.27	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 200MHz < 1.25ns]		2.04	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200MHz < 1.25ns]		-0.24	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C.

4.5.3.2 EMMC Specification [EMMC_RST_N]

Table 4-19. EMMC Specification [EMMC_RST_N] Signal DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V_{OH}	Output High Voltage	1.35		V	@1.80V nominal (Vcc-0.45), @1.5mA Load
V_{OL}	Output Low Voltage		0.45	V	@-1.5mA Load

Table 4-19. EMMC Specification [EMMC_RST_N] Signal DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
V_{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
I_{PAD}	Pad Leakage Current	-5	5	uA	
Z_{UP}	Driver Pull-up Impedance	160	240	Ω	200 Ω nominal
Z_{DN}	Driver Pull-down Impedance	160	240	Ω	200 Ω nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
V_{hys}	RX hysteresis		100	mV	
C_{in}	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 4MHz < 2.5 ns]		2.29	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 4MHz < 2.5 ns]		-0.49	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 4MHz < 5 ns]		2.23	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 4MHz <5 ns]		-0.43	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 4MHz < 10 ns]		2.17	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 4MHz < 10 ns]		-0.37	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.4 JTAG

Table 4-20. JTAG DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figures
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@ 1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@ 1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@ 3mA load
VOL	Output Low Voltage		0.67	V	@ -3mA load
Wwpu-20K	Weak Pull-up Impedance 20K	8	44	kΩ	20 kΩ nominal
Wwpd-20K	Weak Pull-down Impedance 20K	8	44	kΩ	20 kΩ nominal
Zup	Driver Pull-up Impedance	40	60	Ω	Nominal=50 Ω

Table 4-20. JTAG DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figures
Zdn	Driver Pull-down Impedance	40	60	Ω	Nominal=50 Ω
Vhys	RX hysteresis		100	mV	
Ipad	Pad Current	-5	5	µA	
VOS	Overshoot Voltage Magnitude [Time Duration for 200 MHz < 0.4 ns]		2.15	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200 MHz < 0.4 ns]		-0.35	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 200 MHz < 0.8 ns]		2.1	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200 MHz < 0.8ns]		-0.3	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 200 MHz < 1.25 ns]		2.6	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200 MHz < 1.25 ns]		-0.26	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.5 USB

4.5.5.1 USB 2.0 Specification

Table 4-21. USB 2.0 Host DC Specification (Sheet 1 of 3)

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
VBUS	High-power Port	4.75	5.25	V	2
VBUS	Low-power Port	4.2	5.25		
ICCPRT	High-power Hub Port (out)	500		mA	
ICCUPT	Low-power Hub Port (out)	100		mA	
ICCHPF	High-power Function (in)		500	mA	
ICCLPF	Low-power Function (in)		100	mA	
ICCINIT	Unconfigured Function/Hub (in)		100	mA	
ICCSH	Suspended High-power Device		2.5	mA	15
ICCSL	Suspended Low-power Device		500	µA	
VIH	High (driven)	2		V	4
VIHZ	High (floating)	2.7	3.6	V	4
VIL	Low		0.8	V	4
VDI	Differential Input Sensitivity	0.2		V	4
VCM	Differential Common Mode Range	0.8	2.5	V	4

Table 4-21. USB 2.0 Host DC Specification (Sheet 2 of 3)

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100	150	mV	
VHSDSC	High speed disconnect detection threshold (differential signal amplitude)	525	625	mV	
	High-speed differential input signaling levels				16
VHSCM	High-speed data signaling common mode voltage range (guideline for receiver)	-50	500	mV	
VOL	Low	0	0.3	V	4,5
VOH	High (Driven)	2.8	3.6	V	4,6
VOSE1	SE1	0.8		V	
VCRS	Output Signal Crossover Voltage	1.3	2	V	10
VHSOI	High-speed idle level	-10	10	mV	
VHSOH	High-speed data signaling high	360	440	mV	
VHSOL	High-speed data signaling low	-10	10	mV	
VCHIRPJ	Chirp J level (differential voltage)	700	1100	mV	
VCHIRPK	Chirp K level (differential voltage)	-900	-500	mV	
CHPB	Downstream Facing Port Bypass Capacitance (per hub)	120		µF	
CRPB	Upstream Facing Port Bypass Capacitance	1	10	µF	9
CIND	Downstream Facing Port		150	pF	2
CINUB	Upstream Facing Port (w/o cable)		100	pF	3
CEDGE	Transceiver edge rate control capacitance		75	pF	
RPU	Bus Pull-up Resistor on Upstream Facing Port	1.425	1.575	kΩ	1.5 kΩ±5%
RPD	Bus Pull-down Resistor on Downstream Facing Port	14.25	15.75	kΩ	1.5 kΩ±5%
ZINP	Input impedance exclusive of pull-up/pull-down (for low-/full speed)	300		kΩ	
VTERM	Termination voltage for upstream facing port pull-up (RPU)	3	3.6	V	
VHSTER M	Termination voltage in high speed	-10	10	mV	
RTERM	High Speed Termination	40.5	49.5	Ω	
VBUSD	VBUS Voltage drop for detachable cables		125	mV	Should be 125mV maximum

Table 4-21. USB 2.0 Host DC Specification (Sheet 3 of 3)

Symbol	Parameter	Minimum	Maximum	Units	Notes/ Figure
Notes: 1. Measured at A plug. 2. Measured at A receptacle. 3. Measured at B receptacle. 4. Measured at A or B connector. 5. Measured with RL of 1.425 kΩto 3.6V. 6. Measured with RL of 14.25 kΩto GND. 7. Timing difference between the differential data signals. 8. Measured at crossover point of differential data signals. 9. The maximum load specification is the maximum effective capacitive load allowed that meets the target VBUS drop of 330mV. 10. Excluding the first transition from the Idle state. 11. The two transitions should be a (nominal) bit time apart. 12. For both transitions of differential signaling. 13. Must accept as valid EOP. 14. Single-ended capacitance of D+ or D- is the capacitance of D+/D- to all other conductors and, if present, shield in the cable. That is, to measure the single-ended capacitance of D+, short D-, VBUS, GND, and the shield line together and measure the capacitance of D+ to the other conductors. 15. For high power devices (non-hubs) when enabled for remote wakeup. 16. Specified by eye pattern templates.					

4.5.5.2 USB 3.0 Specification

Table 4-22. USB 3.0 Interface DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
UI	Unit Interval	199.94	200.06	ps	1
VTX-DIFF-PP	Differential peak-peak Tx voltage swing	0.9	1.05	V	
VTX-DIFF-PP- LOW	Low-Power Differential peak-peak Tx voltage swing	0.4	1.2	V	2
VTX-DE-RATIO	Tx De-Emphasis	3	4	dB	
RTX-DIFF-DC	DC differential impedance	68	92	Ω	
VTX-RCV- DETECT	The amount of voltage change allowed during Receiver Detection		0.6	V	3
CAC-COUPLING	AC Coupling Capacitor	75	200	nF	4
tCDR_SLEW_M AX	Maximum slew rate		10	ms/s	
Notes: 1. The specified UI is equivalent to a tolerance of 300 ppm for each device. Period does not account for SSC induced variations. 2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode. 3. Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver's input goes below output. 4. All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.					

4.5.5.3 USB GPIO Specification [USB_OC0_N, USB_OC1_N]

Table 4-23. USB GPIO Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal

Table 4-23. USB GPIO Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VIH	Input High Voltage	1.17		V	@1.80V nominal(0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal(0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal(Vcc-0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	µA	
ZUP	Driver Pull-up Impedance	160	240	Ω	200 Ω nominal
ZDN	Driver Pull-down Impedance	160	240	Ω	200 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 25MHz < 2.5ns]		2.29	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25MHz < 2.5ns]		-0.49	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 5ns]		2.23	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 5ns]		-0.43	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 10 ns]		2.17	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 10ns]		-0.37	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C.

4.5.6 SPI

4.5.6.1 SIO SPI Specification

Table 4-24. SIO SPI Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)

Table 4-24. SIO SPI Signal Group DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
V_{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
V_{OH}	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
V_{OL}	Output Low Voltage		0.45	V	@ -3mA load.
I_{PAD}	Pad Leakage Current	-5	5	uA	
Z_{UP}	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
Z_{DN}	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	44	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	44	kΩ	20 kΩ nominal
V_{hys}	RX hysteresis		100	mV	
C_{in}	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 0.4 ns]		2.15	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 0.4ns]		-0.35	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25MHz < 0.8ns]		2.1	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 0.8 ns]		-0.3	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 1.25 ns]		2.6	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz <1.25 ns]		-0.26	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.6.2 PMC SPI Specification

Table 4-25. PMC SPI Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.80V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc-0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	160	240	Ω	200 Ω nominal

Table 4-25. PMC SPI Signal Group DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
ZDN	Driver Pull-down Impedance	160	240	Ω	200 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
Vhys	RX hysteresis		100	mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 4 MHz < 2.5 ns]		2.29	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 4 MHz < 2.5ns]		-0.49	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 4 MHz < 5 ns]		2.23	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 4 MHz < 5 ns]		-0.43	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 4 MHz < 10 ns]		2.17	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 4 MHz < 10 ns]		-0.37	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.6.3 FAST SPI Specification

Table 4-26. FAST SPI DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
V_{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
V_{OH}	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
V_{OL}	Output Low Voltage		0.45	V	@ -3mA load.
I_{PAD}	Pad Leakage Current	-5	5	µA	
Z_{UP}	Driver Pull-up Impedance	27	40	Ω	33.5 Ω nominal
Z_{DN}	Driver Pull-down Impedance	27	40	Ω	33.5 Ω nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	44	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	44	kΩ	20 kΩ nominal
V_{hys}	RX hysteresis		100	mV	
C_{in}	Pad Capacitance		5	pF	

Table 4-26. FAST SPI DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VOS	Overshoot Voltage Magnitude [Time Duration for 50 MHz < 0.4 ns]		2.15	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 50 MHz < 0.4 ns]		-0.35	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 50 MHz < 0.8 ns]		2.1	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 50 MHz < 0.8 ns]		-0.3	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 50 MHz < 1.25 ns]		2.06	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 50 MHz < 1.25 ns]		-0.26	V	1,2
Notes: 1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US. 2. Tj = 105^0C					

4.5.7 eSPI

Table 4-27. eSPI Signals DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC(1.8)	I/O Voltage (1.8)	1.66	1.89	V	1.8V nominal
VIH(1.8)	Input High Voltage	0.9		V	0.5 * VCC(1.8)
VIL(1.8)	Input Low Voltage		0.486	V	0.27 * VCC(1.8)
VOH(1.8)	Output High Voltage	1.35		V	Vcc- 0.45, @ 3mA load.
VOL(1.8)	Output Low Voltage		0.45	V	@ -3mA load.
IPAD	Pad Leakage Current	-12	12	µA	
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup5K	Weak Pull-up Impedance 5K	1.5	8.5	kΩ	5kΩ nominal
Wpdn5K	Weak Pull-down Impedance 5K	1.5	8.5	kΩ	5kΩ nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	10	30	kΩ	20 kΩ nominal
Cin	Pad Capacitance		10	pF	
Notes: 1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US. 2. Tj = 105^0C					

4.5.8 SVID

4.5.8.1 SVID Specification

Table 4-28. SVID Signal Group DC Specification (SVID_DATA, SVID_CLK, SVID_ALERT_N)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1	1.1	V	1.05V Nominal
V_{IH}	Input High Voltage	0.68		V	@1.05V nominal (0.65*Vcc)
V_{IL}	Input Low Voltage		0.36	V	@1.05V nominal (0.35*Vcc)
V_{OL}	Output Low Voltage		0.45	V	@3mA Load
I_{PAD}	Pad Leakage Current	-5	5	µA	
Z_{DN}	Driver Pull-down Impedance	15	25	Ω	20 Ω Nominal
W_{pup1K}	Weak Pull-up Impedance 1K	0.65	1.35	kΩ	1 kΩ nominal
W_{pup2K}	Weak Pull-up Impedance 2K	1.3	2.7	kΩ	2 kΩ nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
V_{hys}	RX hysteresis	100		mV	
C_{in}	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 1.25 ns]		2.2	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 1. 25 ns]		-0.31	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 2.5 ns]		2.14	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 2.5ns]		-0.25	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 5ns]		2.09	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 5ns]		-0.2	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.9 SIO (LPSS)—UART

Table 4-29. SIO (LPSS) UART Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal

Table 4-29. SIO (LPSS) UART Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
V_{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
V_{OH}	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 1.5mA load.
V_{OL}	Output Low Voltage		0.45	V	@ -1.5mA load.
I_{PAD}	Pad Leakage Current	-5	5	uA	
Z_{UP}	Driver Pull-up Impedance	160	240	Ω	200 Ω nominal
Z_{DN}	Driver Pull-down Impedance	160	240	Ω	200 Ω nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
V_{hys}	RX hysteresis		100	mV	
C_{in}	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 2.5 ns]		2.29	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 2.5 ns]		-0.49	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 5 ns]		2.23	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 5 ns]		-0.43	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25 MHz < 10 ns]		2.17	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25 MHz < 10 ns]		-0.37	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.10 I²S (Audio)

Table 4-30. I²S Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)

Table 4-30. I2S Signal Group DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load
VOL	Output Low Voltage		0.45	V	@ -3mA load
IPAD	Pad Leakage Current	-5	5	µA	
ZUP	Driver Pull-up Impedance	54	80	Ω	67 Ω nominal
ZDN	Driver Pull-down Impedance	54	80	Ω	67 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	44	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	44	kΩ	20 kΩ nominal
Vhys	RX hysteresis		100	mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 12.288 MHz < 0.4 ns]		2.15	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 12.288 MHz < 0.4 ns]		-0.35	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 12.288 MHz < 0.8 ns]		2.1	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 12.288 MHz < 0.8 ns]		-0.3	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 12.288 MHz < 1.25 ns]		2.06	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 12.288 MHz < 1.25 ns]		-0.26	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US
2. Tj = 105^0C

4.5.11 AVS DMIC

Table 4-31. AVS DMIC Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
VOL	Output Low Voltage		0.45	V	@ -3mA load.

Table 4-31. AVS DMIC Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	54	80	Ω	67 Ω nominal
ZDN	Driver Pull-down Impedance	54	80	Ω	67 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 12 MHz < 2.5 ns]		2.29	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 12 MHz < 2.5ns]		-0.49	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 12 MHz < 5 ns]		2.23	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 12 MHz < 5 ns]		-0.43	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 12 MHz < 10 ns]		2.17	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 12 MHz < 10 ns]		-0.37	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US
2. Tj = 105^0C

4.5.12 I²C

4.5.12.1 I²C SIO/PMC/DSI Specification [SIO I2C_0:4]

Table 4-32. I²C SIO/PMC/DSI Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
V_{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
V_{OL}	Output Low Voltage		0.45	V	@ -3mA load.
I_{PAD}	Pad Leakage Current	-5	5	uA	
Z_{DN}	Driver Pull-down Impedance	10	300	Ω	20/40/100/150/300 Ω nominal
W_{pup1K}	Weak Pull-up Impedance 1K	0.65	1.35	kΩ	1 kΩ nominal
W_{pup2K}	Weak Pull-up Impedance 2K	1.3	2.7	kΩ	2 kΩ nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal

Table 4-32. I2C SIO/PMC/DSI Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
V_{hys}	RX hysteresis		100	mV	
C_{in}	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 60 MHz < 1.25 ns]		2.2	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 60 MHz < 1.25 ns]		-0.31	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 60 MHz < 2.5 ns]		2.14	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 60 MHz < 2.5 ns]		-0.25	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 60 MHz < 5 ns]		2.09	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 60 MHz < 5 ns]		-0.2	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US
2. Tj = 105^0C

4.5.12.2 I2C Specification [SIO I2C_5:7]

Table 4-33. I2C DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	3.09	3.47	V	3.3V nominal
VOH	Output HIGH voltage	2.85		V	3mA load.
VOL	Output LOW voltage		0.45	V	@ -3mA load
VIH	Input HIGH voltage	2.31		V	
VIL	Input LOW voltage		0.891	V	
IPAD	Pad Leakage Current	-10	10	µA	
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	15	25	kΩ	20kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	15	25	kΩ	20kΩ nominal
Vhys	RX hysteresis		100	mV	
Cin	Pad Capacitance		8	pF	

4.5.13 HDA

4.5.13.1 HDA Specification

Table 4-34. HDA Signal Group DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.65*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc-0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	44	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	44	kΩ	20 kΩ nominal
Vhys	RX hysteresis		100	mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 25MHz < 0.4 ns]		2.15	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25MHz < 0.4ns]		-0.35	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25MHz < 0.8 ns]		2.1	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25MHz < 0.8 ns]		-0.3	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 25MHz < 1.25 ns]		2.06	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 25MHz < 1.25 ns]		-0.26	V	1,2

4.5.14 LPC

4.5.14.1 LPC Specification

Table 4-35. LPC Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC (3.3)	I/O Voltage (3.3)	3.09	3.47	V	3.3V nominal
VCC(1.8)	I/O Voltage (1.8)	1.66	1.89	V	1.8V nominal
VIH (3.3)	Input high Voltage (3.3)	1.65		V	0.5 * VCC(3.3)

Table 4-35. LPC Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VIL (3.3)	Input Low Voltage (3.3)		0.891	V	0.27 * VCC(3.3)
VIH(1.8)	Input High Voltage	0.9		V	0.5 * VCC(1.8)
VIL(1.8)	Input Low Voltage		0.486	V	0.27 * VCC(1.8)
VOH(3.3)	Output High Voltage	2.85		V	Vcc- 0.45, @ 3mA load.
VOL(3.3)	Output Low Voltage		0.45	V	@ -3mA load.
VOH(1.8)	Output High Voltage	1.35		V	Vcc- 0.45, @ 3mA load.
VOL(1.8)	Output Low Voltage		0.45	V	@ -3mA load.
IPAD	Pad Leakage Current	-12	12	µA	
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup5K	Weak Pull-up Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpdn5K	Weak Pull-down Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	10	30	kΩ	20 kΩ nominal
Cin	Pad Capacitance		10	pF	

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.15 Platform Clock

4.5.15.1 Platform Clock Specification

Table 4-36. Platform Clock GPIO (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V Nominal
V_{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
V_{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
V_{OH}	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 1.5mA load.
V_{OL}	Output Low Voltage		0.45	V	@ -1.5mA load
I_{PAD}	Pad Leakage Current	-5	5	µA	
Z_{UP}	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
Z_{DN}	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
W_{pup20K}	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
W_{pdn20K}	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
V_{hys}	RX hysteresis		100	mV	

Table 4-36. Platform Clock GPIO (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
C_{in}	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 1.25 ns]		2.15	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 1. 25 ns]		-0.35	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 2.5 ns]		2.1	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 2.5ns]		-0.3	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 19.2 MHz < 5ns]		2.06	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 19.2 MHz < 5ns]		-0.26	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.16 PCIe* Specification

4.5.16.1 PCIe* DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	
V_{IH}	Input High Voltage	1.22		V	
V_{IL}	Input Low Voltage		0.581	V	
V_{TXDIFF}	Differential TX Peak to Peak	800	1200	mV	
$V_{TXDIFF-LP}$	Differential TX Peak to Peak (Low power mode)	400	1200	mV	
V_{RXDIFF}	Differential RX Peak to Peak	175	1200	mV	
$V_{RXDIFF-LP}$	Differential RX Peak to Peak (Low power mode)	100	1200	mV	

4.5.16.2 PCIe Specification [PCIe_wake[0:4]_N, PCIe_clkreq[0:3]_N]

Table 4-37. PCIe Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	3.09	3.47	V	3.3V nominal
VOH	Output HIGH voltage	2.85		V	3mA load.

Table 4-37. PCIe Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VOL	Output LOW voltage		0.45	V	@ -3mA load
VIH	Input HIGH voltage	2.475		V	
VIL	Input LOW voltage		0.825	V	
CL	Bus Signal Line capacitance		10	pF	
IPAD	Pad Leakage Current	-12	12	µA	
ZUP	Driver Pull-up Impedance	42.5	57.5	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	42.5	57.5	Ω	50 Ω nominal
Wpup5K	Weak Pull-up Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpdn5K	Weak Pull-down Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpup20K	Weak Pull-up Impedance 20K	15	25	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	15	25	kΩ	20 kΩ nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	

4.5.16.3 SATA Specification

Table 4-38. General Specifications (Sheet 1 of 2)

Parameters	Limit	Gen1	Gen2	Units
Channel Speed	Nom	1.5	3.0	Gbps
Fbaud	Nom	1.5	3.0	GHz
FER, Frame Error Rate	Max	8.2e-8 at 95 % confidence level	8.2e-8 at 95 % confidence level	
TUI, Unit Interval	Min	666.433 3	333.216 7	Ps
	Nom	666.666 7	333.333 3	
	Max	670.233 3	335.116 7	
ftol, Tx Frequency Long Term Accuracy	Min	-350	-350	ppm of Fbaud
	Max	+350	+350	
fSSC, Spread- Spectrum Modulation Frequency	Min	30	30	kHz
	Max	33	33	

Table 4-38. General Specifications (Sheet 2 of 2)

Parameters	Limit	Gen1	Gen2	Units
SSCtol, Spread- Spectrum Modulation Deviation	Min	-5 350	-5 350	ppm of Fbaud
	Max	+350	+350	
SSCtol, Spread- Spectrum Modulation Rate	Max	1 250	1 250	ppm/ us
Vcm,ac coupled, AC Coupled Common Mode Voltage	Min	0	-	mV
	Max	2 000	-	
Zdiff, Nominal Differential Impedance	Nom	100	-	Ω
Cac coupling AC Coupling Capacitance	Max	12	12	nF
tsettle,cm, Common Mode Transient Settle Time	Max	10	-	ns
Vtrans, Sequencing Transient Voltage	Min	-2.0	-2.0	V
	Max	2.0	2.0	

Table 4-39. Transmitted Signal Requirements (Sheet 1 of 2)

Parameter	Unit	Limit	Gen1i	Gen2i
VdiffTxdevice, Tx Differential Device Output Voltage	mVppd	Min	400	400
		Min	-	-
		Nom	500	-
		Max	600	700
		Max	-	-

Table 4-39. Transmitted Signal Requirements (Sheet 2 of 2)

Parameter	Unit	Limit	Gen1i	Gen2i
VdiffTxhost, Tx Differential Host Output Voltage	mVppd	Min	400	400
		Min	-	-
		Nom	500	-
		Max	600	700
		Max	-	-
UIVminTx, Tx Minimum Voltage Measurement Interval	UI		0.45 to 0.55	0.45 to 0.55
			-	-
t20-80Tx, Tx Rise/Fall Time	ps (UI)	Min 20 % to 80 %	50 (0.075)	50 (0.15)
		Max 20 % to 80 %	273 (0.41)	136 (0.41)
tskewTx, Tx Differential Skew	ps	Max	20	20

4.5.17 SMBus Specification

Table 4-40. SMBus DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC (3.3)	I/O Voltage (3.3)	3.05	3.45	V	3.3V Nominal
VCC(1.8)	I/O Voltage (1.8)	1.66	1.89	V	1.8V nominal
VIH (3.3)	Input high Voltage (3.3)	1.65		V	0.5 * VCC(3.3)
VIL (3.3)	Input Low Voltage (3.3)		0.891	V	0.27 * VCC(3.3)
VIH(1.8)	Input High Voltage	0.9		V	0.5 * VCC(1.8)
VIL(1.8)	Input Low Voltage		0.486	V	0.27 * VCC(1.8)
VOH(3.3)	Output High Voltage	2.85		V	Vcc- 0.45, @ 3mA load.
VOL(3.3)	Output Low Voltage		0.45	V	@ -3mA load.
VOH(1.8)	Output High Voltage	1.35		V	Vcc- 0.45, @ 3mA load.
VOL(1.8)	Output Low Voltage		0.45	V	@ -3mA load.
IPAD	Pad Leakage Current	-12	12	µA	
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup5K	Weak Pull-up Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpdn5K	Weak Pull-down Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	10	30	kΩ	20 kΩ nominal
Cin	Pad Capacitance		10	pF	

Notes:

1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^0C

4.5.18 PMU (Power Management Signals)

4.5.18.1 PMU Specification

Table 4-41. PMU Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC (3.3)	I/O Voltage (3.3)	3.05	3.45	V	3.3V nominal
VCC(1.8)	I/O Voltage (1.8)	1.66	1.89	V	1.8V nominal
VIH (3.3)	Input high Voltage (3.3)	1.65		V	0.5 * VCC(3.3)
VIL (3.3)	Input Low Voltage (3.3)		0.891	V	0.27 * VCC(3.3)
VIH(1.8)	Input High Voltage	0.9		V	0.5 * VCC(1.8)
VIL(1.8)	Input Low Voltage		0.486	V	0.27 * VCC(1.8)
VOH(3.3)	Output High Voltage	2.85		V	Vcc- 0.45, @ 3mA load.
VOL(3.3)	Output Low Voltage		0.45	V	@ -3mA load.

Table 4-41. PMU Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VOH(1.8)	Output High Voltage	1.35		V	Vcc- 0.45, @ 3mA load.
VOL(1.8)	Output Low Voltage		0.45	V	@ -3mA load.
IPAD	Pad Leakage Current	-12	12	µA	
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup5K	Weak Pull-up Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpdn5K	Weak Pull-down Impedance 5K	1.5	8.5	kΩ	5 kΩ nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	10	30	kΩ	20 kΩ nominal
Cin	Pad Capacitance		10	pF	

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^{0}C

4.5.19 GPIO/PROCHOT_N/THERMTRIP_N Specification

Table 4-42. DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	160	240	Ω	200 Ω nominal
ZDN	Driver Pull-down Impedance	160	240	Ω	200 Ω nominal
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kΩ	20 kΩ nominal
Vhys	RX hysteresis		100	mV	
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 200 MHz < 0.4 ns]		2.29	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200 MHz < 0.4 ns]		-0.49	V	1,2

Table 4-42. DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VOS	Overshoot Voltage Magnitude [Time Duration for 200 MHz < 0.8 ns]		2.23	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200 MHz < 0.8ns]		-0.43	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 200 MHz < 1.25 ns]		2.17	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 200 MHz < 1.25 ns]		-0.37	V	1,2
Notes: 1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US. 2. Tj = 105^0C					

4.5.20 RTC Signal Specification

Table 4-43. RTC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	2	3.47	V	3.3V nominal
VIH	Input High Voltage	2		V	@3.3V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.78	V	@3.3V nominal (0.35*Vcc)

4.5.21 CNVi

4.5.21.1 CNVi DC Specification [CNV_BRI_DT/CNV_BRI_RSP/CNV_RF_RESET_N/CNV_RGI_DT/CNV_RGI_RSP]

Table 4-44. CNVi Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VOH	Output HIGH voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
VOl	Output LOW voltage		0.45	V	@ -3mA load
VIH	Input HIGH voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input LOW voltage		0.63	V	@1.80V nominal (0.35*Vcc)
CL	Bus Signal Line capacitance		5	pF	
IPAD	Pad Leakage Current	-5	5	µA	
ZUP	Driver Pull-up Impedance	40	60	Ω	50 Ω nominal
ZDN	Driver Pull-down Impedance	40	60	Ω	50 Ω nominal
Wpup20K	Weak Pull-up Impedance 20K	8	44	kΩ	20 kΩ nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	44	kΩ	20 kΩ nominal
Vhys	RX hysteresis		100	mV	

Table 4-44. CNVi Signal Group DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
Cin	Pad Capacitance		5	pF	
VOS	Overshoot Voltage Magnitude [Time Duration for 100MHz < 0.4ns]		2.13	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 100MHz < 0.4ns]		-0.33	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 100MHz < 0.8ns]		2.07	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 100MHz < 0.8ns]		-0.27	V	1,2
VOS	Overshoot Voltage Magnitude [Time Duration for 100MHz < 1.25ns]		2.04	V	1,2
VUS	Undershoot Voltage Magnitude [Time Duration for 100MHz < 1.25ns]		-0.24	V	1,2

Notes:
1. Activity Factor = 0.25, i.e., 1 out of 4 receive cycles will have the OS/US.
2. Tj = 105^{0}C.

4.5.21.2 CNVi DC Specification [CNV_WT_CLK_N/P/ CNV_WT_D0:1[N/P]/CNV_WT_CLK_N/P/ CNV_WT_D0:1[N/P]]

Table 4-45. CNVi DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
ILEAK	Pin Leakage current	-10	10	µA	
VCMTX	HS transmit static common-mode voltage	150	250	mV	
|VCMTX(1,0)|	VCMTX mismatch when output is differential-1 or differential-0		5	mV	
|VOD|	HS transmit differential voltage	140	270	mV	
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0		14	mV	
VOHHS	HS output high voltage		360	mV	
ZOS	Single-ended output impedance	40	62.5	Ω	
ΔZOS	Single-ended output impedance mismatch		10	%	
VOH	Thevenin output high level	1.1	1.3	V	
VOL	Thevenin output low level	-50	50	mV	
ZOLP	Output impedance of LP transmitter	110		Ω	1
VIH	Logic 1 input voltage	880		mV	
VIL	Logic 0 input voltage, not in ULP state		550	mV	
VHYST	Input hysteresis	25		mV	
VIHCD	Logic 1 Contention threshold	450		mV	
VILCD	Logic 0 Contention threshold		200	mV	
Note: Deviates from MIPI*-D-PHY specification Rev 1.1, which has minimum ZOLP of 110 Ω.					

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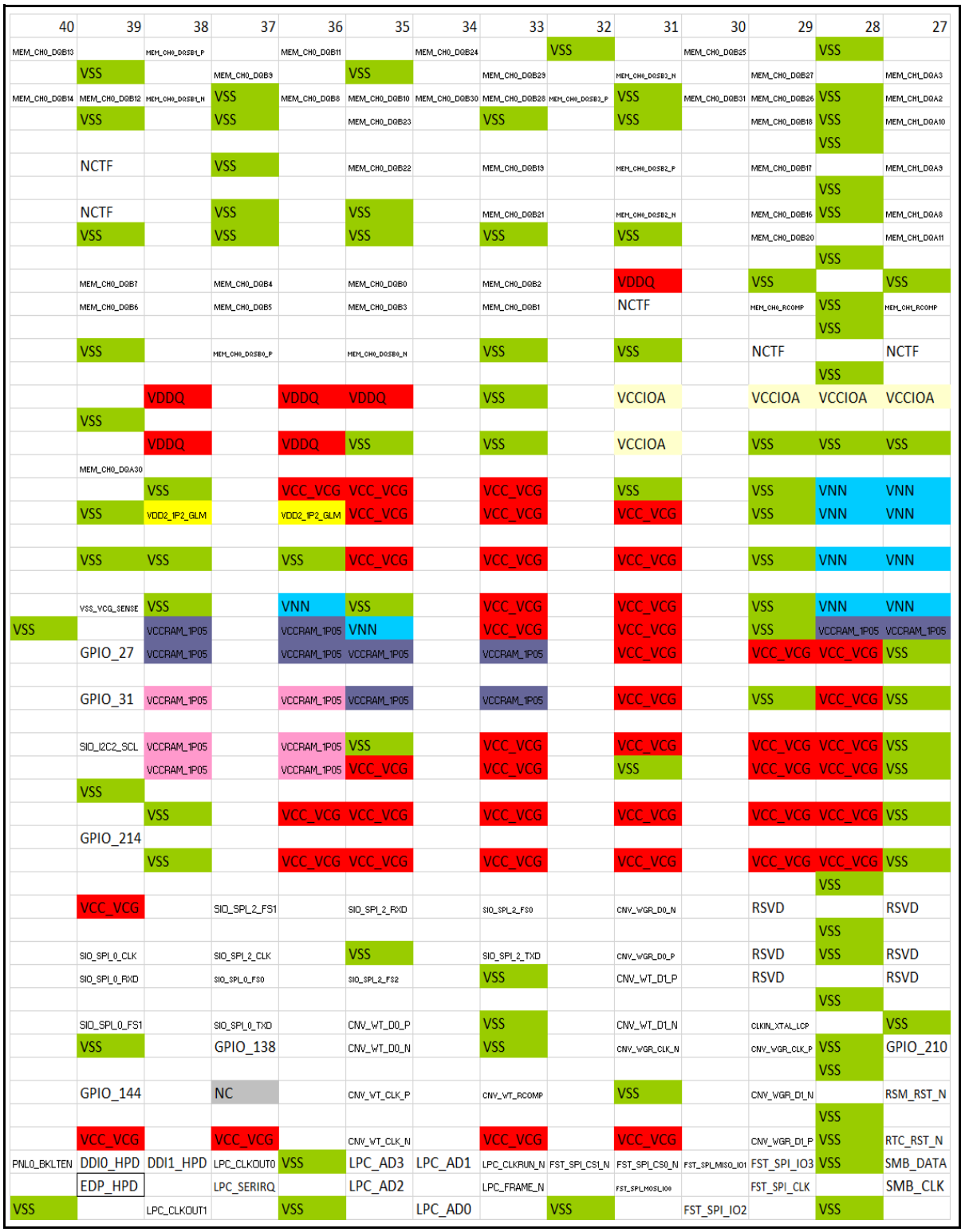
5 Ball Map and SoC Pin Locations

5.1 Ball Map—LPDDR4

Figure 5-1. Ball Map LPDDR4—Left (55–41)

	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41
BL		NC	NC		VSS	MEM_CH0_CAA5		VSS		VSS		MEM_CH0_CS1A		VSS	
BK	VSS								MEM_CH0_CAA4		NCTF		MEM_CH0_CS1B		MEM_CH0_DQB15
BJ		VSS		NCTF	NCTF	NCTF		NCTF	MEM_CH0_CAA3	MEM_CH0_CAA2	MEM_CH0_CAA0	MEM_CH0_CAA1	MEM_CH0_CS0A	MEM_CH0_CS0B	VSS
BH	NC	MEM_CH0_CKE0B			NCTF	NCTF			MEM_CH0_CAB5		VSS		MEM_CH0_CAB0		VSS
BG	VSS	MEM_CH0_CKE1B		NCTF		VSS									
BF	MEM_CH0_CKE0A	MEM_CH0_CKE1A							VSS		NCTF		MEM_CH0_CAB2		MEM_CH0_CAB1
BE		MEM_CH0_DQA22	VSS		MEM_CH0_CLKB_N		MEM_CH0_CLKB_P								
BD	MEM_CH0_DQA21		MEM_CH0_DQA23						VSS		NCTF		MEM_CH0_CAB4		MEM_CH0_CAB3
BC		MEM_CH0_DQSA2_P	MEM_CH0_DQA20		VSS		MEM_CH0_CLKA_P	MEM_CH0_CLKA_N			VSS		MEM_CH0_RESET_N		VSS
BB	VSS		MEM_CH0_DQSA2_N												
BA		MEM_CH0_DQA17	MEM_CH0_DQA18		MEM_CH0_DQA14		MEM_CH0_DQA13	MEM_CH0_DQA12		MEM_CH0_DQA11			VDDQ		VDDQ
AY	MEM_CH0_DQA16		MEM_CH0_DQA19										VSS		VSS
AW		VSS	MEM_CH0_DQA7		VSS		MEM_CH0_DQSA1_P	MEM_CH0_DQSA1_N		VSS		NC			
AV	MEM_CH0_DQA6		MEM_CH0_DQA5												VSS
AU		MEM_CH0_DQA4	VSS		MEM_CH0_DQA8		MEM_CH0_DQA10	MEM_CH0_DQA3		VSS		MEM_CH0_DQA31	MEM_CH0_DQA28		MEM_CH0_DQA27
AT	MEM_CH0_DQSA0_N		MEM_CH0_DQSA0_P												
AR		VSS	MEM_CH0_DQA0		MEM_CH0_DQA15		VSS	MEM_CH0_DQA26		VSS		VSS	MEM_CH0_DQSA3_N		MEM_CH0_DQSA3_P
AP	MEM_CH0_DQA1		MEM_CH0_DQA2												
AN		MEM_CH0_DQA3	VSS		VSS		VSS	VSS		VSS		MEM_CH0_DQA25	MEM_CH0_DQA24		MEM_CH0_DQA29
AM	VSS		JTAG_TCK												
AL		JTAG_TMS	JTAG_TDO		VSS		VNN	VNN		VSS		VSS	VSS		VSS
AK	VSS		JTAG_TRST_N												
AJ		JTAG_TDI	JTAG_PREQ_N		VCC_1P05_INT		NC	VNN		VNN		VSS	VNN_SENSE		VNN_SENSE
AH	JTAG_PRDY_N		JTAGX												
AG		GPIO_9	GPIO_8		VCC_1P05_INT		VCC_1P05_INT	VNN		VNN		NC	NC		VCC_VCG_SENSE
AF	VSS		VSS	VSS		VSS		VSS	VSS		VSS	VSS		VSS	
AE		GPIO_10	GPIO_11		GPIO_20		GPIO_21	VSS		GPIO_28		GPIO_29	VSS		GPIO_26
AD	GPIO_12		GPIO_13												
AC		GPIO_14	GPIO_15		GPIO_22		GPIO_23	GPIO_18		GPIO_19		GPIO_32	GPIO_33		GPIO_30
AB	VSS		GPIO_16												
AA		GPIO_35	GPIO_36		GPIO_24		GPIO_17	VSS		GPIO_25		GPIO_34	VSS		SIO_I2C2_SDA
Y	GPIO_37		GPIO_38												
W		GPIO_39	GPIO_40		VSS		VSS	VSS		VSS		VSS	VSS		VSS
V	VSS		GPIO_41												
U		USB2_OC0_N	USB2_OC1_N		SIO_I2C0_SDA		SIO_I2C0_SCL	SIO_I2C1_SDA		SIO_I2C1_SCL		EMMC_RST_N	GPIO_212		GPIO_213
T	MDSI_A_TE		MDSI_C_TE												
R		MIPI_I2C_SDA	MIPI_I2C_SCL		SIO_I2C4_SDA		SIO_I2C4_SCL	PMC_I2C_SDA		PMC_I2C_SCL		SIO_I2C3_SCL	SIO_I2C3_SDA		NC
P	VSS		SIO_UART0_CTS_N												VCC_VCG
N		SIO_UART0_RTS_N	SIO_UART0_RXD		VSS		PMC_SPI_TXD	PMC_SPI_FS0		VSS		PMC_SPI_FS1			
M	SIO_UART0_TXD		SIO_UART2_CTS_N										GPIO_137		VSS
L		SIO_UART2_RTS_N	SIO_UART2_TXD		PMC_SPI_RXD		PMC_SPI_FS2	PMC_SPI_CLK		GPIO_105			GPIO_136		GPIO_145
K	VSS		SIO_UART2_RXD												
J		PROCHOT_N	THERMTRIP_N		VSS		PMU_SLP_S4_N	PMU_BATLOW_N			VSS		GPIO_140		VSS
H	NC		NC						GPIO_135		GPIO_134		GPIO_139		GPIO_143
G		SVID0_ALERT_N	SVID0_DATA		EMMC_PWR_EN_N		PMU_SUSCLK								
F	SVID0_CLK	SUSPWRDNACK							PCIE_WAKE0_N		PCIE_WAKE2_N		GPIO_142		GPIO_146
E	VSS	PMU_PWRBTN_N		SUS_STAT_N		VSS									
D	VSS	PMU_PLTRST_N			PMU_SLP_S3_N	PCIE_WAKE3_N			PCIE_WAKE1_N		VSS		GPIO_141		VSS
C		NC		PMU_SLP_S0_N	PMU_RSTBTN_N	SIO_I2C5_SCL		SIO_I2C6_SCL	SIO_I2C6_SDA	SIO_I2C7_SDA	PCIE_CLKREQ1_N	PCIE_CLKREQ3_N	DDI0_DDC_SDA	DDI1_DDC_SCL	PNL0_VDDEN
B	VSS								SIO_I2C7_SCL		PCIE_CLKREQ2_N		DDI0_DDC_SCL		PNL0_BKLCTL
A		NC	SKTOCC_N		VSS	SIO_I2C5_SDA		VSS		PCIE_CLKREQ0_N		VSS		DDI1_DDC_SDA	

Figure 5-2. Ball Map LPDDR4—Center (40–27)

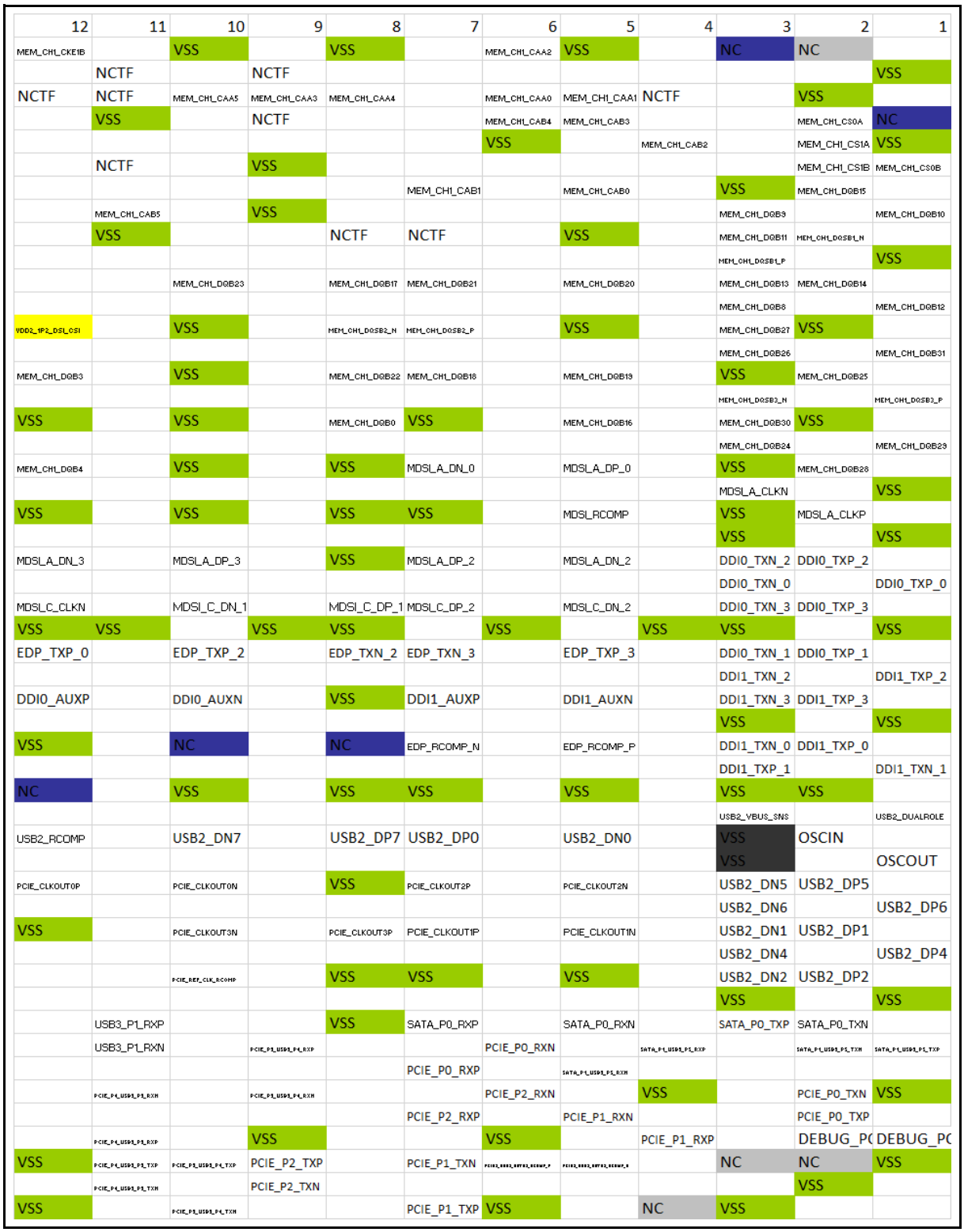


40	39	38	37	36	35	34	33	32	31	30	29	28	27
MEM_CH0_DQB13		MEM_CH0_DQSB1_P		MEM_CH0_DQB11		MEM_CH0_DQB24		VSS		MEM_CH0_DQB25		VSS	
	VSS		MEM_CH0_DQB9		VSS		MEM_CH0_DQB29		MEM_CH0_DQSB3_N		MEM_CH0_DQB27		MEM_CH1_DQA3
MEM_CH0_DQB14	MEM_CH0_DQB12	MEM_CH0_DQSB1_N	VSS	MEM_CH0_DQB8	MEM_CH0_DQB10	MEM_CH0_DQB30	MEM_CH0_DQB28	MEM_CH0_DQSB3_P	VSS	MEM_CH0_DQB31	MEM_CH0_DQB26	VSS	MEM_CH1_DQA2
	VSS		VSS		MEM_CH0_DQB23		VSS		VSS		MEM_CH0_DQB18	VSS	MEM_CH1_DQA10
												VSS	
	NCTF		VSS		MEM_CH0_DQB22		MEM_CH0_DQB19		MEM_CH0_DQSB2_P		MEM_CH0_DQB17		MEM_CH1_DQA9
												VSS	
	NCTF		VSS		VSS		MEM_CH0_DQB21		MEM_CH0_DQSB2_N		MEM_CH0_DQB16	VSS	MEM_CH1_DQA8
	VSS		VSS		VSS		VSS		VSS		MEM_CH0_DQB20		MEM_CH1_DQA11
												VSS	
	MEM_CH0_DQB7		MEM_CH0_DQB4		MEM_CH0_DQB0		MEM_CH0_DQB2		VDDQ		VSS		VSS
	MEM_CH0_DQB6		MEM_CH0_DQB5		MEM_CH0_DQB3		MEM_CH0_DQB1		NCTF		MEM_CH0_RCOMP	VSS	MEM_CH1_RCOMP
												VSS	
	VSS		MEM_CH0_DQSB0_P		MEM_CH0_DQSB0_N		VSS		VSS		NCTF		NCTF
												VSS	
		VDDQ		VDDQ	VDDQ		VSS		VCCIOA		VCCIOA	VCCIOA	VCCIOA
	VSS												
		VDDQ		VDDQ	VSS		VSS		VCCIOA		VSS	VSS	VSS
	MEM_CH0_DQA30												
		VSS		VCC_VCG	VCC_VCG		VCC_VCG		VSS		VSS	VNN	VNN
	VSS	VDD2_1P2_GLM		VDD2_1P2_GLM	VCC_VCG		VCC_VCG		VCC_VCG		VSS	VNN	VNN
	VSS	VSS		VSS	VCC_VCG		VCC_VCG		VCC_VCG		VSS	VNN	VNN
	VSS_VCG_SENSE	VSS		VNN	VSS		VCC_VCG		VCC_VCG		VSS	VNN	VNN
VSS		VCCRAM_1P05		VCCRAM_1P05	VNN		VCC_VCG		VCC_VCG		VSS	VCCRAM_1P05	VCCRAM_1P05
	GPIO_27	VCCRAM_1P05		VCCRAM_1P05	VCCRAM_1P05		VCCRAM_1P05		VCC_VCG		VCC_VCG	VCC_VCG	VSS
	GPIO_31	VCCRAM_1P05		VCCRAM_1P05	VCCRAM_1P05		VCCRAM_1P05		VCC_VCG		VSS	VCC_VCG	VSS
	SIO_I2C2_SCL	VCCRAM_1P05		VCCRAM_1P05	VSS		VCC_VCG		VCC_VCG		VCC_VCG	VCC_VCG	VSS
		VCCRAM_1P05		VCCRAM_1P05	VCC_VCG		VCC_VCG		VSS		VCC_VCG	VCC_VCG	VSS
	VSS												
		VSS		VCC_VCG	VCC_VCG		VCC_VCG		VCC_VCG		VCC_VCG	VCC_VCG	VSS
	GPIO_214												
		VSS		VCC_VCG	VCC_VCG		VCC_VCG		VCC_VCG		VCC_VCG	VCC_VCG	VSS
												VSS	
	VCC_VCG		SIO_SPI_2_FS1		SIO_SPI_2_RXD		SIO_SPI_2_FS0		CNV_WGR_D0_N		RSVD		RSVD
												VSS	
	SIO_SPI_0_CLK		SIO_SPI_2_CLK		VSS		SIO_SPI_2_TXD		CNV_WGR_D0_P		RSVD	VSS	RSVD
	SIO_SPI_0_RXD		SIO_SPI_0_FS0		SIO_SPI_2_FS2		VSS		CNV_WT_D1_P		RSVD		RSVD
												VSS	
	SIO_SPI_0_FS1		SIO_SPI_0_TXD		CNV_WT_D0_P		VSS		CNV_WT_D1_N		CLKIN_XTAL_LCP		VSS
	VSS		GPIO_138		CNV_WT_D0_N		VSS		CNV_WGR_CLK_N		CNV_WGR_CLK_P	VSS	GPIO_210
												VSS	
	GPIO_144		NC		CNV_WT_CLK_P		CNV_WT_RCOMP		VSS		CNV_WGR_D1_N		RSM_RST_N
												VSS	
	VCC_VCG		VCC_VCG		CNV_WT_CLK_N		VCC_VCG		VCC_VCG		CNV_WGR_D1_P	VSS	RTC_RST_N
PNL0_BKLTEN	DDI0_HPD	DDI1_HPD	LPC_CLKOUT0	VSS	LPC_AD3	LPC_AD1	LPC_CLKRUN_N	FST_SPI_CS1_N	FST_SPI_CS0_N	FST_SPI_MISO_IO1	FST_SPI_IO3	VSS	SMB_DATA
	EDP_HPD		LPC_SERIRQ		LPC_AD2		LPC_FRAME_N		FST_SPI_MOSI_IO0		FST_SPI_CLK		SMB_CLK
VSS		LPC_CLKOUT1		VSS		LPC_AD0		VSS		FST_SPI_IO2		VSS	

Figure 5-3. Ball Map LPDDR4—Center (26–13)

26	25	24	23	22	21	20	19	18	17	16	15	14	13
MEM_CH1_DQA1		VSS		MEM_CH1_DQA7		MEM_CH1_DQA18		MEM_CH1_DQSA2_P		MEM_CH1_DQA23		VSS	
	MEM_CH1_DQSA0_N		MEM_CH1_DQA5		VSS		MEM_CH1_DQA16		VSS		MEM_CH1_DQA22		MEM_CH1_CKE0A
MEM_CH1_DQA0	VSS	MEM_CH1_DQSA0_P	MEM_CH1_DQA4	MEM_CH1_DQA6	MEM_CH1_DQA19	MEM_CH1_DQA17	VSS	MEM_CH1_DQSA2_N	MEM_CH1_DQA20	MEM_CH1_DQA21	VSS	MEM_CH1_CKE1A	MEM_CH1_CKE0B
	VSS		VSS		MEM_CH1_DQA12		VSS		VSS		MEM_CH1_CLKA_N		VSS
	MEM_CH1_DQSA1_N		MEM_CH1_DQA13		MEM_CH1_DQA15		VSS		MEM_CH1_CLKB_P		MEM_CH1_CLKA_P		NCTF
	MEM_CH1_DQSA1_P		MEM_CH1_DQA14		VSS		VSS		MEM_CH1_CLKB_N		VSS		NCTF
	VSS		VSS		VSS		VSS		VSS		MEM_CH1_RESET_N		NCTF
	VDDQ		MEM_CH1_DQA26		MEM_CH1_DQA24		MEM_CH1_DQA31		MEM_CH1_DQA27		VDDQ		VDDQ
	NCTF		MEM_CH1_DQA25		MEM_CH1_DQA28		MEM_CH1_DQA30		MEM_CH1_DQA29		VSS		VSS
	VSS		VSS		MEM_CH1_DQSA3_N		MEM_CH1_DQSA3_P		VSS		VSS		
											MEM_CH1_DQB7		MEM_CH1_DQB6
	VCCIOA		VSS		VDDQ	VDDQ		VDDQ					
									VSS		MEM_CH1_DQSB0_N		MEM_CH1_DQSB0_P
	VCCIOA		VSS		VDDQ	VDD2_1P2_GLM		VDDQ					
									MEM_CH1_DQB2		MEM_CH1_DQB1		MEM_CH1_DQB5
	VSS		VSS		VSS	VDD2_1P2_GLM		VDD2_1P2_PLL					
	VSS		VSS		VSS	VSS		VDD2_1P2_PLL	VSS		VSS		VSS
	VSS		VCC_1P8V_A		VCC_3P3V_A	VDD2_1P2_USB3		VSS	MDSI_A_DN_1		MDSI_A_DP_1		VSS
	VSS		VCC_1P8V_A		VCC_3P3V_A	VSS		VDD2_1P2_USB2	MDSI_C_DN_0		MDSI_C_DP_0		MDSI_C_CLKP
	VSS		VSS		VDD2_1P2_MPHY	VDD2_1P2_MPHY		VSS		VSS		VSS	
	VSS		VSS		VDD2_1P2_MPHY	VDD2_1P2_MPHY		VSS	MDSI_C_DN_3		MDSI_C_DP_3		EDP_TXN_0
	VSS		VSS		VDD2_1P2_MPHY	VDD2_1P2_AUD_ISH		VDD2_1P2_AUD_ISH	EDP_TXN_1		EDP_TXP_1		VSS
	VSS		VSS		VSS	VDD2_1P2_VNNAON		VDD2_1P2_VNNAON	VSS		VSS		VSS
	VSS		VSS		VSS	VCC_3P3V_A		VCC_3P3V_A					
									EDP_AUXP		EDP_AUXN		NC
	VCC_1P8V_A		VCC_1P8V_A		VCC_1P8V_A	VCC_3P3V_A		VCC_3P3V_A					
									VCC_3P3V_A		NC		VSS
	VCC_1P8V_A		VCC_1P8V_A		VCC_1P8V_A	VCC_3P3V_A		VCC_3P3V_A					
											USB2_DN3		USB2_DP3
	RSVD		AVS_I2S1_SDO		VSS		EMMC_D4		EMMC_D3		VCCRTC_3P3V		
	VSS		AVS_I2S1_MCLK		AVS_I2S1_SDI		EMMC_D0		EMMC_D7		VSS		EMMC_CMD
	RSVD		RSVD		AVS_I2S1_BCLK		VSS		EMMC_D6		EMMC_RCLK		EMMC_RCOMP
	RSVD		VCC_RTC_EXTPAD		AVS_I2S1_WS_SYNC		EMMC_D2		CNV_BRI_RSP		EMMC_D5		EMMC_CLK
	INTRUDER		VSS		VSS		EMMC_D1		CNV_BRI_DT		VSS		VSS
	RTC_TEST_N		RTC_X2		VSS		XTAL_CLKREQ		CNV_RF_RESET_N		USB3_P0_RXP		PCIE_P5_USB3_P2_RXP
	SOC_PWROK		RTC_X1		VSS		CNV_RGI_DT		CNV_RGI_RSP		USB3_P0_RXN		PCIE_P5_USB3_P2_RXN
AVS_I2S0_MCLK	AVS_I2S0_WS_SYNC	AVS_I2S0_SDI	AVS_HDA_WS_SYNC	AVS_HDA_SDO	AVS_HDA_RST_N	AVS_DMIC_CLK_B1	AVS_DMIC_DATA_1	AVS_DMIC_CLK_AB2	OSC_CLK_OUT_1	VSS	USB3_P0_TXN	USB3_P1_TXP	PCIE_P5_USB3_P2_TXN
	AVS_I2S0_BCLK		AVS_I2S0_SDO		AVS_HDA_SDI		AVS_DMIC_CLK_A1		OSC_CLK_OUT_0		USB3_P0_TXP		PCIE_P5_USB3_P2_TXP
SMB_ALERT_N		VSS		AVS_HDA_BCLK		VSS		AVS_DMIC_DATA_2		VSS		USB3_P1_TXN	

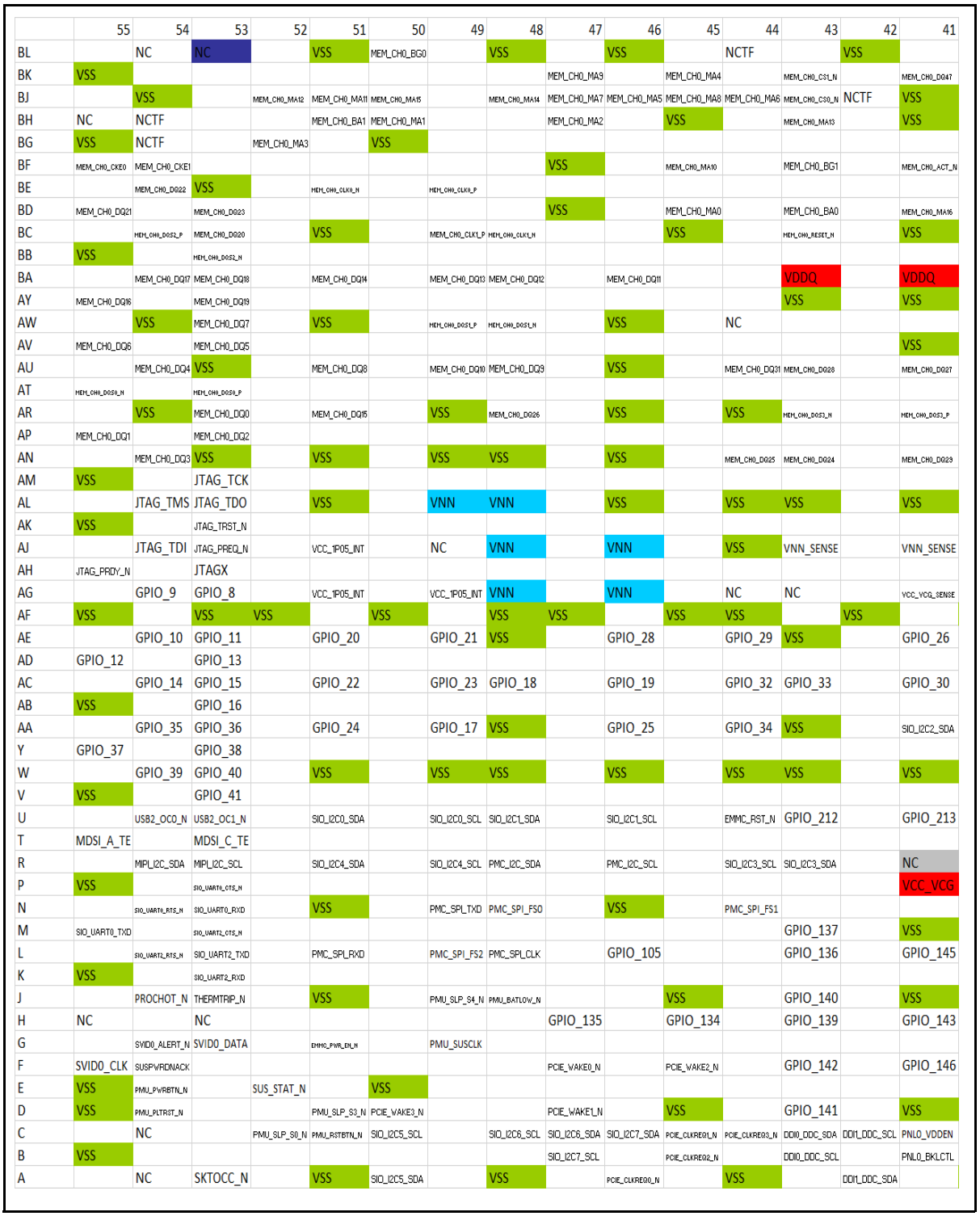
Figure 5-4. Ball Map LPDDR4—(Right 12–1)



12	11	10	9	8	7	6	5	4	3	2	1
MEM_CH1_CKE1B		VSS		VSS		MEM_CH1_CAA2	VSS		NC	NC	
	NCTF		NCTF								VSS
NCTF	NCTF	MEM_CH1_CAA5	MEM_CH1_CAA3	MEM_CH1_CAA4		MEM_CH1_CAA0	MEM_CH1_CAA1	NCTF		VSS	
	VSS		NCTF			MEM_CH1_CAB4	MEM_CH1_CAB3			MEM_CH1_CS0A	NC
						VSS		MEM_CH1_CAB2		MEM_CH1_CS1A	VSS
	NCTF		VSS							MEM_CH1_CS1B	MEM_CH1_CS0B
					MEM_CH1_CAB1		MEM_CH1_CAB0		VSS	MEM_CH1_DQB15	
	MEM_CH1_CAB5		VSS						MEM_CH1_DQB9		MEM_CH1_DQB10
	VSS			NCTF	NCTF		VSS		MEM_CH1_DQB11	MEM_CH1_DQSB1_N	
									MEM_CH1_DQSB1_P		VSS
		MEM_CH1_DQB23		MEM_CH1_DQB17	MEM_CH1_DQB21		MEM_CH1_DQB20		MEM_CH1_DQB13	MEM_CH1_DQB14	
									MEM_CH1_DQB8		MEM_CH1_DQB12
VDD2_1P2_DSI_CSI		VSS		MEM_CH1_DQSB2_N	MEM_CH1_DQSB2_P		VSS		MEM_CH1_DQB27	VSS	
									MEM_CH1_DQB26		MEM_CH1_DQB31
MEM_CH1_DQB3		VSS		MEM_CH1_DQB22	MEM_CH1_DQB18		MEM_CH1_DQB19		VSS	MEM_CH1_DQB25	
									MEM_CH1_DQSB3_N		MEM_CH1_DQSB3_P
VSS		VSS		MEM_CH1_DQB0	VSS		MEM_CH1_DQB16		MEM_CH1_DQB30	VSS	
									MEM_CH1_DQB24		MEM_CH1_DQB29
MEM_CH1_DQB4		VSS		VSS	MDSI_A_DN_0		MDSI_A_DP_0		VSS	MEM_CH1_DQB28	
									MDSI_A_CLKN		VSS
VSS		VSS		VSS	VSS		MDSI_RCOMP		VSS	MDSI_A_CLKP	
									VSS		VSS
MDSI_A_DN_3		MDSI_A_DP_3		VSS	MDSI_A_DP_2		MDSI_A_DN_2		DDI0_TXN_2	DDI0_TXP_2	
									DDI0_TXN_0		DDI0_TXP_0
MDSI_C_CLKN		MDSI_C_DN_1		MDSI_C_DP_1	MDSI_C_DP_2		MDSI_C_DN_2		DDI0_TXN_3	DDI0_TXP_3	
VSS	VSS		VSS	VSS		VSS		VSS	VSS		VSS
EDP_TXP_0		EDP_TXP_2		EDP_TXN_2	EDP_TXN_3		EDP_TXP_3		DDI0_TXN_1	DDI0_TXP_1	
									DDI1_TXN_2		DDI1_TXP_2
DDI0_AUXP		DDI0_AUXN		VSS	DDI1_AUXP		DDI1_AUXN		DDI1_TXN_3	DDI1_TXP_3	
									VSS		VSS
VSS		NC		NC	EDP_RCOMP_N		EDP_RCOMP_P		DDI1_TXN_0	DDI1_TXP_0	
									DDI1_TXP_1		DDI1_TXN_1
NC		VSS		VSS	VSS		VSS		VSS	VSS	
									USB2_VBUS_SNS		USB2_DUALROLE
USB2_RCOMP		USB2_DN7		USB2_DP7	USB2_DP0		USB2_DN0		VSS	OSCIN	
									VSS		OSCOUT
PCIE_CLKOUT0P		PCIE_CLKOUT0N		VSS	PCIE_CLKOUT2P		PCIE_CLKOUT2N		USB2_DN5	USB2_DP5	
									USB2_DN6		USB2_DP6
VSS		PCIE_CLKOUT3N		PCIE_CLKOUT3P	PCIE_CLKOUT1P		PCIE_CLKOUT1N		USB2_DN1	USB2_DP1	
									USB2_DN4		USB2_DP4
		PCIE_REF_CLK_RCOMP		VSS	VSS		VSS		USB2_DN2	USB2_DP2	
									VSS		VSS
	USB3_P1_RXP			VSS	SATA_P0_RXP		SATA_P0_RXN		SATA_P0_TXP	SATA_P0_TXN	
	USB3_P1_RXN		PCIE_P3_USB3_P4_RXP			PCIE_P0_RXN		SATA_P1_USB3_P3_RXP		SATA_P1_USB3_P3_TXN	SATA_P1_USB3_P3_TXP
					PCIE_P0_RXP		SATA_P1_USB3_P3_RXN				
	PCIE_P4_USB3_P3_RXN		PCIE_P3_USB3_P4_RXN			PCIE_P2_RXN		VSS		PCIE_P0_TXN	VSS
					PCIE_P2_RXP		PCIE_P1_RXN			PCIE_P0_TXP	
	PCIE_P4_USB3_P3_RXP		VSS			VSS		PCIE_P1_RXP		DEBUG_P0	DEBUG_P0
VSS	PCIE_P4_USB3_P3_TXP	PCIE_P3_USB3_P4_TXP	PCIE_P2_TXP		PCIE_P1_TXN	PCIE3_RBIAS_EXTRES_RCOMP_P	PCIE3_RBIAS_EXTRES_RCOMP_N		NC	NC	VSS
	PCIE_P4_USB3_P3_TXN		PCIE_P2_TXN							VSS	
VSS		PCIE_P3_USB3_P4_TXN			PCIE_P1_TXP	VSS		NC	VSS		

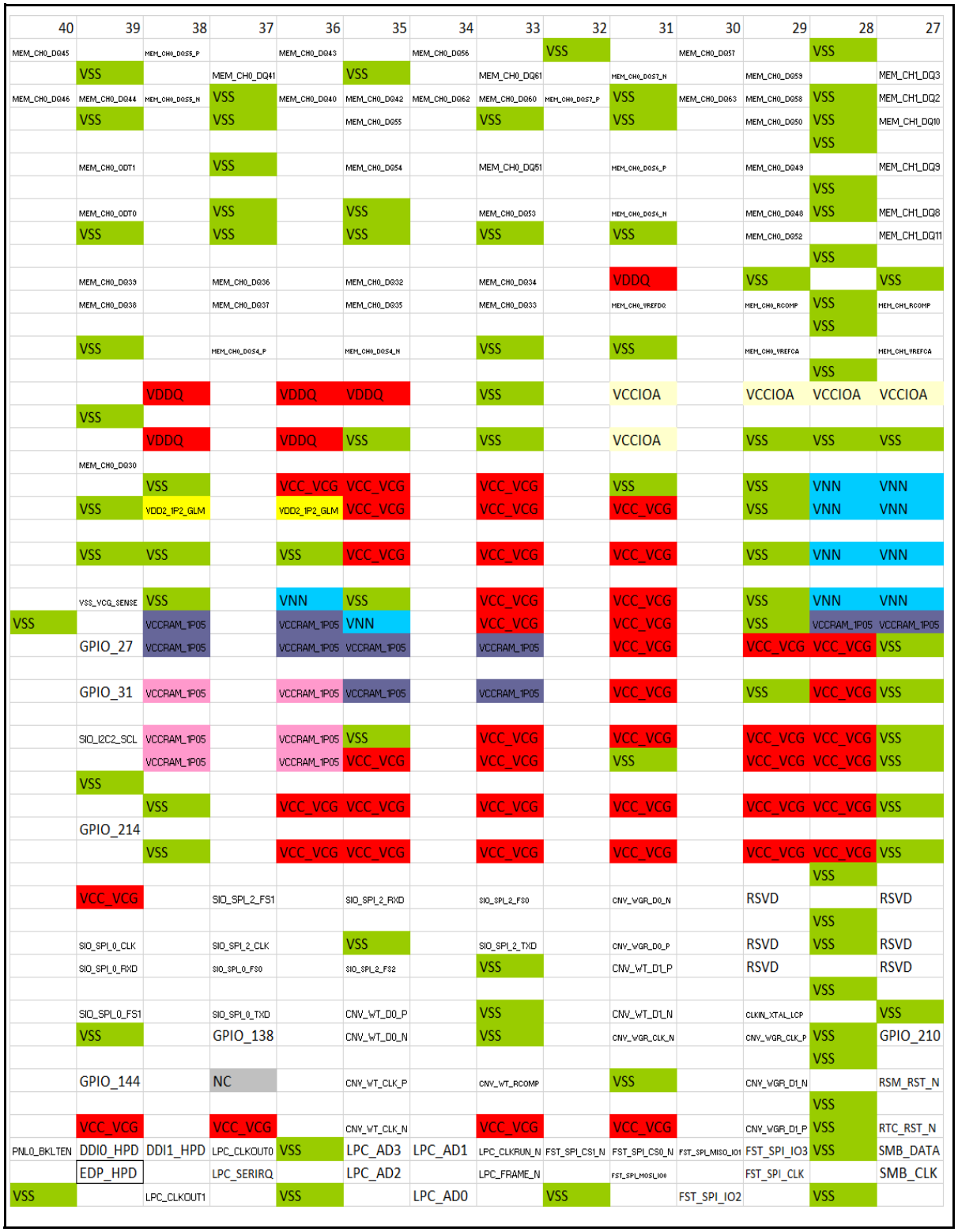
5.2 Ball Map—DDR4

Figure 5-5. Ball Map DDR4—Left (55–41)



	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41
BL		NC	NC		VSS	MEM_CH0_BG0		VSS		VSS		NCTF		VSS	
BK	VSS								MEM_CH0_MA9		MEM_CH0_MA4		MEM_CH0_CS1_N		MEM_CH0_DQ47
BJ		VSS		MEM_CH0_MA12	MEM_CH0_MA11	MEM_CH0_MA15		MEM_CH0_MA14	MEM_CH0_MA7	MEM_CH0_MA5	MEM_CH0_MA8	MEM_CH0_MA6	MEM_CH0_CS0_N	NCTF	VSS
BH	NC	NCTF			MEM_CH0_BA1	MEM_CH0_MA1			MEM_CH0_MA2		VSS		MEM_CH0_MA13		VSS
BG	VSS	NCTF		MEM_CH0_MA3		VSS									
BF	MEM_CH0_CKE0	MEM_CH0_CKE1							VSS		MEM_CH0_MA10		MEM_CH0_BG1		MEM_CH0_ACT_N
BE		MEM_CH0_DQ22	VSS		MEM_CH0_CLK0_N		MEM_CH0_CLK0_P								
BD	MEM_CH0_DQ21		MEM_CH0_DQ23						VSS		MEM_CH0_MA0		MEM_CH0_BA0		MEM_CH0_MA16
BC		MEM_CH0_DQS2_P	MEM_CH0_DQ20		VSS		MEM_CH0_CLK1_P	MEM_CH0_CLK1_N			VSS		MEM_CH0_RESET_N		VSS
BB	VSS		MEM_CH0_DQS2_N												
BA		MEM_CH0_DQ17	MEM_CH0_DQ18		MEM_CH0_DQ14		MEM_CH0_DQ13	MEM_CH0_DQ12		MEM_CH0_DQ11			VDDQ		VDDQ
AY	MEM_CH0_DQ16		MEM_CH0_DQ19										VSS		VSS
AW		VSS	MEM_CH0_DQ7		VSS		MEM_CH0_DQS1_P	MEM_CH0_DQS1_N		VSS		NC			
AV	MEM_CH0_DQ6		MEM_CH0_DQ5												VSS
AU		MEM_CH0_DQ4	VSS		MEM_CH0_DQ8		MEM_CH0_DQ10	MEM_CH0_DQ9		VSS		MEM_CH0_DQ31	MEM_CH0_DQ28		MEM_CH0_DQ27
AT	MEM_CH0_DQS0_N		MEM_CH0_DQS0_P												
AR		VSS	MEM_CH0_DQ0		MEM_CH0_DQ15		VSS	MEM_CH0_DQ26		VSS		VSS	MEM_CH0_DQS3_N		MEM_CH0_DQS3_P
AP	MEM_CH0_DQ1		MEM_CH0_DQ2												
AN		MEM_CH0_DQ3	VSS		VSS		VSS	VSS		VSS		MEM_CH0_DQ25	MEM_CH0_DQ24		MEM_CH0_DQ29
AM	VSS		JTAG_TCK												
AL		JTAG_TMS	JTAG_TDO		VSS		VNN	VNN		VSS		VSS	VSS		VSS
AK	VSS		JTAG_TRST_N												
AJ		JTAG_TDI	JTAG_PREQ_N		VCC_1P05_INT		NC	VNN		VNN		VSS	VNN_SENSE		VNN_SENSE
AH	JTAG_PRDY_N		JTAGX												
AG		GPIO_9	GPIO_8		VCC_1P05_INT		VCC_1P05_INT	VNN		VNN		NC	NC		VCC_VCG_SENSE
AF	VSS		VSS	VSS		VSS		VSS	VSS		VSS	VSS		VSS	
AE		GPIO_10	GPIO_11		GPIO_20		GPIO_21	VSS		GPIO_28		GPIO_29	VSS		GPIO_26
AD	GPIO_12		GPIO_13												
AC		GPIO_14	GPIO_15		GPIO_22		GPIO_23	GPIO_18		GPIO_19		GPIO_32	GPIO_33		GPIO_30
AB	VSS		GPIO_16												
AA		GPIO_35	GPIO_36		GPIO_24		GPIO_17	VSS		GPIO_25		GPIO_34	VSS		SIO_I2C2_SDA
Y	GPIO_37		GPIO_38												
W		GPIO_39	GPIO_40		VSS		VSS	VSS		VSS		VSS	VSS		VSS
V	VSS		GPIO_41												
U		USB2_OC0_N	USB2_OC1_N		SIO_I2C0_SDA		SIO_I2C0_SCL	SIO_I2C1_SDA		SIO_I2C1_SCL		EMMC_RST_N	GPIO_212		GPIO_213
T	MDSI_A_TE		MDSI_C_TE												
R		MIPI_I2C_SDA	MIPI_I2C_SCL		SIO_I2C4_SDA		SIO_I2C4_SCL	PMC_I2C_SDA		PMC_I2C_SCL		SIO_I2C3_SCL	SIO_I2C3_SDA		NC
P	VSS		SIO_UART0_CTS_N												VCC_VCG
N		SIO_UART0_RTS_N	SIO_UART0_RXD		VSS		PMC_SPI_TXD	PMC_SPI_FS0		VSS		PMC_SPI_FS1			
M	SIO_UART0_TXD		SIO_UART2_CTS_N										GPIO_137		VSS
L		SIO_UART2_RTS_N	SIO_UART2_TXD		PMC_SPI_RXD		PMC_SPI_FS2	PMC_SPI_CLK		GPIO_105			GPIO_136		GPIO_145
K	VSS		SIO_UART2_RXD												
J		PROCHOT_N	THERMTRIP_N		VSS		PMU_SLP_S4_N	PMU_BATLOW_N			VSS		GPIO_140		VSS
H	NC		NC						GPIO_135		GPIO_134		GPIO_139		GPIO_143
G		SVID0_ALERT_N	SVID0_DATA		EMMC_PWR_EN_N		PMU_SUSCLK								
F	SVID0_CLK	SUSPWRDNACK							PCIE_WAKE0_N		PCIE_WAKE2_N		GPIO_142		GPIO_146
E	VSS	PMU_PWRBTN_N		SUS_STAT_N		VSS									
D	VSS	PMU_PLTRST_N			PMU_SLP_S3_N	PCIE_WAKE3_N			PCIE_WAKE1_N		VSS		GPIO_141		VSS
C		NC		PMU_SLP_S0_N	PMU_RSTBTN_N	SIO_I2C5_SCL		SIO_I2C6_SCL	SIO_I2C6_SDA	SIO_I2C7_SDA	PCIE_CLKREQ1_N	PCIE_CLKREQ3_N	DDI0_DDC_SDA	DDI1_DDC_SCL	PNL0_VDDEN
B	VSS								SIO_I2C7_SCL		PCIE_CLKREQ2_N		DDI0_DDC_SCL		PNL0_BKLCTL
A		NC	SKTOCC_N		VSS	SIO_I2C5_SDA		VSS		PCIE_CLKREQ0_N		VSS		DDI1_DDC_SDA	

Figure 5-6. Ball Map DDR4—Center (40–27)

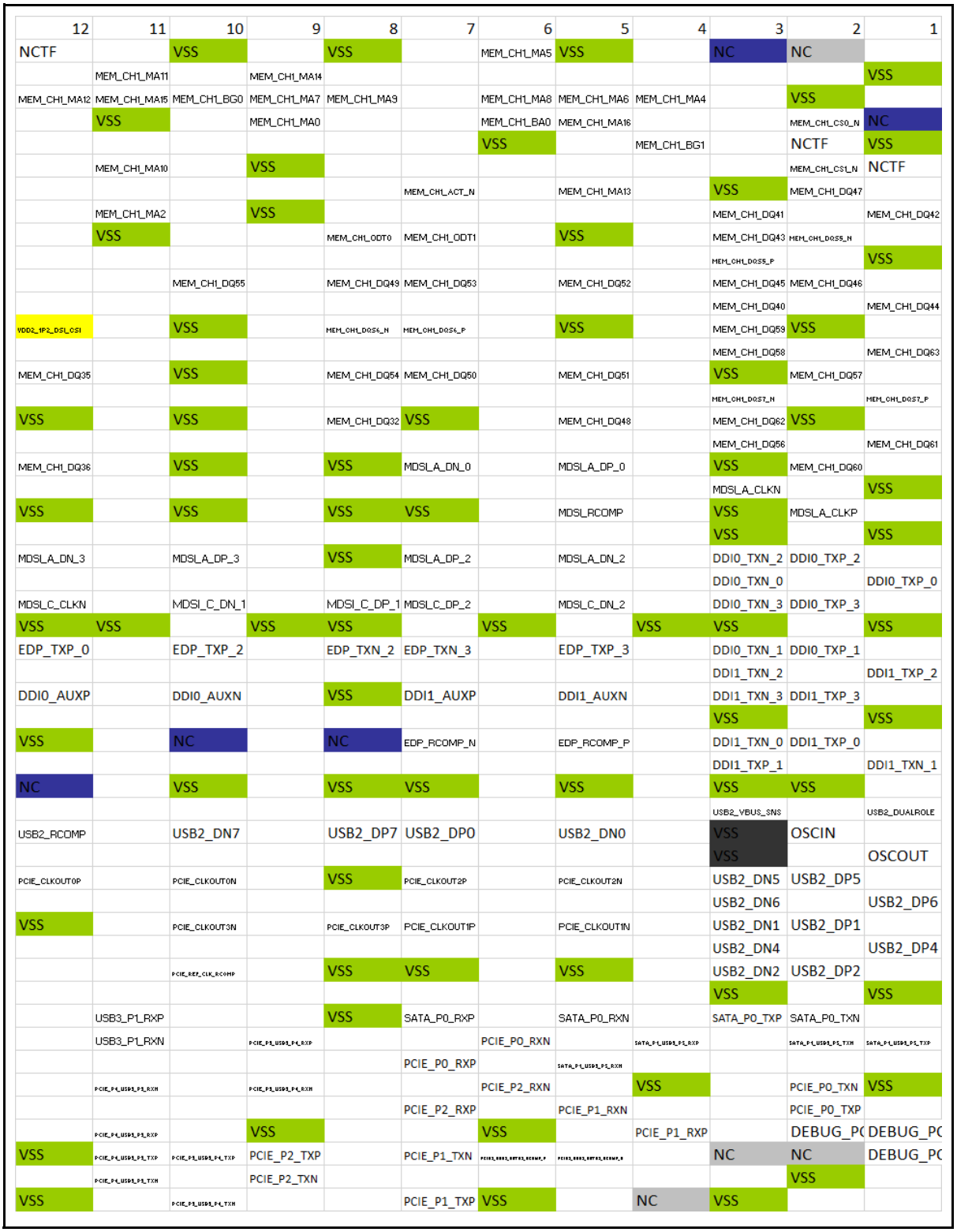


40	39	38	37	36	35	34	33	32	31	30	29	28	27
MEM_CH0_DQ45		MEM_CH0_DQS5_P		MEM_CH0_DQ43		MEM_CH0_DQ56		VSS		MEM_CH0_DQ57		VSS	
	VSS		MEM_CH0_DQ41		VSS		MEM_CH0_DQ61		MEM_CH0_DQS7_N		MEM_CH0_DQ59		MEM_CH1_DQ3
MEM_CH0_DQ46	MEM_CH0_DQ44	MEM_CH0_DQS5_N	VSS	MEM_CH0_DQ40	MEM_CH0_DQ42	MEM_CH0_DQ62	MEM_CH0_DQ60	MEM_CH0_DQS7_P	VSS	MEM_CH0_DQ63	MEM_CH0_DQ58	VSS	MEM_CH1_DQ2
	VSS		VSS		MEM_CH0_DQ55		VSS		VSS		MEM_CH0_DQ50	VSS	MEM_CH1_DQ10
												VSS	
	MEM_CH0_ODT1		VSS		MEM_CH0_DQ54		MEM_CH0_DQ51		MEM_CH0_DQS6_P		MEM_CH0_DQ43		MEM_CH1_DQ9
												VSS	
	MEM_CH0_ODT0		VSS		VSS		MEM_CH0_DQ53		MEM_CH0_DQS6_N		MEM_CH0_DQ48	VSS	MEM_CH1_DQ8
	VSS		VSS		VSS		VSS		VSS		MEM_CH0_DQ52		MEM_CH1_DQ11
												VSS	
	MEM_CH0_DQ39		MEM_CH0_DQ36		MEM_CH0_DQ32		MEM_CH0_DQ34		VDDQ		VSS		VSS
	MEM_CH0_DQ38		MEM_CH0_DQ37		MEM_CH0_DQ35		MEM_CH0_DQ33		MEM_CH0_VREFDQ		MEM_CH0_RCOMP	VSS	MEM_CH1_RCOMP
												VSS	
	VSS		MEM_CH0_DQS4_P		MEM_CH0_DQS4_N		VSS		VSS		MEM_CH0_VREFCA		MEM_CH1_VREFCA
												VSS	
		VDDQ		VDDQ	VDDQ		VSS		VCCIOA		VCCIOA	VCCIOA	VCCIOA
	VSS												
		VDDQ		VDDQ	VSS		VSS		VCCIOA		VSS	VSS	VSS
	MEM_CH0_DQ30												
		VSS		VCC_VCG	VCC_VCG		VCC_VCG		VSS		VSS	VNN	VNN
	VSS	VDD2_1P2_GLM		VDD2_1P2_GLM	VCC_VCG		VCC_VCG		VCC_VCG		VSS	VNN	VNN
	VSS	VSS		VSS	VCC_VCG		VCC_VCG		VCC_VCG		VSS	VNN	VNN
	VSS_VCG_SENSE	VSS		VNN	VSS		VCC_VCG		VCC_VCG		VSS	VNN	VNN
VSS		VCCRAM_1P05		VCCRAM_1P05	VNN		VCC_VCG		VCC_VCG		VSS	VCCRAM_1P05	VCCRAM_1P05
	GPIO_27	VCCRAM_1P05		VCCRAM_1P05	VCCRAM_1P05		VCCRAM_1P05		VCC_VCG		VCC_VCG	VCC_VCG	VSS
	GPIO_31	VCCRAM_1P05		VCCRAM_1P05	VCCRAM_1P05		VCCRAM_1P05		VCC_VCG		VSS	VCC_VCG	VSS
	SIO_I2C2_SCL	VCCRAM_1P05		VCCRAM_1P05	VSS		VCC_VCG		VCC_VCG		VCC_VCG	VCC_VCG	VSS
		VCCRAM_1P05		VCCRAM_1P05	VCC_VCG		VCC_VCG		VSS		VCC_VCG	VCC_VCG	VSS
	VSS												
		VSS		VCC_VCG	VCC_VCG		VCC_VCG		VCC_VCG		VCC_VCG	VCC_VCG	VSS
	GPIO_214												
		VSS		VCC_VCG	VCC_VCG		VCC_VCG		VCC_VCG		VCC_VCG	VCC_VCG	VSS
												VSS	
	VCC_VCG		SIO_SPI_2_FS1		SIO_SPI_2_RXD		SIO_SPI_2_FS0		CNV_WGR_D0_N		RSVD		RSVD
												VSS	
	SIO_SPI_0_CLK		SIO_SPI_2_CLK		VSS		SIO_SPI_2_TXD		CNV_WGR_D0_P		RSVD	VSS	RSVD
	SIO_SPI_0_RXD		SIO_SPI_0_FS0		SIO_SPI_2_FS2		VSS		CNV_WT_D1_P		RSVD		RSVD
												VSS	
	SIO_SPI_0_FS1		SIO_SPI_0_TXD		CNV_WT_D0_P		VSS		CNV_WT_D1_N		CLKIN_XTAL_LCP		VSS
	VSS		GPIO_138		CNV_WT_D0_N		VSS		CNV_WGR_CLK_N		CNV_WGR_CLK_P	VSS	GPIO_210
												VSS	
	GPIO_144		NC		CNV_WT_CLK_P		CNV_WT_RCOMP		VSS		CNV_WGR_D1_N		RSM_RST_N
												VSS	
	VCC_VCG		VCC_VCG		CNV_WT_CLK_N		VCC_VCG		VCC_VCG		CNV_WGR_D1_P	VSS	RTC_RST_N
PNL0_BKLTEN	DDI0_HPD	DDI1_HPD	LPC_CLKOUT0	VSS	LPC_AD3	LPC_AD1	LPC_CLKRUN_N	FST_SPI_CS1_N	FST_SPI_CS0_N	FST_SPI_MISO_IO1	FST_SPI_IO3	VSS	SMB_DATA
	EDP_HPD		LPC_SERIRQ		LPC_AD2		LPC_FRAME_N		FST_SPI_MOSI_IO0		FST_SPI_CLK		SMB_CLK
VSS		LPC_CLKOUT1		VSS		LPC_AD0		VSS		FST_SPI_IO2		VSS	

Figure 5-7. Ball Map DDR4—Center (26–13)

26	25	24	23	22	21	20	19	18	17	16	15	14	13
MEM_CH1_DQ1		VSS		MEM_CH1_DQ7		MEM_CH1_DQ18		MEM_CH1_DQS2_P		MEM_CH1_DQ23		VSS	
	MEM_CH1_DQS0_N		MEM_CH1_DQ5		VSS		MEM_CH1_DQ16		VSS		MEM_CH1_DQ22		MEM_CH1_CKE0
MEM_CH1_DQ0	VSS	MEM_CH1_DQS0_P	MEM_CH1_DQ4	MEM_CH1_DQ6	MEM_CH1_DQ19	MEM_CH1_DQ17	VSS	MEM_CH1_DQS2_N	MEM_CH1_DQ20	MEM_CH1_DQ21	VSS	MEM_CH1_CKE1	NCTF
	VSS		VSS		MEM_CH1_DQ12		VSS		VSS		MEM_CH1_CLK1_N		VSS
	MEM_CH1_DQS1_N		MEM_CH1_DQ13		MEM_CH1_DQ15		VSS		MEM_CH1_CLK0_P		MEM_CH1_CLK1_P		MEM_CH1_BA1
	MEM_CH1_DQS1_P		MEM_CH1_DQ14		VSS		VSS		MEM_CH1_CLK0_N		VSS		MEM_CH1_MA3
	VSS		VSS		VSS		VSS		VSS		MEM_CH1_RESET_N		MEM_CH1_MA1
	VDDQ		MEM_CH1_DQ26		MEM_CH1_DQ24		MEM_CH1_DQ31		MEM_CH1_DQ27		VDDQ		VDDQ
	MEM_CH1_VREFDQ		MEM_CH1_DQ25		MEM_CH1_DQ28		MEM_CH1_DQ30		MEM_CH1_DQ29		VSS		VSS
	VSS		VSS		MEM_CH1_DQS3_N		MEM_CH1_DQS3_P		VSS		VSS		
											MEM_CH1_DQ39		MEM_CH1_DQ38
	VCCIOA		VSS		VDDQ	VDDQ		VDDQ					
									VSS		MEM_CH1_DQS4_N		MEM_CH1_DQS4_P
	VCCIOA		VSS		VDDQ	VDD2_1P2_GLM		VDDQ					
									MEM_CH1_DQ34		MEM_CH1_DQ33		MEM_CH1_DQ37
	VSS		VSS		VSS	VDD2_1P2_GLM		VDD2_1P2_PLL					
	VSS		VSS		VSS	VSS		VDD2_1P2_PLL	VSS		VSS		VSS
	VSS		VCC_1P8V_A		VCC_3P3V_A	VDD2_1P2_USB3		VSS	MDSI_A_DN_1		MDSI_A_DP_1		VSS
	VSS		VCC_1P8V_A		VCC_3P3V_A	VSS		VDD2_1P2_USB2	MDSI_C_DN_0		MDSI_C_DP_0		MDSI_C_CLKP
	VSS		VSS		VDD2_1P2_MPHY	VDD2_1P2_MPHY		VSS		VSS		VSS	
	VSS		VSS		VDD2_1P2_MPHY	VDD2_1P2_MPHY		VSS	MDSI_C_DN_3		MDSI_C_DP_3		EDP_TXN_0
	VSS		VSS		VDD2_1P2_MPHY	VDD2_1P2_AUD_ISH		VDD2_1P2_AUD_ISH	EDP_TXN_1		EDP_TXP_1		VSS
	VSS		VSS		VSS	VDD2_1P2_VNNAON		VDD2_1P2_VNNAON	VSS		VSS		VSS
	VSS		VSS		VSS	VCC_3P3V_A		VCC_3P3V_A					
									EDP_AUXP		EDP_AUXN		NC
	VCC_1P8V_A		VCC_1P8V_A		VCC_1P8V_A	VCC_3P3V_A		VCC_3P3V_A					
									VCC_3P3V_A		NC		VSS
	VCC_1P8V_A		VCC_1P8V_A		VCC_1P8V_A	VCC_3P3V_A		VCC_3P3V_A					
											USB2_DN3		USB2_DP3
	RSVD		AVS_I2S1_SDO		VSS		EMMC_D4		EMMC_D3		VCCRTC_3P3V		
	VSS		AVS_I2S1_MCLK		AVS_I2S1_SDI		EMMC_D0		EMMC_D7		VSS		EMMC_CMD
	RSVD		RSVD		AVS_I2S1_BCLK		VSS		EMMC_D6		EMMC_RCLK		EMMC_RCOMP
	RSVD		VCC_RTC_EXTPAD		AVS_I2S1_WS_SYNC		EMMC_D2		CNV_BRI_RSP		EMMC_D5		EMMC_CLK
	INTRUDER		VSS		VSS		EMMC_D1		CNV_BRI_DT		VSS		VSS
	RTC_TEST_N		RTC_X2		VSS		XTAL_CLKREQ		CNV_RF_RESET_N		USB3_P0_RXP		PCIE_P5_USBP3_P2_RXP
	SOC_PWROK		RTC_X1		VSS		CNV_RGI_DT		CNV_RGI_RSP		USB3_P0_RXN		PCIE_P5_USBP3_P2_RXN
AVS_I2S0_MCLK	AVS_I2S0_WS_SYNC	AVS_I2S0_SDI	AVS_HDA_WS_SYNC	AVS_HDA_SDO	AVS_HDA_RST_N	AVS_DMIC_CLK_B1	AVS_DMIC_DATA_1	AVS_DMIC_CLK_AB2	OSC_CLK_OUT_1	VSS	USB3_P0_TXN	USB3_P1_TXP	PCIE_P5_USBP3_P2_TXN
	AVS_I2S0_BCLK		AVS_I2S0_SDO		AVS_HDA_SDI		AVS_DMIC_CLK_A1		OSC_CLK_OUT_0		USB3_P0_TXP		PCIE_P5_USBP3_P2_TXP
SMB_ALERT_N		VSS		AVS_HDA_BCLK		VSS		AVS_DMIC_DATA_2		VSS		USB3_P1_TXN	

Figure 5-8. Ball Map DDR4—Right (12–1)



12	11	10	9	8	7	6	5	4	3	2	1
NCTF		VSS		VSS		MEM_CH1_MA5	VSS		NC	NC	
	MEM_CH1_MA11		MEM_CH1_MA14								VSS
MEM_CH1_MA12	MEM_CH1_MA15	MEM_CH1_BG0	MEM_CH1_MA7	MEM_CH1_MA3		MEM_CH1_MA8	MEM_CH1_MA6	MEM_CH1_MA4		VSS	
	VSS		MEM_CH1_MA0			MEM_CH1_BA0	MEM_CH1_MA16			MEM_CH1_CS0_N	NC
						VSS		MEM_CH1_BG1		NCTF	VSS
	MEM_CH1_MA10		VSS							MEM_CH1_CS1_N	NCTF
					MEM_CH1_ACT_N		MEM_CH1_MA13		VSS	MEM_CH1_DQ47	
	MEM_CH1_MA2		VSS						MEM_CH1_DQ41		MEM_CH1_DQ42
	VSS			MEM_CH1_ODT0	MEM_CH1_ODT1		VSS		MEM_CH1_DQ43	MEM_CH1_DQS5_N	
									MEM_CH1_DQS5_P		VSS
		MEM_CH1_DQ55		MEM_CH1_DQ49	MEM_CH1_DQ53		MEM_CH1_DQ52		MEM_CH1_DQ45	MEM_CH1_DQ46	
									MEM_CH1_DQ40		MEM_CH1_DQ44
VDD2_1P2_DSI_CSI		VSS		MEM_CH1_DQS6_N	MEM_CH1_DQS6_P		VSS		MEM_CH1_DQ59	VSS	
									MEM_CH1_DQ58		MEM_CH1_DQ63
MEM_CH1_DQ35		VSS		MEM_CH1_DQ54	MEM_CH1_DQ50		MEM_CH1_DQ51		VSS	MEM_CH1_DQ57	
									MEM_CH1_DQS7_N		MEM_CH1_DQS7_P
VSS		VSS		MEM_CH1_DQ32	VSS		MEM_CH1_DQ48		MEM_CH1_DQ62	VSS	
									MEM_CH1_DQ56		MEM_CH1_DQ61
MEM_CH1_DQ36		VSS		VSS	MDSI_A_DN_0		MDSI_A_DP_0		VSS	MEM_CH1_DQ60	
									MDSI_A_CLKN		VSS
VSS		VSS		VSS	VSS		MDSI_RCOMP		VSS	MDSI_A_CLKP	
									VSS		VSS
MDSI_A_DN_3		MDSI_A_DP_3		VSS	MDSI_A_DP_2		MDSI_A_DN_2		DDI0_TXN_2	DDI0_TXP_2	
									DDI0_TXN_0		DDI0_TXP_0
MDSI_C_CLKN		MDSI_C_DN_1		MDSI_C_DP_1	MDSI_C_DP_2		MDSI_C_DN_2		DDI0_TXN_3	DDI0_TXP_3	
VSS	VSS		VSS	VSS		VSS		VSS	VSS		VSS
EDP_TXP_0		EDP_TXP_2		EDP_TXN_2	EDP_TXN_3		EDP_TXP_3		DDI0_TXN_1	DDI0_TXP_1	
									DDI1_TXN_2		DDI1_TXP_2
DDI0_AUXP		DDI0_AUXN		VSS	DDI1_AUXP		DDI1_AUXN		DDI1_TXN_3	DDI1_TXP_3	
									VSS		VSS
VSS		NC		NC	EDP_RCOMP_N		EDP_RCOMP_P		DDI1_TXN_0	DDI1_TXP_0	
									DDI1_TXP_1		DDI1_TXN_1
NC		VSS		VSS	VSS		VSS		VSS	VSS	
									USB2_VBUS_SNS		USB2_DUALROLE
USB2_RCOMP		USB2_DN7		USB2_DP7	USB2_DP0		USB2_DN0		VSS	OSCIN	
									VSS		OSCOUT
PCIE_CLKOUT0P		PCIE_CLKOUT0N		VSS	PCIE_CLKOUT2P		PCIE_CLKOUT2N		USB2_DN5	USB2_DP5	
									USB2_DN6		USB2_DP6
VSS		PCIE_CLKOUT3N		PCIE_CLKOUT3P	PCIE_CLKOUT1P		PCIE_CLKOUT1N		USB2_DN1	USB2_DP1	
									USB2_DN4		USB2_DP4
		PCIE_REF_CLK_RCOMP		VSS	VSS		VSS		USB2_DN2	USB2_DP2	
									VSS		VSS
	USB3_P1_RXP			VSS	SATA_P0_RXP		SATA_P0_RXN		SATA_P0_TXP	SATA_P0_TXN	
	USB3_P1_RXN		PCIE_P3_USB3_P4_RXP			PCIE_P0_RXN		SATA_P1_USB3_P3_RXP		SATA_P1_USB3_P3_TXN	SATA_P1_USB3_P3_TXP
					PCIE_P0_RXP		SATA_P1_USB3_P3_RXN				
	PCIE_P4_USB3_P3_RXN		PCIE_P3_USB3_P4_RXN			PCIE_P2_RXN		VSS		PCIE_P0_TXN	VSS
					PCIE_P2_RXP		PCIE_P1_RXN			PCIE_P0_TXP	
	PCIE_P4_USB3_P3_RXP		VSS			VSS		PCIE_P1_RXP		DEBUG_P(	DEBUG_P(
VSS	PCIE_P4_USB3_P3_TXP	PCIE_P3_USB3_P4_TXP	PCIE_P2_TXP		PCIE_P1_TXN	PCIE3_RBIAS_SATA3_RCOMP_P	PCIE3_RBIAS_SATA3_RCOMP_N		NC	NC	DEBUG_P(
	PCIE_P4_USB3_P3_TXN		PCIE_P2_TXN							VSS	
VSS		PCIE_P3_USB3_P4_TXN			PCIE_P1_TXP	VSS		NC	VSS		

5.3 SoC Pin List Numbers and Locations—DDR4 and LPDDR4

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 1 of 29)

Ball#	DDR4	LPDDR4
B19	AVS_DMIC_CLK_A1	AVS_DMIC_CLK_A1J25
C18	AVS_DMIC_CLK_AB2	AVS_DMIC_CLK_AB2
C20	AVS_DMIC_CLK_B1	AVS_DMIC_CLK_B1
C19	AVS_DMIC_DATA_1	AVS_DMIC_DATA_1
A18	AVS_DMIC_DATA_2	AVS_DMIC_DATA_2
A22	AVS_HDA_BCLK	AVS_HDA_BCLK
C21	AVS_HDA_RST_N	AVS_HDA_RST_N
B21	AVS_HDA_SDI	AVS_HDA_SDI
C22	AVS_HDA_SDO	AVS_HDA_SDO
C23	AVS_HDA_WS_SYNC	AVS_HDA_WS_SYNC
B25	AVS_I2S0_BCLK	AVS_I2S0_BCLK
C26	AVS_I2S0_MCLK	AVS_I2S0_MCLK
C24	AVS_I2S0_SDI	AVS_I2S0_SDI
B23	AVS_I2S0_SDO	AVS_I2S0_SDO
C25	AVS_I2S0_WS_SYNC	AVS_I2S0_WS_SYNC
L21	AVS_I2S1_BCLK	AVS_I2S1_BCLK
M23	AVS_I2S1_MCLK	AVS_I2S1_MCLK
M21	AVS_I2S1_SDI	AVS_I2S1_SDI
P23	AVS_I2S1_SDO	AVS_I2S1_SDO
J21	AVS_I2S1_WS_SYNC	AVS_I2S1_WS_SYNC
J29	CLKIN_XTAL_LCP	CLKIN_XTAL_LCP
H17	CNV_BRI_DT	CNV_BRI_DT
J17	CNV_BRI_RSP	CNV_BRI_RSP
F17	CNV_RF_RESET_N	CNV_RF_RESET_N
D19	CNV_RGI_DT	CNV_RGI_DT
D17	CNV_RGI_RSP	CNV_RGI_RSP
H31	CNV_WGR_CLK_N	CNV_WGR_CLK_N
H29	CNV_WGR_CLK_P	CNV_WGR_CLK_P
P31	CNV_WGR_D0_N	CNV_WGR_D0_N
M31	CNV_WGR_D0_P	CNV_WGR_D0_P
F29	CNV_WGR_D1_N	CNV_WGR_D1_N
D29	CNV_WGR_D1_P	CNV_WGR_D1_P
D35	CNV_WT_CLK_N	CNV_WT_CLK_N
F35	CNV_WT_CLK_P	CNV_WT_CLK_P
H35	CNV_WT_D0_N	CNV_WT_D0_N
J35	CNV_WT_D0_P	CNV_WT_D0_P

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 2 of 29)

Ball#	DDR4	LPDDR4
J31	CNV_WT_D1_N	CNV_WT_D1_N
L31	CNV_WT_D1_P	CNV_WT_D1_P
F33	CNV_WT_RCOMP	CNV_WT_RCOMP
AC10	DDI0_AUXN	DDI0_AUXN
AC12	DDI0_AUXP	DDI0_AUXP
B43	DDI0_DDC_SCL	DDI0_DDC_SCL
C43	DDI0_DDC_SDA	DDI0_DDC_SDA
AH3	DDI0_TXN_0	DDI0_TXN_0
AE3	DDI0_TXN_1	DDI0_TXN_1
AJ3	DDI0_TXN_2	DDI0_TXN_2
AG3	DDI0_TXN_3	DDI0_TXN_3
AH1	DDI0_TXP_0	DDI0_TXP_0
AE2	DDI0_TXP_1	DDI0_TXP_1
AJ2	DDI0_TXP_2	DDI0_TXP_2
AG2	DDI0_TXP_3	DDI0_TXP_3
AC5	DDI1_AUXN	DDI1_AUXN
AC7	DDI1_AUXP	DDI1_AUXP
C42	DDI1_DDC_SCL	DDI1_DDC_SCL
A42	DDI1_DDC_SDA	DDI1_DDC_SDA
AA3	DDI1_TXN_0	DDI1_TXN_0
Y1	DDI1_TXN_1	DDI1_TXN_1
AD3	DDI1_TXN_2	DDI1_TXN_2
AC3	DDI1_TXN_3	DDI1_TXN_3
AA2	DDI1_TXP_0	DDI1_TXP_0
Y3+	DDI1_TXP_1	DDI1_TXP_1
AD1	DDI1_TXP_2	DDI1_TXP_2
AC2	DDI1_TXP_3	DDI1_TXP_3
W15	EDP_AUXN	EDP_AUXN
W17	EDP_AUXP	EDP_AUXP
AA7	EDP_RCOMP_N	EDP_RCOMP_N
AA5	EDP_RCOMP_P	EDP_RCOMP_P
AE13	EDP_TXN_0	EDP_TXN_0
AC17	EDP_TXN_1	EDP_TXN_1
AE8	EDP_TXN_2	EDP_TXN_2
AE7	EDP_TXN_3	EDP_TXN_3
AE12	EDP_TXP_0	EDP_TXP_0
AC15	EDP_TXP_1	EDP_TXP_1

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 3 of 29)

Ball#	DDR4	LPDDR4
AE10	EDP_TXP_2	EDP_TXP_2
AE5	EDP_TXP_3	EDP_TXP_3
J13	EMMC_CLK	EMMC_CLK
M13	EMMC_CMD	EMMC_CMD
M19	EMMC_D0	EMMC_D0
H19	EMMC_D1	EMMC_D1
J19	EMMC_D2	EMMC_D2
P17	EMMC_D3	EMMC_D3
P19	EMMC_D4	EMMC_D4
J15	EMMC_D5	EMMC_D5
L17	EMMC_D6	EMMC_D6
M17	EMMC_D7	EMMC_D7
G51	EMMC_PWR_EN_N	EMMC_PWR_EN_N
L15	EMMC_RCLK	EMMC_RCLK
L13	EMMC_RCOMP	EMMC_RCOMP
U44	EMMC_RST_N	EMMC_RST_N
B29	FST_SPI_CLK	FST_SPI_CLK
C31	FST_SPI_CS0_N	FST_SPI_CS0_N
C32	FST_SPI_CS1_N	FST_SPI_CS1_N
A30	FST_SPI_IO2	FST_SPI_IO2
C29	FST_SPI_IO3	FST_SPI_IO3
C30	FST_SPI_MISO_IO1	FST_SPI_MISO_IO1
B31	FST_SPI_MOSI_IO0	FST_SPI_MOSI_IO0
AE54	GPIO_10	GPIO_10
L46	GPIO_105	GPIO_105
AE53	GPIO_11	GPIO_11
AD55	GPIO_12	GPIO_12
AD53	GPIO_13	GPIO_13
H45	GPIO_134	GPIO_134
H47	GPIO_135	GPIO_135
L43	GPIO_136	GPIO_136
M43	GPIO_137	GPIO_137
H37	GPIO_138	GPIO_138
H43	GPIO_139	GPIO_139
AC54	GPIO_14	GPIO_14
J43	GPIO_140	GPIO_140
D43	GPIO_141	GPIO_141
F43	GPIO_142	GPIO_142

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 4 of 29)

Ball#	DDR4	LPDDR4
H41	GPIO_143	GPIO_143
F39	GPIO_144	GPIO_144
L41	GPIO_145	GPIO_145
F41	GPIO_146	GPIO_146
AC53	GPIO_15	GPIO_15
AB53	GPIO_16	GPIO_16
AA49	GPIO_17	GPIO_17
AC48	GPIO_18	GPIO_18
AC46	GPIO_19	GPIO_19
AE51	GPIO_20	GPIO_20
AE49	GPIO_21	GPIO_21
H27	GPIO_210	GPIO_210
U43	GPIO_212	GPIO_212
U41	GPIO_213	GPIO_213
U39	GPIO_214	GPIO_214
AC51	GPIO_22	GPIO_22
AC49	GPIO_23	GPIO_23
AA51	GPIO_24	GPIO_24
AA46	GPIO_25	GPIO_25
AE41	GPIO_26	GPIO_26
AE39	GPIO_27	GPIO_27
AE46	GPIO_28	GPIO_28
AE44	GPIO_29	GPIO_29
AC41	GPIO_30	GPIO_30
AC39	GPIO_31	GPIO_31
AC44	GPIO_32	GPIO_32
AC43	GPIO_33	GPIO_33
AA44	GPIO_34	GPIO_34
AA54	GPIO_35	GPIO_35
AA53	GPIO_36	GPIO_36
Y55	GPIO_37	GPIO_37
Y53	GPIO_38	GPIO_38
W54	GPIO_39	GPIO_39
W53	GPIO_40	GPIO_40
V53	GPIO_41	GPIO_41
AG53	GPIO_8	GPIO_8
AG54	GPIO_9	GPIO_9
C39	DDI0_HPD	DDI0_HPD
C38	DDI1_HPD	DDI1_HPD

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 5 of 29)

Ball#	DDR4	LPDDR4
B39	EDP_HPD	EDP_HPD
H25	INTRUDER	INTRUDER
AH55	JTAG_PRDY_N	JTAG_PRDY_N
AJ53	JTAG_PREQ_N	JTAG_PREQ_N
AM53	JTAG_TCK	JTAG_TCK
AJ54	JTAG_TDI	JTAG_TDI
AL53	JTAG_TDO	JTAG_TDO
AL54	JTAG_TMS	JTAG_TMS
AK53	JTAG_TRST_N	JTAG_TRST_N
AH53	JTAGX	JTAGX
A34	LPC_AD0	LPC_AD0
C34	LPC_AD1	LPC_AD1
B35	LPC_AD2	LPC_AD2
C35	LPC_AD3	LPC_AD3
C37	LPC_CLKOUT0	LPC_CLKOUT0
A38	LPC_CLKOUT1	LPC_CLKOUT1
C33	LPC_CLKRUN_N	LPC_CLKRUN_N
B33	LPC_FRAME_N	LPC_FRAME_N
B37	LPC_SERIRQ	LPC_SERIRQ
AM3	MDSI_A_CLKN	MDSI_A_CLKN
AL2	MDSI_A_CLKP	MDSI_A_CLKP
AN7	MDSI_A_DN_0	MDSI_A_DN_0
AJ17	MDSI_A_DN_1	MDSI_A_DN_1
AJ5	MDSI_A_DN_2	MDSI_A_DN_2
AJ12	MDSI_A_DN_3	MDSI_A_DN_3
AN5	MDSI_A_DP_0	MDSI_A_DP_0
AJ15	MDSI_A_DP_1	MDSI_A_DP_1
AJ7	MDSI_A_DP_2	MDSI_A_DP_2
AJ10	MDSI_A_DP_3	MDSI_A_DP_3
T55	MDSI_A_TE	MDSI_A_TE
AG12	MDSI_C_CLKN	MDSI_C_CLKN
AG13	MDSI_C_CLKP	MDSI_C_CLKP
AG17	MDSI_C_DN_0	MDSI_C_DN_0
AG10	MDSI_C_DN_1	MDSI_C_DN_1
AG5	MDSI_C_DN_2	MDSI_C_DN_2
AE17	MDSI_C_DN_3	MDSI_C_DN_3
AG15	MDSI_C_DP_0	MDSI_C_DP_0

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 6 of 29)

Ball#	DDR4	LPDDR4
AG8	MDSI_C_DP_1	MDSI_C_DP_1
AG7	MDSI_C_DP_2	MDSI_C_DP_2
AE15	MDSI_C_DP_3	MDSI_C_DP_3
T53	MDSI_C_TE	MDSI_C_TE
AL5	MDSI_RCOMP	MDSI_RCOMP
BF41	MEM_CH0_ACT_N	MEM_CH0_CAB1
BD43	MEM_CH0_BA0	MEM_CH0_CAB4
BH51	MEM_CH0_BA1	NCTF
BL50	MEM_CH0_BG0	MEM_CH0_CAA5
BF43	MEM_CH0_BG1	MEM_CH0_CAB2
BF55	MEM_CH0_CKE0	MEM_CH0_CKE0A
BF54	MEM_CH0_CKE1	MEM_CH0_CKE1A
BE51	MEM_CH0_CLK0_N	MEM_CH0_CLKB_N
BE49	MEM_CH0_CLK0_P	MEM_CH0_CLKB_P
BC48	MEM_CH0_CLK1_N	MEM_CH0_CLKA_N
BC49	MEM_CH0_CLK1_P	MEM_CH0_CLKA_P
BJ43	MEM_CH0_CS0_N	MEM_CH0_CS0A
BK43	MEM_CH0_CS1_N	MEM_CH0_CS1B
AR53	MEM_CH0_DQ0	MEM_CH0_DQA0
AP55	MEM_CH0_DQ1	MEM_CH0_DQA1
AU49	MEM_CH0_DQ10	MEM_CH0_DQA10
BA46	MEM_CH0_DQ11	MEM_CH0_DQA11
BA48	MEM_CH0_DQ12	MEM_CH0_DQA12
BA49	MEM_CH0_DQ13	MEM_CH0_DQA13
BA51	MEM_CH0_DQ14	MEM_CH0_DQA14
AR51	MEM_CH0_DQ15	MEM_CH0_DQA15
AY55	MEM_CH0_DQ16	MEM_CH0_DQA16
BA54	MEM_CH0_DQ17	MEM_CH0_DQA17
BA53	MEM_CH0_DQ18	MEM_CH0_DQA18
AY53	MEM_CH0_DQ19	MEM_CH0_DQA19
AP53	MEM_CH0_DQ2	MEM_CH0_DQA2
BC53	MEM_CH0_DQ20	MEM_CH0_DQA20
BD55	MEM_CH0_DQ21	MEM_CH0_DQA21
BE54	MEM_CH0_DQ22	MEM_CH0_DQA22
BD53	MEM_CH0_DQ23	MEM_CH0_DQA23
AN43	MEM_CH0_DQ24	MEM_CH0_DQA24

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 7 of 29)

Ball#	DDR4	LPDDR4
AN44	MEM_CH0_DQ25	MEM_CH0_DQA25
AR48	MEM_CH0_DQ26	MEM_CH0_DQA26
AU41	MEM_CH0_DQ27	MEM_CH0_DQA27
AU43	MEM_CH0_DQ28	MEM_CH0_DQA28
AN41	MEM_CH0_DQ29	MEM_CH0_DQA29
AN54	MEM_CH0_DQ3	MEM_CH0_DQA3
AN39	MEM_CH0_DQ30	MEM_CH0_DQA30
AU44	MEM_CH0_DQ31	MEM_CH0_DQA31
BA35	MEM_CH0_DQ32	MEM_CH0_DQB0
AY33	MEM_CH0_DQ33	MEM_CH0_DQB1
BA33	MEM_CH0_DQ34	MEM_CH0_DQB2
AY35	MEM_CH0_DQ35	MEM_CH0_DQB3
BA37	MEM_CH0_DQ36	MEM_CH0_DQB4
AY37	MEM_CH0_DQ37	MEM_CH0_DQB5
AY39	MEM_CH0_DQ38	MEM_CH0_DQB6
BA39	MEM_CH0_DQ39	MEM_CH0_DQB7
AU54	MEM_CH0_DQ4	MEM_CH0_DQA4
BJ36	MEM_CH0_DQ40	MEM_CH0_DQB8
BK37	MEM_CH0_DQ41	MEM_CH0_DQB9
BJ35	MEM_CH0_DQ42	MEM_CH0_DQB10
BL36	MEM_CH0_DQ43	MEM_CH0_DQB11
BJ39	MEM_CH0_DQ44	MEM_CH0_DQB12
BL40	MEM_CH0_DQ45	MEM_CH0_DQB13
BJ40	MEM_CH0_DQ46	MEM_CH0_DQB14
BK41	MEM_CH0_DQ47	MEM_CH0_DQB15
BD29	MEM_CH0_DQ48	MEM_CH0_DQB16
BF29	MEM_CH0_DQ49	MEM_CH0_DQB17
AV53	MEM_CH0_DQ5	MEM_CH0_DQA5
BH29	MEM_CH0_DQ50	MEM_CH0_DQB18
BF33	MEM_CH0_DQ51	MEM_CH0_DQB19
BC29	MEM_CH0_DQ52	MEM_CH0_DQB20
BD33	MEM_CH0_DQ53	MEM_CH0_DQB21
BF35	MEM_CH0_DQ54	MEM_CH0_DQB22
BH35	MEM_CH0_DQ55	MEM_CH0_DQB23
BL34	MEM_CH0_DQ56	MEM_CH0_DQB24
BL30	MEM_CH0_DQ57	MEM_CH0_DQB25

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 8 of 29)

Ball#	DDR4	LPDDR4
BJ29	MEM_CH0_DQ58	MEM_CH0_DQB26
BK29	MEM_CH0_DQ59	MEM_CH0_DQB27
AV55	MEM_CH0_DQ6	MEM_CH0_DQA6
BJ33	MEM_CH0_DQ60	MEM_CH0_DQB28
BK33	MEM_CH0_DQ61	MEM_CH0_DQB29
BJ34	MEM_CH0_DQ62	MEM_CH0_DQB30
BJ30	MEM_CH0_DQ63	MEM_CH0_DQB31
AW53	MEM_CH0_DQ7	MEM_CH0_DQA7
AU51	MEM_CH0_DQ8	MEM_CH0_DQA8
AU48	MEM_CH0_DQ9	MEM_CH0_DQA9
AT55	MEM_CH0_DQS0_N	MEM_CH0_DQSA0_N
AT53	MEM_CH0_DQS0_P	MEM_CH0_DQSA0_P
AW48	MEM_CH0_DQS1_N	MEM_CH0_DQSA1_N
AW49	MEM_CH0_DQS1_P	MEM_CH0_DQSA1_P
BB53	MEM_CH0_DQS2_N	MEM_CH0_DQSA2_N
BC54	MEM_CH0_DQS2_P	MEM_CH0_DQSA2_P
AR43	MEM_CH0_DQS3_N	MEM_CH0_DQSA3_N
AR41	MEM_CH0_DQS3_P	MEM_CH0_DQSA3_P
AV35	MEM_CH0_DQS4_N	MEM_CH0_DQSB0_N
AV37	MEM_CH0_DQS4_P	MEM_CH0_DQSB0_P
BJ38	MEM_CH0_DQS5_N	MEM_CH0_DQSB1_N
BL38	MEM_CH0_DQS5_P	MEM_CH0_DQSB1_P
BD31	MEM_CH0_DQS6_N	MEM_CH0_DQSB2_N
BF31	MEM_CH0_DQS6_P	MEM_CH0_DQSB2_P
BK31	MEM_CH0_DQS7_N	MEM_CH0_DQSB3_N
BJ32	MEM_CH0_DQS7_P	MEM_CH0_DQSB3_P
BD45	MEM_CH0_MA0	NCTF
BH50	MEM_CH0_MA1	NCTF
BF45	MEM_CH0_MA10	NCTF
BJ51	MEM_CH0_MA11	NCTF
BJ52	MEM_CH0_MA12	NCTF
BH43	MEM_CH0_MA13	MEM_CH0_CAB0
BJ48	MEM_CH0_MA14	NCTF
BJ50	MEM_CH0_MA15	NCTF
BD41	MEM_CH0_MA16	MEM_CH0_CAB3
BH47	MEM_CH0_MA2	MEM_CH0_CAB5

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 9 of 29)

Ball#	DDR4	LPDDR4
BG52	MEM_CH0_MA3	NCTF
BK45	MEM_CH0_MA4	NCTF
BJ46	MEM_CH0_MA5	MEM_CH0_CAA2
BJ44	MEM_CH0_MA6	MEM_CH0_CAA1
BJ47	MEM_CH0_MA7	MEM_CH0_CAA3
BJ45	MEM_CH0_MA8	MEM_CH0_CAA0
BK47	MEM_CH0_MA9	MEM_CH0_CAA4
BD39	MEM_CH0_ODT0	NCTF
BF39	MEM_CH0_ODT1	NCTF
AY29	MEM_CH0_RCOMP	MEM_CH0_RCOMP
BC43	MEM_CH0_RESET_N	MEM_CH0_RESET_N
AV29	MEM_CH0_VREFCA	NCTF
AY31	MEM_CH0_VREFDQ	NCTF
BE7	MEM_CH1_ACT_N	MEM_CH1_CAB1
BH6	MEM_CH1_BA0	MEM_CH1_CAB4
BF13	MEM_CH1_BA1	NCTF
BJ10	MEM_CH1_BG0	MEM_CH1_CAA5
BG4	MEM_CH1_BG1	MEM_CH1_CAB2
BK13	MEM_CH1_CKE0	MEM_CH1_CKE0A
BJ14	MEM_CH1_CKE1	MEM_CH1_CKE1A
BD17	MEM_CH1_CLK0_N	MEM_CH1_CLKB_N
BF17	MEM_CH1_CLK0_P	MEM_CH1_CLKB_P
BH15	MEM_CH1_CLK1_N	MEM_CH1_CLKA_N
BF15	MEM_CH1_CLK1_P	MEM_CH1_CLKA_P
BH2	MEM_CH1_CS0_N	MEM_CH1_CS0A
BF2	MEM_CH1_CS1_N	MEM_CH1_CS1B
BJ26	MEM_CH1_DQ0	MEM_CH1_DQA0
BL26	MEM_CH1_DQ1	MEM_CH1_DQA1
BH27	MEM_CH1_DQ10	MEM_CH1_DQA10
BC27	MEM_CH1_DQ11	MEM_CH1_DQA11
BH21	MEM_CH1_DQ12	MEM_CH1_DQA12
BF23	MEM_CH1_DQ13	MEM_CH1_DQA13
BD23	MEM_CH1_DQ14	MEM_CH1_DQA14
BF21	MEM_CH1_DQ15	MEM_CH1_DQA15
BK19	MEM_CH1_DQ16	MEM_CH1_DQA16
BJ20	MEM_CH1_DQ17	MEM_CH1_DQA17

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 10 of 29)

Ball#	DDR4	LPDDR4
BL20	MEM_CH1_DQ18	MEM_CH1_DQA18
BJ21	MEM_CH1_DQ19	MEM_CH1_DQA19
BJ27	MEM_CH1_DQ2	MEM_CH1_DQA2
BJ17	MEM_CH1_DQ20	MEM_CH1_DQA20
BJ16	MEM_CH1_DQ21	MEM_CH1_DQA21
BK15	MEM_CH1_DQ22	MEM_CH1_DQA22
BL16	MEM_CH1_DQ23	MEM_CH1_DQA23
BA21	MEM_CH1_DQ24	MEM_CH1_DQA24
AY23	MEM_CH1_DQ25	MEM_CH1_DQA25
BA23	MEM_CH1_DQ26	MEM_CH1_DQA26
BA17	MEM_CH1_DQ27	MEM_CH1_DQA27
AY21	MEM_CH1_DQ28	MEM_CH1_DQA28
AY17	MEM_CH1_DQ29	MEM_CH1_DQA29
BK27	MEM_CH1_DQ3	MEM_CH1_DQA3
AY19	MEM_CH1_DQ30	MEM_CH1_DQA30
BA19	MEM_CH1_DQ31	MEM_CH1_DQA31
AR8	MEM_CH1_DQ32	MEM_CH1_DQB0
AN15	MEM_CH1_DQ33	MEM_CH1_DQB1
AN17	MEM_CH1_DQ34	MEM_CH1_DQB2
AU12	MEM_CH1_DQ35	MEM_CH1_DQB3
AN12	MEM_CH1_DQ36	MEM_CH1_DQB4
AN13	MEM_CH1_DQ37	MEM_CH1_DQB5
AU13	MEM_CH1_DQ38	MEM_CH1_DQB6
AU15	MEM_CH1_DQ39	MEM_CH1_DQB7
BJ23	MEM_CH1_DQ4	MEM_CH1_DQA4
AY3	MEM_CH1_DQ40	MEM_CH1_DQB8
BD3	MEM_CH1_DQ41	MEM_CH1_DQB9
BD1	MEM_CH1_DQ42	MEM_CH1_DQB10
BC3	MEM_CH1_DQ43	MEM_CH1_DQB11
AY1	MEM_CH1_DQ44	MEM_CH1_DQB12
BA3	MEM_CH1_DQ45	MEM_CH1_DQB13
BA2	MEM_CH1_DQ46	MEM_CH1_DQB14
BE2	MEM_CH1_DQ47	MEM_CH1_DQB15
AR5	MEM_CH1_DQ48	MEM_CH1_DQB16
BA8	MEM_CH1_DQ49	MEM_CH1_DQB17
BK23	MEM_CH1_DQ5	MEM_CH1_DQA5

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 11 of 29)

Ball#	DDR4	LPDDR4
AU7	MEM_CH1_DQ50	MEM_CH1_DQB18
AU5	MEM_CH1_DQ51	MEM_CH1_DQB19
BA5	MEM_CH1_DQ52	MEM_CH1_DQB20
BA7	MEM_CH1_DQ53	MEM_CH1_DQB21
AU8	MEM_CH1_DQ54	MEM_CH1_DQB22
BA10	MEM_CH1_DQ55	MEM_CH1_DQB23
AP3	MEM_CH1_DQ56	MEM_CH1_DQB24
AU2	MEM_CH1_DQ57	MEM_CH1_DQB25
AV3	MEM_CH1_DQ58	MEM_CH1_DQB26
AW3	MEM_CH1_DQ59	MEM_CH1_DQB27
BJ22	MEM_CH1_DQ6	MEM_CH1_DQA6
AN2	MEM_CH1_DQ60	MEM_CH1_DQB28
AP1	MEM_CH1_DQ61	MEM_CH1_DQB29
AR3	MEM_CH1_DQ62	MEM_CH1_DQB30
AV1	MEM_CH1_DQ63	MEM_CH1_DQB31
BL22	MEM_CH1_DQ7	MEM_CH1_DQA7
BD27	MEM_CH1_DQ8	MEM_CH1_DQA8
BF27	MEM_CH1_DQ9	MEM_CH1_DQA9
BK25	MEM_CH1_DQS0_N	MEM_CH1_DQSA0_N
BJ24	MEM_CH1_DQS0_P	MEM_CH1_DQSA0_P
BF25	MEM_CH1_DQS1_N	MEM_CH1_DQSA1_N
BD25	MEM_CH1_DQS1_P	MEM_CH1_DQSA1_P
BJ18	MEM_CH1_DQS2_N	MEM_CH1_DQSA2_N
BL18	MEM_CH1_DQS2_P	MEM_CH1_DQSA2_P
AV21	MEM_CH1_DQS3_N	MEM_CH1_DQSA3_N
AV19	MEM_CH1_DQS3_P	MEM_CH1_DQSA3_P
AR15	MEM_CH1_DQS4_N	MEM_CH1_DQSB0_N
AR13	MEM_CH1_DQS4_P	MEM_CH1_DQSB0_P
BC2	MEM_CH1_DQS5_N	MEM_CH1_DQSB1_N
BB3	MEM_CH1_DQS5_P	MEM_CH1_DQSB1_P
AW8	MEM_CH1_DQS6_N	MEM_CH1_DQSB2_N
AW7	MEM_CH1_DQS6_P	MEM_CH1_DQSB2_P
AT3	MEM_CH1_DQS7_N	MEM_CH1_DQSB3_N
AT1	MEM_CH1_DQS7_P	MEM_CH1_DQSB3_P
BH9	MEM_CH1_MA0	NCTF
BC13	MEM_CH1_MA1	NCTF

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 12 of 29)

Ball#	DDR4	LPDDR4
BF11	MEM_CH1_MA10	NCTF
BK11	MEM_CH1_MA11	NCTF
BJ12	MEM_CH1_MA12	NCTF
BE5	MEM_CH1_MA13	MEM_CH1_CAB0
BK9	MEM_CH1_MA14	NCTF
BJ11	MEM_CH1_MA15	NCTF
BH5	MEM_CH1_MA16	MEM_CH1_CAB3
BD11	MEM_CH1_MA2	MEM_CH1_CAB5
BD13	MEM_CH1_MA3	NCTF
BJ4	MEM_CH1_MA4	NCTF
BL6	MEM_CH1_MA5	MEM_CH1_CAA2
BJ5	MEM_CH1_MA6	MEM_CH1_CAA1
BJ9	MEM_CH1_MA7	MEM_CH1_CAA3
BJ6	MEM_CH1_MA8	MEM_CH1_CAA0
BJ8	MEM_CH1_MA9	MEM_CH1_CAA4
BC8	MEM_CH1_ODT0	NCTF
BC7	MEM_CH1_ODT1	NCTF
AY27	MEM_CH1_RCOMP	MEM_CH1_RCOMP
BC15	MEM_CH1_RESET_N	MEM_CH1_RESET_N
AV27	MEM_CH1_VREFCA	NCTF
AY25	MEM_CH1_VREFDQ	NCTF
R53	MIPI_I2C_SCL	MIPI_I2C_SCL
R54	MIPI_I2C_SDA	MIPI_I2C_SDA
A4	NC	NC
A54	NC	NC
AA10	NC	NC
AA18	VDD2_1P2_VNNAON	VDD2_1P2_VNNAON
AA20	VDD2_1P2_VNNAON	VDD2_1P2_VNNAON
AA8	NC	NC
AG43	NC	NC
AG44	NC	NC
AJ49	NC	NC
AW44	NC	NC
BH1	NC	NC
BH55	NC	NC
BL2	NC	NC
BL3	NC	NC
BL53	NC	NC

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 13 of 29)

Ball#	DDR4	LPDDR4
BL54	NC	NC
C2	NC	NC
C3	NC	NC
C54	NC	NC
D1	DEBUG_PORT_A0	DEBUG_PORT_A0
D2	DEBUG_PORT_A1	DEBUG_PORT_A1
F37	NC	NC
H53	NC	NC
H55	NC	NC
R41	NC	NC
U15	NC	NC
W12	NC	NC
W13	NC	NC
BF1	NCTF	MEM_CH1_CS0B
BG2	NCTF	MEM_CH1_CS1A
BG54	NCTF	MEM_CH0_CKE1B
BH54	NCTF	MEM_CH0_CKE0B
BJ13	NCTF	MEM_CH1_CKE0B
BJ42	NCTF	MEM_CH0_CS0B
BL12	NCTF	MEM_CH1_CKE1B
BL44	NCTF	MEM_CH0_CS1A
B17	OSC_CLK_OUT_0	OSC_CLK_OUT_0
C17	OSC_CLK_OUT_1	OSC_CLK_OUT_1
U2	OSCIN	OSCIN
T1	OSCOUT	OSCOUT
R10	PCIE_CLKOUT0N	PCIE_CLKOUT0N
R12	PCIE_CLKOUT0P	PCIE_CLKOUT0P
N5	PCIE_CLKOUT1N	PCIE_CLKOUT1N
N7	PCIE_CLKOUT1P	PCIE_CLKOUT1P
R5	PCIE_CLKOUT2N	PCIE_CLKOUT2N
R7	PCIE_CLKOUT2P	PCIE_CLKOUT2P
N10	PCIE_CLKOUT3N	PCIE_CLKOUT3N
N8	PCIE_CLKOUT3P	PCIE_CLKOUT3P
C45	PCIE_CLKREQ1_N	PCIE_CLKREQ1_N
B45	PCIE_CLKREQ2_N	PCIE_CLKREQ2_N
C44	PCIE_CLKREQ3_N	PCIE_CLKREQ3_N
A46	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 14 of 29)

Ball#	DDR4	LPDDR4
H6	PCIE_P0_RXN	PCIE_P0_RXN
G7	PCIE_P0_RXP	PCIE_P0_RXP
F2	PCIE_P0_TXN	PCIE_P0_TXN
E2	PCIE_P0_TXP	PCIE_P0_TXP
E5	PCIE_P1_RXN	PCIE_P1_RXN
D4	PCIE_P1_RXP	PCIE_P1_RXP
C7	PCIE_P1_TXN	PCIE_P1_TXN
A7	PCIE_P1_TXP	PCIE_P1_TXP
F6	PCIE_P2_RXN	PCIE_P2_RXN
E7	PCIE_P2_RXP	PCIE_P2_RXP
B9	PCIE_P2_TXN	PCIE_P2_TXN
C9	PCIE_P2_TXP	PCIE_P2_TXP
F9	PCIE_P3_USB3_P4_RXN	PCIE_P3_USB3_P4_RXN
H9	PCIE_P3_USB3_P4_RXP	PCIE_P3_USB3_P4_RXP
A10	PCIE_P3_USB3_P4_TXN	PCIE_P3_USB3_P4_TXN
C10	PCIE_P3_USB3_P4_TXP	PCIE_P3_USB3_P4_TXP
F11	PCIE_P4_USB3_P3_RXN	PCIE_P4_USB3_P3_RXN
D11	PCIE_P4_USB3_P3_RXP	PCIE_P4_USB3_P3_RXP
B11	PCIE_P4_USB3_P3_TXN	PCIE_P4_USB3_P3_TXN
C11	PCIE_P4_USB3_P3_TXP	PCIE_P4_USB3_P3_TXP
D13	PCIE_P5_USB3_P2_RXN	PCIE_P5_USB3_P2_RXN
F13	PCIE_P5_USB3_P2_RXP	PCIE_P5_USB3_P2_RXP
C13	PCIE_P5_USB3_P2_TXN	PCIE_P5_USB3_P2_TXN
B13	PCIE_P5_USB3_P2_TXP	PCIE_P5_USB3_P2_TXP
L10	PCIE_REF_CLK_RCOMP	PCIE_REF_CLK_RCOMP
F47	PCIE_WAKE0_N	PCIE_WAKE0_N
D47	PCIE_WAKE1_N	PCIE_WAKE1_N
F45	PCIE_WAKE2_N	PCIE_WAKE2_N
D50	PCIE_WAKE3_N	PCIE_WAKE3_N
C5	PCIE2_USB3_SATA3_RCOMP_N	PCIE2_USB3_SATA3_RCOMP_N
C6	PCIE2_USB3_SATA3_RCOMP_P	PCIE2_USB3_SATA3_RCOMP_P
R46	PMC_I2C_SCL	PMC_I2C_SCL
R48	PMC_I2C_SDA	PMC_I2C_SDA
L48	PMC_SPI_CLK	PMC_SPI_CLK
N48	PMC_SPI_FS0	PMC_SPI_FS0
N44	PMC_SPI_FS1	PMC_SPI_FS1

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 15 of 29)

Ball#	DDR4	LPDDR4
L49	PMC_SPI_FS2	PMC_SPI_FS2
L51	PMC_SPI_RXD	PMC_SPI_RXD
N49	PMC_SPI_TXD	PMC_SPI_TXD
J48	PMU_BATLOW_N	PMU_BATLOW_N
D54	PMU_PLTRST_N	PMU_PLTRST_N
E54	PMU_PWRBTN_N	PMU_PWRBTN_N
C51	PMU_RSTBTN_N	PMU_RSTBTN_N
C52	PMU_SLP_S0_N	PMU_SLP_S0_N
D51	PMU_SLP_S3_N	PMU_SLP_S3_N
J49	PMU_SLP_S4_N	PMU_SLP_S4_N
G49	PMU_SUSCLK	PMU_SUSCLK
B41	PNL0_BKLCTL	PNL0_BKLCTL
C40	PNL0_BKLTEN	PNL0_BKLTEN
C41	PNL0_VDDEN	PNL0_VDDEN
J54	PROCHOT_N	PROCHOT_N
F27	RSM_RST_N	RSM_RST_N
D27	RTC_RST_N	RTC_RST_N
F25	RTC_TEST_N	RTC_TEST_N
D23	RTC_X1	RTC_X1
F23	RTC_X2	RTC_X2
J5	SATA_P0_RXN	SATA_P0_RXN
J7	SATA_P0_RXP	SATA_P0_RXP
J2	SATA_P0_TXN	SATA_P0_TXN
J3	SATA_P0_TXP	SATA_P0_TXP
G5	SATA_P1_USB3_P5_RXN	SATA_P1_USB3_P5_RXN
H4	SATA_P1_USB3_P5_RXP	SATA_P1_USB3_P5_RXP
H2	SATA_P1_USB3_P5_TXN	SATA_P1_USB3_P5_TXN
H1	SATA_P1_USB3_P5_TXP	SATA_P1_USB3_P5_TXP
L25	RSVD	RSVD
L29	RSVD	RSVD
L27	RSVD	RSVD
M29	RSVD	RSVD
P29	RSVD	RSVD
M27	RSVD	RSVD
P27	RSVD	RSVD
P25	RSVD	RSVD
L23	RSVD	RSVD

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 16 of 29)

Ball#	DDR4	LPDDR4
J25	RSVD	RSVD
U49	SIO_I2C0_SCL	SIO_I2C0_SCL
U51	SIO_I2C0_SDA	SIO_I2C0_SDA
U46	SIO_I2C1_SCL	SIO_I2C1_SCL
U48	SIO_I2C1_SDA	SIO_I2C1_SDA
AA39	SIO_I2C2_SCL	SIO_I2C2_SCL
AA41	SIO_I2C2_SDA	SIO_I2C2_SDA
R44	SIO_I2C3_SCL	SIO_I2C3_SCL
R43	SIO_I2C3_SDA	SIO_I2C3_SDA
R49	SIO_I2C4_SCL	SIO_I2C4_SCL
R51	SIO_I2C4_SDA	SIO_I2C4_SDA
C50	SIO_I2C5_SCL	SIO_I2C5_SCL
A50	SIO_I2C5_SDA	SIO_I2C5_SDA
C48	SIO_I2C6_SCL	SIO_I2C6_SCL
C47	SIO_I2C6_SDA	SIO_I2C6_SDA
B47	SIO_I2C7_SCL	SIO_I2C7_SCL
C46	SIO_I2C7_SDA	SIO_I2C7_SDA
M39	SIO_SPI_0_CLK	SIO_SPI_0_CLK
L37	SIO_SPI_0_FS0	SIO_SPI_0_FS0
J39	SIO_SPI_0_FS1	SIO_SPI_0_FS1
L39	SIO_SPI_0_RXD	SIO_SPI_0_RXD
J37	SIO_SPI_0_TXD	SIO_SPI_0_TXD
M37	SIO_SPI_2_CLK	SIO_SPI_2_CLK
P33	SIO_SPI_2_FS0	SIO_SPI_2_FS0
P37	SIO_SPI_2_FS1	SIO_SPI_2_FS1
L35	SIO_SPI_2_FS2	SIO_SPI_2_FS2
P35	SIO_SPI_2_RXD	SIO_SPI_2_RXD
M33	SIO_SPI_2_TXD	SIO_SPI_2_TXD
P53	SIO_UART0_RXD	SIO_UART0_RXD
N54	SIO_UART0_TXD	SIO_UART0_TXD
N53	SIO_UART0_RTS_N	SIO_UART0_RTS_N
M55	SIO_UART0_CTS_N	SIO_UART0_CTS_N
M53	SIO_UART2_RXD	SIO_UART2_RXD
L54	SIO_UART2_TXD	SIO_UART2_TXD
K53	SIO_UART2_RTS_N	SIO_UART2_RTS_N
L53	SIO_UART2_CTS_N	SIO_UART2_CTS_N

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 17 of 29)

Ball#	DDR4	LPDDR4
A53	SKTOCC_N	SKTOCC_N
A26	SMB_ALERT_N	SMB_ALERT_N
B27	SMB_CLK	SMB_CLK
C27	SMB_DATA	SMB_DATA
D25	SOC_PWROK	SOC_PWROK
E52	SUS_STAT_N	SUS_STAT_N
F54	SUSPWRDNACK	SUSPWRDNACK
G54	SVID0_ALERT_N	SVID0_ALERT_N
G53	SVID0_DATA	SVID0_DATA
F55	SVID0_CLK	SVID0_CLK
J53	THERMTRIP_N	THERMTRIP_N
U5	USB2_DN0	USB2_DN0
N3	USB2_DN1	USB2_DN1
L3	USB2_DN2	USB2_DN2
R15	USB2_DN3	USB2_DN3
M3	USB2_DN4	USB2_DN4
R3	USB2_DN5	USB2_DN5
P3	USB2_DN6	USB2_DN6
U10	USB2_DN7	USB2_DN7
U7	USB2_DP0	USB2_DP0
N2	USB2_DP1	USB2_DP1
L2	USB2_DP2	USB2_DP2
R13	USB2_DP3	USB2_DP3
M1	USB2_DP4	USB2_DP4
R2	USB2_DP5	USB2_DP5
P1	USB2_DP6	USB2_DP6
U8	USB2_DP7	USB2_DP7
U54	USB2_OC0_N	USB2_OC0_N
U53	USB2_OC1_N	USB2_OC1_N
V1	USB2_DUALROLE	USB2_DUALROLE
U12	USB2_RCOMP	USB2_RCOMP
V3	USB2_VBUS_SNS	USB2_VBUS_SNS
D15	USB3_P0_RXN	USB3_P0_RXN
F15	USB3_P0_RXP	USB3_P0_RXP
C15	USB3_P0_TXN	USB3_P0_TXN
B15	USB3_P0_TXP	USB3_P0_TXP
H11	USB3_P1_RXN	USB3_P1_RXN

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 18 of 29)

Ball#	DDR4	LPDDR4
J11	USB3_P1_RXP	USB3_P1_RXP
A14	USB3_P1_TXN	USB3_P1_TXN
C14	USB3_P1_TXP	USB3_P1_TXP
AG49	VCC_1P05_INT	VCC_1P05_INT
AG51	VCC_1P05_INT	VCC_1P05_INT
AJ51	VCC_1P05_INT	VCC_1P05_INT
AG23	VCC_1P8V_A	VCC_1P8V_A
AJ23	VCC_1P8V_A	VCC_1P8V_A
T21	VCC_1P8V_A	VCC_1P8V_A
T23	VCC_1P8V_A	VCC_1P8V_A
T25	VCC_1P8V_A	VCC_1P8V_A
V21	VCC_1P8V_A	VCC_1P8V_A
V23	VCC_1P8V_A	VCC_1P8V_A
V25	VCC_1P8V_A	VCC_1P8V_A
AG21	VCC_3P3V_A	VCC_3P3V_A
AJ21	VCC_3P3V_A	VCC_3P3V_A
T18	VCC_3P3V_A	VCC_3P3V_A
T20	VCC_3P3V_A	VCC_3P3V_A
U17	VCC_3P3V_A	VCC_3P3V_A
V18	VCC_3P3V_A	VCC_3P3V_A
V20	VCC_3P3V_A	VCC_3P3V_A
Y18	VCC_3P3V_A	VCC_3P3V_A
Y20	VCC_3P3V_A	VCC_3P3V_A
J23	VCC_RTC_EXTPAD	VCC_RTC_EXTPAD
AA28	VCC_VCG	VCC_VCG
AA29	VCC_VCG	VCC_VCG
AA31	VCC_VCG	VCC_VCG
AA33	VCC_VCG	VCC_VCG
AC28	VCC_VCG	VCC_VCG
AC31	VCC_VCG	VCC_VCG
AE28	VCC_VCG	VCC_VCG
AE29	VCC_VCG	VCC_VCG
AE31	VCC_VCG	VCC_VCG
AF31	VCC_VCG	VCC_VCG
AF33	VCC_VCG	VCC_VCG
AG31	VCC_VCG	VCC_VCG
AG33	VCC_VCG	VCC_VCG
AJ31	VCC_VCG	VCC_VCG
AJ33	VCC_VCG	VCC_VCG

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 19 of 29)

Ball#	DDR4	LPDDR4
AJ35	VCC_VCG	VCC_VCG
AL31	VCC_VCG	VCC_VCG
AL33	VCC_VCG	VCC_VCG
AL35	VCC_VCG	VCC_VCG
AM33	VCC_VCG	VCC_VCG
AM35	VCC_VCG	VCC_VCG
AM36	VCC_VCG	VCC_VCG
D31	VCC_VCG	VCC_VCG
D33	VCC_VCG	VCC_VCG
D37	VCC_VCG	VCC_VCG
D39	VCC_VCG	VCC_VCG
P39	VCC_VCG	VCC_VCG
P41	VCC_VCG	VCC_VCG
T28	VCC_VCG	VCC_VCG
T29	VCC_VCG	VCC_VCG
T31	VCC_VCG	VCC_VCG
T33	VCC_VCG	VCC_VCG
T35	VCC_VCG	VCC_VCG
T36	VCC_VCG	VCC_VCG
V28	VCC_VCG	VCC_VCG
V29	VCC_VCG	VCC_VCG
V31	VCC_VCG	VCC_VCG
V33	VCC_VCG	VCC_VCG
V35	VCC_VCG	VCC_VCG
V36	VCC_VCG	VCC_VCG
Y28	VCC_VCG	VCC_VCG
Y29	VCC_VCG	VCC_VCG
Y33	VCC_VCG	VCC_VCG
Y35	VCC_VCG	VCC_VCG
AG41	VCC_VCG_SENSE	VCC_VCG_SENSE
AP25	VCCIOA	VCCIOA
AP31	VCCIOA	VCCIOA
AT25	VCCIOA	VCCIOA
AT27	VCCIOA	VCCIOA
AT28	VCCIOA	VCCIOA
AT29	VCCIOA	VCCIOA
AT31	VCCIOA	VCCIOA
AA36	VCCRAM_1P05	VCCRAM_1P05
AA38	VCCRAM_1P05	VCCRAM_1P05

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 20 of 29)

Ball#	DDR4	LPDDR4
AC33	VCCRAM_1P05	VCCRAM_1P05
AC35	VCCRAM_1P05	VCCRAM_1P05
AC36	VCCRAM_1P05	VCCRAM_1P05
AC38	VCCRAM_1P05	VCCRAM_1P05
AE33	VCCRAM_1P05	VCCRAM_1P05
AE35	VCCRAM_1P05	VCCRAM_1P05
AE36	VCCRAM_1P05	VCCRAM_1P05
AE38	VCCRAM_1P05	VCCRAM_1P05
AF27	VCCRAM_1P05	VCCRAM_1P05
AF28	VCCRAM_1P05	VCCRAM_1P05
AF36	VCCRAM_1P05	VCCRAM_1P05
AF38	VCCRAM_1P05	VCCRAM_1P05
Y36	VCCRAM_1P05	VCCRAM_1P05
Y38	VCCRAM_1P05	VCCRAM_1P05
P15	VCCRTC_3P3V	VCCRTC_3P3V
AC18	VDD2_1P2_AUD_ISH	VDD2_1P2_AUD_ISH
AC20	VDD2_1P2_AUD_ISH	VDD2_1P2_AUD_ISH
AW12	VDD2_1P2_DSI_CSI	VDD2_1P2_DSI_CSI
AL36	VDD2_1P2_CPU	VDD2_1P2_CPU
AL38	VDD2_1P2_CPU	VDD2_1P2_CPU
AM20	VDD2_1P2_CPU	VDD2_1P2_CPU
AP20	VDD2_1P2_CPU	VDD2_1P2_CPU
AC21	VDD2_1P2_MPHY	VDD2_1P2_MPHY
AE20	VDD2_1P2_MPHY	VDD2_1P2_MPHY
AE21	VDD2_1P2_MPHY	VDD2_1P2_MPHY
AF20	VDD2_1P2_MPHY	VDD2_1P2_MPHY
AF21	VDD2_1P2_MPHY	VDD2_1P2_MPHY
AL18	VDD2_1P2_PLL	VDD2_1P2_PLL
AM18	VDD2_1P2_PLL	VDD2_1P2_PLL
AG18	VDD2_1P2_USB2	VDD2_1P2_USB2
AJ20	VDD2_1P2_USB3	VDD2_1P2_USB3
AP18	VDDQ	VDDQ
AP21	VDDQ	VDDQ
AP36	VDDQ	VDDQ
AP38	VDDQ	VDDQ
AT18	VDDQ	VDDQ
AT20	VDDQ	VDDQ
AT21	VDDQ	VDDQ
AT35	VDDQ	VDDQ

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 21 of 29)

Ball#	DDR4	LPDDR4
AT36	VDDQ	VDDQ
AT38	VDDQ	VDDQ
BA13	VDDQ	VDDQ
BA15	VDDQ	VDDQ
BA25	VDDQ	VDDQ
BA31	VDDQ	VDDQ
BA41	VDDQ	VDDQ
BA43	VDDQ	VDDQ
AF35	VNN	VNN
AG27	VNN	VNN
AG28	VNN	VNN
AG36	VNN	VNN
AG46	VNN	VNN
AG48	VNN	VNN
AJ27	VNN	VNN
AJ28	VNN	VNN
AJ46	VNN	VNN
AJ48	VNN	VNN
AL27	VNN	VNN
AL28	VNN	VNN
AL48	VNN	VNN
AL49	VNN	VNN
AM27	VNN	VNN
AM28	VNN	VNN
AJ41	VNN_SENSE	VNN_SENSE
AJ43	VNN_VSS_SENSE	VNN_VSS_SENSE
A12	VSS	VSS
A16	VSS	VSS
A20	VSS	VSS
A24	VSS	VSS
A28	VSS	VSS
A3	VSS	VSS
A32	VSS	VSS
A36	VSS	VSS
A40	VSS	VSS
A44	VSS	VSS
A48	VSS	VSS
A51	VSS	VSS
A6	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 22 of 29)

Ball#	DDR4	LPDDR4
AA12	VSS	VSS
AA13	VSS	VSS
AA15	VSS	VSS
AA17	VSS	VSS
AA21	VSS	VSS
AA23	VSS	VSS
AA25	VSS	VSS
AA27	VSS	VSS
AA35	VSS	VSS
AA43	VSS	VSS
AA48	VSS	VSS
AB1	VSS	VSS
AB3	VSS	VSS
AB55	VSS	VSS
AC13	VSS	VSS
AC23	VSS	VSS
AC25	VSS	VSS
AC27	VSS	VSS
AC29	VSS	VSS
AC8	VSS	VSS
AE18	VSS	VSS
AE23	VSS	VSS
AE25	VSS	VSS
AE27	VSS	VSS
AE43	VSS	VSS
AE48	VSS	VSS
AF1	VSS	VSS
AF11	VSS	VSS
AF12	VSS	VSS
AF14	VSS	VSS
AF16	VSS	VSS
AF18	VSS	VSS
AF23	VSS	VSS
AF25	VSS	VSS
AF29	VSS	VSS
AF3	VSS	VSS
AF4	VSS	VSS
AF40	VSS	VSS
AF42	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 23 of 29)

Ball#	DDR4	LPDDR4
AF44	VSS	VSS
AF45	VSS	VSS
AF47	VSS	VSS
AF48	VSS	VSS
AF50	VSS	VSS
AF52	VSS	VSS
AF53	VSS	VSS
AF55	VSS	VSS
AF6	VSS	VSS
AF8	VSS	VSS
AF9	VSS	VSS
AG20	VSS	VSS
AG25	VSS	VSS
AG29	VSS	VSS
AG35	VSS	VSS
AG38	VSS	VSS
AJ13	VSS	VSS
AJ18	VSS	VSS
AJ25	VSS	VSS
AJ29	VSS	VSS
AJ36	VSS	VSS
AJ38	VSS	VSS
AJ39	VSS	VSS
AJ44	VSS	VSS
AJ8	VSS	VSS
AK1	VSS	VSS
AK3	VSS	VSS
AK55	VSS	VSS
AL10	VSS	VSS
AL12	VSS	VSS
AL13	VSS	VSS
AL15	VSS	VSS
AL17	VSS	VSS
AL20	VSS	VSS
AL21	VSS	VSS
AL23	VSS	VSS
AL25	VSS	VSS
AL29	VSS	VSS
AL3	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 24 of 29)

Ball#	DDR4	LPDDR4
AL39	VSS	VSS
AL41	VSS	VSS
AL43	VSS	VSS
AL44	VSS	VSS
AL46	VSS	VSS
AL51	VSS	VSS
AL7	VSS	VSS
AL8	VSS	VSS
AM1	VSS	VSS
AM21	VSS	VSS
AM23	VSS	VSS
AM25	VSS	VSS
AM29	VSS	VSS
AM31	VSS	VSS
AM38	VSS	VSS
AM55	VSS	VSS
AN10	VSS	VSS
AN3	VSS	VSS
AN46	VSS	VSS
AN48	VSS	VSS
AN49	VSS	VSS
AN51	VSS	VSS
AN53	VSS	VSS
AN8	VSS	VSS
AP23	VSS	VSS
AP27	VSS	VSS
AP28	VSS	VSS
AP29	VSS	VSS
AP33	VSS	VSS
AP35	VSS	VSS
AR10	VSS	VSS
AR12	VSS	VSS
AR17	VSS	VSS
AR2	VSS	VSS
AR39	VSS	VSS
AR44	VSS	VSS
AR46	VSS	VSS
AR49	VSS	VSS
AR54	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 25 of 29)

Ball#	DDR4	LPDDR4
AR7	VSS	VSS
AT23	VSS	VSS
AT33	VSS	VSS
AU10	VSS	VSS
AU28	VSS	VSS
AU3	VSS	VSS
AU46	VSS	VSS
AU53	VSS	VSS
AV15	VSS	VSS
AV17	VSS	VSS
AV23	VSS	VSS
AV25	VSS	VSS
AV31	VSS	VSS
AV33	VSS	VSS
AV39	VSS	VSS
AV41	VSS	VSS
AW10	VSS	VSS
AW2	VSS	VSS
AW28	VSS	VSS
AW46	VSS	VSS
AW5	VSS	VSS
AW51	VSS	VSS
AW54	VSS	VSS
AY13	VSS	VSS
AY15	VSS	VSS
AY28	VSS	VSS
AY41	VSS	VSS
AY43	VSS	VSS
B2	VSS	VSS
B55	VSS	VSS
BA27	VSS	VSS
BA29	VSS	VSS
BB1	VSS	VSS
BB28	VSS	VSS
BB55	VSS	VSS
BC11	VSS	VSS
BC17	VSS	VSS
BC19	VSS	VSS
BC21	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 26 of 29)

Ball#	DDR4	LPDDR4
BC23	VSS	VSS
BC25	VSS	VSS
BC31	VSS	VSS
BC33	VSS	VSS
BC35	VSS	VSS
BC37	VSS	VSS
BC39	VSS	VSS
BC41	VSS	VSS
BC45	VSS	VSS
BC5	VSS	VSS
BC51	VSS	VSS
BD15	VSS	VSS
BD19	VSS	VSS
BD21	VSS	VSS
BD28	VSS	VSS
BD35	VSS	VSS
BD37	VSS	VSS
BD47	VSS	VSS
BD9	VSS	VSS
BE28	VSS	VSS
BE3	VSS	VSS
BE53	VSS	VSS
BF19	VSS	VSS
BF37	VSS	VSS
BF47	VSS	VSS
BF9	VSS	VSS
BG1	VSS	VSS
BG28	VSS	VSS
BG50	VSS	VSS
BG55	VSS	VSS
BG6	VSS	VSS
BH11	VSS	VSS
BH13	VSS	VSS
BH17	VSS	VSS
BH19	VSS	VSS
BH23	VSS	VSS
BH25	VSS	VSS
BH28	VSS	VSS
BH31	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 27 of 29)

Ball#	DDR4	LPDDR4
BH33	VSS	VSS
BH37	VSS	VSS
BH39	VSS	VSS
BH41	VSS	VSS
BH45	VSS	VSS
BJ15	VSS	VSS
BJ19	VSS	VSS
BJ2	VSS	VSS
BJ25	VSS	VSS
BJ28	VSS	VSS
BJ31	VSS	VSS
BJ37	VSS	VSS
BJ41	VSS	VSS
BJ54	VSS	VSS
BK1	VSS	VSS
BK17	VSS	VSS
BK21	VSS	VSS
BK35	VSS	VSS
BK39	VSS	VSS
BK55	VSS	VSS
BL10	VSS	VSS
BL14	VSS	VSS
BL24	VSS	VSS
BL28	VSS	VSS
BL32	VSS	VSS
BL42	VSS	VSS
BL46	VSS	VSS
BL48	VSS	VSS
BL5	VSS	VSS
BL51	VSS	VSS
BL8	VSS	VSS
C1	VSS	VSS
C12	VSS	VSS
C16	VSS	VSS
C28	VSS	VSS
C36	VSS	VSS
D21	VSS	VSS
D28	VSS	VSS
D41	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 28 of 29)

Ball#	DDR4	LPDDR4
D45	VSS	VSS
D55	VSS	VSS
D6	VSS	VSS
D9	VSS	VSS
E28	VSS	VSS
E50	VSS	VSS
E55	VSS	VSS
F1	VSS	VSS
F21	VSS	VSS
F31	VSS	VSS
F4	VSS	VSS
G28	VSS	VSS
H13	VSS	VSS
H15	VSS	VSS
H21	VSS	VSS
H23	VSS	VSS
H28	VSS	VSS
H33	VSS	VSS
H39	VSS	VSS
J27	VSS	VSS
J33	VSS	VSS
J41	VSS	VSS
J45	VSS	VSS
J51	VSS	VSS
J8	VSS	VSS
K1	VSS	VSS
K28	VSS	VSS
K3	VSS	VSS
K55	VSS	VSS
L19	VSS	VSS
L33	VSS	VSS
L5	VSS	VSS
L7	VSS	VSS
L8	VSS	VSS
M15	VSS	VSS
M25	VSS	VSS
M28	VSS	VSS
M35	VSS	VSS
M41	VSS	VSS

Table 5-1. SoC Pin List for DDR4 and LPDDR4 (Sheet 29 of 29)

Ball#	DDR4	LPDDR4
N12	VSS	VSS
N28	VSS	VSS
N46	VSS	VSS
N51	VSS	VSS
P21	VSS	VSS
P55	VSS	VSS
R28	VSS	VSS
R8	VSS	VSS
T27	VSS	VSS
T3	VSS	VSS
T38	VSS	VSS
U13	VSS	VSS
U3	VSS	VSS
V27	VSS	VSS
V38	VSS	VSS
V55	VSS	VSS
W10	VSS	VSS
W2	VSS	VSS
W3	VSS	VSS
W39	VSS	VSS
W41	VSS	VSS
W43	VSS	VSS
W44	VSS	VSS
W46	VSS	VSS
W48	VSS	VSS
W49	VSS	VSS
W5	VSS	VSS
W51	VSS	VSS
W7	VSS	VSS
W8	VSS	VSS
Y21	VSS	VSS
Y23	VSS	VSS
Y25	VSS	VSS
Y27	VSS	VSS
Y31	VSS	VSS
AG39	VSS_VCG_SENSE	VSS_VCG_SENSE
F19	XTAL_CLKREQ	XTAL_CLKREQ

5.4 X and Y Pin List

Table 5-2. X and Y Pin List (Sheet 1 of 28)

Pin	X	Y
A10	8.1153	-11.3141
A12	7.2136	-11.3141
A14	6.3119	-11.3141
A16	5.4102	-11.3141
A18	4.5085	-11.3141
A20	3.6068	-11.3141
A22	2.7051	-11.3141
A24	1.8034	-11.3141
A26	0.9017	-11.3141
A28	0	-11.3141
A3	11.0305	-11.3141
A30	-0.9017	-11.3141
A32	-1.8034	-11.3141
A34	-2.7051	-11.3141
A36	-3.6068	-11.3141
A38	-4.5085	-11.3141
A4	10.4336	-11.3141
A40	-5.4102	-11.3141
A42	-6.3119	-11.3141
A44	-7.2136	-11.3141
A46	-8.1153	-11.3141
A48	-9.017	-11.3141
A50	-9.5885	-11.3141
A51	-10.1854	-11.3141
A53	-10.795	-11.3141
A54	-11.4046	-11.3141
A6	9.83666	-11.3141
A7	9.06196	-11.3141
AA10	7.96747	-2.3495
AA12	7.25627	-2.3495
AA13	6.54507	-2.3495
AA15	5.83387	-2.3495
AA17	5.12267	-2.3495
AA18	4.572	-2.1717
AA2	11.5029	-2.25425
AA20	3.81	-2.1717
AA21	3.048	-2.1717
AA23	2.286	-2.1717

Table 5-2. X and Y Pin List (Sheet 2 of 28)

Pin	X	Y
AA25	1.524	-2.1717
AA27	0.762	-2.1717
AA28	0	-2.1717
AA29	-0.762	-2.1717
AA3	10.8801	-2.25425
AA31	-1.524	-2.1717
AA33	-2.286	-2.1717
AA35	-3.048	-2.1717
AA36	-3.81	-2.1717
AA38	-4.572	-2.1717
AA39	-5.12267	-2.3495
AA41	-5.83387	-2.3495
AA43	-6.54507	-2.3495
AA44	-7.25627	-2.3495
AA46	-7.96747	-2.3495
AA48	-8.67867	-2.3495
AA49	-9.38987	-2.3495
AA5	10.1011	-2.3495
AA51	-10.1011	-2.3495
AA53	-10.8801	-2.25425
AA54	-11.5029	-2.25425
AA7	9.38987	-2.3495
AA8	8.67867	-2.3495
AB1	11.8143	-1.8034
AB3	11.1915	-1.8034
AB53	-11.1915	-1.8034
AB55	-11.8143	-1.8034
AC10	7.96747	-1.397
AC12	7.25627	-1.397
AC13	6.54507	-1.397
AC15	5.83387	-1.397
AC17	5.12267	-1.397
AC18	4.572	-1.4478
AC2	11.5029	-1.35255
AC20	3.81	-1.4478
AC21	3.048	-1.4478
AC23	2.286	-1.4478
AC25	1.524	-1.4478
AC27	0.762	-1.4478
AC28	0	-1.4478

Table 5-2. X and Y Pin List (Sheet 3 of 28)

Pin	X	Y
AC29	-0.762	-1.4478
AC3	10.8801	-1.35255
AC31	-1.524	-1.4478
AC33	-2.286	-1.4478
AC35	-3.048	-1.4478
AC36	-3.81	-1.4478
AC38	-4.572	-1.4478
AC39	-5.12267	-1.397
AC41	-5.83387	-1.397
AC43	-6.54507	-1.397
AC44	-7.25627	-1.397
AC46	-7.96747	-1.397
AC48	-8.67867	-1.397
AC49	-9.38987	-1.397
AC5	10.1011	-1.397
AC51	-10.1011	-1.397
AC53	-10.8801	-1.35255
AC54	-11.5029	-1.35255
AC7	9.38987	-1.397
AC8	8.67867	-1.397
AD1	11.8143	-0.9017
AD3	11.1915	-0.9017
AD53	-11.1915	-0.9017
AD55	-11.8143	-0.9017
AE10	7.96747	-0.5207
AE12	7.25627	-0.5207
AE13	6.54507	-0.5207
AE15	5.83387	-0.5207
AE17	5.12267	-0.5207
AE18	4.572	-0.7239
AE2	11.5029	-0.45085
AE20	3.81	-0.7239
AE21	3.048	-0.7239
AE23	2.286	-0.7239
AE25	1.524	-0.7239
AE27	0.762	-0.7239
AE28	0	-0.7239
AE29	-0.762	-0.7239
AE3	10.8801	-0.45085
AE31	-1.524	-0.7239

Table 5-2. X and Y Pin List (Sheet 4 of 28)

Pin	X	Y
AE33	-2.286	-0.7239
AE35	-3.048	-0.7239
AE36	-3.81	-0.7239
AE38	-4.572	-0.7239
AE39	-5.12267	-0.5207
AE41	-5.83387	-0.5207
AE43	-6.54507	-0.5207
AE44	-7.25627	-0.5207
AE46	-7.96747	-0.5207
AE48	-8.67867	-0.5207
AE49	-9.38987	-0.5207
AE5	10.1011	-0.5207
AE51	-10.1011	-0.5207
AE53	-10.8801	-0.45085
AE54	-11.5029	-0.45085
AE7	9.38987	-0.5207
AE8	8.67867	-0.5207
AF1	11.8143	0
AF11	7.61187	0
AF12	6.90067	0
AF14	6.18947	0
AF16	5.47827	0
AF18	4.572	0
AF20	3.81	0
AF21	3.048	0
AF23	2.286	0
AF25	1.524	0
AF27	0.762	0
AF28	0	0
AF29	-0.762	0
AF3	11.1915	0
AF31	-1.524	0
AF33	-2.286	0
AF35	-3.048	0
AF36	-3.81	0
AF38	-4.572	0
AF4	10.5687	0
AF40	-5.47827	0
AF42	-6.18947	0
AF44	-6.90067	0

Table 5-2. X and Y Pin List (Sheet 5 of 28)

Pin	X	Y
AF45	-7.61187	0
AF47	-8.32307	0
AF48	-9.03427	0
AF50	-9.74547	0
AF52	-10.5687	0
AF53	-11.1915	0
AF55	-11.8143	0
AF6	9.74547	0
AF8	9.03427	0
AF9	8.32307	0
AG10	7.96747	0.5207
AG12	7.25627	0.5207
AG13	6.54507	0.5207
AG15	5.83387	0.5207
AG17	5.12267	0.5207
AG18	4.572	0.7239
AG2	11.5029	0.45085
AG20	3.81	0.7239
AG21	3.048	0.7239
AG23	2.286	0.7239
AG25	1.524	0.7239
AG27	0.762	0.7239
AG28	0	0.7239
AG29	-0.762	0.7239
AG3	10.8801	0.45085
AG31	-1.524	0.7239
AG33	-2.286	0.7239
AG35	-3.048	0.7239
AG36	-3.81	0.7239
AG38	-4.572	0.7239
AG39	-5.12267	0.5207
AG41	-5.83387	0.5207
AG43	-6.54507	0.5207
AG44	-7.25627	0.5207
AG46	-7.96747	0.5207
AG48	-8.67867	0.5207
AG49	-9.38987	0.5207
AG5	10.1011	0.5207
AG51	-10.1011	0.5207
AG53	-10.8801	0.45085

Table 5-2. X and Y Pin List (Sheet 6 of 28)

Pin	X	Y
AG54	-11.5029	0.45085
AG7	9.38987	0.5207
AG8	8.67867	0.5207
AH1	11.8143	0.9017
AH3	11.1915	0.9017
AH53	-11.1915	0.9017
AH55	-11.8143	0.9017
AJ10	7.96747	1.397
AJ12	7.25627	1.397
AJ13	6.54507	1.397
AJ15	5.83387	1.397
AJ17	5.12267	1.397
AJ18	4.572	1.4478
AJ2	11.5029	1.35255
AJ20	3.81	1.4478
AJ21	3.048	1.4478
AJ23	2.286	1.4478
AJ25	1.524	1.4478
AJ27	0.762	1.4478
AJ28	0	1.4478
AJ29	-0.762	1.4478
AJ3	10.8801	1.35255
AJ31	-1.524	1.4478
AJ33	-2.286	1.4478
AJ35	-3.048	1.4478
AJ36	-3.81	1.4478
AJ38	-4.572	1.4478
AJ39	-5.12267	1.397
AJ41	-5.83387	1.397
AJ43	-6.54507	1.397
AJ44	-7.25627	1.397
AJ46	-7.96747	1.397
AJ48	-8.67867	1.397
AJ49	-9.38987	1.397
AJ5	10.1011	1.397
AJ51	-10.1011	1.397
AJ53	-10.8801	1.35255
AJ54	-11.5029	1.35255
AJ7	9.38987	1.397
AJ8	8.67867	1.397

Table 5-2. X and Y Pin List (Sheet 7 of 28)

Pin	X	Y
AK1	11.8143	1.8034
AK3	11.1915	1.8034
AK53	-11.1915	1.8034
AK55	-11.8143	1.8034
AL10	7.96747	2.3495
AL12	7.25627	2.3495
AL13	6.54507	2.3495
AL15	5.83387	2.3495
AL17	5.12267	2.3495
AL18	4.572	2.1717
AL2	11.5029	2.25425
AL20	3.81	2.1717
AL21	3.048	2.1717
AL23	2.286	2.1717
AL25	1.524	2.1717
AL27	0.762	2.1717
AL28	0	2.1717
AL29	-0.762	2.1717
AL3	10.8801	2.25425
AL31	-1.524	2.1717
AL33	-2.286	2.1717
AL35	-3.048	2.1717
AL36	-3.81	2.1717
AL38	-4.572	2.1717
AL39	-5.12267	2.3495
AL41	-5.83387	2.3495
AL43	-6.54507	2.3495
AL44	-7.25627	2.3495
AL46	-7.96747	2.3495
AL48	-8.67867	2.3495
AL49	-9.38987	2.3495
AL5	10.1011	2.3495
AL51	-10.1011	2.3495
AL53	-10.8801	2.25425
AL54	-11.5029	2.25425
AL7	9.38987	2.3495
AL8	8.67867	2.3495
AM1	11.8143	2.7051
AM18	4.572	2.8956
AM20	3.81	2.8956

Table 5-2. X and Y Pin List (Sheet 8 of 28)

Pin	X	Y
AM21	3.048	2.8956
AM23	2.286	2.8956
AM25	1.524	2.8956
AM27	0.762	2.8956
AM28	0	2.8956
AM29	-0.762	2.8956
AM3	11.1915	2.7051
AM31	-1.524	2.8956
AM33	-2.286	2.8956
AM35	-3.048	2.8956
AM36	-3.81	2.8956
AM38	-4.572	2.8956
AM53	-11.1915	2.7051
AM55	-11.8143	2.7051
AN10	7.96747	3.2258
AN12	7.25627	3.2258
AN13	6.54507	3.2258
AN15	5.83387	3.2258
AN17	5.12267	3.2258
AN2	11.5029	3.15595
AN3	10.8801	3.15595
AN39	-5.12267	3.2258
AN41	-5.83387	3.2258
AN43	-6.54507	3.2258
AN44	-7.25627	3.2258
AN46	-7.96747	3.2258
AN48	-8.67867	3.2258
AN49	-9.38987	3.2258
AN5	10.1011	3.2258
AN51	-10.1011	3.2258
AN53	-10.8801	3.15595
AN54	-11.5029	3.15595
AN7	9.38987	3.2258
AN8	8.67867	3.2258
AP1	11.8143	3.6068
AP18	4.572	3.6195
AP20	3.81	3.6195
AP21	3.048	3.6195
AP23	2.286	3.6195
AP25	1.524	3.6195

Table 5-2. X and Y Pin List (Sheet 9 of 28)

Pin	X	Y
AP27	0.762	3.6195
AP28	0	3.6195
AP29	-0.762	3.6195
AP3	11.1915	3.6068
AP31	-1.524	3.6195
AP33	-2.286	3.6195
AP35	-3.048	3.6195
AP36	-3.81	3.6195
AP38	-4.572	3.6195
AP53	-11.1915	3.6068
AP55	-11.8143	3.6068
AR10	7.96747	3.9116
AR12	7.25627	3.9116
AR13	6.54507	3.9116
AR15	5.83387	3.9116
AR17	5.12267	3.9116
AR2	11.5029	4.05765
AR3	10.8801	4.05765
AR39	-5.12267	3.9116
AR41	-5.83387	3.9116
AR43	-6.54507	3.9116
AR44	-7.25627	3.9116
AR46	-7.96747	3.9116
AR48	-8.67867	3.9116
AR49	-9.38987	3.9116
AR5	10.1011	3.9116
AR51	-10.1011	3.9116
AR53	-10.8801	4.05765
AR54	-11.5029	4.05765
AR7	9.38987	3.9116
AR8	8.67867	3.9116
AT1	11.8143	4.5085
AT18	4.572	4.3434
AT20	3.81	4.3434
AT21	3.048	4.3434
AT23	2.286	4.3434
AT25	1.524	4.3434
AT27	0.762	4.3434
AT28	0	4.3434
AT29	-0.762	4.3434

Table 5-2. X and Y Pin List (Sheet 10 of 28)

Pin	X	Y
AT3	11.1915	4.5085
AT31	-1.524	4.3434
AT33	-2.286	4.3434
AT35	-3.048	4.3434
AT36	-3.81	4.3434
AT38	-4.572	4.3434
AT53	-11.1915	4.5085
AT55	-11.8143	4.5085
AU10	7.96747	4.7879
AU12	7.25627	4.7879
AU13	6.54507	4.7879
AU15	5.83387	4.7879
AU2	11.5029	4.95935
AU28	0	4.97802
AU3	10.8801	4.95935
AU41	-5.83387	4.7879
AU43	-6.54507	4.7879
AU44	-7.25627	4.7879
AU46	-7.96747	4.7879
AU48	-8.67867	4.7879
AU49	-9.38987	4.7879
AU5	10.1011	4.7879
AU51	-10.1011	4.7879
AU53	-10.8801	4.95935
AU54	-11.5029	4.95935
AU7	9.38987	4.7879
AU8	8.67867	4.7879
AV1	11.8143	5.4102
AV15	5.6642	5.33362
AV17	4.7879	5.33362
AV19	3.9116	5.33362
AV21	3.2258	5.33362
AV23	2.3495	5.33362
AV25	1.397	5.33362
AV27	0.5207	5.33362
AV29	-0.5207	5.33362
AV3	11.1915	5.4102
AV31	-1.397	5.33362
AV33	-2.3495	5.33362
AV35	-3.2258	5.33362

Table 5-2. X and Y Pin List (Sheet 11 of 28)

Pin	X	Y
AV37	-3.9116	5.33362
AV39	-4.7879	5.33362
AV41	-5.6642	5.33362
AV53	-11.1915	5.4102
AV55	-11.8143	5.4102
AW10	7.96747	5.7404
AW12	7.25627	5.7404
AW2	11.5029	5.86105
AW28	0	5.68922
AW3	10.8801	5.86105
AW44	-7.25627	5.7404
AW46	-7.96747	5.7404
AW48	-8.67867	5.7404
AW49	-9.38987	5.7404
AW5	10.1011	5.7404
AW51	-10.1011	5.7404
AW53	-10.8801	5.86105
AW54	-11.5029	5.86105
AW7	9.38987	5.7404
AW8	8.67867	5.7404
AY1	11.8143	6.3119
AY13	6.6929	6.04482
AY15	5.7404	6.04482
AY17	4.7879	6.04482
AY19	3.9116	6.04482
AY21	3.2258	6.04482
AY23	2.3495	6.04482
AY25	1.397	6.04482
AY27	0.5207	6.04482
AY28	0	6.40042
AY29	-0.5207	6.04482
AY3	11.1915	6.3119
AY31	-1.397	6.04482
AY33	-2.3495	6.04482
AY35	-3.2258	6.04482
AY37	-3.9116	6.04482
AY39	-4.7879	6.04482
AY41	-5.7404	6.04482
AY43	-6.6929	6.04482
AY53	-11.1915	6.3119

Table 5-2. X and Y Pin List (Sheet 12 of 28)

Pin	X	Y
AY55	-11.8143	6.3119
B11	7.66445	-11.0026
B13	6.76275	-11.0026
B15	5.86105	-11.0026
B17	4.95935	-11.0026
B19	4.05765	-11.0026
B2	11.4338	-10.9336
B21	3.15595	-11.0026
B23	2.25425	-11.0026
B25	1.35255	-11.0026
B27	0.45085	-11.0026
B29	-0.45085	-11.0026
B31	-1.35255	-11.0026
B33	-2.25425	-11.0026
B35	-3.15595	-11.0026
B37	-4.05765	-11.0026
B39	-4.95935	-11.0026
B41	-5.86105	-11.0026
B43	-6.76275	-11.0026
B45	-7.66445	-11.0026
B47	-8.56615	-11.0026
B55	-11.8143	-10.8736
B9	8.56615	-11.0026
BA10	7.96747	6.6929
BA13	6.6929	6.75602
BA15	5.7404	6.75602
BA17	4.7879	6.75602
BA19	3.9116	6.75602
BA2	11.5029	6.76275
BA21	3.2258	6.75602
BA23	2.3495	6.75602
BA25	1.397	6.75602
BA27	0.5207	6.75602
BA29	-0.5207	6.75602
BA3	10.8801	6.76275
BA31	-1.397	6.75602
BA33	-2.3495	6.75602
BA35	-3.2258	6.75602
BA37	-3.9116	6.75602
BA39	-4.7879	6.75602

Table 5-2. X and Y Pin List (Sheet 13 of 28)

Pin	X	Y
BA41	-5.7404	6.75602
BA43	-6.6929	6.75602
BA46	-7.96747	6.6929
BA48	-8.67867	6.6929
BA49	-9.38987	6.6929
BA5	10.1011	6.6929
BA51	-10.1011	6.6929
BA53	-10.8801	6.76275
BA54	-11.5029	6.76275
BA7	9.38987	6.6929
BA8	8.67867	6.6929
BB1	11.8143	7.2136
BB28	0	7.11162
BB3	11.1915	7.2136
BB53	-11.1915	7.2136
BB55	-11.8143	7.2136
BC11	7.6454	7.46722
BC13	6.6929	7.46722
BC15	5.7404	7.46722
BC17	4.7879	7.46722
BC19	3.9116	7.46722
BC2	11.5029	7.66445
BC21	3.2258	7.46722
BC23	2.3495	7.46722
BC25	1.397	7.46722
BC27	0.5207	7.46722
BC29	-0.5207	7.46722
BC3	10.8801	7.66445
BC31	-1.397	7.46722
BC33	-2.3495	7.46722
BC35	-3.2258	7.46722
BC37	-3.9116	7.46722
BC39	-4.7879	7.46722
BC41	-5.7404	7.46722
BC43	-6.6929	7.46722
BC45	-7.6454	7.46722
BC48	-8.67867	7.6454
BC49	-9.38987	7.6454
BC5	10.1011	7.6454
BC51	-10.1011	7.6454

Table 5-2. X and Y Pin List (Sheet 14 of 28)

Pin	X	Y
BC53	-10.8801	7.66445
BC54	-11.5029	7.66445
BC7	9.38987	7.6454
BC8	8.67867	7.6454
BD1	11.8143	8.1153
BD11	7.6454	8.17842
BD13	6.6929	8.17842
BD15	5.7404	8.17842
BD17	4.7879	8.17842
BD19	3.9116	8.17842
BD21	3.2258	8.17842
BD23	2.3495	8.17842
BD25	1.397	8.17842
BD27	0.5207	8.17842
BD28	0	7.82282
BD29	-0.5207	8.17842
BD3	11.1915	8.1153
BD31	-1.397	8.17842
BD33	-2.3495	8.17842
BD35	-3.2258	8.17842
BD37	-3.9116	8.17842
BD39	-4.7879	8.17842
BD41	-5.7404	8.17842
BD43	-6.6929	8.17842
BD45	-7.6454	8.17842
BD47	-8.5217	8.17842
BD53	-11.1915	8.1153
BD55	-11.8143	8.1153
BD9	8.5217	8.17842
BE2	11.5029	8.56615
BE28	0	8.53402
BE3	10.8801	8.56615
BE49	-9.38987	8.5979
BE5	10.1011	8.5979
BE51	-10.1011	8.5979
BE53	-10.8801	8.56615
BE54	-11.5029	8.56615
BE7	9.38987	8.5979
BF1	11.8143	9.05751
BF11	7.6454	8.88962

Table 5-2. X and Y Pin List (Sheet 15 of 28)

Pin	X	Y
BF13	6.6929	8.88962
BF15	5.7404	8.88962
BF17	4.7879	8.88962
BF19	3.9116	8.88962
BF2	11.2634	9.12482
BF21	3.2258	8.88962
BF23	2.3495	8.88962
BF25	1.397	8.88962
BF27	0.5207	8.88962
BF29	-0.5207	8.88962
BF31	-1.397	8.88962
BF33	-2.3495	8.88962
BF35	-3.2258	8.88962
BF37	-3.9116	8.88962
BF39	-4.7879	8.88962
BF41	-5.7404	8.88962
BF43	-6.6929	8.88962
BF45	-7.6454	8.88962
BF47	-8.5979	8.88962
BF54	-11.2634	9.12482
BF55	-11.8143	9.05751
BF9	8.5979	8.88962
BG1	11.8143	9.65441
BG2	11.2634	9.67092
BG28	0	9.24522
BG4	10.6761	9.69747
BG50	-9.5504	9.60082
BG52	-10.6761	9.69747
BG54	-11.2634	9.67092
BG55	-11.8143	9.65441
BG6	9.5504	9.60082
BH1	11.8143	10.264
BH11	7.6454	9.60082
BH13	6.6929	9.60082
BH15	5.7404	9.60082
BH17	4.7879	9.60082
BH19	3.9116	9.60082
BH2	11.2634	10.217
BH21	3.2258	9.60082
BH23	2.3495	9.60082

Table 5-2. X and Y Pin List (Sheet 16 of 28)

Pin	X	Y
BH25	1.397	9.60082
BH27	0.5207	9.60082
BH28	0	10.0684
BH29	-0.5207	9.60082
BH31	-1.397	9.60082
BH33	-2.3495	9.60082
BH35	-3.2258	9.60082
BH37	-3.9116	9.60082
BH39	-4.7879	9.60082
BH41	-5.7404	9.60082
BH43	-6.6929	9.60082
BH45	-7.6454	9.60082
BH47	-8.5979	9.60082
BH5	10.1051	10.2149
BH50	-9.55294	10.217
BH51	-10.1051	10.2149
BH54	-11.2634	10.217
BH55	-11.8143	10.264
BH6	9.55294	10.217
BH9	8.5979	9.60082
BJ10	8.1153	10.6912
BJ11	7.66445	10.3798
BJ12	7.2136	10.6912
BJ13	6.76275	10.3798
BJ14	6.3119	10.6912
BJ15	5.86105	10.3798
BJ16	5.4102	10.6912
BJ17	4.95935	10.3798
BJ18	4.5085	10.6912
BJ19	4.05765	10.3798
BJ2	11.2634	10.7631
BJ20	3.6068	10.6912
BJ21	3.15595	10.3798
BJ22	2.7051	10.6912
BJ23	2.25425	10.3798
BJ24	1.8034	10.6912
BJ25	1.35255	10.3798
BJ26	0.9017	10.6912
BJ27	0.45085	10.3798
BJ28	0	10.6912

Table 5-2. X and Y Pin List (Sheet 17 of 28)

Pin	X	Y
BJ29	-0.45085	10.3798
BJ30	-0.9017	10.6912
BJ31	-1.35255	10.3798
BJ32	-1.8034	10.6912
BJ33	-2.25425	10.3798
BJ34	-2.7051	10.6912
BJ35	-3.15595	10.3798
BJ36	-3.6068	10.6912
BJ37	-4.05765	10.3798
BJ38	-4.5085	10.6912
BJ39	-4.95935	10.3798
BJ4	10.7173	10.7631
BJ40	-5.4102	10.6912
BJ41	-5.86105	10.3798
BJ42	-6.3119	10.6912
BJ43	-6.76275	10.3798
BJ44	-7.2136	10.6912
BJ45	-7.66445	10.3798
BJ46	-8.1153	10.6912
BJ47	-8.56615	10.3798
BJ48	-9.017	10.6912
BJ5	10.1712	10.7631
BJ50	-9.62508	10.7631
BJ51	-10.1712	10.7631
BJ52	-10.7173	10.7631
BJ54	-11.2634	10.7631
BJ6	9.62508	10.7631
BJ8	9.017	10.6912
BJ9	8.56615	10.3798
BK1	11.8143	10.8736
BK11	7.66445	11.0026
BK13	6.76275	11.0026
BK15	5.86105	11.0026
BK17	4.95935	11.0026
BK19	4.05765	11.0026
BK21	3.15595	11.0026
BK23	2.25425	11.0026
BK25	1.35255	11.0026
BK27	0.45085	11.0026
BK29	-0.45085	11.0026

Table 5-2. X and Y Pin List (Sheet 18 of 28)

Pin	X	Y
BK31	-1.35255	11.0026
BK33	-2.25425	11.0026
BK35	-3.15595	11.0026
BK37	-4.05765	11.0026
BK39	-4.95935	11.0026
BK41	-5.86105	11.0026
BK43	-6.76275	11.0026
BK45	-7.66445	11.0026
BK47	-8.56615	11.0026
BK55	-11.8143	10.8736
BK9	8.56615	11.0026
BL10	8.1153	11.3141
BL12	7.2136	11.3141
BL14	6.3119	11.3141
BL16	5.4102	11.3141
BL18	4.5085	11.3141
BL2	11.4046	11.3141
BL20	3.6068	11.3141
BL22	2.7051	11.3141
BL24	1.8034	11.3141
BL26	0.9017	11.3141
BL28	0	11.3141
BL3	10.795	11.3141
BL30	-0.9017	11.3141
BL32	-1.8034	11.3141
BL34	-2.7051	11.3141
BL36	-3.6068	11.3141
BL38	-4.5085	11.3141
BL40	-5.4102	11.3141
BL42	-6.3119	11.3141
BL44	-7.2136	11.3141
BL46	-8.1153	11.3141
BL48	-9.017	11.3141
BL5	10.1854	11.3141
BL50	-9.5885	11.3141
BL51	-10.1854	11.3141
BL53	-10.795	11.3141
BL54	-11.4046	11.3141
BL6	9.5885	11.3141
BL8	9.017	11.3141

Table 5-2. X and Y Pin List (Sheet 19 of 28)

Pin	X	Y
C1	11.8143	-10.5302
C10	8.1153	-10.6912
C11	7.66445	-10.3798
C12	7.2136	-10.6912
C13	6.76275	-10.3798
C14	6.3119	-10.6912
C15	5.86105	-10.3798
C16	5.4102	-10.6912
C17	4.95935	-10.3798
C18	4.5085	-10.6912
C19	4.05765	-10.3798
C2	11.2634	-10.3694
C20	3.6068	-10.6912
C21	3.15595	-10.3798
C22	2.7051	-10.6912
C23	2.25425	-10.3798
C24	1.8034	-10.6912
C25	1.35255	-10.3798
C26	0.9017	-10.6912
C27	0.45085	-10.3798
C28	0	-10.6912
C29	-0.45085	-10.3798
C3	10.8697	-10.7631
C30	-0.9017	-10.6912
C31	-1.35255	-10.3798
C32	-1.8034	-10.6912
C33	-2.25425	-10.3798
C34	-2.7051	-10.6912
C35	-3.15595	-10.3798
C36	-3.6068	-10.6912
C37	-4.05765	-10.3798
C38	-4.5085	-10.6912
C39	-4.95935	-10.3798
C40	-5.4102	-10.6912
C41	-5.86105	-10.3798
C42	-6.3119	-10.6912
C43	-6.76275	-10.3798
C44	-7.2136	-10.6912
C45	-7.66445	-10.3798
C46	-8.1153	-10.6912

Table 5-2. X and Y Pin List (Sheet 20 of 28)

Pin	X	Y
C47	-8.56615	-10.3798
C48	-9.017	-10.6912
C5	10.3236	-10.7631
C50	-9.62508	-10.7631
C51	-10.1712	-10.7631
C52	-10.7173	-10.7631
C54	-11.2634	-10.7631
C6	9.77748	-10.7631
C7	9.23138	-10.7631
C9	8.56615	-10.3798
D1	11.8143	-9.93331
D11	7.6454	-9.60082
D13	6.6929	-9.60082
D15	5.7404	-9.60082
D17	4.7879	-9.60082
D19	3.9116	-9.60082
D2	11.2634	-9.82332
D21	3.2258	-9.60082
D23	2.3495	-9.60082
D25	1.397	-9.60082
D27	0.5207	-9.60082
D28	0	-10.0684
D29	-0.5207	-9.60082
D31	-1.397	-9.60082
D33	-2.3495	-9.60082
D35	-3.2258	-9.60082
D37	-3.9116	-9.60082
D39	-4.7879	-9.60082
D4	10.6919	-10.217
D41	-5.7404	-9.60082
D43	-6.6929	-9.60082
D45	-7.6454	-9.60082
D47	-8.5979	-9.60082
D50	-9.55294	-10.217
D51	-10.1051	-10.2149
D54	-11.2634	-10.217
D55	-11.8143	-10.264
D6	9.65048	-10.2297
D9	8.5217	-9.60082
E2	11.2634	-9.27722

Table 5-2. X and Y Pin List (Sheet 21 of 28)

Pin	X	Y
E28	0	-9.24522
E5	10.1585	-9.72172
E50	-9.5504	-9.60082
E52	-10.6761	-9.69747
E54	-11.2634	-9.67092
E55	-11.8143	-9.65441
E7	9.07415	-9.69632
F1	11.8143	-9.33641
F11	7.6454	-8.88962
F13	6.6929	-8.88962
F15	5.7404	-8.88962
F17	4.7879	-8.88962
F19	3.9116	-8.88962
F2	11.2634	-8.73112
F21	3.2258	-8.88962
F23	2.3495	-8.88962
F25	1.397	-8.88962
F27	0.5207	-8.88962
F29	-0.5207	-8.88962
F31	-1.397	-8.88962
F33	-2.3495	-8.88962
F35	-3.2258	-8.88962
F37	-3.9116	-8.88962
F39	-4.7879	-8.88962
F4	10.6919	-9.20102
F41	-5.7404	-8.88962
F43	-6.6929	-8.88962
F45	-7.6454	-8.88962
F47	-8.5979	-8.88962
F54	-11.2634	-9.12482
F55	-11.8143	-9.05751
F6	9.65048	-9.21372
F9	8.5217	-8.88962
G28	0	-8.53402
G49	-9.38987	-8.5979
G5	10.1585	-8.68032
G51	-10.1011	-8.5979
G53	-10.8801	-8.56615
G54	-11.5029	-8.56615
G7	9.07415	-8.68032

Table 5-2. X and Y Pin List (Sheet 22 of 28)

Pin	X	Y
H1	11.8143	-8.5617
H11	7.6454	-8.17842
H13	6.6929	-8.17842
H15	5.7404	-8.17842
H17	4.7879	-8.17842
H19	3.9116	-8.17842
H2	11.2459	-8.15188
H21	3.2258	-8.17842
H23	2.3495	-8.17842
H25	1.397	-8.17842
H27	0.5207	-8.17842
H28	0	-7.82282
H29	-0.5207	-8.17842
H31	-1.397	-8.17842
H33	-2.3495	-8.17842
H35	-3.2258	-8.17842
H37	-3.9116	-8.17842
H39	-4.7879	-8.17842
H4	10.6919	-8.18502
H41	-5.7404	-8.17842
H43	-6.6929	-8.17842
H45	-7.6454	-8.17842
H47	-8.5217	-8.17842
H53	-11.1915	-8.1153
H55	-11.8143	-8.1153
H6	9.65048	-8.19772
H9	8.5217	-8.17842
J11	7.6454	-7.46722
J13	6.6929	-7.46722
J15	5.7404	-7.46722
J17	4.7879	-7.46722
J19	3.9116	-7.46722
J2	11.5029	-7.66445
J21	3.2258	-7.46722
J23	2.3495	-7.46722
J25	1.397	-7.46722
J27	0.5207	-7.46722
J29	-0.5207	-7.46722
J3	10.8801	-7.66445
J31	-1.397	-7.46722

Table 5-2. X and Y Pin List (Sheet 23 of 28)

Pin	X	Y
J33	-2.3495	-7.46722
J35	-3.2258	-7.46722
J37	-3.9116	-7.46722
J39	-4.7879	-7.46722
J41	-5.7404	-7.46722
J43	-6.6929	-7.46722
J45	-7.6454	-7.46722
J48	-8.67867	-7.6454
J49	-9.38987	-7.6454
J5	10.1011	-7.5692
J51	-10.1011	-7.6454
J53	-10.8801	-7.66445
J54	-11.5029	-7.66445
J7	9.38987	-7.5692
J8	8.67867	-7.5692
K1	11.8143	-7.2136
K28	0	-7.11162
K3	11.1915	-7.2136
K53	-11.1915	-7.2136
K55	-11.8143	-7.2136
L10	7.96747	-6.6929
L13	6.6929	-6.75602
L15	5.7404	-6.75602
L17	4.7879	-6.75602
L19	3.9116	-6.75602
L2	11.5029	-6.76275
L21	3.2258	-6.75602
L23	2.3495	-6.75602
L25	1.397	-6.75602
L27	0.5207	-6.75602
L29	-0.5207	-6.75602
L3	10.8801	-6.76275
L31	-1.397	-6.75602
L33	-2.3495	-6.75602
L35	-3.2258	-6.75602
L37	-3.9116	-6.75602
L39	-4.7879	-6.75602
L41	-5.7404	-6.75602
L43	-6.6929	-6.75602
L46	-7.96747	-6.6929

Table 5-2. X and Y Pin List (Sheet 24 of 28)

Pin	X	Y
L48	-8.67867	-6.6929
L49	-9.38987	-6.6929
L5	10.1011	-6.6929
L51	-10.1011	-6.6929
L53	-10.8801	-6.76275
L54	-11.5029	-6.76275
L7	9.38987	-6.6929
L8	8.67867	-6.6929
M1	11.8143	-6.3119
M13	6.6929	-6.04482
M15	5.7404	-6.04482
M17	4.7879	-6.04482
M19	3.9116	-6.04482
M21	3.2258	-6.04482
M23	2.3495	-6.04482
M25	1.397	-6.04482
M27	0.5207	-6.04482
M28	0	-6.40042
M29	-0.5207	-6.04482
M3	11.1915	-6.3119
M31	-1.397	-6.04482
M33	-2.3495	-6.04482
M35	-3.2258	-6.04482
M37	-3.9116	-6.04482
M39	-4.7879	-6.04482
M41	-5.7404	-6.04482
M43	-6.6929	-6.04482
M53	-11.1915	-6.3119
M55	-11.8143	-6.3119
N10	7.96747	-5.7404
N12	7.25627	-5.7404
N2	11.5029	-5.86105
N28	0	-5.68922
N3	10.8801	-5.86105
N44	-7.25627	-5.7404
N46	-7.96747	-5.7404
N48	-8.67867	-5.7404
N49	-9.38987	-5.7404
N5	10.1011	-5.7404
N51	-10.1011	-5.7404

Table 5-2. X and Y Pin List (Sheet 25 of 28)

Pin	X	Y
N53	-10.8801	-5.86105
N54	-11.5029	-5.86105
N7	9.38987	-5.7404
N8	8.67867	-5.7404
P1	11.8143	-5.4102
P15	5.6642	-5.33362
P17	4.7879	-5.33362
P19	3.9116	-5.33362
P21	3.2258	-5.33362
P23	2.3495	-5.33362
P25	1.397	-5.33362
P27	0.5207	-5.33362
P29	-0.5207	-5.33362
P3	11.1915	-5.4102
P31	-1.397	-5.33362
P33	-2.3495	-5.33362
P35	-3.2258	-5.33362
P37	-3.9116	-5.33362
P39	-4.7879	-5.33362
P41	-5.6642	-5.33362
P53	-11.1915	-5.4102
P55	-11.8143	-5.4102
R10	7.96747	-4.7879
R12	7.25627	-4.7879
R13	6.54507	-4.7879
R15	5.83387	-4.7879
R2	11.5029	-4.95935
R28	0	-4.97802
R3	10.8801	-4.95935
R41	-5.83387	-4.7879
R43	-6.54507	-4.7879
R44	-7.25627	-4.7879
R46	-7.96747	-4.7879
R48	-8.67867	-4.7879
R49	-9.38987	-4.7879
R5	10.1011	-4.7879
R51	-10.1011	-4.7879
R53	-10.8801	-4.95935
R54	-11.5029	-4.95935
R7	9.38987	-4.7879

Table 5-2. X and Y Pin List (Sheet 26 of 28)

Pin	X	Y
R8	8.67867	-4.7879
T1	11.8143	-4.5085
T18	4.572	-4.3434
T20	3.81	-4.3434
T21	3.048	-4.3434
T23	2.286	-4.3434
T25	1.524	-4.3434
T27	0.762	-4.3434
T28	0	-4.3434
T29	-0.762	-4.3434
T3	11.1915	-4.5085
T31	-1.524	-4.3434
T33	-2.286	-4.3434
T35	-3.048	-4.3434
T36	-3.81	-4.3434
T38	-4.572	-4.3434
T53	-11.1915	-4.5085
T55	-11.8143	-4.5085
U10	7.96747	-3.9116
U12	7.25627	-3.9116
U13	6.54507	-3.9116
U15	5.83387	-3.9116
U17	5.12267	-3.9116
U2	11.5029	-4.05765
U3	10.8801	-4.05765
U39	-5.12267	-3.9116
U41	-5.83387	-3.9116
U43	-6.54507	-3.9116
U44	-7.25627	-3.9116
U46	-7.96747	-3.9116
U48	-8.67867	-3.9116
U49	-9.38987	-3.9116
U5	10.1011	-3.9116
U51	-10.1011	-3.9116
U53	-10.8801	-4.05765
U54	-11.5029	-4.05765
U7	9.38987	-3.9116
U8	8.67867	-3.9116
V1	11.8143	-3.6068
V18	4.572	-3.6195

Table 5-2. X and Y Pin List (Sheet 27 of 28)

Pin	X	Y
V20	3.81	-3.6195
V21	3.048	-3.6195
V23	2.286	-3.6195
V25	1.524	-3.6195
V27	0.762	-3.6195
V28	0	-3.6195
V29	-0.762	-3.6195
V3	11.1915	-3.6068
V31	-1.524	-3.6195
V33	-2.286	-3.6195
V35	-3.048	-3.6195
V36	-3.81	-3.6195
V38	-4.572	-3.6195
V53	-11.1915	-3.6068
V55	-11.8143	-3.6068
W10	7.96747	-3.2258
W12	7.25627	-3.2258
W13	6.54507	-3.2258
W15	5.83387	-3.2258
W17	5.12267	-3.2258
W2	11.5029	-3.15595
W3	10.8801	-3.15595
W39	-5.12267	-3.2258
W41	-5.83387	-3.2258
W43	-6.54507	-3.2258
W44	-7.25627	-3.2258
W46	-7.96747	-3.2258
W48	-8.67867	-3.2258
W49	-9.38987	-3.2258
W5	10.1011	-3.2258
W51	-10.1011	-3.2258
W53	-10.8801	-3.15595
W54	-11.5029	-3.15595
W7	9.38987	-3.2258
W8	8.67867	-3.2258
Y1	11.8143	-2.7051
Y18	4.572	-2.8956
Y20	3.81	-2.8956
Y21	3.048	-2.8956
Y23	2.286	-2.8956

Table 5-2. X and Y Pin List (Sheet 28 of 28)

Pin	X	Y
Y25	1.524	-2.8956
Y27	0.762	-2.8956
Y28	0	-2.8956
Y29	-0.762	-2.8956
Y3	11.1915	-2.7051
Y31	-1.524	-2.8956
Y33	-2.286	-2.8956
Y35	-3.048	-2.8956
Y36	-3.81	-2.8956
Y38	-4.572	-2.8956
Y53	-11.1915	-2.7051
Y55	-11.8143	-2.7051

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6 Package Information

The SoC comes in Flip-Chip Ball Grid Array (FCBGA) package.

6.1 Package Attributes

Table 6-1. Package Attributes

Category	SoC
Package	Flip-Chip Ball Grid Array (FCBGA)
Type	24x25 mm^2 8L Type-3
I/O count	616
Ball count	1090
Ball pitch	0.546 mm
Z-height	1.344 mm +/-0.092

6.2 Package Drawings

Figure 6-1. Package Mechanical Drawing - Part 1 of 3

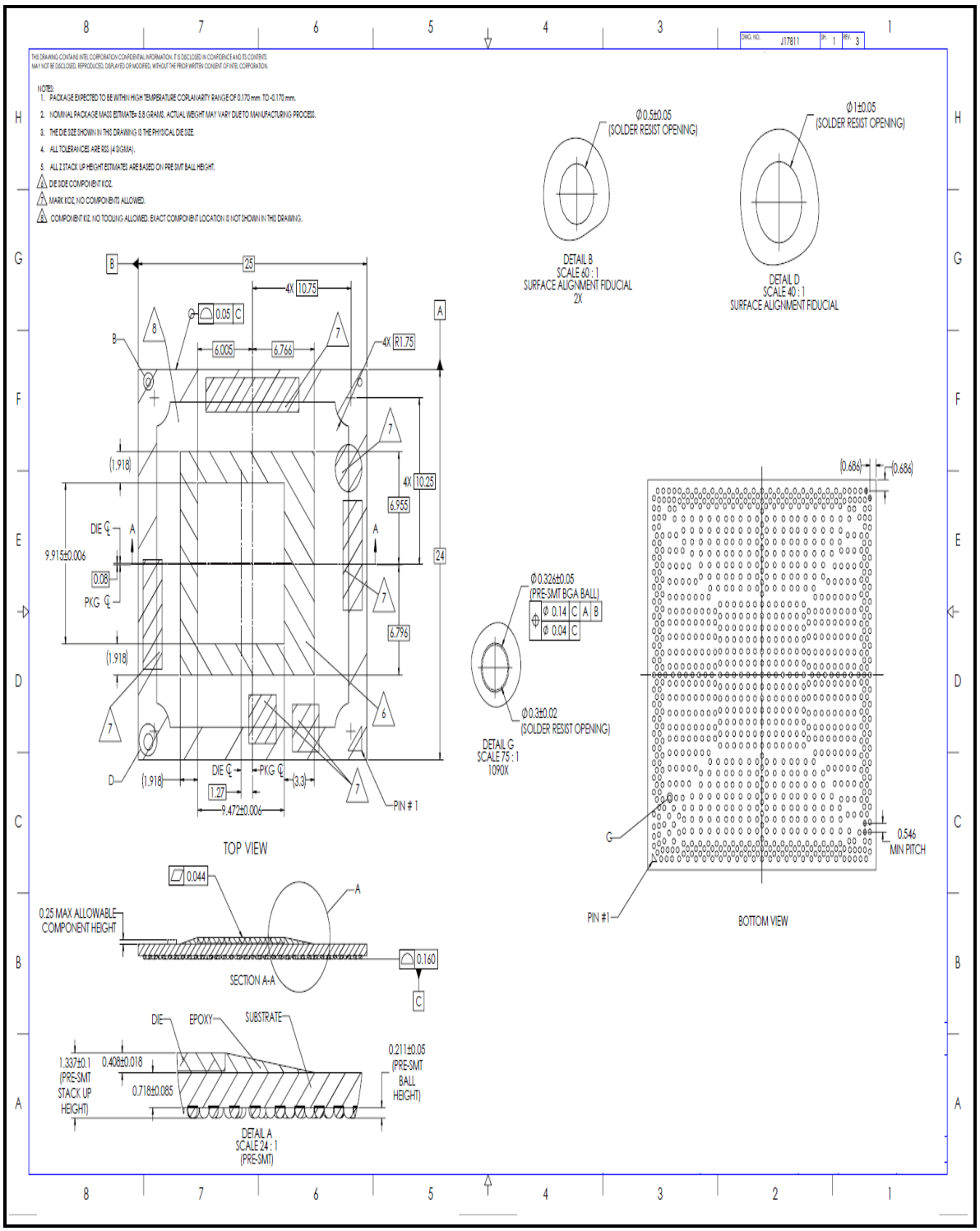


Figure 6-2. Package Mechanical Drawing Part 2 of 2

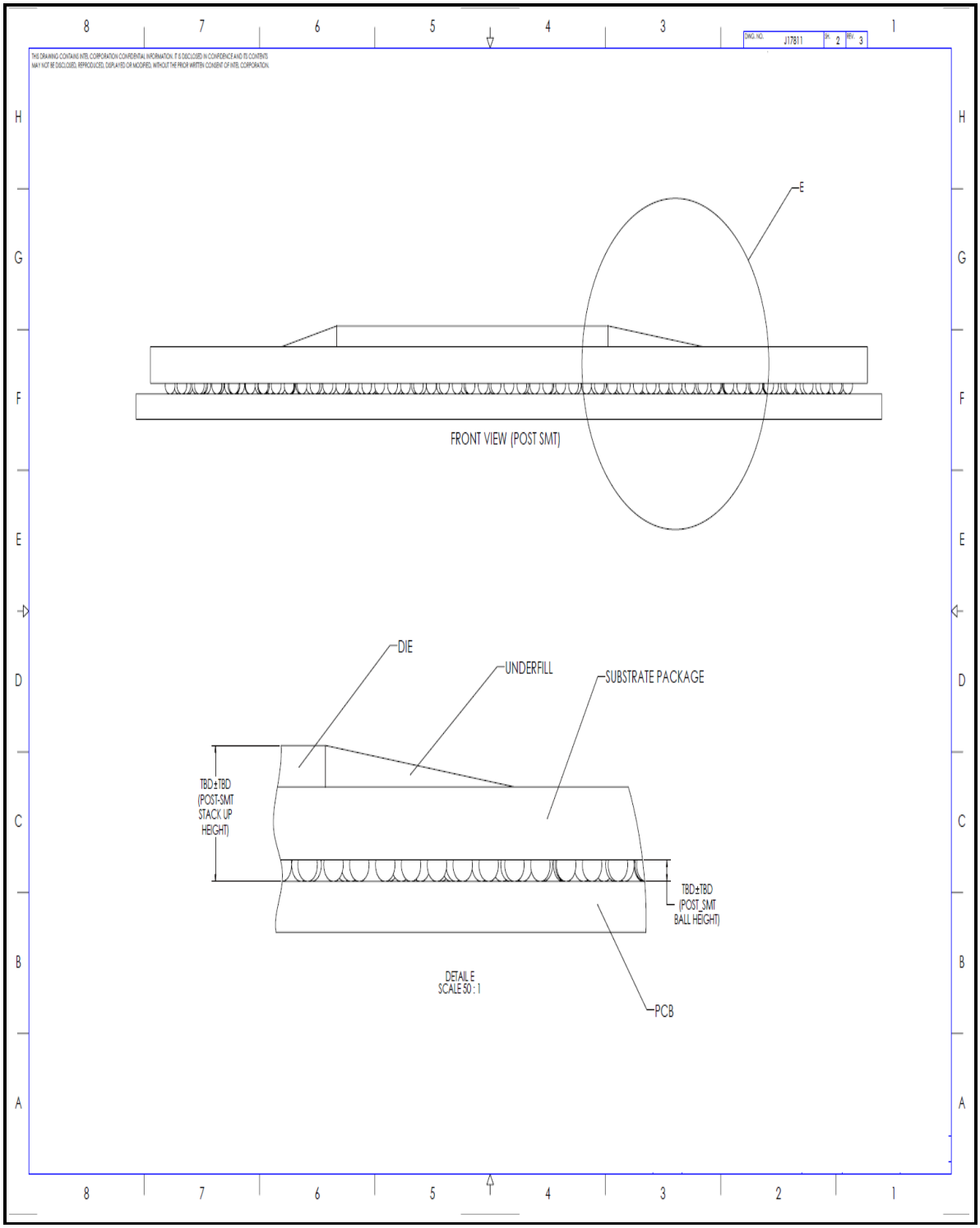
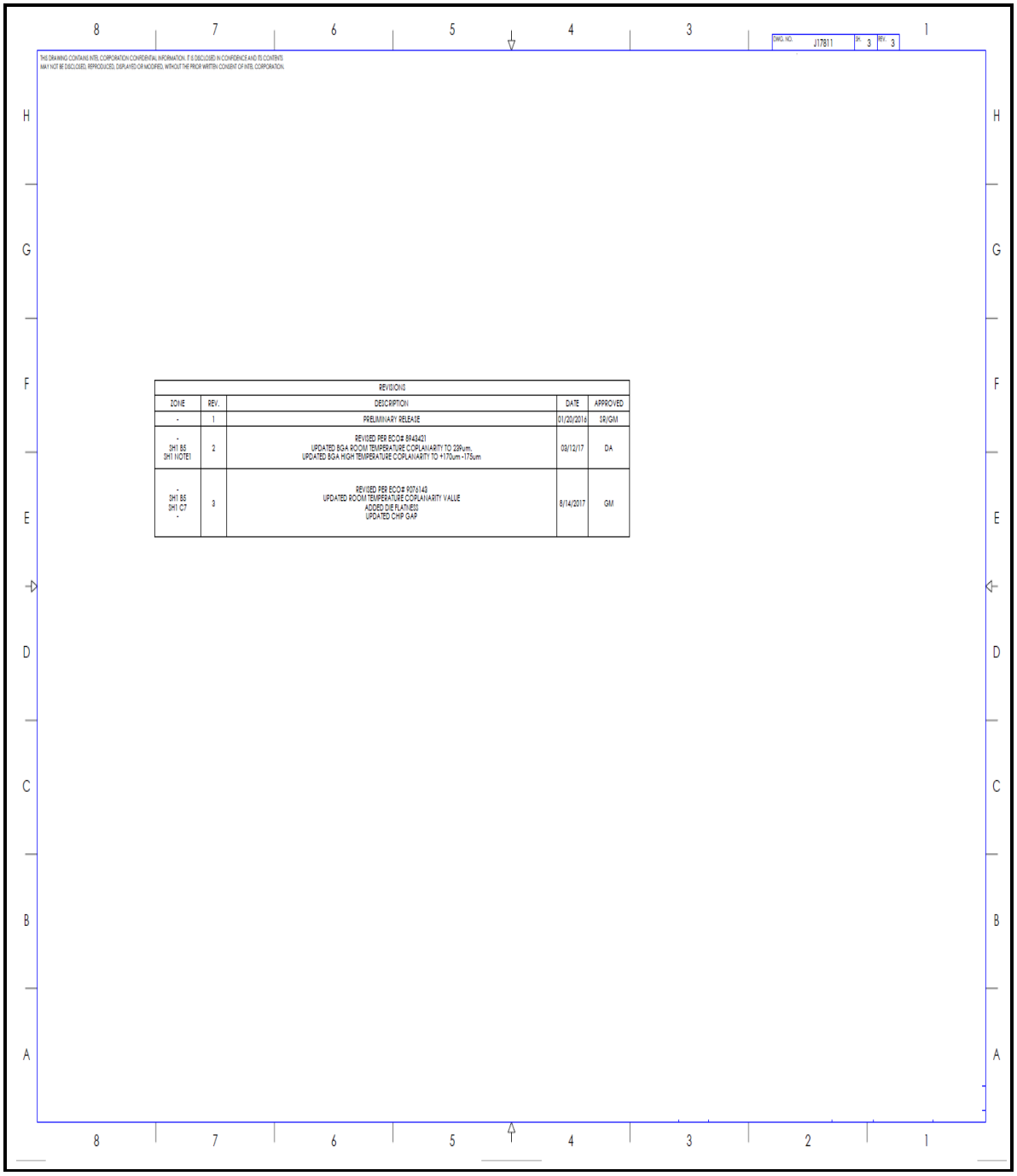


Figure 6-3. Package Mechanical Drawing Part 3 of 3



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