

6th Generation Intel® Core™ Processor, Intel® Pentium® Processor, Intel® Celeron® Processor, and Intel® Xeon® Processor E3 v5 Family (Formerly Known as Skylake) – Desktop, Workstation, and Mobile Platforms

External Design Specification (EDS) Addendum

May 2016

Revision 001

Document Number: 334408-001US



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Revision History

Date	Revision	Description
May 2016	001	Initial release

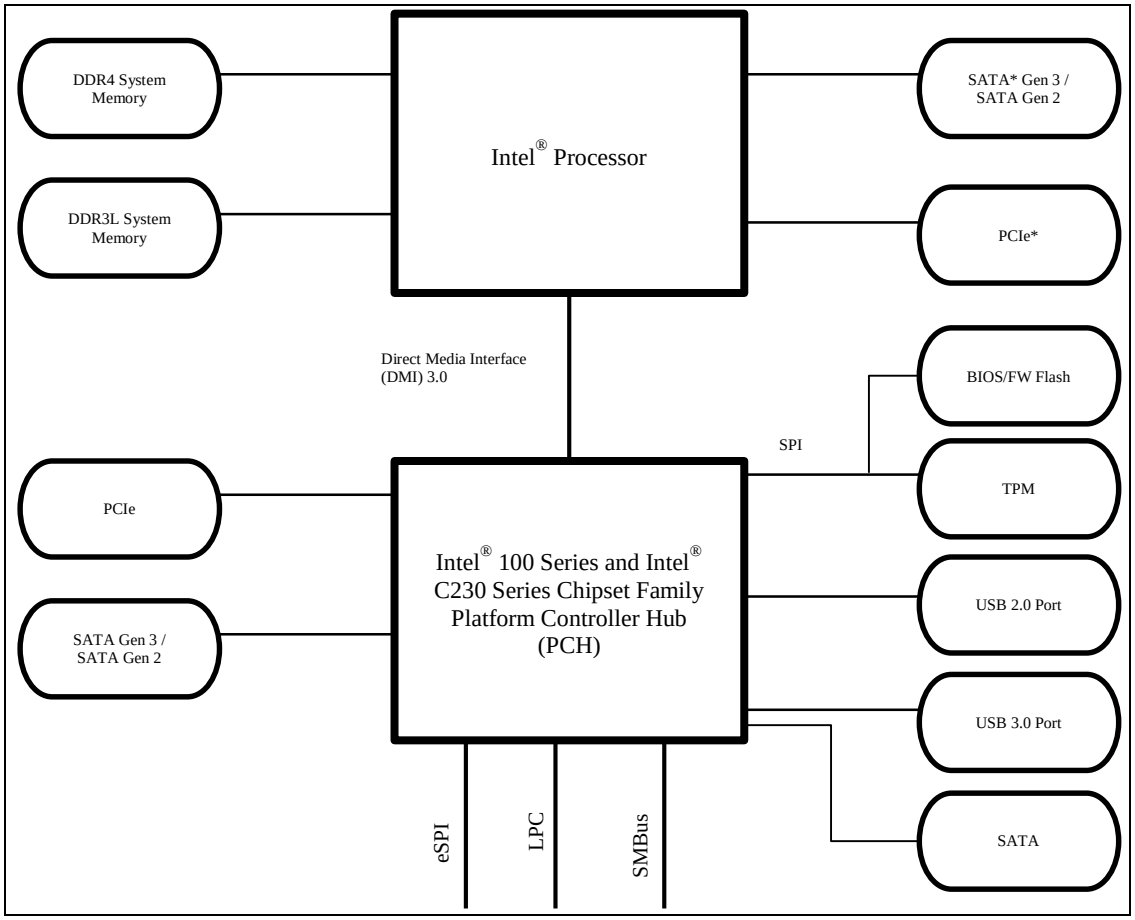
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1 Introduction

This External Design Specification (EDS) Addendum is a supplement to the 6th Generation Intel® Core™ Processor Family and Intel® Xeon® Processor E3-1200 v5 Product Family (formerly known as Skylake) Processor External Design Specification. It contains the additional electrical specifications, signal information, interface functional descriptions, additional feature information, and configuration registers pertinent to the implementation and operation of the H-processor line and S-processor line.

The H-processor line and S-processor line are offered in a 2-Chip Platform and connected to a discrete Platform Controller Hub (PCH) chip on the motherboard.

Figure 1. H-Processor and S-Processor Line Platform



The processors are manufactured based on Intel's 14 nm process technology that increases CPU performance and improves graphics micro-architecture.



Two DIMMs per DDR4 and DDR3L channel with ECC/ Non-ECC are supported on this platform.

1.1 Terminology

Table 1. Terminology

Term	Description
DIMM	Dual In-line Memory Module
DMI	Direct Media Interface
DDR3L	DDR3 Low Voltage
DDR4	Fourth-Generation Double Data Rate SDRAM Memory Technology
ECC	Error Correction Code - used to fix DDR transactions errors
EDRAM	Embedded Dynamic Random Access Memory
IBP	Intel Business Portal
OPC	On Package Cache (eDRAM)
PCH	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features. The PCH may also be referred as “chipset”.
Processor Core	The term “processor core” refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the LLC.
RVP	Reference Validation Platform provided to customers as the Customer Reference Board. RVP7/8/11 is for U/S/H-line platforms.
SDP	Scenario Design Power
TBD	To Be Determined
TDP	Thermal Design Power
T_{jmax}	Maximum junction temperature rating (°C)
TDC	Thermal Design Current
TDP	Thermal Design Power
TPM	Trusted Platform Module
VCC	Common Collector Voltage (V+)

1.2 Reference Documents

Table 2. Reference Documents

Document	Document Number in IBP
Skylake-H Platform Design Guide	546884
Guide to Skylake Power Delivery Documents	552379
Intel® 100 Series Chipset Family PCH Datasheet, Vol. 1	332690
Intel® 100 Series Chipset Family PCH Datasheet, Vol. 2	332691
Skylake PCH-H(SKL-H/S) IBIS Model	545919
Skylake Platform Power Architecture Guide for the H and S Processor Lines	543842
Skylake Platform Power Architecture Guide for the U- and Y- Processor Lines	543977
6th Generation Intel® Processor Datasheet for S-Platforms, Volume 1 of 2	332687
6th Generation Intel® Processor Datasheet for S-Platforms, Volume 2 of 2	332688
6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2	332986
6th Generation Intel® Processor Datasheet for H-Platforms, Volume 2 of 2	332987
Skylake Processor BSDL	550040
Skylake Platforms Design-In	556527
Skylake Mobile Thermal Mechanical Design Guide for Embedded Applications	554457
Skylake S Platform and Greenlow-WS Platform – Design Guide	543611

1.3 Supported Package and Die Plan

Table 3. Processor Lines Package and Die Plan

Processor Line	Die Type	Package Type (mm)	TDP (W)	PCH
H	4+4e	BGA 1440 (42x28x1.49)	45 W	PCH
H	4+2	BGA1440 (42x28x1.46)	25W, 35 W, 45 W	PCH
S	4+2	LGA 1151 (37.5x37.5x4.4)	95 W, 65 W, 35 W	PCH
S	2+2	LGA 1151 (37.5x37.5x4.4)	35 W, 65 W	PCH

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2 Interface

2.1 System Memory Interface and Supported Technology

Refer to Table 2, *6th Generation Intel® Processor Datasheet for S-Platforms, Volume 1 of 2* (IBP Doc# 332687) and *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986) for further information.

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3 Thermal Management

3.1 Processor Thermal Management

The thermal solution provides component-level and system-level thermal management. To allow optimal operation and long-term reliability of Intel® processor based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature (T_{jmax}) specification at the maximum Thermal Design Power (TDP).
- Conforms to system constraints, such as system acoustics, system skin temperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

Note: This section supplements the information in the following documents: *6th Generation Intel® Processor Datasheet for S-Platforms, Volume 1 of 2* (IBP Doc# 332687) and *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986). For further details on parameters, refer to the aforementioned documents.

3.2 S/H-Processor Line TDP Specifications

Table 3. TDP Specifications

Segment and Package	Processor Intel® Architecture Cores, Graphics Configuration and TDP	Configuration	Processor Intel® Architecture Core Frequency	Graphics Core Frequency	TDP (W)	SDP (W)
H-Processor Line BGA	Quad Core GT2 25W	Base	1.9 GHz to 2.0 GHz	350 MHz to 1 GHz	25	NA
H-Processor Line BGA	Dual Core GT2/GT1 25W	Base	1.6 GHz to 1.9 GHz	350 MHz to 0.95 GHz	25	NA
H-Processor Line BGA	Dual Core GT2/GT1 35W	Base	2.4 GHz to 2.7 GHz	350 MHz to 0.95 GHz	35	NA



3.3 H-Processor Line TDP Specifications

Table 4. Package Turbo Specifications

Segment and Package	Processor Intel® Architecture Cores, Graphics Configuration and TDP	Parameter	Min.	Hardware Default	Max.	Units
H-Processor Line BGA	Quad Core GT2 25 W	Power Limit 1 Time (PL1 Tau)	0.01	1	448	s
		Power Limit 1 (PL1)	N/A	25	N/A	W
		Power Limit 2 (PL2)	N/A	1.25 x 25	N/A	W
	Dual Core GT2/GT1 35W	Power Limit 1 Time (PL1 Tau)	0.01	1	448	s
		Power Limit 1 (PL1)	N/A	35	N/A	W
		Power Limit 2 (PL2)	N/A	1.25 x 35	N/A	W
	Dual Core GT2/GT1 25W	Power Limit 1 Time (PL1 Tau)	0.01	1	448	s
		Power Limit 1 (PL1)	N/A	25	N/A	W
		Power Limit 2 (PL2)	N/A	1.25 x 25	N/A	W

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4 Electrical Specifications

4.1 Processor Intel® Architecture Core (VCC) and VCCGT/VCCGT$_X$ Current Specifications

Note: This section supplements the information in the following documents: *6th Generation Intel® Processor Datasheet for S-Platforms, Volume 1 of 2* (IBP Doc# 332687) and *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986). For further details on other Intel® architecture core (VCC) and **VCCGT/VCCGTX** parameters not listed in Table 5, refer to the aforementioned documents.

Table 5. Processor Graphics (VccGT and VccGT-X) Supply Current Specifications

Symbol	Parameter	Segment	Max.	Unit
ICCMAX	Maximum Processor Intel® Architecture Core I_{CC}	H Quad Core GT2 25 W	50	A
		H Dual Core GT2/GT1 35 W	50	A
		H Dual Core GT2/GT1 25 W	30	A
Iccmax_GT/ **Iccmax**_GTX	Maximum Current for Processor Graphic Rail	H Quad Core GT2 25 W	38	A
		H Dual Core GT2/GT1 35 W	48	A
		H Dual Core GT2/GT1 25 W	38	A

4.2 EDRAM Power Signals for Processor

Refer to the *Skylake Platform Power Architecture Guide for the H and S Processor Lines* (IBP Doc# 543842) and *Skylake Platform Power Architecture Guide for the U- and Y-Processor Lines* (IBP Doc# 543977) for power requirements and specifications that support all SKUs in processors which have EDRAM.

In platforms that are designed specifically for the processor *without* EDRAM, disconnect the power signals listed in Table 6.

Table 6. EDRAM Power Signals

Power Signal
VccGTX
VccOPC
VccOPC_1P8
VccEOPIO



Note: Platforms that do not support processors with EDRAM are unable to boot up when using the processor with EDRAM.

For more information on platform design types that support processors with and without EDRAM, refer to the Reference Validation Platform (RVP) RVP7, RVP8, and RVP11.

4.3 H-Processor Power Rails

The **VDDQC/VCCVDDQ_CLK** is connected to **VDDQ/+VCCDU** through an LP filter.

The **+VCCVDDQ_CLK** and the **+VCCDU** are connected directly with the copper trace on RVP11.

4.4 TDC Specification

Table 7. Thermal Design Current (TDC) Specification

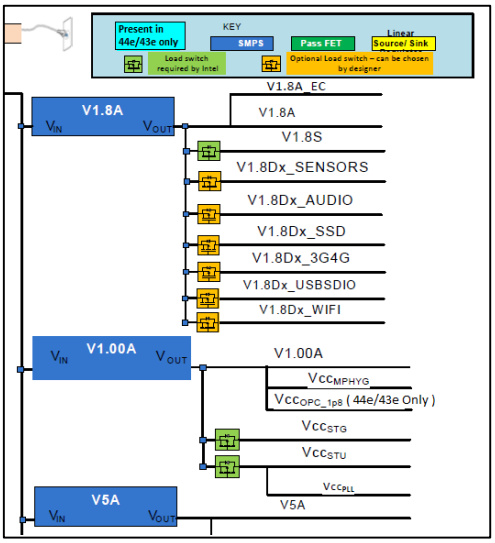
Parameter	Vcc	VccGT	VCCSA
H-Line 4+2 25W			
TDC[A]	34	25	10
Iccmax current 10 ms max.	Refer to the EDS (Doc# 332986) for the VCCSA Iccmax numbers Refer to EDS Addendum (Doc#334408) for Vcc/VccGT Iccmax numbers		
Iccmax_App current	85% of Iccmax	N/A	
Di (Iccmax transient) [A] (Note 6)	43	27	3
Di (Iccmax_App transient)	Iccmax_App di = Iccmax_App - (Iccmax - Iccmax di)	N/A	
dt (ns) (Slew time for the di step) (Note 3)	65	65	200
H-Line 2+2 25W			
TDC[A]	23	25	10
Iccmax current 10 ms max.	Refer to the EDS (Doc# 332986) for the VCCSA Iccmax numbers Refer to EDS Addendum (Doc#334408) for Vcc/VccGT Iccmax numbers		
Iccmax_App current	85% of Iccmax	N/A	
Di (Iccmax transient) [A] (Note 6)	26	27	3
Di (Iccmax_App transient)	Iccmax_App di = Iccmax_App - (Iccmax - Iccmax di)	N/A	
dt (ns) (Slew time for the di step) (Note 3)	65	65	200
H-Line 2+2 35W			
TDC[A]	33	22	10
Iccmax current 10 ms max.	Refer to the EDS (Doc# 332986) for the VCCSA Iccmax numbers Refer to EDS Addendum (Doc#334408) for Vcc/VccGT Iccmax numbers		
Iccmax_App current	85% of Iccmax	NA	NA
(Iccmax transient) [A] (Note 6)	43	34	3
Di (Iccmax_App transient)	Iccmax_App di = Iccmax_App - (Iccmax - Iccmax di)	N/A	
Di (Iccmax_App transient)	65	65	200

NOTES:

1. **Iccmax_APP** is not a spec. It is a characterization of limited samples using limited set of benchmarks under default PL1 and PL2 conditions. It aims to show more realistic current envelope that can be exceeded.
2. Simulated at processor motherboard pads. This parameter is not tested.
3. The time durations given here are for VR design only.
4. If using Psys, Intel recommends sizing the VR's thermal solution to support the domains equivalent PL2_max TDC currents. By continually monitoring the platform's total power dissipation, Psys optimizes the AC adapter's PsysPL2 power capability, maximizing PL2 power delivered to the CPU (e.g. PL2_maxoperation) when rest-of-platform power headroom exists. Note: PsysPL2 is the sum of PL2 and ROP as measured at the power input. As ROP is reduced, PL2 may increase but PsysPL2 remains constant.
5. The SET_VR_TDC_CONFIG mailbox register in the BIOS assumes a default tau of 1ms.
6. Subject to change. Vcc can be estimated at 85% of Iccmax. VccGT can be estimated at 70% of Iccmax.

4.5 H-Line Platform Power Map and Rail Requirements

Figure 2. Processor Platform Power Map - H –Line



Note: For the complete figure, refer to Figure 3-1 in *Skylake Platform Power Architecture Guide for the H and S Processor Lines* (IBP Doc# 543842).

4.5.1 IMVP8 Voltage and Current Requirements - H-Line

Table 8. General Processor VR Parameters for the H-line

Parameter	Description	Power Rail	H-Line CPU SKU 42/22/21	H-Line CPU SKU 44e/43e	Notes
R_DC_LL (mV/A) MAX	Loadline slope within the VR regulation loop capability 0-1 kHz	Vcc	1.8	1.6	Decoupling recommendations and associated VR bandwidth requirements are shown in the Skylake Platform Design Guide.
		VccGT	2.65	1.4	
		VccGTX		6.0	
		VccSA	10	6	
R_AC_LL (mV/A) MAX	Loadline slope in response to dynamic load increase events 1 kHz-1 MHz	Vcc	1.8	1.6	
		VccGT	2.65	1.4	
		VccGTX		6.0	
		VccSA	10	6	

Note: For more information, refer to Table 4-1 in *Skylake Platform Power Architecture Guide for the H and S Processor Lines* (IBP Doc# 543842).

Table 9. OPC Processor VR Design Values

Parameter	Vcc	VccGT	VccGTX	VccSA
H-line 44e/43e 45W				
TDC [A] with Extreme PL2 setting from Table 8-1	56	70	9	7
TDC [A] with Default PL2 setting from Table 8-1	TBD	TBD	TBD	TBD

Note: For more information, refer to Table 4-4 in *Skylake Platform Power Architecture Guide for the H and S Processor Lines* (IBP Doc# 543842).

Table 10. Server and Workstation SKUs

Parameter	Vcc	VccGT	VccGTX	VccSA
H-line 44e/43e 35W				
TDC [A] with Extreme PL2 setting from Table 8-1	46	63	TBD	7
TDC [A] with Default PL2 setting from Table 8-1	TBD	TBD	TBD	7

Note: For more information, refer Table 4-5 in *Skylake Platform Power Architecture Guide for the H and S Processor Lines* (IBP Doc# 543842).

4.5.2 AC Adapter Considerations

Table 11. Power Levels (PLx) for the Different SKUs

SKU	PL1 (W)	Default PL2 & PL4 Pairs		Extreme PL2 and PL4 Pairs	
		PL2 (W)	PL4 (W)	PL2 (W)	PL4 (W)
Mobile Workstation 44e/43e 45W	45	60	87	115	183
Mobile Workstation 44e/43e 35W	35	44	TBD	96	135

Note: For more information, refer to Table 8-1 in *Skylake Platform Power Architecture Guide for the H and S Processor Lines* (IBP Doc# 543842).



4.5.3 GT2/3/4 Graphics Frequency

Table 12. GT2/3/4 Graphics Frequency (S/H/U/Y-Processor Line)

Segment	GT Unslice	GT Unslice + 1 GT Slice	GT Unslice + 2 GT Slice	GT Unslice + 3 GT Slice
H - quad core GT4/GT3+OPC	GT Max. Dynamic frequency	[GT Unslice only] - (1 or 2)BIN	[GT Unslice + 1 Slice] - (1or2)BIN	[GT Unslice + 2 Slice] - (1or2)BIN

Note: For more information, refer to *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

4.5.4 H-Processor Line Thermal and Power Specifications

Table 13. TDP Specifications (H-Processor Line)

Segment and Package	Processor Intel® Architecture Cores, Graphics Configuration, and TDP	Configuration	Processor Intel® Architecture Core Frequency	Graphics Core Frequency	TDP (W)	SDP (W)
H-Processor Line BGA	Quad Core GT4/GT3 35W with OPC	Base	2.5 GHz to TBD GHz	350 MHz to 1.05 GHz	35	N/A
		LPM	800 MHz	350 MHz	34.5	
	Quad Core GT4/GT3 45W with OPC	Base	2.3 GHz to 3 GHz	350 MHz to 1.05 GHz	45	N/A
		Configurable TDPDown/ LFM	1.9 to 2.5 MHz		35	
		LPM	800 MHz	350 MHz	34.5	
	Quad Core GT4/GT3 35W with OPC	Base	2.7 GHz	350 GHz to 0.9 GHz	35	N/A
		LPM	800 MHz	350 MHz	34.5	

Note: For more information, refer to Table 5-2 in *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

Table 14. Package Turbo Specifications (H-Processor Line)

Segment and Package	Processor Intel® Architecture Cores, Graphics Configuration, and TDP	Parameter	Min.	Hardware Default	Max.	Units
H-Processor Line BGA	Quad Core GT4/GT3 45W with OPC	Power Limit 1 Time (PL1 Tau) Power Limit 1 (PL1) Power Limit 2 (PL2)	0.01 N/A N/A	1 45 1.25*45	448 N/A N/A	S W W

Note: For more information, refer to Table 5-3 in *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

4.5.5 Processor Power Rails DC Specifications

Table 15. Processor Intel® Architecture Core (Vcc) Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1]
I_{CCMAX}	Maximum Processor Intel® Architecture Core I_{CC}	H(35W) - quad core GT4/GT3+OPC	-	-	57[15]	A	4, 6, 7, 11
		H(45) - quad core GT4/GT3+OPC	-	-	74[15]		
DC_LL	Loadline slope within the VR regulation loop capability	Y-processor line U-dual core GT2 U-dual core GT3+OPC H-dual/quad core GT2 H-quad core GT4/GT3+OPC S-processor line	—	4.7 — — — — —	5.9 2.4 2.4 1.8 1.6 2.1	mΩ	10, 13, 14

Note: For more information, refer to Table 7-2 in *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

Table 16. Processor Graphics (VccGT and VccGT-X) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1]
ICCMax_GT/ICCMax_GTx	Max. Current for Processor Graphics Rail	H(35W) - quad core GT4/GT3+OPC	-	-	94/20(GTx)11	A	6
		H(45W) - quad core GT4/GT3+OPC	-	-	94/20(GTx)11		
DC_LL	vccGT Loadline slope	Y-processor line U-dual core GT2 U-dual core GT3+OPC H-dual/quad core GT2 H-quad core GT4/GT3+OPC S-processor line	— — — — — —	4.2 — — — — —	5.7 3.1 2/6.0(GTx) 2.65 1.4/6.0(GTx) 3.1	mΩ	7, 9, 10



Note: For more information, refer to Table 7-3 in *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

4.5.6 Vcc_{SA} DC Specifications

Table 17. System Agent (VccSA) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1,2]
I_{CCMAX_VCCSA}	Max. Current for VCCSA Rail	Y-processor line U-dual core GT2 U-dual core GT3+OPC H-dual/quad core GT2 H-quad core GT4/GT3+OPC S-processor line	— — — — — —	— — — — — —	4.1 4.5 5.1 11.1 8 11.1	A	
DC_LL	vccSA Loadline	Y-processor line U-dual core GT2 U-dual core GT3+OPC H-dual/quad core GT2 H-quad core GT4/GT3+OPC	— — — — —	14 — — — —	18 10.3 10.3 10 6	mΩ	6,7

Note: For more information, refer to Table 7-5 in *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

4.5.7 Vcc_{PLL} DC Specifications

Table 18. Processor PLL OC (VccPLL_OC) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min.	Typ.	Max.	Unit	Note[1,2]
ICCMAX_VCCPLL_OC	Max. Current for VCCPLL_OC Rail	Y U-dual core GT2 U-dual core GT3+OPC H-dual/quad core GT2 H-quad core GT4/GT3+OPC S-dual core GT2 S-quad core GT2	— — — — — — —	— — — — — — —	100 100 120 130 150 100 130	mA	

Note: For more information, refer to Table 7-15 in *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

4.5.8 Package Mechanical Specifications

Table 19. Package Mechanical Attributes

Package	Parameter	Y-Processor Line	U-Processor Line		H-Processor Line		S-Processor Line
		Dual Core	Dual Core	Dual Core	Quad Core	Quad Core	Quad Core/

		GT2	GT3+OPC	GT2	GT4/GT3+OPC	GT2	Dual Core GT2

Note: The details for this table, refer to Table 8-1 in *6th Generation Intel® Processor Datasheet for H-Platforms, Volume 1 of 2* (IBP Doc# 332986).

4.6 USB On-The-Go Specification

The embedded 6th generation Intel® processor for S-Platform SKU does not support USB On-The-Go specification mentioned in *Intel® 100 Series Chipset Family Platform Controller Hub (PCH) Datasheet – Volume 1 of 2* (IBP Doc# 332690) and *Skylake S Platform and Greenlow-WS Platform – Design Guide* (IBP Doc# 543611).

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5 Processor Listings

Table 20. H-Processor Family Listing/Package BGA1440

Spec #	Processor Number	Stepping	Cache Size (MB)	Func. Core	Integrated Graphics Core SKU	Max. Turbo Freq. Rate (GHz)	Memory DDR3L (MHz)	Memory DDR4 (MHz)	Core Freq. (GHz)	Graphic Freq. (GHz)	TDP	ECC	Package
SR2TT	E3-1578LV5	N-0	8	4	4	1 Core : 3.4 2 Core : 3.3 3 Core : 3.2 4 Core : 3.2	1600	2133	2.0	0.70	45W	Yes	BGA1440
SR2TU	E3-1558LV5	N-0	8	4	3	1 Core : 3.3 2 Core : 3.2 3 Core : 3.1 4 Core : 3.1	1600	2133	1.9	0.65	45W	Yes	BGA1440
SR2QT	E3-1515MV5	N-0	8	4	4	1 Core : 3.7 2 Core : 3.6 3 Core : 3.5 4 Core : 3.3	1600	2133	2.8	0.35	45 W	Yes	BGA1440
SR2FN	E3-1505MV5	R-0	8	4	2	1 Core : 3.7 2 Core : 3.5 3 Core : 3.4 4 Core : 3.3	1600	2133	2.8	0.35	45 W	Yes	BGA1440
SR2E0	E3-1505LV5	R-0	8	4	2	1 Core : 2.8 2 Core : 2.7 3 Core : 2.6 4 Core : 2.5	1600	2133	2.0	0.35	25 W	Yes	BGA1440
SR2DT	i7-6820EQ	R-0	8	4	2	1 Core : 3.5 2 Core : 3.4 3 Core : 3.3 4 Core : 3.2	1600	2133	2.8	0.35	45 W	No	BGA1440
SR2DW	i7-6822EQ	R-0	8	4	2	1 Core : 2.8 2 Core : 2.7 3 Core : 2.6 4 Core : 2.5	1600	2133	2.0	0.35	25 W	No	BGA1440
SR2DU	i5-6440EQ	R-0	6	4	2	1 Core : 3.4 2 Core : 3.3 3 Core : 3.2 4 Core : 3.1	1600	2133	2.7	0.35	45 W	No	BGA1440
SR2DY	i5-6442EQ	R-0	6	4	2	1 Core : 2.7 2 Core : 2.6 3 Core : 2.5 4 Core : 2.4	1600	2133	1.9	0.35	25 W	No	BGA1440
SR2DV	i3-6100E	R-0	3	2	2	1 Core : 2.7 2 Core : 2.7	1600	2133	2.7	0.35	35 W	Yes	BGA1440
SR2DX	i3-6102E	R-0	3	2	2	1 Core : 1.9 2 Core : 1.9	1600	2133	1.9	0.35	25 W	Yes	BGA1440
SR2GH	G3900E	R-0	2	2	1	1 Core : 2.4 2 Core : 2.4	1600	2133	2.4	0.35	35 W	Yes	BGA1440
SR2GJ	G3902E	R-0	2	2	1	1 Core : 1.6 2 Core : 1.6	1600	2133	1.6	0.35	25 W	Yes	BGA1440

Table 21. S-Processor Family Listing/Package LGA1151

Spec #	Processor Number	Stepping	Cache Size (MB)	Func. Core	Integrated Graphics Core SKU	Max. Turbo Freq. Rate (GHz)	Memory DDR3L (MHz)	Memory DDR4 (MHz)	Core Freq. (GHz)	Graphic Freq (GHz)	TDP	ECC	Package
SR2LK	E3-1275V5	R-0	8	4	2	1 Core: 4.0 2 Core: 3.9 3 Core: 3.8 4 Core: 3.7	1600	2133	3.6	0.4	80 W	Yes	LGA1151
SR2LJ	E3-1225V5	R-0	8	4	2	1 Core: 3.7 2 Core: 3.6 3 Core: 3.5 4 Core: 3.4	1600	2133	3.3	0.4	80 W	Yes	LGA1151
SR2LQ	E3-1268LV5	R-0	8	4	2	1 Core: 3.4 2 Core: 3.3 3 Core: 3.2 4 Core: 3.1	1600	2133	2.4	0.35	35 W	Yes	LGA1151
SR2L2	i7-6700	R-0	8	4	2	1 Core: 4.0 2 Core: 3.9 3 Core: 3.8 4 Core 3.7	1866	2133	3.4	0.35	65 W	No	LGA1151
SR2LP	i7-6700TE	R-0	8	4	2	1 Core: 3.4 2 Core: 3.3 3 Core: 3.2 4 Core: 3.1	1600	2133	2.4	0.35	35 W	No	LGA1151
SR2L6	i5-6500	R-0	6	4	2	1 Core: 3.6 2 Core: 3.5 3 Core: 3.4 4 Core 3.3	1866	2133	3.2	0.35	65 W	No	LGA1151
SR2LR	i5-6500TE	R-0	6	4	2	1 Core: 3.3 2 Core: 3.2 3 Core: 3.1 4 Core: 3.0	1600	2133	2.3	0.35	35 W	No	LGA1151
SR2HG	i3-6100	S-0	3	2	2	1 Core: 3.7 2 Core: 3.7	1866	2133	3.7	0.35	65 W	Yes	LGA1151
SR2LS	i3-6100TE	R-0	4	2	2	1 Core: 2.7 2 Core: 2.7	1600	2133	2.7	0.35	35 W	Yes	LGA1151
SR2HK	G4400	S-0	3	2	1	1 Core: 3.3 2 Core: 3.3	1600	2133	3.3	0.35	65 W	Yes	LGA1151
SR2LT	G4400TE	R-0	3	2	1	1 Core: 2.4 2 Core: 2.4	1600	2133	2.4	0.35	35 W	Yes	LGA1151
SR2HV	G3900	S-0	2	2	1	1 Core: 2.8 2 Core: 2.8	1600	2133	2.8	0.35	65 W	Yes	LGA1151
SR2LU	G3900TE	R-0	2	2	1	1 Core: 2.3 2 Core: 2.3	1600	2133	2.3	0.35	35 W	Yes	LGA1151

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