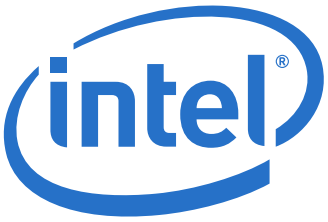

Intel® Quark™ SoC X1000

Specification Update

February 2015

Document Number: 329677 Revision 006

Contents

Revision History

Date	Revision	Description
February 2015	006	Added Specification Clarification 3 Added Document-Only Changes 5
August 2014	005	No Errata Added or Deleted Document Standardization
May 2014	004	Added Errata 24 Added Specification Change 5
March 2014	003	Added Specification Changes 1, 2, 3, 4 Added Specification Clarifications 1, 2 Added Documentation-Only Changes 2, 3, 4
November 2013	002	Updated Errata 2 Added Errata 22, 23 Added Documentation-Only Change 1 Updated Component Markings table
October 2013	001	Initial revision

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Introduction

Purpose/Scope/Audience

This document is an update to the specifications listed in the Parent Documents/ Related Documents table that follows. This document is a compilation of Errata, Specification Changes, Specification Clarifications, and Document-Only Changes. It is intended for hardware and software system designers and manufacturers as well as developers of applications, operating systems, or tools.

Information types defined in Conventions and Terminology are consolidated into the Specification Update and are no longer published in other documents.

This document may also contain information that was not previously published.

Table 1. Parent Documents/Related Documents

Title	Number
Intel® Quark™ SoC X1000 Datasheet	329676-001US
Intel® Quark SoC™ X1000 Platform Design Guide	Note 1

Notes:
1. Contact your Intel sales representative. Some documents may not be available at this time.

Conventions and Terminology

Note: Errata remain in the Specification Update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the Specification Update are archived and available upon request. Specification Changes, Specification Clarifications and Document-Only Changes are removed from the Specification Update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Table 2. Conventions and Terminology (Sheet 1 of 2)

Term	Definition
Document-Only Changes	Document-Only Changes are changes to an Intel Parent Specification that result in changes only to an Intel customer document but no changes to a specification or to a parameter for an Intel product. An example of a document-only change is the correction of a typographical error.
Errata (plural) Erratum (singular)	Errata are design defects or errors. These may cause the Intel® Quark™ SoC X1000's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Table 2. Conventions and Terminology (Sheet 2 of 2)

Term	Definition
Parent Specification	A parent specification is a top-level specification from which other documents can be derived, depending on the product or platform. Typically, a parent specification includes a product's pinout, architectural overview, device operation, hardware interface, or electrical specifications. Examples of parent specifications include the following: Datasheet, External Design Specification (EDS), Developer's Manual, Technical Product Specification. The derived documents may be used for purposes other than that for which the parent specification is used.
Specification Changes	Specification Changes are the result of adding, removing, or changing a feature, after which an Intel product subsequently operates differently than specified in an Intel Parent Specification, but typically the customer does not have to do anything to achieve proper device functionality as a result of Intel adding, removing, or changing a feature.
Specification Clarifications	Specification Clarifications are changes to a document that arise when an Intel Parent Specification must be reworded so that the specification is either more clear or not in conflict with another specification.

Summary Tables of Current Product Issue Activity

Table 4 through Table 7 indicate the Errata, Specification Changes, Specification Clarifications, and Document-Only Changes that apply to the SoC product. Intel may fix some of the Errata in a future stepping of the component as noted in Table 3 or account for the other outstanding issues through Specification Changes, Specification Clarifications, or Document-Only Changes. Table 4 through Table 7 use the codes listed in Table 3.

Table 3. Codes Used in Summary Tables

Code	Column	Definition
X	Stepping	Indicates either that, for the stepping/revision listed, • an erratum exists and is not yet fixed • a specification change or specification clarification applies
No mark or blank	Stepping	Indicates either that, for the stepping/revision listed, • an erratum is fixed • a specification change or specification clarification does not apply
Plan Fix	Status	This erratum may be fixed in a future stepping/revision.
Fixed	Status	This erratum has been previously fixed.
No Fix	Status	There are no plans to fix this erratum.
A change bar to the left of a table row indicates an item that is either new or modified from the previous version of the Specification Update document.		

Table 4. Errata

No.	Stepping/ Revision	Status	Errata Title
	A0		
1	X	No Fix	4930600: High Speed SD Cards and eMMC Cards Fail to Initialize
2	X	No Fix	4930644: PCIe Non-posted Transactions Can Overtake Posted Ones
3	X	No Fix	4394797: ESP Register Address Increment During POPA/POPAD Instruction Execution
4	X	No Fix	4394803: Missing Code Break Point
5	X	No Fix	4394825: Ucode Incorrectly Takes GPF on RDTSC Instruction in VM86 Mode with CPL=3 & CR4.TSD Not Set
6	X	No Fix	4394828: WBINVD Instruction Failed to Return Correct EIP
7	X	No Fix	4394829: Incorrect Processor State in V86/VME Mode
8	X	No Fix	4394832: Quark Core Incorrectly Updates ESP
9	X	No Fix	4394843: Fault Address is Not Loaded into CR2
10	X	No Fix	4394874: #UB Exception not Detected in Protected Mode
11	X	No Fix	4394871: ESP Update Lost Following #UD
12	X	No Fix	4394902: EFLAGS.OF Incorrectly Updated in 16-bit Mode
13	X	No Fix	4394909: Possible Core Hang During Probe Mode if the SMM Region is Cached
14	X	No Fix	4395001: Page Fault Not Detected on Exit from Probe Mode
15	X	No Fix	4394993: #GP Fault Incorrectly Generated in Real Mode
16	X	No Fix	4395097: Quark Core Fails to Generate #GP During a 4G Address Increment Wrap Around
17	X	No Fix	4395099: A Write to CR3 Does not Flush Prefetched Instructions
18	X	No Fix	4395192: #GP Fault When EIP Roll Over Occurs
19	X	No Fix	4395217: #PF Incorrectly Detected in Protected Mode
20	X	No Fix	4395219: Precision Bits in FCW are Set Incorrectly
21	X	No Fix	4395444: Erroneous Debug Breakpoint in PAE Mode
22	X	No Fix	4930704: The Valid Time Bit in the RTC is Set Regardless of Whether There is a Valid Time
23	X	Plan Fix	85384: IEEE 1588 Support in 10/100 Ethernet MACs is Not Supported
24	X	No Fix	Possible Incorrect CPU Operation with LOCK Prefix Instructions Under Specific Circumstances

Table 5. Specification Changes (Sheet 1 of 2)

No.	Stepping/ Revision	Specification Changes
	A0	
1	X	ECC Scrubbing Has Been Defeatured and is No Longer Supported on the Intel® Quark™ SoC X1000
2	X	Remote Management Unit DMA via IOSF Primary is No Longer Supported on the Intel® Quark™ SoC X1000

Table 5. Specification Changes (Sheet 2 of 2)

No.	Stepping/ Revision	Specification Changes
	A0	
3	X	Lock Out DMA Capability Past Boot
4	X	Hardware Strap Repurposed
5	X	Thermal Design Point (TDP) Updated

Table 6. Specification Clarifications

No.	Stepping/ Revision	Specification Clarifications
	A0	
1	X	Is x16 DDR3 Supported On the Intel® Quark™ SoC X1000?
2	X	Additional Details about MAC Descriptors
3	X	SPI Status Register (SSSR) – SPI Busy Flag

Table 7. Document-Only Changes

No.	Document Title	Rev.	Document-Only Changes
1	Intel® Quark™ SoC X1000 Datasheet	001	Tables Missing from Section 4.4 Configurable IO Characteristics
2	Intel® Quark™ SoC X1000 Datasheet	001	VNNSENSE and VSSSENSE are listed as Analog Across S5/4, S3, and S0 in Table 18
3	Intel® Quark™ SoC X1000 Datasheet	001	Miscellaneous Legacy Signal Enables (HLEGACY) Register Not In Datasheet
4	Intel® Quark™ SoC X1000 Datasheet	001	RTC 70976: No JEDEC Functionality in Datasheet
5	Intel® Quark™ SoC X1000 Datasheet	001	Register Missing from Section 14.5 PCI Configuration Registers

General Product Information

The Intel® Quark™ SoC X1000 SoC can be identified by the following register contents:

Table 8. Identification Information

Part Number	Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
Contact your Intel sales representative.	A0	8086	0958	00

Notes:

1. The Vendor ID corresponds to bits [15:0] of the VID - Vendor Identification Register located at Offset 00–01h in the PCI Function 0 configuration space.
2. The Device ID corresponds to bits [15:0] of the DID - Device Identification Register located at Offset 02–03h in the PCI Function 0 configuration space.
3. The Revision Number corresponds to bits [7:0] of the RID - Revision Identification Register located at Offset 08h in the PCI Function 0 configuration space.

The Intel® Quark™ SoC X1000 stepping can be identified by the following component markings:

Stepping	SKU	Identifier	ECC	Secure Boot	MM #	SPEC Code
A0	2	Intel® Quark™ SoC X1000(16K Cache, 400MHz)	Y	Y	929172	ES
A0	2	Intel® Quark™ SoC X1000(16K Cache, 400MHz)	Y	Y	930236	SS
A0	4	Intel® Quark™ SoC X1000(16K Cache, 400MHz)	N	N	929184	ES
A0	4	Intel® Quark™ SoC X1000(16K Cache, 400MHz)	N	N	930237	SS
A0	5	Intel® Quark™ SoC X1000(16K Cache, 400MHz)	Y	N	929518	ES
A0	5	Intel® Quark™ SoC X1000(16K Cache, 400MHz)	Y	N	930239	SS

Errata

1. 4930600: High Speed SD Cards and eMMC Cards Fail to Initialize

Problem: High Speed SD cards and eMMC cards fail to initialize correctly when connected to Quark X1000.

Implication: High Speed SD card or eMMC cards are not available for use in the system.

Workaround: A driver workaround exists to resolve this issue.

The driver tells the SD controller that the hi-speed SD card does not have a high speed bit. This workaround changes the high speed enable bit in the host control 1 register (28H) to always be set to 0.

This workaround is enabled by default in the sdhci driver within the Intel® Quark™ SoC X1000 software release version 0.6.0 and later.

Status: No Fix

Please use the workaround detailed above.

2. 4930644: PCIe Non-posted Transactions Can Overtake Posted Ones

Problem: IPF bit in PCIe configuration register (B0:D23:F0:D4h-MCP2), which is currently defaulting to '0', needs to be set to '1' in PCIe configuration.

Implication: PCIe non-posted transactions are passing out posted ones. The result is PCIe timeout error or invalid data read.

Workaround: UEFI firmware must set the following:

B0:D23:F0:RegD4h bit[11]=1

B0:D23:F1:RegD4h bit[11]=1

The workaround is enabled in software release version 0.5.0 and later.

Status: No Fix

Firmware workaround is implemented as detailed above.

3. 4394797: ESP Register Address Increment During POPA/POPAD Instruction Execution

Problem: During POPA/POPAD instruction execution the contents of the stack are popped off the stack, if ESP is incremented as part of the operation, new address is not checked for page faults or breakpoints.

Implication: Some page faults/breakpoints for a specific code flow will be missed.

Workaround: None

Status: No Fix

4. 4394803: Missing Code Break Point

Problem: When a conditional jump followed by jcc/short near jmp/near call and bit [2:0] of target address of second branch instruction is '0, code break point could potentially be missed.

Implication: Code break point set at addresses matching this code pattern might not be triggered.

Workaround: Set break point earlier in flow and step through each instruction.

Status: No Fix

5. 4394825: Ucode Incorrectly Takes GPF on RDTSC Instruction in VM86 Mode with CPL=3 & CR4.TSD Not Set

Problem: The Quark core incorrectly takes GPF on RDTSC instruction in VM86 mode with CPL=3 & CR4.TSD not set.

Implication: User may experience spurious invalid General Purpose Fault.

Workaround: None

Status: No Fix

6. 4394828: WBINVD Instruction Failed to Return Correct EIP

Problem: In 16-bit mode, the execution of the WBINVD instruction may not return the correct EIP value.

Implication: The WBINVD instruction may corrupt the contents of EIP in 16-bit mode.

Workaround: None

Status: No Fix

7. 4394829: Incorrect Processor State in V86/VME Mode

Problem: The Quark Core incorrectly sets processor state in V86/VME mode on the RETD instr triggering a #GP trap.

Implication: Spurious General Purpose Fault.

Workaround: None

Status: No Fix

8. 4394832: Quark Core Incorrectly Updates ESP

Problem: Processor incorrectly updates upper 16 bits of ESP during RETD instruction execution with privilege level change following ADD operation with result above 0xFFFFh.

Implication: ESP is corrupted during privilege mode change.

Workaround: None

Status: No Fix

9. 4394843: Fault Address is Not Loaded into CR2

Problem: Following a double fault scenario, the second fault address is not loaded into CR2 register.

Implication: The source of the second fault address in a double fault scenario will not be accessible.

Workaround: None

Status: No Fix

10. 4394874: #UB Exception not Detected in Protected Mode

Problem: In protected mode, #UD exception is not detected while accessing CR7 register during instruction MOV CR7, EBP.

Implication: #UD exception is not generated as expected in protected mode when doing a MOV CR7, r32.

Workaround: None

Status: No Fix

11. 4394871: ESP Update Lost Following #UD

Problem: After an instruction updates the ESP value and the next inst. causes a #UD, the ESP update is lost.

Implication: Spurious corruption of the ESP register leading to corrupt code execution.

Workaround: None

Status: No Fix

12. 4394902: EFLAGS.OF Incorrectly Updated in 16-bit Mode

Problem: In 16-bit mode, EFLAGS.OF is incorrectly updated on RCL instruction with zero count.

Implication: Corrupt code execution may occur in 16-bit mode.

Workaround: None

Status: No Fix

13. 4394909: Possible Core Hang During Probe Mode if the SMM Region is Cached

Problem: Core microcode flush after a Probe Mode save cycle will cause the core to hang if the SMM region is cached.

Implication: Core will hang on Probe mode exit.

Workaround: Do not cache System Management Mode memory. This is implemented by Intel's provided UEFI firmware.

Status: No Fix

14. 4395001: Page Fault Not Detected on Exit from Probe Mode

Problem: The Probe Mode entry is currently the highest priority event and when a page fault happens in the same clock as the probe mode entry, the CR2 register is corrupted.

Implication: Page fault is not detected and on exit from probe mode, the CPU shall start executing from the wrong address.

Workaround: None

Status: No Fix

15. 4394993: #GP Fault Incorrectly Generated in Real Mode

Problem: #GP Fault is incorrectly generated in Real Mode when executing the mov word ptr cs:[di + 0x48], cs instruction due to the stale Access Right bits when transitioning from Protected Mode to Real Mode.

Implication: Spurious general purpose fault may occur on transition from protected mode to real mode.

Workaround: None

Status: No Fix

16. 4395097: Quark Core Fails to Generate #GP During a 4G Address Increment Wrap Around

Problem: On a 4G address increment wrap around, processor will fail to generate general purpose fault under certain circumstances.

Implication: Incorrect code execution and possible core hang for specific code flow and timing circumstances.

Workaround: None

Status: No Fix

17. 4395099: A Write to CR3 Does not Flush Prefetched Instructions

Problem: Write to CR3 doesn't flush prefetched instruction when PAEXD is not enabled.

Implication: If CR3 value changes, prefetched instruction may use stale CR3 value, leading to corrupt code execution.

Workaround: None

Status: No Fix

18. 4395192: #GP Fault When EIP Roll Over Occurs

Problem: #GP fault generated in case of EIP rollover in JO instruction with OF=0.

Implication: Spurious incorrect General purpose fault triggered.

Workaround: None

Status: No Fix

19. 4395217: #PF Incorrectly Detected in Protected Mode

Problem: Incorrect detection of #PF by JNP instruction in Protected Mode.

Implication: Spurious protection fault generated.

Workaround: None

Status: No Fix

20. 4395219: Precision Bits in FCW are Set Incorrectly

Problem: Whenever there is a GP fault on FLDENV, the precision bits are changed from 11 (double extended precision) to 00 (single precision).

Implication: Incorrect precision is set in the context of general purpose fault leading to incorrect code execution.

Workaround: None

Status: No Fix

21. 4395444: Erroneous Debug Breakpoint in PAE Mode

Problem: Debug Break Point triggered incorrectly when PDPTE entries are reloaded during task switching.

Implication: The system will spuriously enter probe mode. Recovery involves connecting a debugger to trigger a probe mode exit or a reboot.

Workaround: None

Status: No Fix

22. 4930704: The Valid Time Bit in the RTC is Set Regardless of Whether There is a Valid Time

Problem: The default value for the Valid Time bit in the RTC indicates that there is a valid time in the RTC RAM even if there is not.

Implication: If the Valid Time bit is trusted, an incorrect value may be read back from the RTC RAM.

Workaround: None

Status: No Fix

23. 85384: IEEE 1588 Support in 10/100 Ethernet MACs is Not Supported

Problem: The 1588 timestamping capability included in the 2 10/100 Ethernet interfaces is currently not supported.

Implication: 1588 packet timestamping cannot be done by HW.

Workaround: Packet timestamping should be done by software.

Status: Plan Fix

24. Possible Incorrect CPU Operation with LOCK Prefix Instructions Under Specific Circumstances

Problem: When a memory instruction with LOCK prefix executes and if it encounters a page fault (#PF) the state of the CPU could potentially get corrupted.

Implication: Invalid CPU operation may occur for specific instruction sequences when using the LOCK prefix instruction if the instruction generates a page fault.

Workaround: Software should avoid using the LOCK prefix for instructions that may cause page fault (#PF).

Status: No Fix

Specification Changes

1. ECC Scrubbing Has Been Defeatured and is No Longer Supported on the Intel® Quark™ SoC X1000

Old Text: ECC Scrubber Registers (Offsets 50h, 76h, 77h, 7Ch) have been removed.

Table 71. Summary of Message Bus Registers—0x04

Offset	Register Name (Register Symbol)	Default Value
50h	"ECC Scrubber Configuration Register (P_CFG_50)—Offset 50h" on page 7	00530864h
60h	"SPI DMA Count Register (P_CFG_60)—Offset 60h" on page 7	00000000h
61h	"SPI DMA Destination Register (P_CFG_61)—Offset 61h" on page 8	00000000h
62h	"SPI DMA Source Register (P_CFG_62)—Offset 62h" on page 8	00000000h
70h	"Processor Register Block (P_BLK) Base Address (P_CFG_70)—Offset 70h" on page 9	00000000h
71h	"Control Register (P_CFG_71)—Offset 71h" on page 9	00000009h
74h	"Watchdog Control Register (P_CFG_74)—Offset 74h" on page 10	00040000h
76h	"12.7.3.8 ECC Scrubber Start Address Register (P_CFG_76)—Offset 76h" on page 18	00000000h
77h	"12.7.3.9 ECC Scrubber End Address Register (P_CFG_77)—Offset 77h" on page 19	00000000h
7Ch	"12.7.3.10 ECC Scrubber Next Address Register (P_CFG_7C)—Offset 7Ch" on page 19	00000000h
B0h	"Thermal Sensor Mode Register (P_CFG_B0)—Offset B0h" on page 12	00000000h
B1h	"Thermal Sensor Temperature Register (P_CFG_B1)—Offset B1h" on page 13	00000000h
B2h	"Thermal Sensor Programmable Trip Point Register (P_CFG_B2)—Offset B2h" on page 13	FFFFFFFFh

New Text:

Table 71. Summary of Message Bus Registers—0x04

Offset	Register Name (Register Symbol)	Default Value
60h	"SPI DMA Count Register (P_CFG_60)—Offset 60h" on page 7	00000000h
61h	"SPI DMA Destination Register (P_CFG_61)—Offset 61h" on page 8	00000000h
62h	"SPI DMA Source Register (P_CFG_62)—Offset 62h" on page 8	00000000h
70h	"Processor Register Block (P_BLK) Base Address (P_CFG_70)—Offset 70h" on page 9	00000000h
71h	"Control Register (P_CFG_71)—Offset 71h" on page 9	00000009h
74h	"Watchdog Control Register (P_CFG_74)—Offset 74h" on page 10	00040000h
B0h	"Thermal Sensor Mode Register (P_CFG_B0)—Offset B0h" on page 12	00000000h
B1h	"Thermal Sensor Temperature Register (P_CFG_B1)—Offset B1h" on page 13	00000000h
B2h	"Thermal Sensor Programmable Trip Point Register (P_CFG_B2)—Offset B2h" on page 13	FFFFFFFFh

~~12.7.3.1 ECC Scrubber Configuration Register (P_CFG_50)—Offset 50h~~

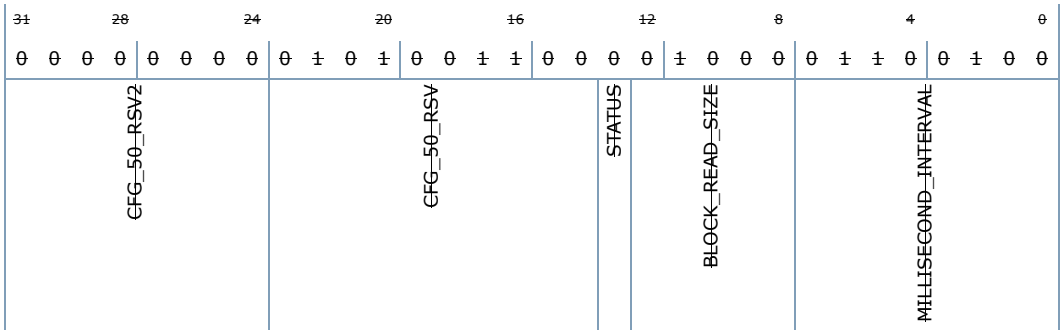
~~Access Method~~

~~Type:~~ ~~Message Bus Register (Size: 32 bits)~~

~~Offset:~~ ~~[Port: 0x04] + 50h~~

~~Op Codes:~~
~~10h - Read, 11h - Write~~

~~Default:~~ ~~00530864h~~



~~Bit Range~~	~~Default & Access~~	~~Field Name (ID): Description~~
~~31:24~~	~~00h RO~~	**~~Reserved (CFG_50_RSV2):~~** ~~Reserved.~~
~~23:14~~	~~14Ch RW~~	**~~Reserved (CFG_50_RSV):~~** ~~Reserved.~~
~~13~~	~~0b RW~~	**~~Status (STATUS):~~** ~~Indicates if ECC scrubbing is active or inactive.~~ ~~0b : Scrubbing Inactive~~ ~~1b : Scrubbing Active~~
~~12:8~~	~~08h RW~~	**~~Block Read Size (BLOCK_READ_SIZE):~~** ~~Block read size in DWORDs (4 bytes). Range 1 to 128 (4-512 bytes).~~
~~7:0~~	~~64h RW~~	**~~Millisecond Interval (MILLISECOND_INTERVAL):~~** ~~Millisecond interval between block reads. Range 1-255 msec.~~

~~12.7.3.8 ECC Scrubber Start Address Register (P_CFG_76)—Offset 76h~~

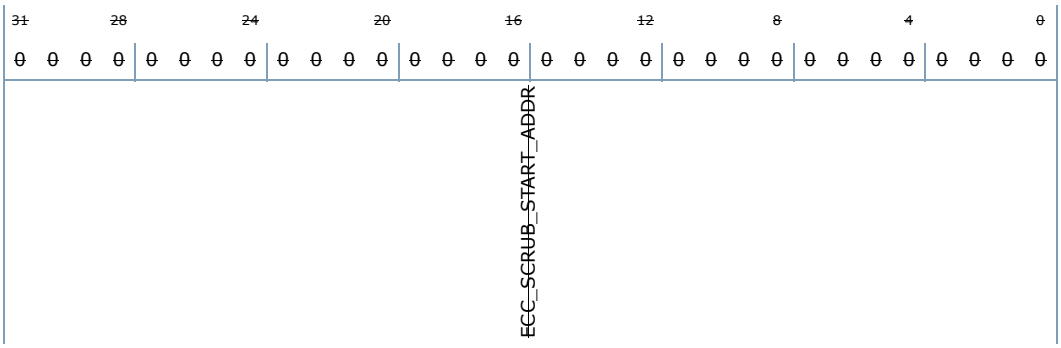
~~Access Method~~

~~Type:~~ ~~Message Bus Register (Size: 32 bits)~~

~~Offset:~~ ~~[Port: 0x04] + 76h~~

~~Op Codes:~~
~~10h - Read, 11h - Write~~

~~Default:~~ ~~00000000h~~



Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**Start Address (ECC_SCRUB_START_ADDR):** Start of memory address.

12.7.3.9 ECC Scrubber End Address Register (P_CFG_77)—Offset 77h

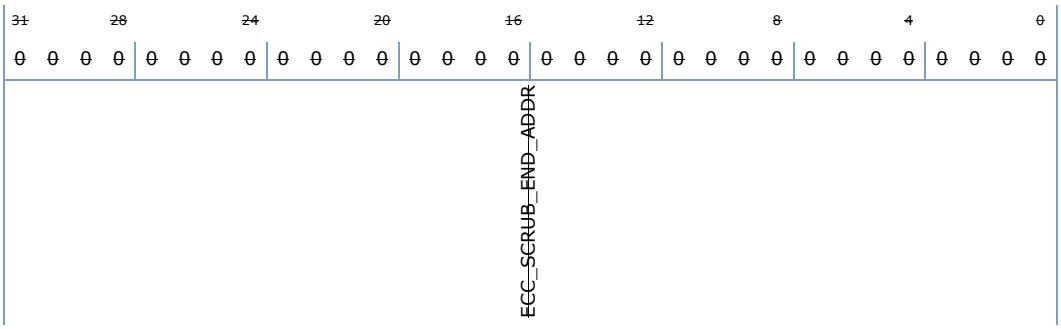
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 77h

Op Codes:
10h - Read, 11h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**End Address (ECC_SCRUB_END_ADDR):** End of memory address.

12.7.3.10 ECC Scrubber Next Address Register (P_CFG_7C)—Offset 7Ch

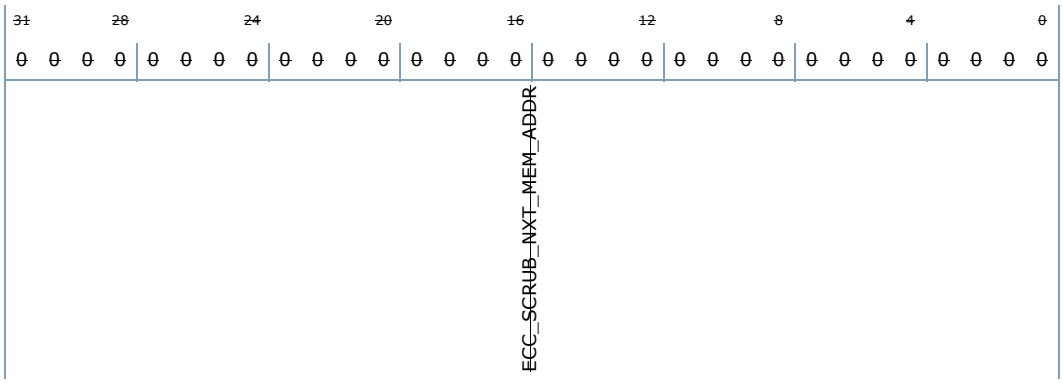
Access Method

Type: Message Bus Register (Size: 32 bits)

Offset: [Port: 0x04] + 7Ch

Op Codes:
10h - Read, 11h - Write

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	0b RW	**Next Address (ECC_SCRUB_NXT_MEM_ADDR):** Next memory address to be scrubbed.

New Text: Section 12.3.1 ECC Scrubbing has been removed.

12.3 ECC Scrubbing

The Remote Management Unit offers an ECC scrubbing function. The ECC scrubber initiates memory reads that triggers the logic to correct single bit ECC errors and detect double bit ECC errors. If single bit ECC errors are not corrected then they may result in double bit ECC errors over time. Double bit ECC errors are fatal errors that cannot be corrected. To avoid double bit ECC errors, the ECC scrubber may be initialized to periodically scrub all physical memory and correct single bit ECC errors. Note that the ECC scrubber will have an effect on the performance and real-time characteristics of the system.

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

2. Remote Management Unit DMA via IOSF Primary is No Longer Supported on the Intel® Quark™ SoC X1000

Issue: The Intel® Quark™ SoC X1000 uses only the sideband option for setting up a DMA transfer.

Old Text:

12.3 Remote Management Unit DMA

The Remote Management Unit supports DMA transfers between System Memory and Legacy SPI Flash. The DMA engine is used on boot-up to perform the initial firmware fetch from SPI Flash. In addition, this can be used for shadowing firmware to DRAM or eSRAM.

SPI DMA Block registers are used to control DMA transfers. These registers are managed by the Remote Management Unit firmware. Firmware will also shadow the SPI_DMA_CNT, SPI_DMA_DST and SPI_DMA_SRC IO-mapped registers to Remote Management Unit message bus registers 0x60, 0x61 and 0x62. The base address for SPI_DMA_BLK IO registers is given my Remote Management Unit message bus register

0x7A. The SPI_DMA_CNT register should be programmed after SPI_DMA_SRC and SPI_DMA_DST as writing to the SPI_DMA_CNT will trigger the start of the DMA transfer.

New Text:

12.3 Remote Management Unit DMA

The Remote Management Unit supports DMA transfers between System Memory and Legacy SPI Flash. The DMA engine is used on boot-up to perform the initial firmware fetch from SPI Flash. In addition, this can be used for shadowing firmware to DRAM or eSRAM.

Remote Management Unit message bus registers - SPI DMA Count Register (P_CFG_60), SPI DMA Destination Register (P_CFG_61) and SPI DMA Source Register (P_CFG_62) are used to control DMA transfers. These registers are managed by the Remote Management Unit firmware.

The SPI DMA Count Register (P_CFG_60) should be programmed after the SPI DMA Source Register (P_CFG_62) and the SPI DMA Destination Register (P_CFG_61) as writing to the SPI DMA Count Register (P_CFG_60) will trigger the start of the DMA transfer.

See Option Register 1(P_CFG_72) bit [0] for details on how to disable DMA functionality.

New Text: Section 12.6.2 has been removed.

~~12.6.2SPI DMA Block~~

~~12.6.2.1SPI DMA Count Register (SPI_DMA_CNT_IOSF)—Offset 0h~~

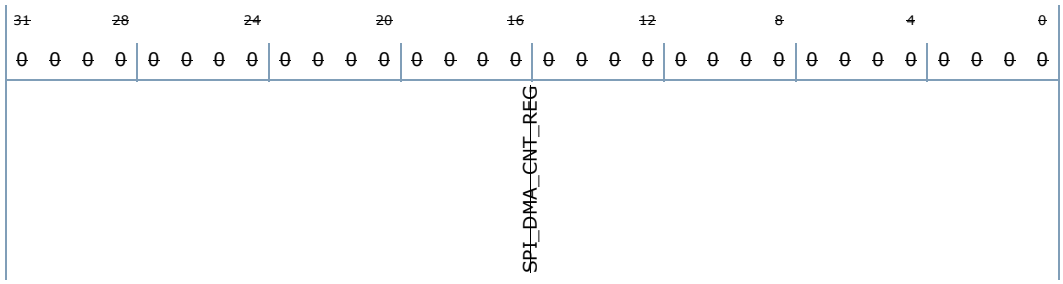
~~Access Method~~

~~Type:~~ ~~I/O Register (Size: 32 bits)~~

~~Offset:~~ ~~[SPI_DMA_BAR] + 0h~~

~~SPI_DMA_BAR Type:~~ ~~Message Bus Register (Size: 32 bits)~~
~~SPI_DMA_BAR Reference:~~ ~~[Port: 0x04] + 7Ah~~

~~Default:~~ ~~00000000h~~



~~Bit Range~~	~~Default & Access~~	~~Field Name (ID): Description~~
~~31:0~~	~~0b RW~~	~~**SPI DMA Count (SPI_DMA_CNT_REG):** Count of 512 byte block transfers. Writing this register triggers the start of the transfer of the indicated number of blocks. Reading this register returns the number of blocks that are remaining to be transferred. A value of 0 indicates the transfer is complete.~~

12.6.2.2SPI DMA Destination Register (SPI_DMA_DST_IOSF)—Offset 4h

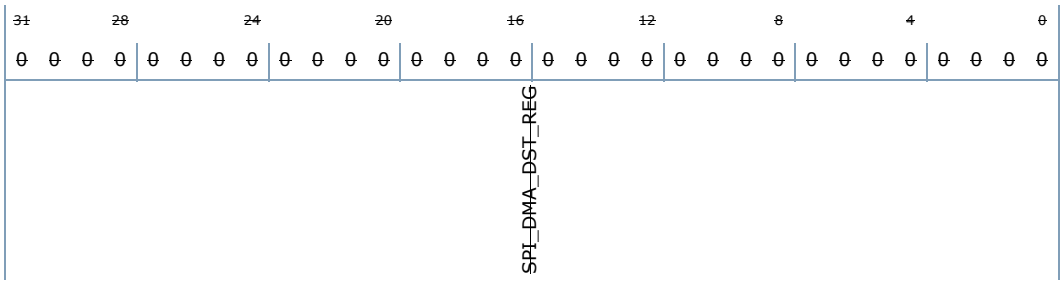
Access Method

Type: I/O Register (Size: 32 bits)

Offset: [SPI_DMA_BAR] + 4h

SPI_DMA_BAR Type: Message Bus Register (Size: 32 bits)
SPI_DMA_BAR Reference: [Port: 0x04] + 7Ah

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**SPI DMA Destination (SPI_DMA_DST_REG):** 32-bit Destination Address of data in System Memory (eSRAM/DRAM).

12.6.2.3SPI DMA Source Register (SPI_DMA_SRC_IOSF)—Offset 8h

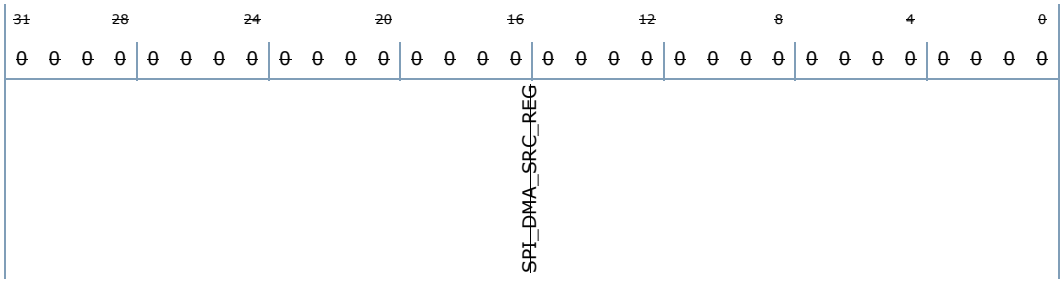
Access Method

Type: I/O Register (Size: 32 bits)

Offset: [SPI_DMA_BAR] + 8h

SPI_DMA_BAR Type: Message Bus Register (Size: 32 bits)
SPI_DMA_BAR Reference: [Port: 0x04] + 7Ah

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:0	00000000h WO	**SPI DMA Source (SPI_DMA_SRC_REG):** 32-bit Source Address of data in Legacy SPI.

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

3. Lock Out DMA Capability Past Boot

Issue: DMA functionality must be disabled on boot completion to prevent an attacker from using it to take control of the system.

New Text: A new register is added:

12.6.2.3 Option Register 1(P_CFG_72) —Offset 72h

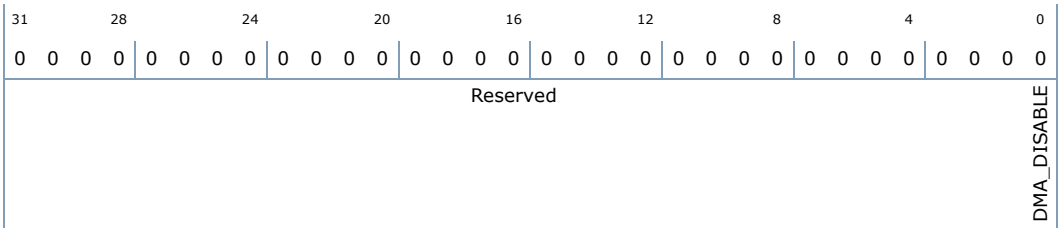
Access Method

Type: I/O Register
(Size: 32 bits)

Offset: [Port: 0x04] + 72h

SPI_DMA_BAR Type: Message Bus Register (Size: 32 bits)
SPI_DMA_BAR Reference: [Port: 0x04] + 72h

Default: 00000000h



Bit Range	Default & Access	Field Name (ID): Description
31:1	0 RO	**Reserved (RSVD):** Reserved.
0	0 RW	**DMA_DISABLE:** Remote Management Unit DMA disable. Once set RMU DMA functionality is disabled until system reset

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

4. Hardware Strap Repurposed

Old Text: Hardware strap signal SPI0_MOSI has been repurposed.

Table 23. Hardware Straps (Sheet 1 of 2)

Signal Name	Default	Strap Description
SPI0_MOSI	1b	Defines Memory Device Width 0b = x16 devices 1b = x8 devices
{SPI0_SCK, SPI1_MOSI}	11b	Defines Memory Device Density 00b = Reserved 01b = 1Gb 10b = 2Gb 11b = 4Gb
LSPI_MOSI	1b	Defines the Number of Ranks Enabled 0b = 1 Rank 1b = 2 Ranks

Table 23. Hardware Straps (Sheet 2 of 2)

Signal Name	Default	Strap Description
{MAC0_TXDATA[1], MAC0_TXDATA[0], MAC1_TXDATA[1]	000b	Frequency SKU Power Optimize Mode [2:1] CPU Clock/DDR Clock 00b = Reserved 01b = 400MHz/800MHz 10b = 200MHz/800MHz 11b = 100MHz/800MHz [0] 0b = Low Latency 1b = Low Power
MAC1_TXDATA[0]	0b	Remote Management Unit Firmware Base Address 0b = FFF0_0000h 1b = FFD0_0000h
{LSPI_SCK, SD_CLK}	00b	SDIO Slot Type 00b = Removable Card Slot 01b = Embedded Slot for One Device 10b = Shared Bus Slot 11b = Reserved
PWR_BTN	0b	Power Button Disable 0b = Power Button Disabled 1b = Power Button Enabled

New Text:

Table 23. Hardware Straps (Sheet 1 of 2)

Signal Name	Default	Strap Description
SPI0_MOSI	1b	Reports the Strap status of Recovery Mode: 0 = Recovery Mode 1 = Normal Mode
{SPI0_SCK, SPI1_MOSI}	11b	Defines Memory Device Density 00b = Reserved 01b = 1Gb 10b = 2Gb 11b = 4Gb
LSPI_MOSI	1b	Defines the Number of Ranks Enabled 0b = 1 Rank 1b = 2 Ranks
{MAC0_TXDATA[1], MAC0_TXDATA[0], MAC1_TXDATA[1]	000b	Frequency SKU Power Optimize Mode [2:1] CPU Clock/DDR Clock 00b = Reserved 01b = 400MHz/800MHz 10b = 200MHz/800MHz 11b = 100MHz/800MHz [0] 0b = Low Latency 1b = Low Power

Table 23. Hardware Straps (Sheet 2 of 2)

Signal Name	Default	Strap Description
MAC1_TXDATA[0]	0b	Remote Management Unit Firmware Base Address 0b = FFF0_0000h 1b = FFD0_0000h
{LSPI_SCK, SD_CLK}	00b	SDIO Slot Type 00b = Removable Card Slot 01b = Embedded Slot for One Device 10b = Shared Bus Slot 11b = Reserved
PWR_BTN	0b	Power Button Disable 0b = Power Button Disabled 1b = Power Button Enabled

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

5. Thermal Design Point (TDP) Updated

Old Text:

Table 3 SKU Definitions

	SKU1 (Commercial)	SKU2 (Extended)
TDP (W)	2.7	2.6
$T_{J\text{-}MAX}$ (^{o}C)	110	
$T_{CASE\text{-}MIN}$ (^{o}C)	0	-40
$T_{AMBIENT}$ (^{o}C)	70	85

Note: Specifications presented in this table are preliminary and subject to change without notice.

New Text:

Table 3 SKU Definitions

	SKU1 (Commercial)	SKU2 (Extended)
TDP (W)	2.2	
$T_{J\text{-}MAX}$ (^{o}C)	110	
$T_{CASE\text{-}MIN}$ (^{o}C)	0	-40
$T_{AMBIENT}$ (^{o}C)	70	85

Note: Specifications presented in this table are preliminary and subject to change without notice.

Affected Docs:*Clanton – Thermal and Mechanical Design Guide*

Specification Clarifications

1. Is x16 DDR3 Supported On the Intel® Quark™ SoC X1000?

x16 devices can be enabled on the Intel® Quark™ SoC X1000, however, there has been no platform level validation performed with such configurations (Board Layout, UEFI Memory Reference Code) and hence these are not supported on the current reference platforms.

Old Text:

13.4.1 DRAM Rank Population (DRP)—Offset 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rsvd_4:** Reserved
30	0h RW/P/L	**16-bit/32-bit Mode Select (MODE32):** 0 - Selects 16-bit DRAM Data Interface. 1 - Selects 32-bit DRAM Data Interface.
29:16	0000h RO	**Rsvd_3:** Reserved
15:14	0h RW/P/L	**Address Map Select (ADDRMAP):** See Address Mapping section for full description. 0 Map 0 1 Map 1 2 Map 2 Note: The address map select should be set the same for both the Memory Controller and the Memory Manager.
13	0h RW	**64B Split Enable (PRI64BSPLITEN):** Setting this bit to '1' enables logic to split 64B PRI transactions to two 32B transactions. This bit must be set if ECC mode is enabled.
12:11	0h RW/P/L	**Rank 1 Device Density (DIMMDDEN1):** This sets the density of the DRAM devices populated in Rank 1. 00 1Gbit 01 2Gbit 10 4Gbit 11 Reserved
10:9	0h RW/P/L	**Rank 1 Device Width (DIMMDWID1):** Indicates the width of the DRAM devices populated in Rank 1. 00 x8 01 x16 10 Reserved 11 Reserved
8	0h RO	**Rsvd_1:** Reserved
7:6	0h RW/P/L	**Rank 0 Device Density (DIMMDDEN0):** This sets the density of the DRAM devices populated in Rank 0. 00 1Gbit 01 2Gbit 10 4Gbit 11 Reserved

13.4.1 DRAM Rank Population (DRP)—Offset 0h

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW/P/L	**Rank 0 Device Width (DIMMDWID0):** Indicates the width of the DRAM devices populated in Rank 0. 00 x8 01 x16 10 Reserved 11 Reserved
3:2	0h RO	**Rsvd_0:** Reserved
1	0h RW/P/L	**Rank Enable 1 (RKEN1):** Should be set to 1 when device has 2 ranks to enable the use of second rank. Otherwise, must be set to 0.
0	0h RW/P/L	**Rank Enable 0 (RKEN0):** Should be set to 1 when Rank 0 is populated to enable the use of this rank. Otherwise, must be set to 0.

New Text:

13.4.1 DRAM Rank Population (DRP)—Offset 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Rsvd_4:** Reserved
30	0h RW/P/L	**16-bit/32-bit Mode Select (MODE32):** 0 - Selects 16-bit DRAM Data Interface. 1 - Selects 32-bit DRAM Data Interface.
29:16	0000h RO	**Rsvd_3:** Reserved
15:14	0h RW/P/L	**Address Map Select (ADDRMAP):** See Address Mapping section for full description. 0 Map 0 1 Map 1 2 Map 2 Note: The address map select should be set the same for both the Memory Controller and the Memory Manager.
13	0h RW	**64B Split Enable (PRI64BSPLITEN):** Setting this bit to '1' enables logic to split 64B PRI transactions to two 32B transactions. This bit must be set if ECC mode is enabled.
12:11	0h RW/P/L	**Rank 1 Device Density (DIMMDDEN1):** This sets the density of the DRAM devices populated in Rank 1. 00 1Gbit 01 2Gbit 10 4Gbit 11 Reserved
10:9	0h RW/P/L	**Rank 1 Device Width (DIMMDWID1):** Indicates the width of the DRAM devices populated in Rank 1. 00 x8 01 Future Support 10 Reserved 11 Reserved
8	0h RO	**Rsvd_1:** Reserved
7:6	0h RW/P/L	**Rank 0 Device Density (DIMMDDEN0):** This sets the density of the DRAM devices populated in Rank 0. 00 1Gbit 01 2Gbit 10 4Gbit 11 Reserved

13.4.1 DRAM Rank Population (DRP)—Offset 0h

Bit Range	Default & Access	Field Name (ID): Description
5:4	0h RW/P/L	**Rank 0 Device Width (DIMMDWID0):** Indicates the width of the DRAM devices populated in Rank 0. 00 x8 01 Future Support 10 Reserved 11 Reserved
3:2	0h RO	**Rsvd_0:** Reserved
1	0h RW/P/L	**Rank Enable 1 (RKEN1):** Should be set to 1 when device has 2 ranks to enable the use of second rank. Otherwise, must be set to 0.
0	0h RW/P/L	**Rank Enable 0 (RKEN0):** Should be set to 1 when Rank 0 is populated to enable the use of this rank. Otherwise, must be set to 0.

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

2. Additional Details about MAC Descriptors

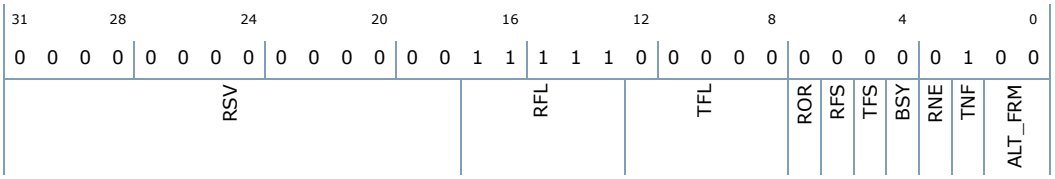
Issue: Revision 001 of the *Intel® Quark™ SoC X1000 Datasheet* describes MAC registers in Section 15.6, however, details of the MAC descriptors are not included. The information in Appendix A, "MAC Descriptor Details" will be added to a future revision of the datasheet.

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

3. SPI Status Register (SSSR) – SPI Busy Flag

Issue: Incorrect description for SPI Busy Flag in SSSR.

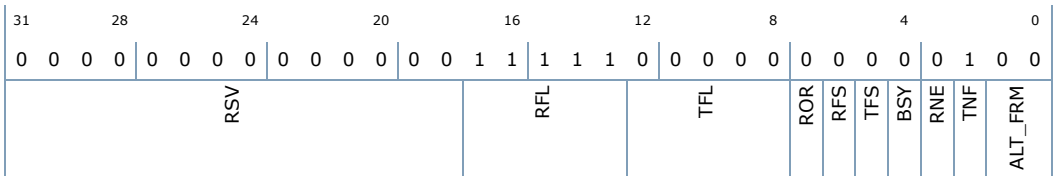
Old Text:



Bit Range	Default & Access	Description
31:18	00h RO	**RSV:** Reserved
17:13	1Fh RO	**Receive FIFO Level (RFL):** This 5-bit value shows how many valid entries are currently in the Receive FIFO (up to 32).
12:8	0b RO	**Transmit FIFO Level (TFL):** This 5-bit value shows how many valid entries are currently in the Transmit FIFO (up to 32).
7	0b RW/C	**Receiver Overrun Status (ROR):** The receiver overrun status bit is a read/write bit which is set when the receive logic attempts to place data into the receive FIFO after it has been completely filled. Each time a new piece of data is received, the set signal to the ROR bit is asserted, and the newly received data is discarded. This process is repeated for each new piece of data received until at least one empty FIFO entry exists. When the ROR bit is set, an interrupt request is made to the CPU which cannot be locally masked by any SPI register bit. Writing a 1 to this bit resets ROR status and its interrupt request; writing a 0 to this bit does not affect ROR status. Receiver Overrun Status is a non-maskable interrupt
6	0b RO	**Receive FIFO Service Reqvuest Flag (RFS):** The receive FIFO service request flag is a read-only bit which is set when the receive FIFO is nearly filled and requires service to prevent an overrun. RFS is set any time the receive FIFO has the same or more entries of valid data than indicated by the Receive FIFO Threshold, and it is cleared when it has fewer entries than the threshold value. When the RFS bit is set, an interrupt request is made unless RIE is cleared. After the CPU reads the FIFO such that it has fewer entries than the RFT value, the RFS flag (and the service request and/or interrupt) is automatically cleared.
5	0b RO	**Transmit FIFO Service Request Flag (TFS):** The Transmit FIFO service request flag is a read-only bit which is set when the transmit FIFO is nearly empty and requires service to prevent an underrun. TFS is set any time the transmit FIFO has the same or fewer entries of valid data than indicated by the Transmit FIFO Threshold, and it is cleared when it has more entries of valid data than the threshold value. When the TFS bit is set, an interrupt request is made unless TIE is cleared. After the CPU fills the FIFO such that it exceeds the threshold, the TFS flag (and the service request and/or interrupt) is automatically cleared.
4	0b RO	**SPI Busy Flag (BSY):** The receive FIFO not empty flag is a read-only bit which is set whenever the receive FIFO contains one or more entries of valid data and is cleared when it no longer contains any valid data. This bit can be polled when using programmed I/O to remove remaining bytes of data from the receive FIFO since CPU interrupt requests are only made when the Receive FIFO Threshold has been met or exceeded. This bit does not request an interrupt.
3	0b RO	**Receive FIFO Not Empty Flag (RNE):** The receive FIFO not empty flag is a read-only bit which is set whenever the receive FIFO contains one or more entries of valid data and is cleared when it no longer contains any valid data. This bit can be polled when using programmed I/O to remove remaining bytes of data from the receive FIFO since interrupt requests are only made when the Receive FIFO Threshold has been met or exceeded. This bit does not request an interrupt.

2	1b RO	**Transmit FIFO Not Full Flag (TNF):** The transmit FIFO not full flag is a read-only bit which is set whenever the transmit FIFO contains one or more entries which do not contain valid data. TNF is cleared when the FIFO is completely full. This bit can be polled when using programmed I/O to fill the transmit FIFO over its threshold level. This bit does not request an interrupt.
1:0	0b RO	**Alternative Frame (ALT_FRM):** This field is not supported and should be treated as reserved.

New Text:



Bit Range	Default & Access	Description
31:18	00h RO	**RSV:** Reserved
17:13	1Fh RO	**Receive FIFO Level (RFL):** This 5-bit value shows how many valid entries are currently in the Receive FIFO (up to 32).
12:8	0b RO	**Transmit FIFO Level (TFL):** This 5-bit value shows how many valid entries are currently in the Transmit FIFO (up to 32).
7	0b RW/C	**Receiver Overrun Status (ROR):** The receiver overrun status bit is a read/write bit which is set when the receive logic attempts to place data into the receive FIFO after it has been completely filled. Each time a new piece of data is received, the set signal to the ROR bit is asserted, and the newly received data is discarded. This process is repeated for each new piece of data received until at least one empty FIFO entry exists. When the ROR bit is set, an interrupt request is made to the CPU which cannot be locally masked by any SPI register bit. Writing a 1 to this bit resets ROR status and its interrupt request; writing a 0 to this bit does not affect ROR status. Receiver Overrun Status is a non-maskable interrupt
6	0b RO	**Receive FIFO Service Request Flag (RFS):** The receive FIFO service request flag is a read-only bit which is set when the receive FIFO is nearly filled and requires service to prevent an overrun. RFS is set any time the receive FIFO has the same or more entries of valid data than indicated by the Receive FIFO Threshold, and it is cleared when it has fewer entries than the threshold value. When the RFS bit is set, an interrupt request is made unless RIE is cleared. After the CPU reads the FIFO such that it has fewer entries than the RFT value, the RFS flag (and the service request and/or interrupt) is automatically cleared.
5	0b RO	**Transmit FIFO Service Request Flag (TFS):** The Transmit FIFO service request flag is a read-only bit which is set when the transmit FIFO is nearly empty and requires service to prevent an underrun. TFS is set any time the transmit FIFO has the same or fewer entries of valid data than indicated by the Transmit FIFO Threshold, and it is cleared when it has more entries of valid data than the threshold value. When the TFS bit is set, an interrupt request is made unless TIE is cleared. After the CPU fills the FIFO such that it exceeds the threshold, the TFS flag (and the service request and/or interrupt) is automatically cleared.
4	0b RO	**SPI Busy Flag (BSY):** The SPI busy (BSY) flag is a read-only bit which is set when the SPI is actively transmitting and/or receiving data, and is cleared when the SPI is idle or disabled (SSE=0). This bit does not request an interrupt.
3	0b RO	**Receive FIFO Not Empty Flag (RNE):** The receive FIFO not empty flag is a read-only bit which is set whenever the receive FIFO contains one or more entries of valid data and is cleared when it no longer contains any valid data. This bit can be polled when using programmed I/O to remove remaining bytes of data from the receive FIFO since interrupt requests are only made when the Receive FIFO Threshold has been met or exceeded. This bit does not request an interrupt.

2	1b RO	**Transmit FIFO Not Full Flag (TNF):** The transmit FIFO not full flag is a read-only bit which is set whenever the transmit FIFO contains one or more entries which do not contain valid data. TNF is cleared when the FIFO is completely full. This bit can be polled when using programmed I/O to fill the transmit FIFO over its threshold level. This bit does not request an interrupt.
1:0	0b RO	**Alternative Frame (ALT_FRM):** This field is not supported and should be treated as reserved.

Affected Docs:Intel® Quark™ SoC X1000 Datasheet

Document-Only Changes

1. Tables Missing from Section 4.4 Configurable IO Characteristics

Issue: Configurable IO (CFIO) Bi-directional Signal Groupings and CFIO DC Characteristics tables were missing from the *Intel® Quark™ SoC X1000 Datasheet* Revision 001.

New Text:

Table 30. Configurable IO (CFIO) Bi-directional Signal Groupings

Group Name	Interfaces	Related Supply (V_{CC})	Signals
S0 CFIO Group 0	SPI Legacy SPI	VCCCFIO_0_3P3	SPI0_MOSI, SPI0_MISO, SPI0_SS_B, SPI0_SCK, SPI1_MOSI, SPI1_MISO, SPI1_SS_B, SPI1_SCK LSPI_MOSI, LSPI_MISO, LSPI_SS_B, LSPI_SCK
S0 CFIO Group 1	UART	VCCCFIO_1_3P3	SIU0_CTS_B, SIU0_DCD_B, SIU0_DSR_B, SIU0_DTR_B, SIU0_RI_B, SIU0_RTS_B, SIU0_RXD, SIU0_TXD, SIU1_CTS_B, SIU1_RTS_B, SIU1_RXD, SIU1_TXD
S0 CFIO Group 2	USB GPIO	VCCCFIO_2_3P3	USB_OC_0, USB_OC_1, USB_PWR_EN[0], USB_PWR_EN[1] GPIO[0], GPIO[1], GPIO[2], GPIO[3], GPIO[4], GPIO[5], GPIO[6], GPIO[7], GPIO[8], GPIO[9]
S0 CFIO Group 3	SDIO	VCCCFIO_3_3P3	SD_DATA[0], SD_DATA[1], SD_DATA[2], SD_DATA[3], SD_DATA[4], SD_DATA[5], SD_DATA[6], SD_DATA[7], SD_CMD , SD_CLK, SD_WP, SD_CD_B,
S0 CFIO Group 4	SDIO Ethernet MAC	VCCCFIO_4_3P3	SD_LED, SD_PWR_B MAC0_TXDATA[1], MAC0_TXDATA[0], MAC0_RXDV, MAC0_RXDATA[1], MAC0_RXDATA[0], MAC1_TXDATA[1], MAC1_TXDATA[0], MAC1_RXDV, MAC1_RXDATA[1], MAC1_RXDATA[0]
S0 CFIO Group 5	Ethernet MAC I2C Legacy	VCCCFIO_5_3P3	MAC0_TXEN, MAC0_MDC, MAC0_MDIO, MAC1_TXEN, MAC1_MDC, MAC1_MDIO I2C_DATA, I2C_CLK THRM_B, SMI_B, RMII_REF_CLK, CLK14
S3 CFIO Group	Legacy Power Management Suspend GPIOs	VCCCFIO_S3_3P3	RESET_BTN, WAKE_B, GPE_B S0_3V3_EN, S0_1V5_EN, S0_1V0_EN GPIO_SUS[0], GPIO_SUS[1], GPIO_SUS[2], GPIO_SUS[3], GPIO_SUS[4], GPIO_SUS[5]
S5 CFIO Group	JTAG/Debug Power Management	VCCCFIO_S5_3P3	TCK, TDI, TDO, TMS, TRST_B PWR_BTN, S3_3V3_EN, S3_1V5_EN, ODRAM_PWROK, OSYSPWRGOOD, PRDY_B, PREQ_B

Table 31. CFIO DC Characteristics

Type	Symbol	Parameter	Min	Max	Unit	Condition	Notes
This data applies to all signals in Table 30. To determine the correct V_{CC} supply for a signal use the related supply shown in Table 30.							
	V_{CC}	Supply Voltage Reference	3.13	3.49	V		
Input	V_{IH}	Input High Voltage	0.625 X V_{CC}	V_{CC} + 0.3	V		2
	V_{IL}	Input Low Voltage	V_{SS} - 0.3	0.25 X V_{CC}	V		2
	I_{IL}	Input Leakage Current	—	35	uA		
	C_{IN}	Input Pin Capacitance	—	10	pF		
Output	V_{OH}	Output High Voltage	0.75 x V_{CC}	—	V	I_{out}=2mA	1, 2
	V_{OL}	Output Low Voltage	—	0.125 x V_{CC}	V	I_{out}=-2mA	2

Notes:
1. The V_{OH} specification does not apply to open-collector or open-drain drivers. Signals of this type must have an external pull-up resistor, and that's what determines the high-output voltage level. Refer to Chapter 2 for details on signal types.
2. Input characteristics apply when a signal is configured as Input or to signals that are only Inputs. Output characteristics apply when a signal is configured as an Output or to signals that are only Outputs. Refer to Chapter 2 for details on signal types.

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

2. VNNSENSE and VSSSENSE are listed as Analog Across S5/4, S3, and S0 in Table 18

Issue: VNNSENSE and VSSSENSE should be listed as Off in S5/4 and S3.

Old Text:

Table 18. Power Management Interface Signals

					Default Buffer State			
Signal Name	Dir	Term	Power	Type	S4/S5	S3	Reset	Enter S0
PWR_BTN_B	I	-	3.3V	CMOS3.3	V_{iH}	V_{iH}	V_{iH}	V_{iH}
RESET_BTN_B	I	20k(H)	3.3V	CMOS3.3	Off	Pull-up	Pull-up	Pull-up
S5_PG	I	-	3.3V	CMOS3.3	V_{iH}	V_{iH}	V_{iH}	V_{iH}
S3_PG	I	-	3.3V	CMOS3.3	V_{iL}	V_{iH}	V_{iH}	V_{iH}
S0_PG	I	-	3.3V	CMOS3.3	V_{iL}	V_{iL}	V_{iH}	V_{iH}
S0_1P0_PG	I	-	3.3V	CMOS3.3	V_{iL}	V_{iL}	V_{iH}	V_{iH}
S3_3V3_EN	O	Ext	3.3V	CMOS3.3	V_{OL}	V_{OH}	V_{OH}	V_{OH}
S3_1V5_EN	O	Ext	3.3V	CMOS3.3	V_{OL}	V_{OH}	V_{OH}	V_{OH}
S0_3V3_EN	O	Ext	3.3V	CMOS3.3	Pull-down	V_{OL}	V_{OL}	V_{OiH}
S0_1V5_EN	O	Ext	3.3V	CMOS3.3	Pull-down	V_{oL}	V_{oH}	V_{oH}
S0_1P0_EN	O	Ext	3.3V	CMOS3.3	Pull-down	V_{oL}	V_{oH}	V_{oH}
ODRAM_PWROK	O	Ext	3.3V	CMOS3.3_OD	Pull-up	Pull-up	Pull-up	Pull-up
OSYSPWRGOOD	O	Ext	3.3V	CMOS3.3_OD	Pull-up	Pull-up	Pull-up	Pull-up
VNNSENSE	I/O	-	1.05V	Analog	Analog	Analog	Analog	Analog
VSSSENSE	I/O	-	GND	Analog	Analog	Analog	Analog	Analog

New Text:

Table 18. Power Management Interface Signals

					Default Buffer State			
Signal Name	**Dir**	**Term**	**Power**	**Type**	**S4/S5**	**S3**	**Reset**	**Enter S0**
PWR_BTN_B	I	-	3.3V	CMOS3.3	V_{iH}	V_{iH}	V_{iH}	V_{iH}
RESET_BTN_B	I	20k(H)	3.3V	CMOS3.3	Off	Pull-up	Pull-up	Pull-up
S5_PG	I	-	3.3V	CMOS3.3	V_{iH}	V_{iH}	V_{iH}	V_{iH}
S3_PG	I	-	3.3V	CMOS3.3	V_{iL}	V_{iH}	V_{iH}	V_{iH}
S0_PG	I	-	3.3V	CMOS3.3	V_{iL}	V_{iL}	V_{iH}	V_{iH}
S0_1P0_PG	I	-	3.3V	CMOS3.3	V_{iL}	V_{iL}	V_{iH}	V_{iH}
S3_3V3_EN	O	Ext	3.3V	CMOS3.3	V_{OL}	V_{OH}	V_{OH}	V_{OH}
S3_1V5_EN	O	Ext	3.3V	CMOS3.3	V_{OL}	V_{OH}	V_{OH}	V_{OH}
S0_3V3_EN	O	Ext	3.3V	CMOS3.3	Pull-down	V_{OL}	V_{OL}	V_{OiH}
S0_1V5_EN	O	Ext	3.3V	CMOS3.3	Pull-down	V_{oL}	V_{oH}	V_{oH}
S0_1P0_EN	O	Ext	3.3V	CMOS3.3	Pull-down	V_{oL}	V_{oH}	V_{oH}
ODRAM_PWROK	O	Ext	3.3V	CMOS3.3_OD	Pull-up	Pull-up	Pull-up	Pull-up
OSYSPWRGOOD	O	Ext	3.3V	CMOS3.3_OD	Pull-up	Pull-up	Pull-up	Pull-up
VNNSENSE	I/O	-	1.05V	Analog	Off	Off	Analog	Analog
VSSSENSE	I/O	-	GND	Analog	Off	Off	Analog	Analog

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

3. Miscellaneous Legacy Signal Enables (HLEGACY) Register Not In Datasheet

New Text: The HLEGACY register is added to Section 12.7.2 Host Bridge (Port 0x03)

Table 19. Summary of Message Bus Registers—0x03

Offset	Register ID—Description	Default Value
3h	"Host Miscellaneous Controls 2 (HMISC2)—Offset 3h" on page 8	00170001h
4h	"Host System Management Mode Controls (HSMMCTL)—Offset 4h" on page 8	00060006h
8h	"Host Memory I/O Boundary (HMBOUND)—Offset 8h" on page 9	40000000h
9h	"Extended Configuration Space (HECREG)—Offset 9h" on page 10	00000000h
Ah	"Miscellaneous Legacy Signal Enables (HLEGACY)—Offset Ah" on page 11	00008000h
Ch	"Host Bridge Write Flush Control (HWFLUSH)—Offset Ch" on page 11	00010000h

12.7.9.2 Miscellaneous Legacy Signal Enables (HLEGACY)—Offset 0Ah

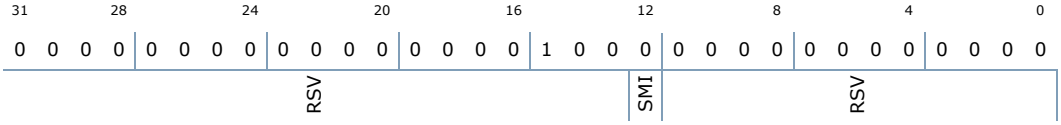
Access Method

Type: Message Bus Register (Size: 32 bits)

HLEGACY: [Port: 0x03] + 0Ah

Op Codes:
10h - Read, 11h - Write

Default: 00008000h



Bit Range	Default & Access	Description
31: 13	0b RO	**Reserved:** Reserved.
12	0b RW/SE	**SMI Pin Value (SMI):** Reflects the value of the SMI pin set via message 0x70. Pin value can also be set by writes to this register field.
11: 0	0b RO	**Reserved:** Reserved.

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

4. RTC 70976: No JEDEC Functionality in Datasheet

New Text: Added Section 13.5 Message Bus Commands

13.5 Message Bus Commands

Table 78. Message Opcode Definition

Opcode	Operation	Type	Description
00h	NOP	Msg	No operation
CAh	Wake	Msg	Wakes the memory from Self-Refresh mode or puts the Memory Controller in working mode after cold-boot. An ACK is sent after the Wake has completed and memory is accessible.
68h	DRAM Init	MsgD	This message enables accessing the DRAM internal registers. Message Data Payload Bits: 31:23 Reserved (set to 0) 22 Rank Address 21:6 Multiplexed Address: Determines the value of MA[15:0] when the initialization command is sent. 5:3 Bank Address: Determines the value of BA[2:0] when the initialization command is sent. 2:0 Command (RAS#,CAS#,WE#): Determines the value driven on the RAS#, CAS# and WE# signals respectively when the initialization command is sent. The supported commands are listed below: 000 – MRS (Extended) Mode Register Set 001 – Refresh 010 – Precharge (single or all as specified by MA[10]) 011 – Bank Activate 100 – Reserved 101 – Reserved 110 – ZQ Calibration (Long/Short as specified by MA[10]) 111 – NOP

New Text: Added Table 54. Message Types to Section 6.4 Message Bus Space

Table 54. Message Types

Msg Type	Message Description
RegWr	Register Write message - used to write to the 32-bit SoC unit registers.
RegRd	Register Read message - used to read from the 32-bit SoC unit registers.
Msg	Simple message without data - used to send atomic commands to SoC units.
MsgD	Simple message with 4 bytes of data - used to send atomic messages with 4 bytes of data to SoC units.

Affected Docs:*Intel® Quark™ SoC X1000 Datasheet*

5. Register Missing from Section 14.5 PCI Configuration Registers

Issue: Spread Spectrum Clocking Control (SSCCTL) register is missing from the Intel® Quark™ SoC X1000 Datasheet.

New Text: Added Section 15.5.54 Spread Spectrum Clocking Control (SSCCTL)

14.5.54 Spread Spectrum Clocking Control (SSCCTL): 0x14 Target ID: 0x03

Register Offset : 0x14

Access : R/W; RO

Size : 32 bits

Register Default: 0000_0000_0000_0000_0000_0000_0000_0000

Bit Range	Access	Default	Fuse Ovrd	Description
31:12	RO	00000h	no	**Reserved:** Reserved
11:8	R/W	0h	no	**Reserved:** Engineering Reserved
7:4	RO	0h	no	**Reserved:** Reserved
3	R/W	0b	no	**SSC Pattern Halt:** Halt generation of the SSC Pattern. Software sets this register field and waits for at least 32us to allow pattern to finish up its current modulated clock period and set SSC phase offset back to 0. After this point, software may make update to these register fields: SSC Max Phase Step, SSC Phase Increment Value, SSC Pattern Repeat Counts, SSC Spread Mode. Then software clear this register field to restart the hardware SCC pattern. 1: Halt generation of SSC; 0: Allow SSC generation to continually run
2:1	R/W	00b	no	**SSC Spread Mode:** Select the spread mode. 00: Down spread; 01: Center spread; 10: Up spread (RSVD); 11: RSVD Note: SSC Pattern Halt must be asserted before this control can be changed.
0	R/W	0b	no	**SSC enabled:** The bit determines whether the entire SSC block is enabled (0) or disabled (1). When the disabled state is entered all components of the SSC will be shutdown, with the exception of logic operating in the CRA domain (I.e. config access). The disable state will only be active when the SSC Reset FSM is in S7 or S0. If this signal becomes a 1 when in S7, the state machine will advance to S0 – thus disabling clocks and biasing. It will remain in S0 until asserted back to 0.

Affected Docs:Intel® Quark™ SoC X1000 Datasheet

Appendix A MAC Descriptor Details

This appendix contains information that will be added to a future revision of the *Intel® Quark™ SoC X1000 Datasheet*.

The information described in this section provides bit-field definitions of the current transmit and receive descriptor registers described in Section 15.6 of the datasheet, specifically:

- Current Host Transmit Descriptor Register (Register 18) (DMA_REG_18)—Offset 1048h
- Current Host Receive Descriptor Register (Register 19) (DMA_REG_19)—Offset 104Ch

A.1 Descriptor Overview

The descriptor structure has 8 DWORDS (32-bytes). The features of the descriptor structure are:

- The descriptor structure is implemented to support buffers of up to 8 KB (useful for Jumbo frames).
- There is a re-assignment of control and status bits in TDES0, TDES1, RDES0 (Advanced timestamp or IPC full offload configuration), and RDES1.
- The transmit descriptor stores the timestamp in TDES6 and TDES7.
- This receive descriptor structure is also used for storing the extended status (RDES4) and timestamp (RDES6 and RDES7).
- You can select one of the following options for descriptor structure:
  - If timestamping is enabled in Register 448 (Timestamp Control Register) or Checksum Offload is enabled in Register 0 (MAC Configuration Register), the software needs to allocate 32-bytes (8 DWORDS) of memory for every descriptor. For this, the software should set Bit 7 (Alternate Descriptor Size) of Register 0 (Bus Mode Register).
  - If timestamping or Checksum Offload is not enabled, the extended descriptors (DES4 to DES7) are not required. Therefore, the software can use alternate descriptors with the default size of 16 bytes.

A.2 Descriptor Endianness

The descriptor addresses must be aligned to the bus width (Word, DWord, or LWordSpecification Update for 32-bit bus). The data bus is configured for little-endian format.

The structure of the descriptor with respect to the data bus endianness is as follows:

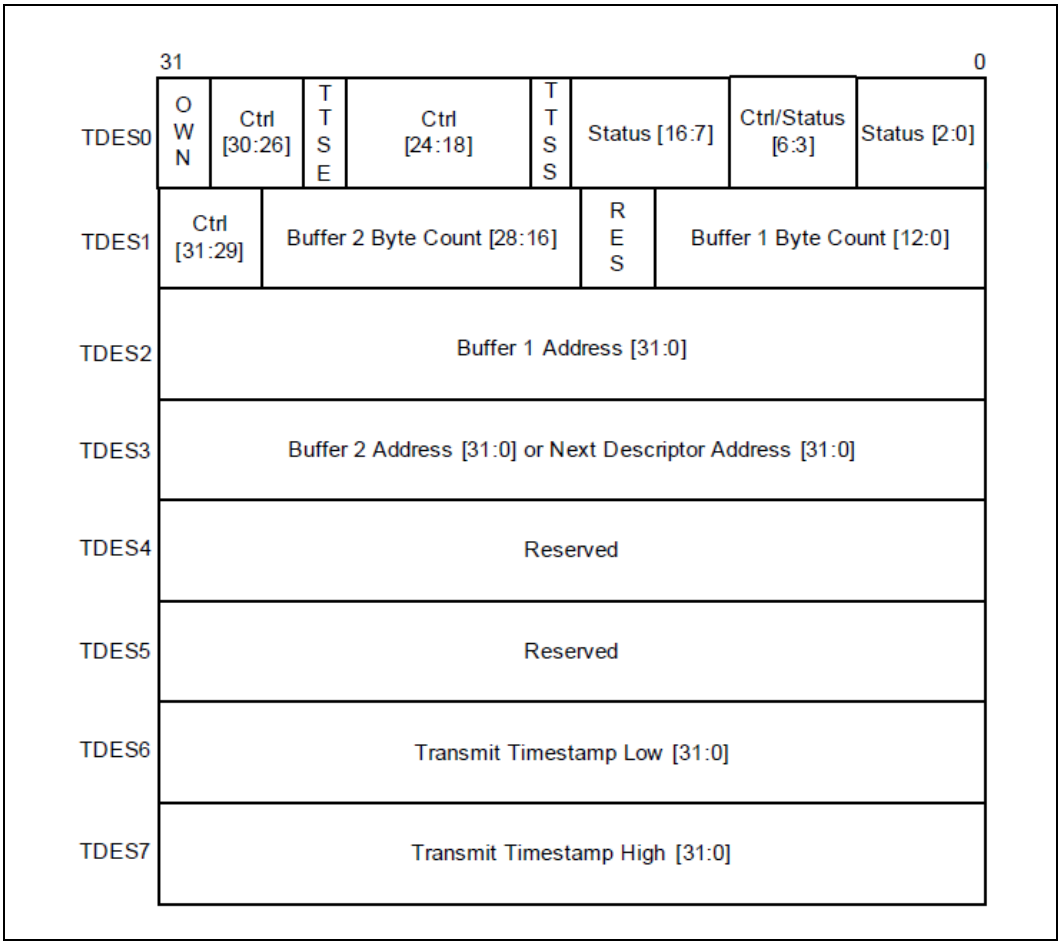
- Data Bus Endianness: Little-endian
- Descriptor Endianness: Same-endian
- Data Bus: 32-bit data bus

A.3 Transmit Descriptor

The transmit descriptor structure is shown in Figure 1. The application software must program the control bits TDES0[31:18] during descriptor initialization. When the DMA updates the descriptor, it writes back all the control bits except the OWN bit (which it clears) and updates the status bits[7:0]. The contents of the transmitter descriptor word 0 (TDES0) through word 3 (TDES3) are given in Table 1 through Table 3, respectively.

The snapshot of the timestamp to be taken can be enabled for a given frame by setting Bit 25 (TTSE) of TDES0. When the descriptor is closed (that is, when the OWN bit is cleared), the timestamp is written into TDES6 and TDES7. This is indicated by the status Bit 17 (TTSS) of TDES0 shown in Figure 1. The contents of TDES6 and TDES7 are mentioned in Table 5 and Table 6.

Figure 1. Transmit Descriptor Fields



The DMA always reads or fetches four DWORDS of the descriptor from system memory to obtain the buffer and control information as shown in Figure 2. When the AV feature is enabled, TDES0 has additional control bits[6:3] for Channel 1 and Channel 2. For Channel 0, Bits [6:3] are ignored. Bits [6:3] are described in Table 1.

Figure 2. Transmit Descriptor Fetch (Read)

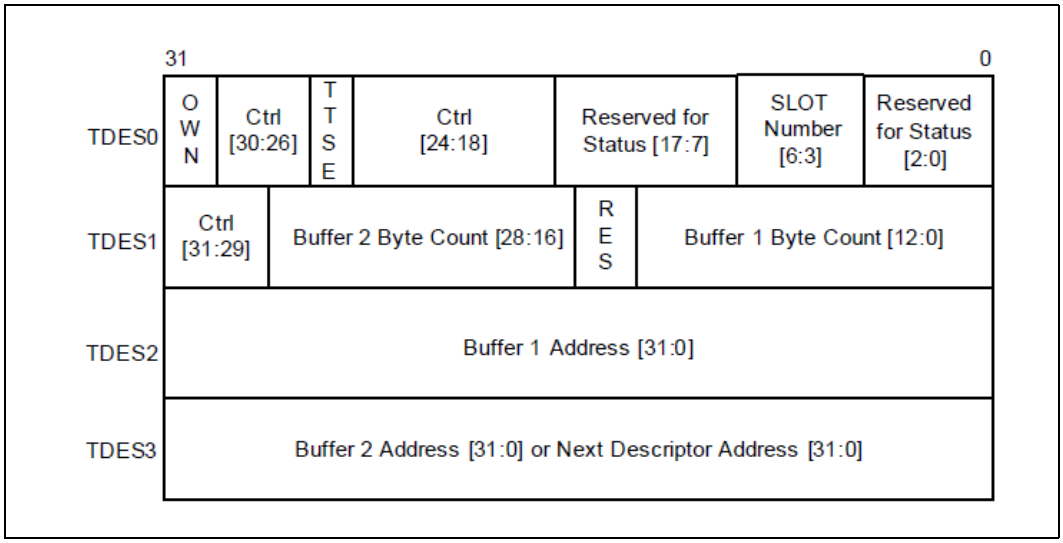


Table 1. Transmit Descriptor Word 0 (TDES0) (Sheet 1 of 3)

Bit	Description
31	OWN: Own Bit When set, this bit indicates that the descriptor is owned by the DMA. When this bit is reset, it indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame transmission or when the buffers allocated in the descriptor are read completely. The ownership bit of the frame's first descriptor must be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between fetching a descriptor and the driver setting an ownership bit.
30	IC: Interrupt on Completion When set, this bit sets the Transmit Interrupt (Register 5[0]) after the present frame has been transmitted.
29	LS: Last Segment When set, this bit indicates that the buffer contains the last segment of the frame. When this bit is set, the TBS1 or TBS2 field in TDES1 should have a non-zero value.
28	FS: First Segment When set, this bit indicates that the buffer contains the first segment of a frame.
27	DC: Disable CRC When this bit is set, the MAC does not append a cyclic redundancy check (CRC) to the end of the transmitted frame. This is valid only when the first segment (TDES0[28]) is set.
26	DP: Disable Pad When set, the MAC does not automatically add padding to a frame shorter than 64 bytes. When this bit is reset, the DMA automatically adds padding and CRC to a frame shorter than 64 bytes, and the CRC field is added despite the state of the DC (TDES0[27]) bit. This is valid only when the first segment (TDES0[28]) is set.
25	TTSE: Transmit Timestamp Enable When set, this bit enables IEEE1588 hardware timestamping for the transmit frame referenced by the descriptor. This field is valid only when the Enable IEEE1588 Timestamping option is selected during core configuration and the First Segment control bit (TDES0[28]) is set.
24	CRCR: CRC Replacement Control When set, the MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The host should ensure that the CRC bytes are present in the frame being transferred from the Transmit Buffer. This bit is valid when the Enable SA, VLAN, and CRC Insertion on TX option is selected during core configuration and the First Segment control bit (TDES0[28]) is set.

Table 1. Transmit Descriptor Word 0 (TDES0) (Sheet 2 of 3)

Bit	Description
23:22	CIC: Checksum Insertion Control These bits control the checksum calculation and insertion. The following list describes the bit encoding: • 2'b00: Checksum Insertion Disabled. • 2'b01: Only IP header checksum calculation and insertion are enabled. • 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. • 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit Full TCP/IP Checksum (Type 2) option is selected during core configuration and the First Segment control bit (TDES0[28]) is set.
21	TER: Transmit End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a descriptor ring.
20	TCH: Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When TDES0[20] is set, TBS2 (TDES1[28:16]) is a "don't care" value. TDES0[21] takes precedence over TDES0[20].
19:18	VLIC: VLAN Insertion Control When set, these bits request the MAC to perform VLAN tagging or untagging before transmitting the frames. If the frame is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: • 2'b00: Do not add a VLAN tag. • 2'b01: Remove the VLAN tag from the frames before transmission. This option should be used only with the VLAN frames. • 2'b10: Insert a VLAN tag with the tag value programmed in Register 353 (VLAN Tag Inclusion or Replacement Register). • 2'b11: Replace the VLAN tag in frames with the Tag value programmed in Register 353 (VLAN Tag Inclusion or Replacement Register). This option should be used only with the VLAN frames. These bits are valid when the Enable SA, VLAN, and CRC Insertion on TX option is selected during core configuration and the First Segment control bit (TDES0[28]) is set.
17	TTSS: Transmit Timestamp Status This field is used as a status bit to indicate that a timestamp was captured for the described transmit frame. When this bit is set, TDES2 and TDES3 have a timestamp value captured for the transmit frame. This field is only valid when the descriptor's Last Segment control bit (TDES0[29]) is set.
16	IHE: IP Header Error When set, this bit indicates that the MAC transmitter detected an error in the IP datagram header. The transmitter checks the header length in the IPv4 packet against the number of header bytes received from the application and indicates an error status if there is a mismatch. For IPv6 frames, a header error is reported if the main header length is not 40 bytes. Furthermore, the Ethernet Length/Type field value for an IPv4 or IPv6 frame must match the IP header version received with the packet. For IPv4 frames, an error status is also indicated if the Header Length field has a value less than 0x5.
15	ES: Error Summary Indicates the logical OR of the following bits: • TDES0[14]: Jabber Timeout • TDES0[13]: Frame Flush • TDES0[11]: Loss of Carrier • TDES0[10]: No Carrier • TDES0[9]: Late Collision • TDES0[8]: Excessive Collision • TDES0[2]: Excessive Deferral • TDES0[1]: Underflow Error • TDES0[16]: IP Header Error • TDES0[12]: IP Payload Error
14	JT: Jabber Timeout When set, this bit indicates the MAC transmitter has experienced a jabber time-out. This bit is only set when Bit 22 (Jabber Disable) of Register 0 (MAC Configuration Register) is not set.

Table 1. Transmit Descriptor Word 0 (TDES0) (Sheet 3 of 3)

Bit	Description
13	FF: Frame Flushed When set, this bit indicates that the DMA or MTL flushed the frame because of a software Flush command given by the CPU.
12	IPE: IP Payload Error When set, this bit indicates that MAC transmitter detected an error in the TCP, UDP, or ICMP IP datagram payload. The transmitter checks the payload length received in the IPv4 or IPv6 header against the actual number of TCP, UDP, or ICMP packet bytes received from the application and issues an error status in case of a mismatch.
11	LC: Loss of Carrier When set, this bit indicates that a loss of carrier occurred during frame transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during frame transmission). This is valid only for the frames transmitted without collision when the MAC operates in the half-duplex mode.
10	NC: No Carrier When set, this bit indicates that the Carrier Sense signal form the PHY was not asserted during transmission.
9	LC: Late Collision When set, this bit indicates that frame transmission is aborted because of a collision occurring after the collision window (64 byte-times, including preamble, in MII mode and 512 byte-times, including preamble and carrier extension, in GMII mode). This bit is not valid if the Underflow Error bit is set.
8	EC: Excessive Collision When set, this bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame. If Bit 9 (Disable Retry) bit in the Register 0 (MAC Configuration Register) is set, this bit is set after the first collision, and the transmission of the frame is aborted.
7	VF: VLAN Frame When set, this bit indicates that the transmitted frame is a VLAN-type frame.
6:3	CC: Collision Count (Status field) These status bits indicate the number of collisions that occurred before the frame was transmitted. This count is not valid when the Excessive Collisions bit (TDES0[8]) is set. The core updates this status field only in the half-duplex mode. -or- SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES2 or TDES3. When the transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the core (Register 11xx). It fetches the data from the buffers only if there is a match in values. These bits are valid only for AV channels (not Channel 0).
2	ED: Excessive Deferral When set, this bit indicates that the transmission has ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1,000-Mbps mode or if Jumbo Frame is enabled) if Bit 4 (Deferral Check) bit in Register 0 (MAC Configuration Register) is set high.
1	UF: Underflow Error When set, this bit indicates that the MAC aborted the frame because the data arrived late from the Host memory. Underflow Error indicates that the DMA encountered an empty transmit buffer while transmitting the frame. The transmission process enters the Suspended state and sets both Transmit Underflow (Register 5[5]) and Transmit Interrupt (Register 5[0]).
0	DB: Deferred Bit When set, this bit indicates that the MAC defers before transmission because of the presence of carrier. This bit is valid only in the half-duplex mode.

Table 2. Transmit Descriptor Word 1 (TDES1)

Bit	Description
31:29	SAIC: SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet frame with the value given in the MAC Address 0 register. If the Source Address field is modified in a frame, the MAC automatically recalculates and replaces the CRC bytes. The Bit 31 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits[30:29]: • 2'b00: Do not include the source address. • 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. • 2'b10: Replace the source address. For reliable transmission, the application must provide frames with source addresses. • 2'b11: Reserved These bits are valid in the GMAC-DMA, GMAC-AXI, and GMAC-AHB configurations when the Enable SA, VLAN, and CRC Insertion on TX is selected during core configuration and when the First Segment control bit (TDES0[28]) is set.
28:16	TBS2: Transmit Buffer 2 Size This field indicates the second data buffer size in bytes. This field is not valid if TDES0[20] is set.
15:13	Reserved
12:0	TBS1: Transmit Buffer 1 Size These bits indicate the first data buffer byte size, in bytes. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or the next descriptor, depending on the value of TCH (TDES0[20]).

Table 3. Transmit Descriptor 2 (TDES2)

Bit	Description
31:0	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1. There is no limitation on the buffer address alignment.

Table 4. Transmit Descriptor 3 (TDES3)

Bit	Description
31:0	Buffer 2 Address Pointer (Next Descriptor Address) Indicates the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (TDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. The buffer address pointer must be aligned to the bus width only when TDES1[24] is set. (LSBs are ignored internally.)

Table 5. Transmit Descriptor 6 (TDES6)

Bit	Description
31:0	TTSL: Transmit Frame Timestamp Low This field is updated by DMA with the least significant 32 bits of the timestamp captured for the corresponding transmit frame. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

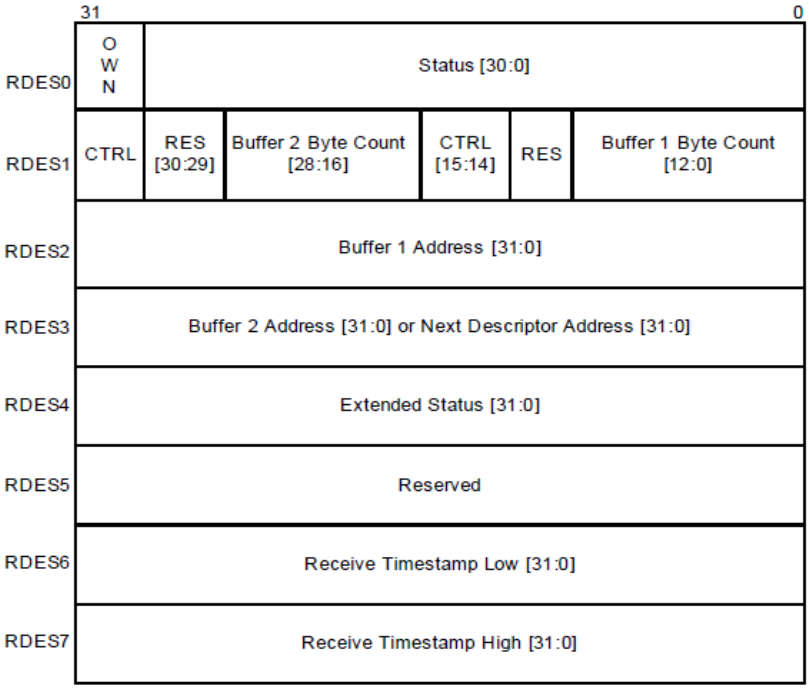
Table 6. Transmit Descriptor 7 (TDES7)

Bit	Description
31:0	TTSH: Transmit Frame Timestamp High This field is updated by DMA with the most significant 32 bits of the timestamp captured for the corresponding receive frame. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

A.4 Receive Descriptor

The structure of the received descriptor is shown in Figure 3. It has 32 bytes of descriptor data (8 DWORDs).

Figure 3. Receive Descriptor Fields



The contents of RDES0 are identified in Table 7. The contents of RDES1 through RDES3 are identified in Table 8 through Table 10, respectively.

Note: Some of the bit functions of RDES0 are not backward compatible to Release 3.41a and previous versions. These bits are Bit 7, Bit 0, and Bit 5. The function of Bit 5 is backward compatible to Release 3.30a and previous versions.

Table 7. Receive Descriptor Fields (RDES0) (Sheet 1 of 2)

Bit	Description
31	OWN: Own Bit When set, this bit indicates that the descriptor is owned by the DMA of the DWC_gmac. When this bit is reset, this bit indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	AFM: Destination Address Filter Fail When set, this bit indicates a frame that failed in the DA Filter in the MAC.
29:16	FL: Frame Length These bits indicate the byte length of the received frame that was transferred to host memory (including CRC). This field is valid when Last Descriptor (RDES0[8]) is set and either the Descriptor Error (RDES0[14]) or Overflow Error bits are reset. The frame length also includes the two bytes appended to the Ethernet frame when IP checksum calculation (Type 1) is enabled and the received frame is not a MAC control frame. This field is valid when Last Descriptor (RDES0[8]) is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current frame.
15	ES: Error Summary Indicates the logical OR of the following bits: • RDES0[1]: CRC Error • RDES0[3]: Receive Error • RDES0[4]: Watchdog Timeout • RDES0[6]: Late Collision • RDES0[7]: Giant Frame • RDES4[4:3]: IP Header or Payload Error • RDES0[11]: Overflow Error • RDES0[14]: Descriptor Error This field is valid only when the Last Descriptor (RDES0[8]) is set.
14	DE: Descriptor Error When set, this bit indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the DMA does not own the Next Descriptor. The frame is truncated. This field is valid only when the Last Descriptor (RDES0[8]) is set.
13	SAF: Source Address Filter Fail When set, this bit indicates that the SA field of frame failed the SA Filter in the MAC.
12	LE: Length Error When set, this bit indicates that the actual length of the frame received and that the Length/ Type field does not match. This bit is valid only when the Frame Type (RDES0[5]) bit is reset.
11	OE: Overflow Error When set, this bit indicates that the received frame was damaged because of buffer overflow in MTL. **Note:** This bit is set only when the DMA transfers a partial frame to the application. This happens only when the Rx FIFO is operating in the threshold mode. In the store-and-forward mode, all partial frames are dropped completely in Rx FIFO.
10	VLAN: VLAN Tag When set, this bit indicates that the frame to which this descriptor is pointing is a VLAN frame tagged by the MAC. The VLAN tagging depends on checking the VLAN fields of received frame based on the VLAN Tag Register (Register 7) (GMAC_REG_7)—Offset 1Ch setting.
9	FS: First Descriptor When set, this bit indicates that this descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next Descriptor contains the beginning of the frame.
8	LS: Last Descriptor When set, this bit indicates that the buffers pointed to by this descriptor are the last buffers of the frame.

Table 7. Receive Descriptor Fields (RDES0) (Sheet 2 of 2)

Bit	Description
7	Timestamp Available, IP Checksum Error (Type1), or Giant Frame When Advanced Timestamp feature is present, when set, this bit indicates that a snapshot of the Timestamp is written in descriptor words 6 (RDES6) and 7 (RDES7). This is valid only when the Last Descriptor bit (RDES0[8]) is set. When IP Checksum Engine (Type 1) is selected, this bit, when set, indicates that the 16-bit IPv4 Header checksum calculated by the core did not match the received checksum bytes. Otherwise, this bit, when set, indicates the Giant Frame Status. Giant frames are larger than 1,518-byte (or 1,522-byte for VLAN or 2,000-byte when Bit 27 (2KPE) of MAC Configuration register is set) normal frames and larger than 9,018-byte (9,022-byte for VLAN) frame when Jumbo Frame processing is enabled.
6	LC: Late Collision When set, this bit indicates that a late collision has occurred while receiving the frame in the half-duplex mode.
5	FT: Frame Type When set, this bit indicates that the Receive Frame is an Ethernet-type frame (the LT field is greater than or equal to 16'h0600). When this bit is reset, it indicates that the received frame is an IEEE802.3 frame. This bit is not valid for Runt frames less than 14 bytes.
4	RWT: Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer has expired while receiving the current frame and the current frame is truncated after the Watchdog Timeout.
3	RE: Receive Error When set, this bit indicates that the gmii_rxer_i signal is asserted while gmii_rxdv_i is asserted during frame reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd ≠ 0f) during extension.
2	DE: Dribble Bit Error When set, this bit indicates that the received frame has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
1	CE: CRC Error When set, this bit indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received frame. This field is valid only when the Last Descriptor (RDES0[8]) is set.
0	Extended Status Available/Rx MAC Address When either Advanced Timestamp or IP Checksum Offload (Type 2) is present, this bit, when set, indicates that the extended status is available in descriptor word 4 (RDES4). This is valid only when the Last Descriptor bit (RDES0[8]) is set. When Advance Timestamp Feature or IPC Full Offload is not selected, this bit indicates Rx MAC Address status. When set, this bit indicates that the Rx MAC Address registers value (1 to 15) matched the frame's DA field. When reset, this bit indicates that the Rx MAC Address Register 0 value matched the DA field.

Table 8. Receive Descriptor Fields 1 (RDES1) (Sheet 1 of 2)

Bit	Description
31	DIC: Disable Interrupt on Completion When set, this bit prevents setting the Status Register's RI bit (CSR5[6]) for the received frame ending in the buffer indicated by this descriptor. This, in turn, disables the assertion of the interrupt to Host because of RI for that frame.
30:29	Reserved
28:16	RBS2: Receive Buffer 2 Size These bits indicate the second data buffer size, in bytes. The buffer size must be a multiple of 4, 8, or 16, depending on the bus widths (32, 64, or 128, respectively), even if the value of RDES3 (buffer2 address pointer) is not aligned to bus width. If the buffer size is not an appropriate multiple of 4, 8, or 16, the resulting behavior is undefined. This field is not valid if RDES1[14] is set.
15	RER: Receive End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a descriptor ring.

Table 8. Receive Descriptor Fields 1 (RDES1) (Sheet 2 of 2)

Bit	Description
14	RCH: Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, RBS2 (RDES1[28:16]) is a "don't care" value. RDES1[15] takes precedence over RDES1[14].
13	Reserved
12:0	RBS1: Receive Buffer 1 Size Indicates the first data buffer size in bytes. The buffer size must be a multiple of 4, 8, or 16, depending upon the bus widths (32, 64, or 128), even if the value of RDES2 (buffer1 address pointer) is not aligned. When the buffer size is not a multiple of 4, 8, or 16, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or next descriptor depending on the value of RCH (Bit 14).

Table 9. Receive Descriptor Fields 2 (RDES2)

Bit	Description
31:0	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1. There are no limitations on the buffer address alignment except for the following condition: The DMA uses the configured value for its address generation when the RDES2 value is used to store the start of frame. The DMA performs a write operation with the RDES2[3:0, 2:0, or 1:0] bits as 0 during the transfer of the start of frame but the frame data is shifted as per the actual Buffer address pointer. The DMA ignores RDES2[3:0, 2:0, or 1:0] (corresponding to bus width of 128, 64, or 32) if the address pointer is to a buffer where the middle or last part of the frame is stored.

Table 10. Receive Descriptor Fields 3 (RDES3)

Bit	Description
31:0	Buffer 2 Address Pointer (Next Descriptor Address) These bits indicate the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (RDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. If RDES1[24] is set, the buffer (Next Descriptor) address pointer must be bus width-aligned (RDES3[3, 2, or 1:0] = 0, corresponding to a bus width of 128, 64, or 32. LSBs are ignored internally.) However, when RDES1[24] is reset, there are no limitations on the RDES3 value, except for the following condition: The DMA uses the configured value for its buffer address generation when the RDES3 value is used to store the start of frame. The DMA ignores RDES3 [3, 2, or 1:0] (corresponding to a bus width of 128, 64, or 32) if the address pointer is to a buffer where the middle or last part of the frame is stored.

The status written is as shown in Table 11. The status is written only when there is status related to IPC or timestamp available. The availability of extended status is indicated by Bit 0 of RDES0. This status is available only when the Advance Timestamp or IPC Full Offload feature is selected.

Table 11. Receive Descriptor Fields 4 (RDES4) (Sheet 1 of 2)

Bit	Description
31:28	Reserved
27:26	Layer 3 and Layer 4 Filter Number Matched These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received frame. • 00: Filter 0 • 01: Filter 1 • 10: Filter 2 • 11: Filter 3 This field is valid only when Bit 24 or Bit 25 is set high. When more than one filter matches, these bits give only the lowest filter number.
25	Layer 4 Filter Match When set, this bit indicates that the received frame matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: • Layer 3 fields are not enabled and all enabled Layer 4 fields match. • All enabled Layer 3 and Layer 4 filter fields match. When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits [27:26].
24	Layer 3 Filter Match When set, this bit indicates that the received frame matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: • All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed. • All enabled filter fields match. When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits [27:26].
23:21	Reserved
20:18	VLAN Tag Priority Value These bits give the VLAN tag's user value in the received packet. These bits are valid only when the RDES4 Bits 16 and 17 are set. These bits are available only when you select the AV feature.
17	AV Tagged Packet Received When set, this bit indicates that an AV tagged packet is received. Otherwise, this bit indicates that an untagged AV packet is received. This bit is valid when Bit 16 is set. This bit is available only when you select the AV feature.
16	AV Packet Received When set, this bit indicates that an AV packet is received. This bit is available only when you select the AV feature.
15	Reserved
14	Timestamp Dropped When set, this bit indicates that the timestamp was captured for this frame but got dropped in the MTL Rx FIFO because of overflow. This bit is available only when you select the Advanced Timestamp feature. Otherwise, this bit is reserved.
13	PTP Version When set, this bit indicates that the received PTP message is having the IEEE 1588 version 2 format. When reset, it has the version 1 format. This bit is available only when you select the Advanced Timestamp feature. Otherwise, this bit is reserved.
12	PTP Frame Type When set, this bit indicates that the PTP message is sent directly over Ethernet. When this bit is not set and the message type is non-zero, it indicates that the PTP message is sent over UDP-IPv4 or UDP-IPv6. The information about IPv4 or IPv6 can be obtained from Bits 6 and 7. This bit is available only when you select the Advanced Timestamp feature.

Table 11. Receive Descriptor Fields 4 (RDES4) (Sheet 2 of 2)

Bit	Description
11:8	Message Type These bits are encoded to give the type of the message received. • 0000: No PTP message received • 0001: SYNC (all clock types) • 0010: Follow_Up (all clock types) • 0011: Delay_Req (all clock types) • 0100: Delay_Resp (all clock types) • 0101: Pdelay_Req (in peer-to-peer transparent clock) • 0110: Pdelay_Resp (in peer-to-peer transparent clock) • 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) • 1000: Announce • 1001: Management • 1010: Signaling • 1011-1110: Reserved • 1111: PTP packet with Reserved message type These bits are available only when you select the Advance Timestamp feature. **Note**: Values 1000, 1001, and 1010 are not backward compatible with release 3.50a.
7	IPv6 Packet Received When set, this bit indicates that the received packet is an IPv6 packet. This bit is updated only when Bit 10 (IPC) of MAC Configuration Register (Register 0) (GMAC_REG_0)—Offset 0h) is set. This bit is available when you select the Enable Receive Full TCP/IP Checksum (Type 2) feature.
6	IPv4 Packet Received When set, this bit indicates that the received packet is an IPv4 packet. This bit is updated only when Bit 10 (IPC) of MAC Configuration Register (Register 0) (GMAC_REG_0)—Offset 0h) is set. This bit is available when you select the Enable Receive Full TCP/IP Checksum (Type 2) feature.
5	IP Checksum Bypassed When set, this bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive Full TCP/IP Checksum (Type 2) feature.
4	IP Payload Error When set, this bit indicates that the 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) that the core calculated does not match the corresponding checksum field in the received segment. It is also set when the TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. This bit is valid when either Bit 7 or Bit 6 is set. This bit is available when you select the Enable Receive Full TCP/IP Checksum (Type 2) feature.
3	IP Header Error When set, this bit indicates that either the 16-bit IPv4 header checksum calculated by the core does not match the received checksum bytes, or the IP datagram version is not consistent with the Ethernet Type value. This bit is valid when either Bit 7 or Bit 6 is set. This bit is available when you select the Enable Receive Full TCP/IP Checksum (Type 2) feature.
2:0	IP Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE). The COE also sets these bits to 2'b00 if it does not process the IP datagram's payload due to an IP header error or fragmented IP. • 3'b000: Unknown or did not process IP payload • 3'b001: UDP • 3'b010: TCP • 3'b011: ICMP • 3'b1xx: Reserved This bit is valid when either Bit 7 or Bit 6 is set. This bit is available when you select the Enable Receive Full TCP/IP Checksum (Type 2) feature.

RDES6 and RDES7 contain the snapshot of the timestamp. The availability of the snapshot of the timestamp in RDES6 and RDES7 is indicated by Bit 7 in the RDES0 descriptor. The contents of RDES6 and RDES7 are identified in Table 12 and Table 13, respectively.

Table 12. Receive Descriptor Fields 6 (RDES6)

Bit	Description
31:0	RTSL: Receive Frame Timestamp Low This field is updated by DMA with the least significant 32 bits of the timestamp captured for the corresponding receive frame. This field is updated by DMA only for the last descriptor of the receive frame which is indicated by Last Descriptor status bit (RDES0[8]).

Table 13. Receive Descriptor Fields 7 (RDES7)

Bit	Description
31:0	RTSH: Receive Frame Timestamp High This field is updated by DMA with the most significant 32 bits of the timestamp captured for the corresponding receive frame. This field is updated by DMA only for the last descriptor of the receive frame which is indicated by Last Descriptor status bit (RDES0[8]).

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